Evaluating Novel Interconnects for Future Cryogenic Computers

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In this article, we describe the Laboratory for Physical Sciences (LPS) test, evaluation, and research activities associated with the Intelligence Advanced Research Projects Activity's (IARPA) SuperCables program. SuperCables is a program focused on developing the capability to egress single flux quanta (SFQ) data from a superconducting processor at a temperature of 4 Kelvin (K) to room temperature. To achieve the goals of the program, four performers are attempting to map data onto pulses of light and output the data over a thermally insulating optical fiber, instead of the typical way which sends the electrical signal over a conducting microwave cable. To assess the performance of these devices, LPS has developed the capability at 4 K to measure the bit error rates (BERs) up to 30 gigabits per second (Gbps), the dissipated and leaked optical power from nanowatts (nW) up to tens of milliwatts (mW), and has researched the fiber-device coupling, which is a significant source of optical loss in these systems.

[Photo credit: Adobe Stock]

Introduction

The electronic industry has relied on scaling down complementary metal-oxide semiconductor (CMOS) transistors for decades, but the semiconductor-only road map ended in 2015 [1], and the new standard map includes "Beyond CMOS" technologies [2], indicating a need to explore new materials and devices. One alternative to semiconductor logic is superconducting logic [3], which uses single flux quanta (SFQ) for bits [4], and is known for energy efficiency as well as speed. The most developed type, rapid single flux quanta (RSFQ), has been studied as a possible system since the 1990s [5, 6, 7], and modern superconducting logic families show further gains in efficiency by reducing or eliminating static power [8, 9, 10]. Additionally, reversible computing [11, 12, 13, 14] promises the ultimate thermodynamic advancements in digital efficiency, and neuromorphic computing [15, 16, 17] promises new computing architectures, both with superconducting logic. The typical operating temperature for this logic is 4 K (-269 degrees Celsius), and researchers are generally interested in the energy dissipated (i.e., heat produced) during cryogenic operation, which is typically estimated by calculation [18].

Aside from logic circuitry dissipation, the total cryogenic power budget also needs to account for the movement of data (i.e., egress and ingress) between room temperature and 4 K which is significant when transmitting large amounts of data at high data rates using traditional means. Standard low-loss copper-based microwave cables would transmit a large amount of passive heat from room temperature into the 4 K environment because of the large associated thermal conductivity of the copper (Cu) metal. For example, a standard 50 centimeter-long high-bandwidth microwave cable made from Cu (assuming a temperature thermal conductivity of 3 W/cm*K for a UT-47 cable) would deliver an estimated 0.3 mW of passive power from room temperature directly to the 4 K environment (corresponding to 0.15 W of wall power), a value too large when scaling the number of inputs and outputs for a cryogenic processor. To decrease this amount of heat, one typically uses alloyed metallic cables so that the thermal conductance of heat is reduced, resulting in approximately an order of magnitude decrease in the passive heat. The downsides with this strategy are that resistive cables result in a smaller bandwidth and still pose a challenge for scaling to a very large number of channels of data.

Is there a better way of getting data and signals to and from a cryogenic environment? IARPA's SuperCables program is addressing this question by having performers design and demonstrate devices which convert electrical data from an SFQ stimulus module into pulses of light [i.e., a cryogenic electrical to optical (EO) device], and then use an optical fiber to carry the data signal to room temperature.

There are potentially several benefits to using an optical fiber:

- Optical fibers enable a much smaller transfer of heat into the cryogenic environment since the thermal conductivity of glass is three orders of magnitude smaller than metal.
- Data transmitted through an optical fiber has a larger bandwidth than electrical data transmitted in an electrical cable.
- Optical fibers have better scalability potential when going to a large number of inputs and outputs.

To guarantee that the demonstrated EO devices work better than traditional means for the egress of cryogenic data, IARPA has created metrics centered around small BERs, large bandwidth, and small energy-per-bit devices (see table 1). To meet these goals, four performer teams are researching cryogenic electro-optic transducers based on tunable ring resonators, a superconducting modulator, or a cryogenic laser [19].

To test and evaluate these unique performer devices, a standard requirement for IARPA's programs, our team has developed the expertise and assembled the facilities needed to evaluate the devices. As we describe in more detail in the following sections, this includes:

1. Measuring BERs of the performer devices up to rates of 10 Gbps using a provided SFQ stimulus module or up to 30 Gbps by driving electrical data from room temperature down to the 4 K environment,
2. Researching and developing new fiber-to-chip couplings for a cryogenic environment, and
3. Researching and developing a cryogenic test platform to measure the dissipated electrical and optical power of the devices at 4 K anywhere in the range of 300 picowatts (pW) to 34 mW.

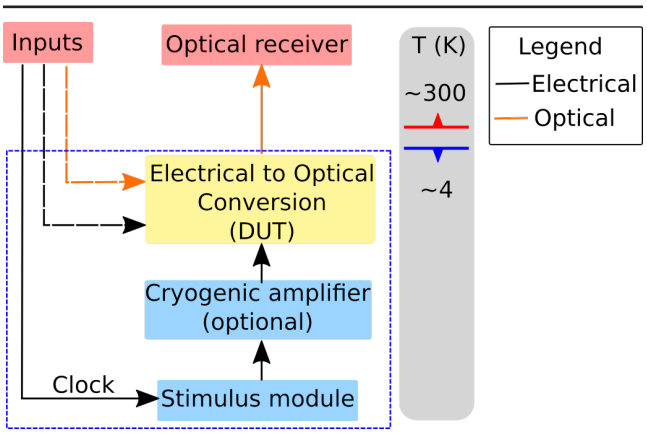

FIGURE 1. In this SuperCables component block diagram, the PRBS pattern is generated at either 300 K using a BERT (dashed black) or at 4 K using a superconducting stimulus module and sent to the electrical input of the EO device under test (DUT) (yellow). The converted optical signal is transported from 4 K to 300 K via an optical fiber (orange) and detected by an optical receiver as part of the BER measurement. Optionally, an input optical signal can be sent in from 300 K to the performer device by a separate optical fiber (dashed orange). The 4 K cryogenic components are shown within the dashed blue box.

Bit error rate measurements

To test the capability of the performer devices to transmit digital data without errors, the SuperCables program specifies the use of bit error rate (BER) measurements. These measurements are performed by a bit error rate tester (BERT) which contains a pattern generator and an error detector. The pattern generator outputs a test pattern, containing a sequence of ones and zeros, that is sent to the input of the performer device. The output of the performer device is then compared to the test pattern by the error detector to determine the number of errors. The BERT result is typically expressed as a ratio, such as 10^{-6}, which means there is one error per million bits. The program goals for BER performance are broken into three tiers including 10^{-6} (threshold), 10^{-8} (objective), and 10^{-10} (stretch).

TABLE 1. IARPA goals for the SuperCables program (The metrics discussed in this article are highlighted in bold.)

Metric	Units	Threshold	Objective	Stretch
Energy per bit at 4 K	aJ/bit	1,000	50	10
Total system energy per bit at room temperature	fJ/bit	65	2	0.2
Bit error rate (BER)	-	10^{-6}	10^{-8}	10^{-10}
Channels per chip area	cm^{-2}	10	100	10,000
Data rate per channel	Gbps	10	50	100
Latency	ns	200	50	10

For the test pattern, the program specifies that we use a pseudorandom bit sequence (PRBS), which is a deterministic, repeating binary pattern that exhibits statistical behavior analogous to a truly random sequence. It is typically denoted by 2^k-1 PRBS or PRBS*k*, with *k* being the length of the shift register used to create the pattern. The pattern 2^k-1 PRBS is a sequence that contains every possible combination of the *k* bits except one. Different length PRBS patterns are used in different applications. For example, 2^7-1 PRBS (127 bits) is often used in Ethernet and Fiber Channel applications [20]. Longer pattern lengths, such as $2^{23}-1$ PRBS (≈8 million bits), are typically used for synchronous optical networking (SONET) and synchronous digital hierarchy (SDH) telecommunication systems, which require a pattern with a lower frequency component. For SuperCables, we use a 2^7-1 pattern (see also next section).

A simplified block diagram of the components of our cryogenic BER test bed is shown in figure 1. The electronic PRBS pattern is sent to the performer device at 4 K from either a BERT at 300 K or the SFQ stimulus module, which outputs PRBS and operates adjacent to the device within the cryogenic environment. The converted optical signal is carried to room temperature via an optical fiber and detected by an optical receiver before going to the BERT error detector for analysis. The stimulus module allows us to test the performer device with representative data outputted from a superconducting computer; however, the voltage output amplitude is fixed at a small, approximately 4-millivolt (mV) peak-to-peak level, and the data rates are limited to approximately 10 Gbps, limiting a complete characterization of the devices. On the other hand, our BERT is capable of outputting signals with variable amplitude and at data rates up to 30 Gbps and is therefore able to ascertain a wider range of frequency and amplitude conditions as detailed in the next paragraph.

We conduct a suite of BER measurements for each performer device by sweeping experimental parameters to characterize the device performance and tolerances. Parameters such as optical input power (a laser power) and PRBS amplitude affect the energy efficiency of the device, so the measurements determine how the BER changes as a function of these parameters. As an example, figure 2 shows the measured BER of a commercial optical modulator as a function of optical input power, and while lower optical power ultimately improves the overall energy efficiency, the error rate increases. Error will also be increased for poor optical coupling into the performer devices. Moreover, the photons that do not couple into the device will increase the dissipated heat and reduce the energy efficiency.

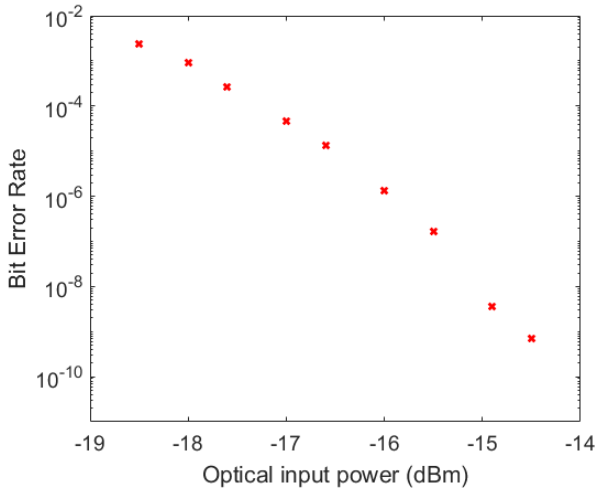

FIGURE 2. The bit error rate (BER) as a function of optical input power is measured here with a commercial optical modulator.

When measuring performer devices, we start by taking measurements at room temperature, when possible, and then repeat the measurements at 4 K. We compare the results of our tests to those provided by the performer and determine if they meet the SuperCables objective goals of 10^{-8}. Furthermore, we vary the device bias and measure BER to determine a relationship between dissipated power and BER.

Single flux quantum source

In order to prepare for future tests of performer devices, we cooled and tested the stimulator module. The module uses Niobium (Nb) superconducting circuitry for internal SFQ generation and conversion from SFQ to efficiently made voltage levels which are outputted (as a PRBS waveform). It produces a PRBS signal with a fixed voltage output. This module, shown in figure 3, is mounted on the 4 K plate of the cryostat, as is the performer device, and is connected to the performer device by a short coaxial cable. The module, which can generate either return-to-zero (RZ) or non-return-to-zero (NRZ) patterns, can generate a deterministic PRBS7 or PRBS15 signal with a peak-to-peak amplitude of ~4 mV and data rates up to 10 Gbps [21]. While the goal of the program was to have the performer devices driven directly by the stimulus module signal, we also included an optional

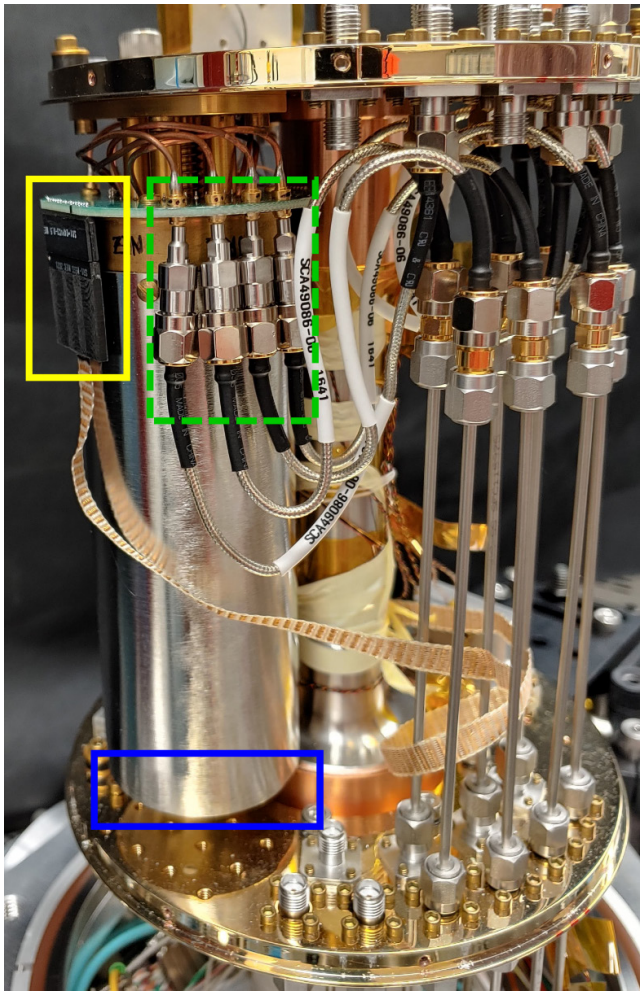

FIGURE 3. In this photo, the stimulus module is mounted to the 4 K plate of the cryostat. The superconducting chip, located at the bottom of the module (not visible, blue box) within the magnetic shield, is attached to the direct current bias and switches (yellow box) and microwave inputs/outputs (dashed green box).

cryogenic amplifier, shown in the schematic of figure 1 to amplify the pattern produced by the stimulus unit as needed. The stimulus module requires 11 direct current biases, four control switches, an input clock signal, and produces two available digital outputs. The module is also encapsulated by two magnetic shields to reduce stray magnetic fields and prevent the trapping of external flux in the niobium (Nb) layers, which would prevent proper operation of the module.

We have successfully operated and characterized the stimulus module between 2.7 K and 4.5 K for data rates up to 10 Gbps. Figure 4 shows a representative PRBS eye diagram generated by the stimulus module, amplified at room temperature and then digitized by an oscilloscope.

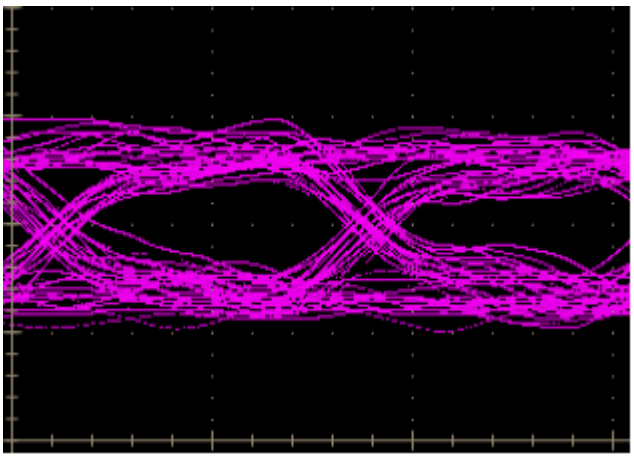

FIGURE 4. This plot shows the output of the SFQ stimulus module operating at 1 Gbps and a temperature of 4 K. The overlaying of repetitive samples produces an eye diagram with the potential to show some of the PRBS signal as ones and zeros. The eye is open in this measurement such that the signal is large compared to noise and the measurement gave a low BER.

Development of low-loss fiber device couplers

One of the biggest challenges in the practical implementation of a cryogenic electro-optic transducer is coupling light between an optical waveguide of the transducer chip and an optical fiber. Typical on-chip optical waveguides are around a few hundred nanometers (nm) wide, whereas the core of a single-mode fiber is around 10 microns (μm) in diameter. Some kind of mode conversion is necessary to efficiently couple between the two. In addition, the method by which the fiber is aligned and affixed to the chip must be cryogenically compatible. Reducing the optical loss due to mode conversion and misalignment is especially important because it not only degrades the performance, but also contributes to heating the cryogenic environment.

Fiber-to-chip coupling strategies generally fall into three categories: edge coupling, grating coupling, and evanescent coupling (see figure 5). Edge coupling is broadband, polarization-independent, and has shown losses as low as 0.7 decibels (dB) for a single fiber [22], but the alignment tolerance is very low, so thermal contraction from room temperature to the cryogenic environment must be carefully accounted for in the packaging. Grating couplers have better alignment tolerance, but they are typically wavelength-dependent and higher-loss than edge couplers. Evanescent coupling is a less mature

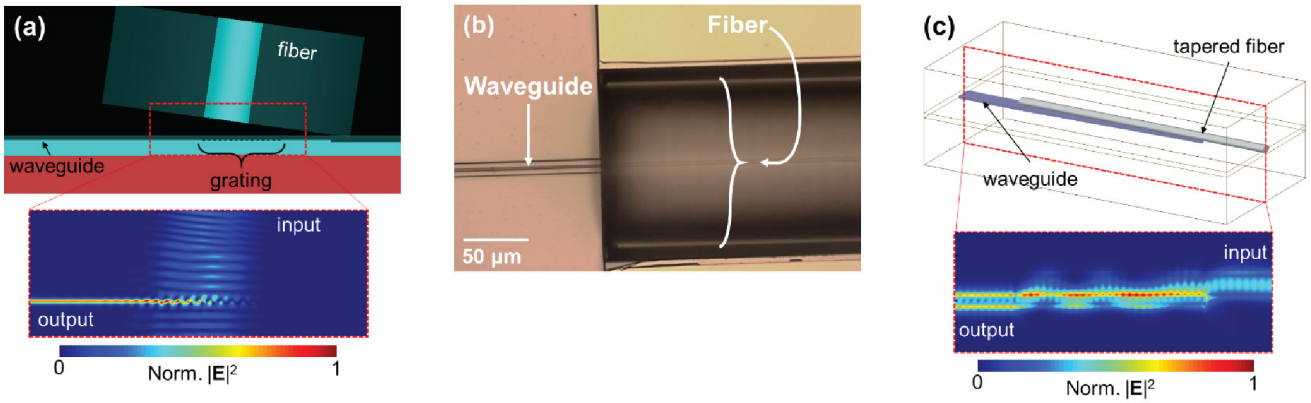

FIGURE 5. The three main strategies for fiber-to-chip coupling are: **(a)** grating coupling, **(b)** edge coupling, and **(c)** evanescent coupling.

coupling strategy but shows similar performance to edge coupling [23]. None of these has emerged as a standard option for packaged cryogenic coupling, partly due to the fact that fibers aligned and affixed at room temperature can move or even break off when cooling down. As a result, most cryogenic electro-optic transducers have been characterized using active alignment with micropositioners in the cryogenic environment, a strategy that is not scalable or power efficient. Here, we describe our work testing epoxy compatibility with the cryogenic environment, then use one of those epoxies in an experiment to test the cryo-robustness of a three-dimensional micron-scale structure for mechanically aligning optical fibers to on-chip devices.

One of the important components for a cryo-robust package is the epoxy used to affix the optical fibers. The physical properties of epoxy will change as it cools, potentially becoming brittle or losing adhesion. As a result, we tested a wide array of epoxies to determine which work best to adhere optical fibers over a wide range of temperatures. We used a sheet of untreated Cu as a substrate and epoxied pieces of optical fiber to the Cu (see figure 6). The epoxies we tested included J-B KwikWeld [24], VGE-7031 [25], Eccobond 286 [26], Silver-impregnated room-temperature-vulcanizing silicon (RTV), rubber cement, and STYCAST 2850 [27]. For each of these, we tried different dilutions with toluene to control the flow around the optical fiber.

We then submerged the sample in liquid nitrogen (77 K) for about 10 minutes to allow it to equilibrate with the nitrogen. After pulling it out, we warmed it with a heat gun. This thermal shock is much greater than would be experienced in a typical cryostat cooling cycle. We then looked for visible changes in the epoxy, and pulled on the fibers to evaluate adhesion. Most of the epoxies survived without visible changes, but a few did not do well holding the fibers through our pull test. Rubber cement, in particular, did not adhere well to the fiber; it may be useful for other applications, but not for firm fiber attachment.

Having characterized these adhesives, we packaged an integrated photonic chip for cryogenic testing. For this experiment, we leveraged a collaboration with the Lipson Nanophotonics Group at Columbia University to test their "plug-and-play" devices, three-dimensional funnel-like structures that guide

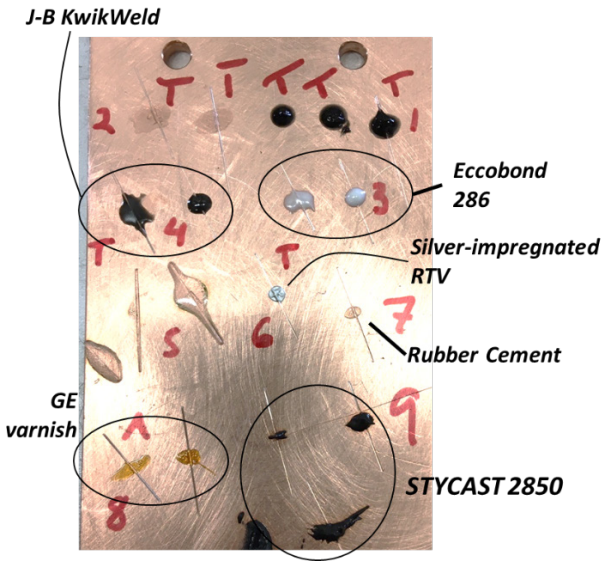

FIGURE 6. The fiber segments are epoxied to copper substrate for a thermal cycling test.

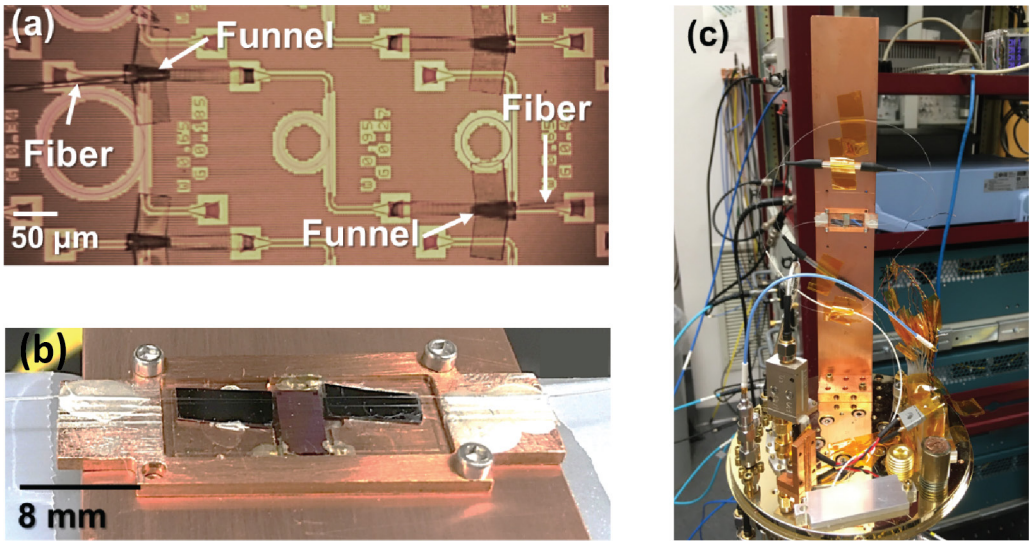

FIGURE 7. (a) In this microscope image of plug-and-play funnels on an integrated photonic chip, fibers are present in the funnels. **(b)** On this copper mount, chip and fibers are epoxied in place. **(c)** Here, the chip is mounted inside cryostat.

a tapered optical fiber into alignment with an on-chip grating coupler [see figure 7(a)] [28]. We used silver-impregnated RTV, which survived the thermal shock test particularly well, to hold the fibers in place. A fiber-pigtailed device is shown in figure 7(b).

We mounted the device in a 4 K cryostat provided under the program [figure 7(c)] and monitored the transmission with respect to wavelength as the device cooled. Data from the measurement is shown in figure 8. We were able to see transmission through the device down to the base temperature of the cryostat. Although the maximum transmission did not change very much with temperature, the bandwidth and spectral characteristics shifted slightly, likely due to thermo-optic changes in the refractive index of all three of the materials involved [silicon (Si), silicon dioxide (SiO2), and the plug-and-play device polymer]. Afterward, we warmed the device back to room temperature.

We repeated this cool-down and warm-up cycle again, and the transmission characteristics did not significantly change. Surviving two cryostat cooling cycles suggests that this packaging strategy is promising as a cryo-robust technique for aligning and affixing fibers to chips. We expect the design can be optimized to further reduce the optical insertion loss. The best reported measurements of these plug-and-play devices was 9.5 dB total insertion loss, with approximately 0.05 dB loss attributable to each plug-and-play structure (at room temperature) [29]. In addition, the plug-and-play funnel is a versatile, additively-manufactured structure that could be adapted for use with edge couplers and other coupling strategies.

4 K device dissipation measurements

An important metric of the SuperCables program is the 4 K dissipated energy-per-bit of the performer devices. To directly measure small amounts of dissipated electrical and optical power, our team at LPS has researched and developed new capabilities to measure dissipated powers between 0.3 nW and 30 mW [30].

Figures 9(a) and (b) show pictures and a cross-sectional schematic of our test stage module which allows measurement of heat dissipation. The DUT is bolted to the test stage. Since the module operates in a vacuum, any electrical or optical heat dissipated from the performer device readily conducts into the test stage containing a thermometer and three identical electrical heaters labeled: bias, applied, and feedback heater. The applied electrical current and voltage to each heater is measured to determine the applied heat on the test stage. A thermometer and heater are also mounted to the base plate to actively maintain a stable 3 K cold thermal reservoir.

To simplify discussion of basic heat flow concepts, the test stage with mounted components (heaters, DUT, and thermometer) is hypothetically assumed to be very well thermally isolated. In this idealized scenario, all generated heat that flows into the test stage is energetically stored by raising its temperature. The increase in temperature (ΔT) depends on the total mass (m) of the stage and mounted components. The stored thermal energy is given by $E=(m\, c_s)\, \Delta T$, where c_s is the average specific heat of the materials. Measuring small amounts of heat generated from a

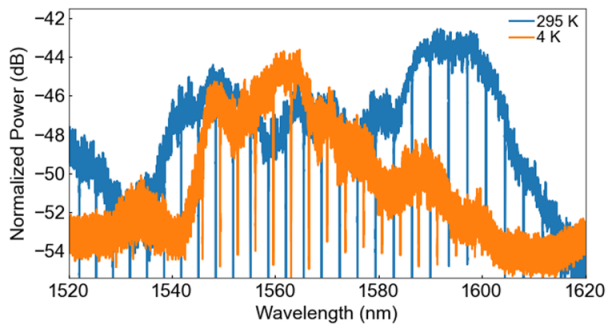

FIGURE 8. Normalized transmission spectrum at room temperature (295 K) and base temperature (4 K).

macroscopic device with large mass is challenging since the signal, which is the rise in temperature, is very small. Rewriting the energy as a heat flow $q=E/\Delta t$ (in watts) and using the definition of heat capacity, $C_S=m\ c_s$, the instantaneous heat flow into the stage can be written as $q=C_S\ \partial T/\partial t$. This expression for the storage of heat in material from heat flow is analogous to the storage of charge in a capacitor from a charge flow $I=C\ \partial V/\partial t$, where current and voltage substitute for heat flow and temperature, and capacitance substitutes for heat capacity.

Connecting the hypothetical test stage to the base plate with a thermally conducting link causes heat to flow from the test stage into the colder base plate. This heat flow depends on the temperature difference across the thermal link, $\Delta T=q\ R_L$, where R_L is the thermal resistance of the link that is tuned by selecting its material (thermal conductivity) and adjusting the length and cross-sectional area. A useful electrical analogy is Ohm's law, $\Delta V=I\ R$, which has electrical resistance R. In order to maintain the test stage at 4 K while tethered to the colder reservoir at 3 K, the test stage bias heater needs to dissipate a power of $q=(4-3)\text{K}/R_L$ to maintain the temperature difference of 1 K (assuming no power is dissipated by the performer device). Any steady parasitic heat flow into or out of the test stage (from thermal radiation, conduction, and ohmic self-heating of wires and thermometers) is compensated by changing the bias heater power required to maintain the 1 K difference. All parasitic heat leaks between the test stage and base plate are engineered to be much smaller than the heat flow through the thermal link.

A sudden increase in heat flow Δq into the test stage from the performer device that has been turned on will cause a time-dependent rise in temperature away from 4 K. As the temperature rises, added heat energy is stored in the test stage while the temperature difference across the thermal link increases. This results in additional heat flow into the cold reservoir, which reaches a new steady state equilibrium temperature where $\Delta q=\Delta T_{eq}/R_L$. At any time t, the heat flow into the test stage must either go into heating it up or conduct through the link into the cold bath so

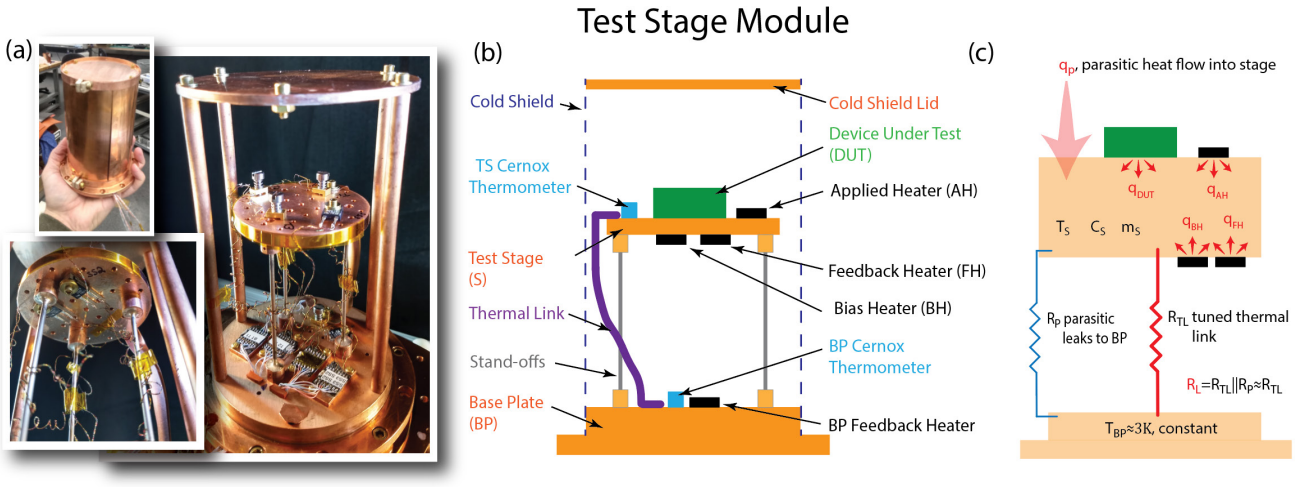

FIGURE 9. (a) These images and **(b)** this diagram depict the test stage module that measures heat dissipation of cryogenically maintained devices. The module's base plate mounts to a cryostat cold plate in vacuum. A copper test stage is structurally supported by three thin-walled stainless steel tube stand-offs. The test stage is cooled by the base plate through a metal thermal link. **(c)** A thermal diagram of the test stage module idealizes the test stage as a homogeneous block with a heat capacity C_S, mass m_S and temperature T_S. All test stage heating is from parasitic heating effects q_P plus intentional heating by test devices q_{DUT} and test stage heaters that include the applied heater q_{AH}, feedback heater q_{FH}, and bias heater q_{BH}.

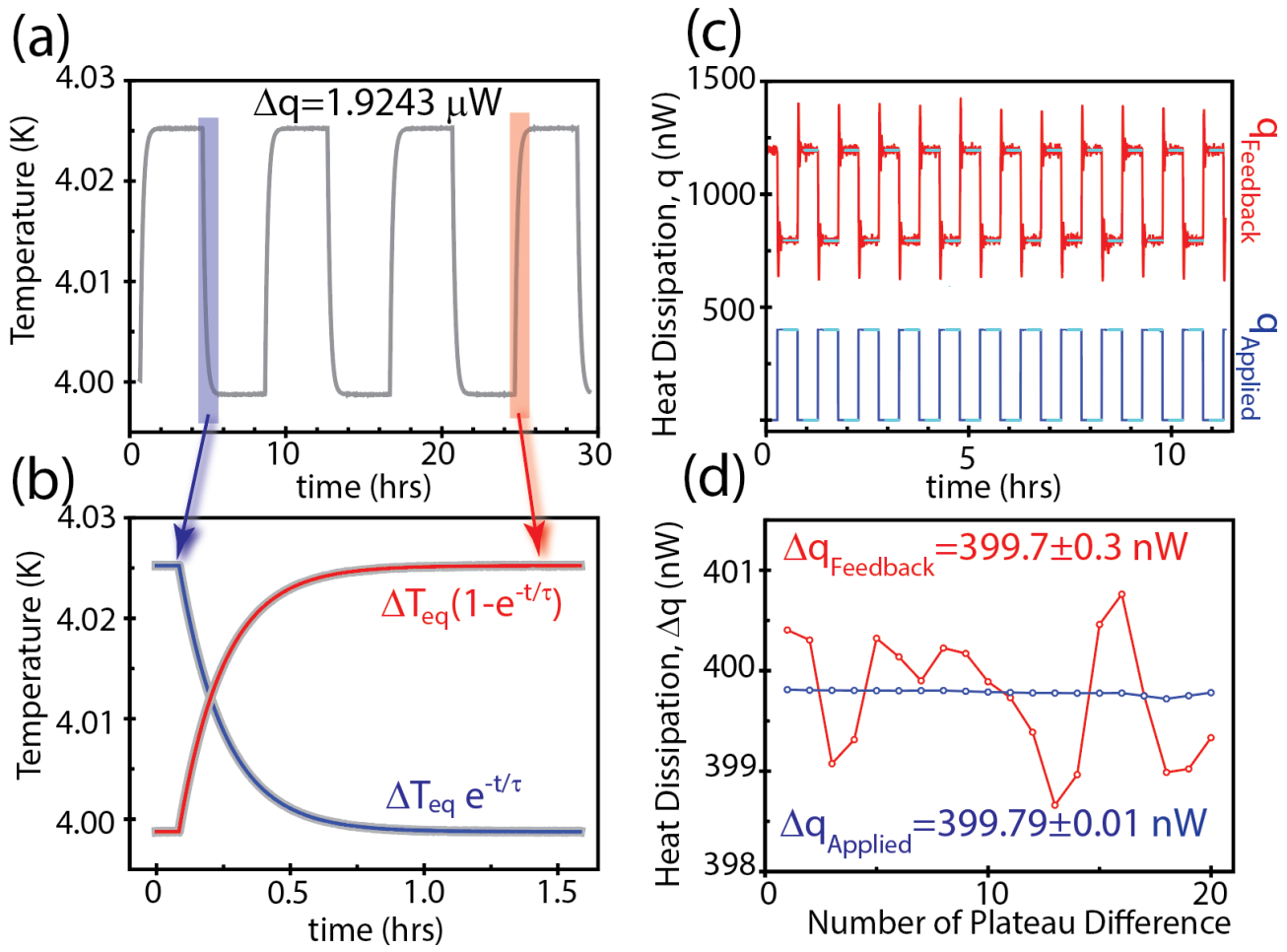

FIGURE 10. (a, b) An applied heater is cyclically toggled off and on (gray) and the temperature response is fit (red and blue) with the parameters ΔT_{eq} and τ, from which R_L and Δq are determined. **(c)** An active feedback measurement scheme is demonstrated using a weak thermal link. An applied heat of 399.79 nW is cyclically applied (blue) while a feedback heater compensates to maintain the test stage at 4 K (red). The changes in electrical dissipated power Δq are fit (cyan). **(d)** Each sequential plateau difference Δq_i is plotted for the applied (blue) and feedback heater (red), and the 95% confidence interval of the standard error of the mean reported.

that $\Delta q = C_S \bullet (\partial \Delta T(t)/\partial t) + \Delta T(t)/R_L$. This differential equation has an exponential solution for the time dependence of the test stage temperature and is the same differential equation and solution as a charging capacitor in a series resistor-capacitor (RC) circuit. Multiplying both sides of the equation by resistance, and substituting ΔV for ΔT and ΔI for Δq, gives Kirchhoff's voltage rule. In both cases, the solution has a characteristic RC time constant. For our test stage module, the thermal time constant $\tau = R_L C_S$ is between a few seconds to 10 minutes, depending upon the mass of the device and thermal link selected. The response time is slow when either the resistance is high, which is necessary to produce a measurable rise in temperature when devices dissipate very small heat flows, or when the combined mass of the test stage and mounted components is large.

To characterize the system, we toggle an applied heater off and on and measure the change in temperature of the test stage, as shown in figure 10(a) and (b). Exponential fits of the data determine ΔT_{eq} and τ, and therefore R_L. The measured thermal dissipation, found by $\Delta q = \Delta T_{eq}/R_L$, is equal to the measured electrical power supplied to the heater.

Unknown heat loads can be measured by similarly toggling test devices on and off and measuring the temperature rise. However, this measurement method has the inherent shortcoming that devices are measured over a range of temperatures. Thermal conductivity and specific heat of many materials are strongly temperature dependent at cryogenic temperatures, which not only effect R_L and C_S but can also impact device performance.

To circumvent these issues and therefore drastically improve the measurement method, we maintain the test stage and devices at a constant temperature using an active feedback heater. Instead of measuring deviations in the test stage temperature, we measure changes in the electrical power supplied to a feedback heater. While electrical and optical power supplied to the performer device are cyclically toggled on and off, the test stage temperature is measured and maintained at a constant 4 K. The critical engineering considerations using this feedback method remain essentially the same as before. The test stage still responds to changes in heat flow with a characteristic time involving $\tau=R_L C_S$ that critically depends on the mass of the test stage and components. The smallest possible change in heat flow applied by the feedback circuit is predicated upon the smallest measurable temperature deviation as $\delta q_{min}=\delta T_{min}/R_L$, where the maximum thermal resistance R_L (at 4 K) is pragmatically limited by the longest tolerable cool down time of the test stage from room temperature (where the response time τ is much slower).

To demonstrate this feedback method, we use the applied heater to mimic turning off and on the total dissipated power of a performer device with ~400 nW as shown in figure 10(d) (blue). The power supplied by the feedback heater compensates (red). Immediately following each toggle event, the response of the feedback heater shows an overshoot followed by rapidly damped oscillations, standard for an optimally tuned proportional integral derivative (PID) feedback circuit. After settling, the feedback heater power plateaus and maintains the test stage at 4 K. Each plateau is averaged (cyan), and averaging the differences between each sequential pair of plateau values results in a noise floor of 300 pW [see figure 10(d)].

Heat dissipation measurements, using two different thermal links R_L, have been demonstrated using a 430-gram net stage mass of Cu from a minimum of 300 pW up to 30 mW, a dynamic range of 10^8. Except for the lowest power levels near 300 pW, the precision and accuracy of this technique is measured to four or five significant figures.

Conclusion

Data egress is an important task for the maturation of superconducting computing. With LPS' unique expertise and capabilities in the field of fiber optics, integrated optics, cryogenics, and cryogenic computing, our team has set up a test and evaluation site to evaluate 4 K cryogenic EO devices manufactured under IARPA's SuperCables program. This includes evaluating the error rate of the EO devices by either electrically stimulating it from a superconducting SFQ module or a room temperature data source, measuring the bandwidths of the devices up to 30 Gbps, measuring the dissipation from the devices from 300 pW up to 30 mW, and performing research on the fiber-to-chip coupling.

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References

[1] HPC Wire. "Transistors won't shrink beyond 2021, says final ITRS report." 2021. *HPC Wire.* Available at: https://www.hpcwire.com/2016/07/28/transistors-wont-shrink-beyond-2021-says-final-itrs-report/. [Accessed Sep 2021.]

[2] IRDS IEEE. International Roadmap for Devices and Systems (IRDS) 2020 Edition. Available at: https://irds.ieee.org/editions/2020. [Accessed 8 Sep 2021.]

[3] Holmesc DS, Ripple AL, Manheimer MA. "Energy-efficient superconducting computing—power budgets and requirements." *IEEE Transactions on Applied Superconductivity.* 2013;23(3):1701610–1701610. doi: 10.1109/TASC.2013.2244634.

[4] Likharev KK, Semenov VK. "RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems." *IEEE Transactions on Applied Superconductivity.* 1991;1(1):3–28. doi: 10.1109/77.80745.

[5] Likharev KK. "Ultrafast superconductor digital electronics: RSFQ technology roadmap." *Czechoslovak Journal of Physics.* 1996;46:3331–3338. Available at: https://doi.org/10.1007/BF02548149.

[6] Dorojevets M. "Current status and recent developments in RSFQ processor design" In: Luryi S, Xu JM, Zaslavsky A (editors). *Future Trends in Microelectronics: From Nanophotonics to Sensors and Energy.* Wiley & Sons, Inc.; 2010. pp. 229–238. doi: 10.1002/9780470649343.ch19.

[7] Ishida K, Tanaka M, Nagaoka I, Ono T, Kawakami S, Tanimoto T, Fujimaki A, Inoue K. "32 GHz 6.5 mW gate-level-pipelined 4-bit processor using superconductor single-flux-quantum logic." In: *2020 IEEE Symposium on VLSI Circuits.* 2020 Jun: pp. 1–2. doi: 10.1109/VLSICircuits18222.2020.9162826.

[8] Kirichenko AJ, Vernik IV, Kamkar MY, Walter J, Miller M, Albu LR, Mukhanov OA. "ERSFQ 8-bit parallel arithmetic logic unit." *IEEE Transactions on Applied Superconductivity.* 2019;29(5):1–7. doi: 10.1109/tasc.2019.2904484.

[9] Herr QP, Herr AY, Oberg OT, Ioannidis AG. "Ultra-low-power superconductor logic." *Journal of Applied Physics.* 2011;109(10):103903. Available at: https://doi.org/10.1063/1.3585849.

[10] Ayala CL, Tanaka T, Saito R, Nozoe M, Takeuchi N, Yoshikawa N. "MANA: A monolithic adiabatic iNtegration architecture microprocessor using 1.4-zJ/op unshunted superconductor Josephson Junction devices." *IEEE Journal of Solid-State Circuits.* 2021;56(4):1152–1165. doi: 10.1109/JSSC.2020.3041338.

[11] Osborn KD, Wustmann W. "Reversible fluxon logic with optimized CNOT gate components." *IEEE Transactions on Applied Superconductivity.* 2021;31(2):1–13.

[12] Takeuchi N, Yamanashi Y, Yoshikawa N. "Reversibility and energy dissipation in adiabatic superconductor logic." *Scientific Reports.* 2017;7(1):75. doi: 10.1038/s41598-017-00089-9.

[13] Ren J, Semenov VK. "Progress with physically and logically reversible superconducting digital circuits." *IEEE Transactions on Applied Superconductivity.* 2011;21(3):780–786. doi: 10.1109/TASC.2011.2104352.

[14] Frank MP, Lewis RM, Missert NA, Wolak MA, Henry MD. "Asynchronous ballistic reversible fluxon logic." *IEEE Transactions on Applied Superconductivity.* 2019;29(5):1–7. doi: 10.1109/TASC.2019.2904962.

[15] Shainline JM, Buckley SM, Mirin RP, Nam SW. "Superconducting optoelectronic circuits for neuromorphic computing." *Physical Review Applied.* 2017;7. Available at: https://doi.org/10.1103/PhysRevApplied.7.034013.

[16] Schneider ML, Segall K. "Fan-out and fan-in properties of superconducting neuromorphic circuits." *Journal of Applied Physics.* 2020;128(1). Available at: https://doi.org/10.1063/5.0025168.

[17] Rowlands GE, Nguyen MH, Ribeill GJ, Wagner AP, Govia LCG, Barbosa WAS, Gauthier DJ, Ohki TA. "Reservoir computing with superconducting electronics." 2021. Cornell University Library, arXiv: 2103.02522.

[18] Takeuchi N, Yamanashi Y, Yoshikawa N. "Measurement of 10 zJ energy dissipation of adiabatic quantum-flux-parametron logic using a superconducting resonator." *Applied Physics Letters.* 2013;102(5). Available at: https://doi.org/10.1063/1.4790276.

[19] Wu H, Fu W, Feng M, Deppe D. "2.6 K VCSEL data link for cryogenic computing." *Applied Physics Letters.* 2021;119(4). Available at: https://doi.org/10.1063/5.0054128.

[20] Maxim Integrated. "Spectral content of NRZ test patters." Available at: https://pdfserv.maximintegrated.com/en/an/AN3455.pdf.

[21] Lehmann AE, Filippov TV, Sarwana SM, Kirichenko DE, Dotsenko VV, Sahu A, Gupta D. "Embedded RSFQ pseudo-random binary sequence generator for multichannel high-speed digital data link testing and synchronization." *IEEE Transactions on Applied Superconductivity.* 2017;27(4). doi: 10.1109/TASC.2017.2667408.

[22] Barwicz T, Peng B, Leidy R, Janta-Polczynski A, Houghton T, Khater M, Engelmann S, Fortier P, Boyer N, Green WMJ. "Integrated metamaterial interfaces for self-aligned fiber-to-chip coupling in volume manufacturing." *IEEE Journal of Selected Topics in Quantum Electronics.* 2019;25(3):1–13. doi: 10.1109/JSTQE.2018.2879018.

[23] Tiecke TJ, Nayak KP, Thompson JD, Peyronel T, de Leon NP, Vuletić V, Lukin MD. "Efficient fiber-optical interface for nanophotonic devices." *Optica.* 2015;2(2):70–75. Available at: https://doi.org/10.1364/OPTICA.2.000070.

[24] JB Weld. KwikWeld. Available at: https://www.jbweld.com/product/kwikweld-twin-tube.

[25] Lake Shore Cryotronics. Varnish. Available at: https://www.lakeshore.com/products/categories/overview/temperature-products/cryogenic-accessories/varnish.

[26] Ellsworth Adhesives. Henkel loctite ablestik 286 thermally conductive adhesive white 6 oz kit. Available at: https://www.ellsworth.com/products/by-market/general-industry/thermally-conductive-materials/adhesives/henkel-loctite-ablestik-286-thermally-conductive-adhesive-white-6-oz-kit/.

[27] Henkel Adhesive Technologies. Loctite stycast 2850FT. Available at: https://www.henkel-adhesives.com/us/en/product/potting-compounds/loctite_stycast_2850ft.html.

[28] Gordillo OAJ, Chaitanya S, Chang YC, Dave UD, Mohanty A, Lipson M. "Plug-and-play fiber to waveguide connector." *Optics Express.* 2019;27(15):20305–20310. Available at: https://doi.org/10.1364/OE.27.020305.

[29] Chakraborty T, Gordillo OAJ, Barrow M, Lipson M, Murphy TE, Grutter KE. "Thermo-optic characterization of SU-8 at cryogenic temperature." In: *Conference on Lasers and Electro-Optics, Technical Digest Series* (Optica Publishing Group, 2022), paper SF3O.7. Available at: https://doi.org/10.1364/CLEO_SI.2022.SF3O.7.

[30] Jenkins GS, Grutter KE, Petruzzi P, Palmer BS. "Closed cycle 4 K nanowatt meter for hectogram payloads." *AIP Advances*. 2022;12(6):065105. doi: 10.1063/5.0089788.