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Design and Test Evaluation of SiC Diode Modules

by Timothy E. Griffin and M. Gail Koebke

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14. ABSTRACT
Two high-temperature modules, one of p-i-n SiC diodes and one of junction barrier Schottky SiC diodes, were fabricated on A1N. Material choice, thermal conductivity, compatibility, design, and performance are discussed. A curve tracer measured each diode on a module for forward and reverse current versus voltage. Diodes in parallel were measured for reverse recovery charge and time, at different currents and to 150 °C substrate, including operation in a DC-to-DC converter. A silicone overcoat permitted testing the p-i-n to the rated 1200-V reverse.

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Contents

List of Figures

List of Tables

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1. Introduction

An open package planar module for silicon carbide (SiC) power diodes was engineered and fabricated. Materials, experiences, and electrical measurements are discussed. The chips of the crystal structure 4H of SiC each had a diode and were mounted on a module. Diodes were tested for reverse recovery at substrate temperature as great as 150 ºC. We began with *p-i-n* (p-type surface layer over a nearly intrinsic base layer over the n-type bulk) diodes rated at 1200 V blocking and 5 A. The devices were first tested for forward and reverse characteristics on a digital storage curve tracer. Switching evaluation was then performed in a reverse recovery apparatus. The diodes were then tested in a DC-to-DC buck converter (repetitive reverse recovery, cycles to "buck" the voltage down). After significant or stressful switching in the circuits, new measurements were taken of the diodes by the curve tracer and these were compared to the measurements before the stress. The reverse recovery time was evaluated as a function of the case temperature of the devices. Reverse recovery current and voltage versus time were measured to calculate charge, peak current, and power dissipation. Current sharing by diodes in parallel operation was less than equal to varying extents, and current shifted to another diode during the microseconds after reverse recovery. One problem discovered with the devices was the gold upper layer "creep-back" from the edge of a very heated chip. The gold should have had better passivation to prevent this.

Four chips, each with a junction barrier Schottky (JBS) diode rated 500 V and 4 A, were mounted on a module. Semiconductor fabrication calculations favor the low forward voltage and low reverse leakage of JBS diodes at less than such voltage. Electrically, these JBS were not adequately durable; one blew at less than 230 V and 1 A, and one blew at less than 300 V and 2.3 A. The JBS had much less reverse recovery time and charge (such as 14.4 ns and 10 nC) than the *p-i-n*. Initial study of new JBS diode showed each at 20 A and blocking voltage of 1100 V to 150 °C.

2 SiC Properties and Diode Theory

The wide band-gap semiconductor 4H-SiC has properties favorable for power and high temperature semiconductor devices. The 3.2-eV band gap makes the intrinsic carrier concentration negligible at working temperatures. For a wide band-gap semiconductor, its electron mobility is good in all directions. At a given doping, the breakdown electric field was at least 2×10^6 V/cm (10× that of Si); this permitted higher doping and a thinner base region of the *p-i-n*. For a high reverse voltage rating, this gives a much-needed

lower series resistance. This would more than compensate for SiC's higher built-in junction voltage; Schottky or JBS diodes have lower junction voltage. SiC reverse recovery is faster than Si and has less charge (reverse recovery current during its time); when multiplied by the reverse recovery voltage, this would produce less power loss and generate less heat as the flyback diode for an Si-insulated gate bipolar transistor during switching. SiC lets devices operate at a higher junction temperature than Si—in theory, much higher. This permits greater power density and current density for power electronics. It also permits operation at a higher case temperature and for a given power, at a higher thermal gradient; these reduce the cooling requirements. SiC has high radiation hardness, chemical and physical inertness, and ruggedness as for thermal shock. SiC in furnace processing can grow good quality SiO_2 to protect the device. Many SiC advances are found in the International Conference on SiC and Related Materials (ICSCRM) held in odd-numbered years and in the European Conference on Silicon Carbide and Related Materials (ECSCRM) held in even-numbered years.

Grown crystal quality continues to improve and possibly will use 4° and not the usual 8° off the (0001) plane (*1*). Micropipes are open core defects and are decreasing below 0.5 cm^{-2} (*2*). However, (*3*) nanopipe closed core screw dislocations are 1000 to 5000 cm^{-2}, basal plane dislocations are $>10^4$ cm^{-2}, and low angle grain boundaries are 100 to 1000 cm^{-2} and reduce lifetime. Stacking faults are 1 to 100 cm^{-2}. Defect density must be low for reduced reverse leakage current (calling 10 mA cm^{-2} breakdown) and for increased carrier lifetimes (low forward voltage) (*2*). In devices (*4*) through (*16*), triangular defects enlarge with current. During forward operation, the *p-i-n* forward voltage was reported to drift positively, presumably because of carrier recombination generating stacking faults (recombination-enhanced dislocation glide) from the cathode side through the entire "*i*" layer (*17*). Stacking faults create a low lifetime (more resistive) region under the diode, increasing the forward voltage drop. Stacking faults can be reduced or their growth arrested by continuous growth epitaxy, by a sufficiently thick buffer layer to prevent drift of minority carriers to lower quality regions (notably the substrate/epilayer interface), by no scratches on the chip, and by carrier confinement away from sawn edges and other lower quality parts of the chip (*18*). Forward voltage instability arises from stacking faults from basal screw dislocations. However, unfamiliar growth on the (1 −1 2 0) plane could orient stacking faults to be a small fraction of the device area (*3*).

The (*19*) triangular extended defects that forward current creates are stacking faults in the (0 0 0 1) basal plane extending through the entire *n* (called *i*) base of the SiC *p-i-n* diode. Carrier recombination gives energy so partial dislocations that are the boundaries of the stacking faults move during current. Negative is often denoted by an overline bar; origin of some stacking faults is by slip of a <1 0 −1 0> dislocation in the (0 0 0 1) plane attributable to (probably shear) stress in the epilayer, forming a stacking fault bound by a

partial dislocation with Burger's vector **b** = $a/3\langle 1\ 0\ -1\ 0\rangle$ or $a/3\langle 0\ 1\ -1\ 0\rangle$, possibly nucleating from a perfect dislocation with Burger's vector $1/3\langle 1\ 1\ -2\ 0\rangle$. This gives a triangular defect with its base near or at the epilayer surface. These dislocation loops have a 90° and 30° dislocation segment with line directions along [1 1 −2 0], [−1 2 −1 0] directions and [1 1 −2 0], [2 −1 −1 0] directions, respectively, along the Pierl's valleys. Dissociation of a screw dislocation yields a C and a Si partial; one is much more mobile and moves along the Pierl's valleys $\langle 2\ -1\ -1\ 0\rangle$, so the stacking fault starts to expand like a trapezoid; then the epilayer height limits expansion to triangular. The fact that trapezoid stacking faults are sometimes outside the diode indicates different or multiple origins for the expanding stacking fault. A second origin of stacking faults is as single-layer Shockley faults with Burger's vector of 1/3<1 –1 0 0>; the built-in stress drives deformation while the electron–hole recombination provides the activation energy for motion of a leading partial dislocation which causes triangular stacking faults. Growth of the stacking fault as a single dislocation loop with a Burger's vector $a/3\langle 1\ -1\ 0\ 0\rangle$ starts at the surface and forms a rhombic or triangular fault. Dislocation loops may nucleate at threading screw dislocations and basal plane dislocations, at the top interface and at the bottom interface with the substrate. These stacking faults are formed with a higher threshold and preferably at the highest electron plasma density contact.

A second type of stacking fault is formed when threading edge dislocations with Burger's vector 1/3<1 1 –2 0> bend along the substrate/epitaxial basal plane during epitaxy, obtaining a screw character. If they are perfect dislocations, they dissociate into two 30° Shockley partial dislocations, 1/3[0 1 –1 0] and 1/3[1 0 –1 0], close together forming trapezoid stacking faults. The third, non-dominant origin of stacking faults is dissociation of dislocations along [1 –1 0 0] at the *p*-*n* interface. With Burger vector <1 1 –2 0>, these rare dislocations are misfit dislocations with a pure edge component and a large extension and are usually terminated at other (such as screw) dislocations. Sometimes, these have dissociated, as perfect 1/3[1 1 –2 0] dislocations into 1/3[1 0 –1 0] + 1/3[0 1 –1 0] Shockley partial dislocations. Future understanding and improvements are expected.

Commercial SiC Schottky diodes are beginning to compete with Si power diodes. Gallium nitride (GaN) power devices are not on GaN wafers of as good a quality as SiC and are not as developed. With high production volume and proper engineering, Si devices proved to be very reliable. Having only one isotope of Si, as in a thin surface layer, would improve its thermal conductivity slightly from 1.5 W/cm°C; we do not know of its commercial usage in Si devices. Otherwise, power devices in Si are close to mature within Si's smaller material performance parameters. Compared to Si, the higher doping in the SiC base (*20*), along with deeper ionization level of impurity giving lower ionized doping in the emitter and end regions, cause minority carrier injection from the base into the emitter and end regions to dominate forward conduction at much lower current

densities than in Si. Thus, at a fraction of rated current, the reverse recovery charge (charge in the base) stops increasing and the emitter and end region recombination currents dominate. The temperature dependence of the band-gap describes that of the diode saturation current and forward voltage.

Theory (*21*) describing reverse recovery of a power *p*-*i*-*n* diode (the base is long in Si) begins with forward current in the high-level injection state having injected a large concentration of carriers in the base region. Then the newly reversed voltage starts to sweep out most of the stored carriers at the junction edge and proceeding toward the middle of the base. An electric field is built up by this mostly swept-out space charge region. During this, carriers from the injected large concentration of the base region flow by diffusion to the lower concentration at the junction edge. There they support the maximum constant reverse current. Modeled as $V_{\mathrm{rev}}/R_{\mathrm{load}}$, this is larger than the forward current since V_{rev} is large and is many times larger than carrier recombination current. In the space charge region, the concentration of carriers is much lower than the "injected large" concentration, and the carriers travel at their maximum velocity. Then current becomes only a small fraction of that after the excess carriers in the base are swept out; recombination of remaining excess carriers in the base region causes the long tail of small current. The much higher breakdown field of SiC permits a shorter base to reduce the reverse recovery charge and time. Schottky and JBS diodes conduct as majority carrier diodes with almost no minority carriers to recombine; thus, any tail is much smaller and in SiC disappears rapidly. At 3×10^{14} cm^{-3} doping, the hole minority carrier lifetime was reported (*22*) as being as great as 1.55 μs but may be much shorter in a poorer layer between the p^+ and base in the p^+n_0n diode. Upon turn-on with a high di/dt, *p*-*i*-*n* diodes can have forward voltage overshoot before injection of the large concentration of carriers is complete, but we did not observe much. SiC Schottky and, with better reverse current-voltage, JBS diodes are designed for fast switching speed with small switching loss, low forward voltage drop, and high temperature capability; they would be favored as a free-wheeling diode in a motor drive.

An earlier description (*23*) of *p*-*i*-*n* reverse recovery notes that the impurity distribution on the *p*-doped side is more important for higher $b = \mu_e/\mu_h$, which is 3 in Si but 7.5 in 4H-SiC. Conduction carriers in high-level injection have a nearly uniform concentration, so the sweeping out of charge carriers occurs from two sides. SiC diodes for better ohmic contacts and higher mobility use *n*-type wafers; in Si, this has reverse recovery current decaying soon but slowly, and switching takes relatively longer. By application of external negative voltage, the load current in the reverse direction draws injected carriers backward and out. In the first period of time, the equal carrier concentrations are decreasing to thermal equilibrium at the *n* border of the space-charge zone; the *p*-*n* junction is still forward biased. Initially, the ratio of gradient of carrier concentrations at the *p*-*i* boundary to that at the *i*-*n* boundary is about $-b$. The concentration at the *p*-*i*

boundary reaches 0 sooner than that at the *i-n* boundary. Doping may influence its duration. The period ends when the hole and electron concentrations on the *n* border of the space-charge zone reach their thermal equilibrium so the space-charge zone has zero forward voltage. In a second period with less definite ending, the space-charge zone widens by further withdrawal of the stored electrons to the *p* side (and holes to the *n* side) at an advancing sweep-out boundary, and the *p-n* junction becomes reverse biased with the space-charge zone having almost all the voltage. In the middle of the zone with carrier concentration still at the high-level injection level (doping not dominant, especially for narrow space-charge zone), the absolute value of i_h is $i_R\mu_h/(\mu_e + \mu_h)$ and of i_e is a larger $i_R\mu_e/(\mu_e + \mu_h)$. At the moving boundary on the *p* side, i_h jumps by $i_R\mu_e/(\mu_e + \mu_h)$, sweeping out with such a current (i_e jumps by minus that). At the other moving boundary on the *n* side, i_e jumps by $i_R\mu_h/(\mu_e + \mu_h)$ and i_h by minus that. The fraction $b^2/(b^2 + 1)$ of the voltage develops on the *p* side, for Si 0.9 and for SiC >0.98. The third period has the carrier concentrations decay with almost no sweeping-out current. Practical thickness is larger than the carrier diffusion length so the decay is recombination (not a small diffusion current) with the lifetime as the time constant to the final steady state distributions. In all these periods, there is recombination and sweeping out of carriers by reverse current; if initially large, these dominate the first and second periods. The carrier concentration is larger near the *p* than near the *n* since μ_h/μ_e is less than 1. Displacement current is negligible; total current is *i*. At the *n* border ($x = d$) of the intrinsic layer, the electron diffusion current equals the electron field current at $i/2$. At the *p* border, they are + and - $(\mu_e/\mu_h)i/2$. With forward current density i_F and ambipolar diffusion length $L = (2\mu_e\mu_h kT/q(\mu_e + \mu_h))^{0.5}$, in steady state

$$n(x) = \tau\, i_F[\cosh(x/L)/\sinh(d/L) - \{(\mu_e - \mu_h)/(\mu_e + \mu_h)\}\sinh(x/L)/\cosh(d/L)]/2qL.$$

Our previous projects packaged and tested 4H-SiC gate-turnoff thyristors with flyback *p-i-n* diodes, tested JBS diodes, and compared Si and SiC diodes (*24*) through (*31*).

3. Packaging and Commonly Used Materials

Many materials are available for the manufacturing and packaging of microelectronic components, devices, and modules (see table 1). A few factors for choosing substrates and die attach materials are cost, size constraints, inter-metallic compatibility, thermal and electrical characteristics, junction operating temperature, resistance to thermal transients and mechanical shock, and the product reliability in the environment where it will be used.

Table 1. Properties of materials used to package microelectronic components.

Material	Linear coefficient of thermal expansion (ppm/°C)	Thermal conductivity (W/cm°C)	Melting point (eutectic °C)	Source
SiC	4.2 in-plane 4.68 c axis	3 – 3.8	-	Cree, Inc.
Si	4.1	1.5	-	Micrel Assoc.
aluminum nitride (AlN)	4.7	1.8	-	Marketech International
alumina (Al_2O_3)	6.9	0.25		Micrel Assoc.
AuSn (80/20)	16	0.57 – 0.58	280	Cookson Electronics and Indium Corp.
AuGe (88/12)	13	0.44	356	Cookson Electronics and Indium Corp.
AuSi (97/3)	12	0.27	363	Indium Corp.
Epo-Tek P-1011	37	0.0129	-	Epoxy Tech.

Both AlN (polycrystalline) and alumina (polycrystalline Al_2O_3) are commonly used, available, and generally economical as substrates. The major difference is the superior thermal conductivity of AlN, an advantage for applications where high temperature and thermal stress are expected.

These materials have many uses in the electronics industry, such as direct die attachment with wire bond connections, flip chip applications, and standard surface mount soldered components. Both are mechanically sturdy and can be manufactured to meet customer specifications. Additionally, they can be metallized by standard processes such as thin film deposition and thick film screening.

As with substrate materials, there are many types of die attach methods and products. A variety of commonly used eutectic Au alloy solders is available: Au80-Sn20, Au88-Ge12, and Au97Si3 as solder preforms. Eutectic AuSn is also readily available in paste form. All these Au alloy solders are useful when both electrical conductivity and a strong mechanical attachment are needed from the back side of the die to the substrate.

The AuSn melting (eutectic) temperature is 280 ºC, AuGe is 356 ºC, and AuSi is 363 ºC; these differences are beneficial when packaging must be completed in several steps. For instance, AuSi may be used for die attach, AuGe may be used to attach leads, and AuSn may be used to seal the package; this should not disturb the previously placed parts since the process temperature lowers with each alloy.

Epoxy is another material that is commonly used for packaging microelectronic devices. It is available in many forms including one-part, two-part, electrically isolating, electrically and thermally conductive, Ag filled, Ni filled, Al filled, heat cured, and room temperature cured, just to name a few. Most of these epoxies can be machine or manually dispensed or silkscreen printed onto the substrate. Some epoxies withstand temperatures as great as 500 ºC, which makes them useful die attach materials, especially for SiC devices.

4. Packaging Process With Our Choice of Materials

4.1 Substrate Material Compatible With SiC Devices

In some cases, the same packaging methods and materials that are used for Si devices can be used for SiC. However, if SiC devices are used in high power and possibly high ambient temperature applications, the operating temperature may exceed the capability of the Si packaging, and device failure would be imminent.

We conducted research, testing, and evaluation of SiC devices, especially 4H-SiC crystal. Fabrication of the module required materials that withstand high temperature and have adequate thermal conductivity away from a device to lower its temperature, improving its performance and longevity. Adequate thermal conductivity also reduces expansion and thermal shock from a device's sudden heat surge.

AlN was the substrate chosen for this module because of its physical and thermal properties. The thermal conductivity is very high, and the coefficient of thermal expansion (CTE) almost equals that of the SiC (see table 1). These characteristics maximize the thermal conductivity for direct active device attachment; this and the close match of CTE minimizes thermal and physical stress on the packaged device.

4.2 Metallization of Substrate Material

The ceramic-like AlN substrate was 2.54 cm square and 0.0635 cm thick. It was thin film patterned with Ti 30 nm, Pt 30 nm, and Au 1 μm in an electron beam evaporator system to create the anode and cathode connection pads. Layers of Ti/Pt/Au, when deposited on AlN, act as a chemically inert, thermally stable electrode to which leads, devices, and wire bonds can be attached.

The pad that connects the anode of each device was 1 cm by 1.75 cm; this is the pad used for die attach. The pads that connect the cathodes were 0.5 cm square. To prevent voltage breakdown, the connection pads are isolated by a 0.2-cm gap of exposed AlN. The module will accommodate as many as four diodes.

For complete compatibility in this packaging process, a top layer of Au is ideal for attaching the die, wire bonding, and attaching leads to the AlN package module. The back side and bonding pads of the devices being packaged were thin-film patterned with a top layer of Au. The connector leads (0.026 cm thick) were plated with Au, and Au wire was used for wire bonding. In addition, Au is an excellent conductor that does not corrode or oxidize.

Au by itself does not adhere well to the AlN substrate. However, Ti adheres very well to most substrates and metals used in microelectronics packaging; therefore, a thin base layer of Ti is deposited on the AlN. Au adheres very well to Ti, and in many microcircuits, the two metals are deposited to act as a conductor. However, in high temperatures applications, as in this experiment, the inter-metallic bond of the Ti/Au may be degraded, which could compromise the electrical conductivity. For high temperature applications, a thin barrier layer of Pt is deposited between the Ti/Au to thermally stabilize the metals.

4.3 Attaching Connector Leads

Dupont's 5087 Braze Alloy Thick Film Composition was the material chosen to attach Au leads to the Ti/Pt/Au patterned AlN. The composition of this braze is Au80/Sn20 with trace amounts of Cu and Ag; for practical purposes, it is considered eutectic AuSn. This thick film composition was chosen for its mechanical strength, electrical properties, and thermal conductivity. Even though the operating temperature of the device may exceed the 280 ºC eutectic temperature of the braze, the thermal conductivity of the AlN should significantly lower the lead-to-substrate junction temperature.

The Au leads were placed along the outer edges of the anode and cathode bonding pads on the AlN with a thin layer of the braze paste, about 50 μm. To reflow the paste, the package was heated to 340 ºC on a hot plate for 45 seconds. The package was slowly cooled to room temperature to prevent thermal stress. We removed flux residue by cleaning the package in boiling isopropyl alcohol alternated with 10-second intervals in an ultrasonic cleaner.

4.4 Attaching the Diode and Thermistor

Epo-Tek P-1011 modified polyimide Ag system was used for die attach (referred to as epoxy in this report). This epoxy was chosen for several reasons: it is a one-part system, the thixotropic paste consistency makes it easy to apply, it cures at low temperatures but withstands high temperatures, the CTE and thermal properties were acceptable, and the electrical conductivity improves rather than degrades during high temperature aging. This material withstands continuous operation at 300 ºC and intermittent 500 ºC. High temperatures were expected in this experiment, possibly in excess of 280 ºC at the

device-to-substrate junction. The improved electrical conductivity at elevated temperatures was an added advantage for our application.

A thin layer of epoxy was deposited on the AlN substrate in an area slightly less than the dimensions of the die. The device was placed on the wet epoxy and gently pushed down to ensure complete coverage on the back side of the die. Pressure was stopped when epoxy was visible around the edges of the die. The resulting thickness of the epoxy was approximately 25 μm. To cure the epoxy, the AlN was placed in a bench top oven for a total of 90 minutes. Curing begins with a 30-minute prebake at 80 ºC, immediately followed by the final bake of 60 minutes at 150 ºC.

A thermistor, used to measure the module temperature during operation, was attached to the top surface of the substrate with Epo-Tek P-1011 epoxy. The reasons for choosing this material were basically the same as those for using it as a die attach. Additionally, P-1011 works well to bond dissimilar materials. This was critical since the thermistor was made of a glass composition and was being attached to a Au surface. In this application, the electrical conductivity was not an issue.

For temperature accuracy, the thermistor should be placed as close as possible to the diode. However, since high voltage was introduced during circuit operation, the thermistor was placed on the substrate approximately 0.76 cm away from the diode to prevent voltage breakdown between the two components. Attachment of the thermistor and the diode to the AlN used the same technique; they were attached and baked at the same time.

4.5 Wire Bonding

Once the diode was attached to the AlN module, electrical connections were made from the anode to the pads where connector leads had been attached with Au/Sn braze. The connections were made with 25.4-μm Au wire by a Kulicke and Soffa Model 4124 Ball Bonder. The cathode is the back of the diode and is directly attached to the module, so wire bonding is only needed on the anode.

Each strand of 25.4-μm Au wire is capable of carrying 0.5 A at ambient temperatures. The expected operating current of this diode was 10 A, and the operating temperature may have exceeded 150 ºC. Because of the elevated operating temperature, we de-rated the current carrying value of the Au wire and placed 36 wire bonds per device on module3 and module4 (see figures 3, 5, and 6). The bonds were made in a symmetrical pattern for even distribution of the current flow across the device surface. In addition, they served as a precautionary measure in the event of an unexpected current spike.

4.6 Lessons Learned From Previous Device and Packaging Evaluation

Using an alumina module that was thin film patterned in the same manner as previously discussed, we packaged a high power SiC gate turn-off thyristor (GTO). AuSn braze was used for die and lead attach (see figure 1).

After only a short operating time, the module suffered a catastrophic failure. Upon examination of the failed GTO module, we found the device suspended above the alumina with all the wire bonds still intact. However, the alumina was cracked and the origin appeared to be centered under the GTO. Given the fact that neither the device nor the wire bonds were damaged, it is believed the high operating temperature of the GTO caused thermal stress on the alumina. It is also believed that the device temperature exceeded 280 ºC since the AuSn eutectic braze had melted and released the GTO, seemingly undamaged, from the substrate. If the braze had not melted, the GTO would have remained attached to the alumina, and the device would also have cracked rather than detach from the substrate in one piece. This appeared to be a classic example of poor thermal conductivity on the part of the alumina.

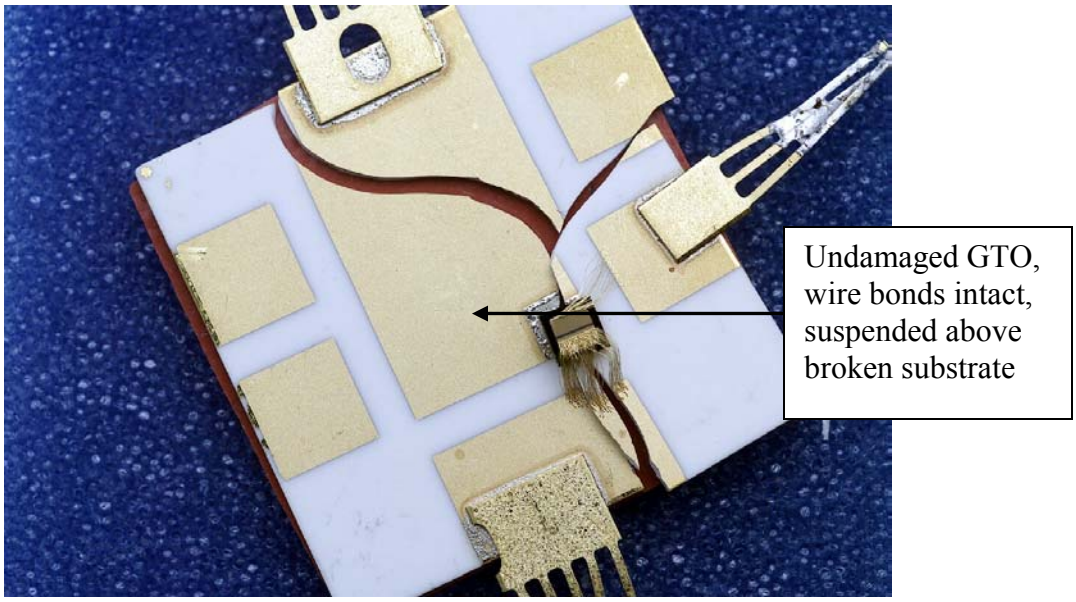

Figure 1. Results of poor thermal conductivity. (SiC GTO thyristor on alumina module.)

AlN was the next choice for substrate material after the GTO on alumina module failure. The thermal conductivity of the AlN that we used for this module is about 7 times greater than alumina, and the CTE is a close match to SiC. The AlN module was thin film patterned in the same manner as previously discussed. On this module, we packaged two high power SiC diodes (see figure 2). When the module was initially packaged, the two

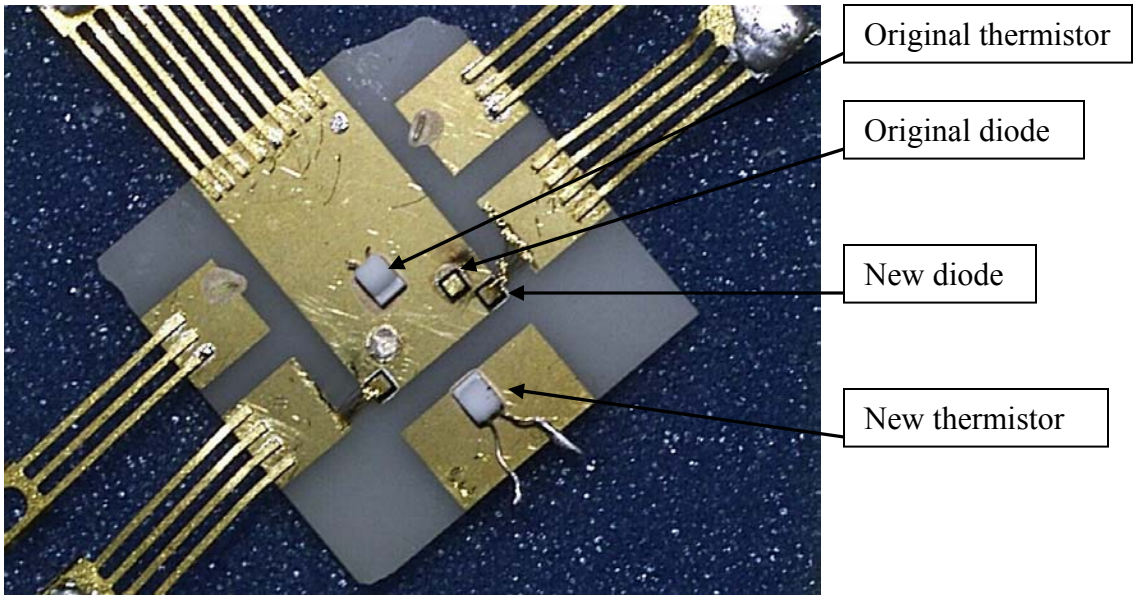

Figure 2. Reworked AlN substrate, diodes originally attached with AuSn, reworked with epoxy.

diodes and the leads were attached with AuSn braze. A thermistor was attached with epoxy (center of module, leads were cut off at a later time).

Device failure occurred during initial testing. Both diodes literally blew off the module, leaving charred discolorations in the areas where the wire bonds had hovered over the metallized substrate. One of the diodes had detached from the AlN (leaving the shiny circle of braze near the bottom left corner of the larger pad). This was a sure indication that the temperature at that junction had exceeded 280 ºC. The good news was that the AlN withstood the high temperature and thermal stress without cracking, unlike the alumina.

We determined that several factors might have led to the failure of these devices. One cause might have been voltage breakdown between the anode and cathode of each diode, since the wire bonds from the top side of the devices were hovering over the cathode pad. The small air gap, formed by the curvature of the wire bonds, may not have been enough to withstand the 600 V that were applied to the devices. Another possibility was that the operating temperature of the devices was so hot that they simply self-destructed, since the devices were operating in a thermally uncontrolled environment, with no efficient means of drawing heat away from the package. A temperature reading was not being monitored by the thermistor so the actual temperature of the package is unknown. However, we know that at least one of the diodes exceeded 280 ºC because the device detached from the braze and substrate. Also possible, but not probable, was that a breakdown path may have been present where the leads of the thermistor hovered above the cathode pad.

Considering all the possibilities for device failure, the AlN module was reworked with two new diodes. The diodes were placed at the edges of the cathode pad to eliminate the problem of the hovering wires; only bare AlN was underneath the wire bonds (see figure 2). A new thermistor was attached on a separate pad, where its leads would not be close to the diode connections, to eliminate the possibility of voltage breakdown. The leads from the original thermistor were removed. All attachments were made with the epoxy since it would withstand continuous temperatures of 300 ºC. The defective diode that did not lift off when it failed remained on the module; however, the wire bonds were removed.

The reworked module was placed in the test circuit; this time, a thin layer of heat sink compound was applied to the back of the module to improve heat dissipation. The module was secured to a flat metal plate. The thermistor was connected to a circuit that would monitor the module temperature. The new devices successfully operated at 600 V and 4 A per diode. The temperature of the module was maintained at 150 ºC.

Several important lessons were learned here. Avoid placing a diode in a location where the wire bonds will hover above the cathode connection pad (back side of the device). Ensure that adequate heat dissipation is provided for packaged devices, and monitor the temperature of operating devices so the circuit can be shut down if the temperature exceeds a safe level. Figure 2 shows the reworked module with two new diodes placed at the corners of the large pad. The air gap of 0.2 cm, with no metallization under the wire bonds, proved to be adequate for preventing voltage breakdown of these diodes.

Another lesson learned dealt with the adhesion of the thin film Ti/Pt/Au metallization to the AlN substrate. In earlier experiments, we used AlN that was polished with a 2-µin. finish and had a glass-like smoothness. Repeatedly, when physical stress was applied, the leads that were attached with the AuSn braze popped off the AlN. Our initial thought was that the AuSn braze had poor mechanical strength. However, upon examination of the leads and substrate we, noticed that the Ti/Pt/Au had completely detached from the AlN and was clinging to the braze on the leads. This clearly indicated poor adhesion of the thin film metals to the substrate. This problem had not occurred when alumina was used as a substrate. Though the degree of polish on the alumina was unknown, its appearance was a much less smooth, matte finish.

We began using AlN that was polished with a 20-µin. finish, having a matte appearance similar to the alumina. The adhesion of the Ti/Pt/Au was greatly improved. We believe the improvement was attributable to the rougher toothed surface of the 20-µin. finish. During thin film deposition, the evaporated metals naturally filled the crevices and allowed the metals to grab into the substrate. It is possible to pull the metallization and brazed leads off this substrate by applying excessive force. However, pieces of the AlN will be broken off and will cling to the metals on the lead.

Trial and error brought us to the module packaging process that was used to successfully package, test, and evaluate the SiC diodes shown in figure 3. The diode test results and operation of this module are discussed further in this report. The devices are the same type of diodes that were packaged in figure 2.

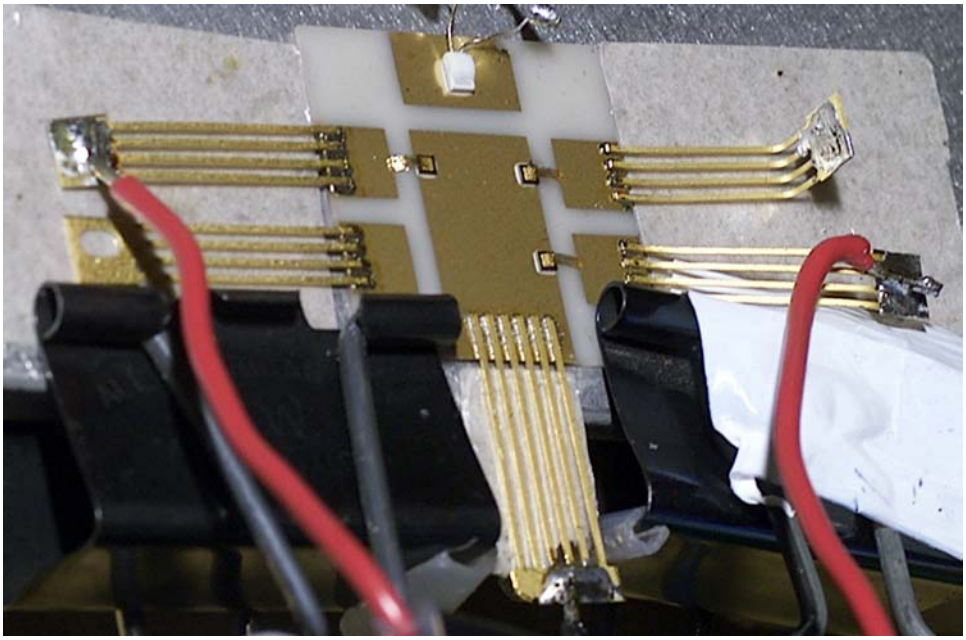

Figure 3. Completed module in test setup. (Substrate is AlN, diodes attached with epoxy, leads attached with AuSn braze.)

Though the thermal conductivity of the epoxy used for die attach is in fact very poor, it withstood the high operating temperature of the diodes and sufficiently transferred heat away from the devices. The high thermal conductivity of the AlN substrate proved to be adequate for dissipating heat from the operating diodes.

4.7 Heat Sink and Encapsulation Materials

Packaging these SiC devices required that we explore suitable packaging materials. In some cases, the same packaging methods and materials that are used for Si devices can be used for SiC. However, when SiC devices were used in high power and possibly high ambient temperature applications, the operating temperature exceeded the capability of the Si packaging and failure was imminent. Therefore, for SiC devices to be commonly used, packages of materials that will withstand elevated temperatures and –55 ºC must be engineered and readily producible. We packaged high power SiC diodes on AlN; this work was done to demonstrate the performance of such diodes, which operate with junctions as hot as 300 ºC.

For heat flow, mounting, and encapsulation of packaged devices, some materials and their properties are as shown in table 2:

Table 2. Properties of materials considered to test microelectronic components.

Material	**Linear coefficient of thermal expansion (ppm/°C)**	**Thermal conductivity (W/cm°C)**	**Breakdown field (V/cm)**
AlN	4.7	1.8	125,000
alumina, various purity	~6.9	0.15-0.2, rarely 0.33	94,000
SiC wafer 25 °C 100 °C 227 °C 4H	4.2 in-plane (4.68 c axis)	3.8 n^- 2.9 n+ 2.3- 2.8 1.8 n^- and n^+	2,400,000 parallel to c-axis
4460 epoxy	64	0.0058	218,000
1531 silicone encapsulant	soft	0.0029	197,000
heat sink compounds: AOS HTC-61 silicone	grease, to 205 °C	0.0258	133,000
AOS 52027	grease, to 350 °C	0.0075	115,000
Electrolube HTSP silicone	grease, to 200 °C	0.03	180,000
AOS 57000	grease, to 200 °C	0.0721	conducts
materials considered with the package: Fluorinert 5312	liquid, boils >200 °C	0.007	157,000
air	-	-	30,000
Al	25	2.37	conducts
Cu	12	4	conducts
water	-	0.0065	conducts
diamond		>13	high

To obtain a large area for current conduction, our diodes were vertical through the SiC, so it was doped and not semi-insulating. Thus, unless in depletion such as in reverse bias, SiC material near devices would conduct and lack this high breakdown field. From

AOS[1] a heat sink compound HTC-61 was later used. Its thermal conductivity was about as high as available but much lower than that of adjacent materials mounted as the thermal conduction path, so a layer should be just thick enough to be continuous at an interface. The Cotronics 4460 epoxy overcoat-encapsulant for electrical insulation withstands 315 °C and overcoated the later testing of module4. The Cotronics 1531 silicone withstands 343 °C continually and 427 °C briefly; it was rubbery with usable but weak adhesion. It was a final coat on the very last measurements of module4 and permitted testing to –1200 V. The liquid Fluorinert 5312 has a high breakdown field, and since it must be "walled in" to displace air, it was only used to test non-encapsulated chips above 600 V at room temperature. Krytox 16350 is more viscous at 3500 centistokes. The outer package of fielded devices might be cooled by motor oil; transformer oil conductivity is 0.018 W/cm°C.

AlN and our direct device attachment give adequate thermal conductivity—a critical property for high power SiC devices that operate at high temperatures. Thermal conductivity of SiC is notably high and like other semiconductors, decreases slightly faster than 1/(absolute temperature); electrically semi-insulating SiC would have economically limited, specialized applications. Materials such as polycrystalline diamond or diamond-like films have even more impressive properties for a heat spreader close below the chip but are far from commercially available or economical. Pb-free is a future consideration.

5. Electrical Testing

5.1 General and *p-i-n* Diodes

We project that a SiC diode's package in future power electronics will be cooled to 150 °C. Then its junction temperature will be perhaps 200° to 250 °C if such operation proves reliable. The properties of SiC would enhance the reliable performance of power electronics designs. Thus, we examined both the performance to 150 °C and some of the vital durability. The diodes in parallel should share equally both forward current and reverse recovery current as a function of time; this would permit use of practically all of the rated current. Diodes should have parameters such as the current-voltage curve narrowly distributed originally and only slightly shifted during operation. Diodes should be reliable and rugged, especially during voltage and current transients.

Cree, Inc. grew our SiC crystal and their epitaxial layers then fabricated the *p-i-n* (and the JBS) diodes, 0.1 cm square, each on a 0.14-cm square chip. The *p-i-n* were rated 1200 V reverse and 5 A forward, but we attempted to be less than 600 V and 4 A of constant

[1] Not an acronym.

conduction. SiC *p-i-n* diode chips on a module were electrically tested for reverse recovery and basic durability. An inductive "ring-down" reverse recovery apparatus was used to measure sharing of forward current and reverse current; changing the load resistance or the voltage would change the current. Late in this testing, a printed circuit board was used for other than the resistor and inductor. Reverse recovery was measured at various voltages, currents, and temperature to 150 °C. Currents near the rating of a diode would have practical use and were emphasized. Another test apparatus was a 100-kHz DC-to-DC buck converter on a printed circuit board with an inductor capable of accepting to 500 V and outputting to 100 V (5 to 1 reduction) and to 10 A; brief operation was used. JBS diodes have closely spaced, alternating stripes of Schottky junction and *p-n* junction. Forward constant voltage in other JBS diodes has the Schottky areas conduct at almost as low a voltage and with comparable low series resistance as would an all-Schottky diode of the same diode area. Reverse constant voltage expands and merges horizontally together the *p-n* junctions' individual depletion regions. This is almost the depletion of a reverse biased *p-n* junction, and other JBS have almost the same low reverse leakage current and high breakdown voltage. For our JBS the DC-to-DC buck converter was used for brief running times.

A module had two *p-i-n* diode chips mounted, diode 1 near the left and diode 2 near the right edge. A small thermistor (RTD, Omega F3105) was mounted near the middle of the top edge. A curve tracer first tested and recorded the current versus voltage curve of each diode in a module to 4 A (at 3.75 to 3.9 V forward, within 20 seconds reached at least 100 °C) and to 600 V reverse at 5 μA/division for leakage. Two medium bindery clips then clamped the module to near the edge of the hot plate; the clips were insulated from the cathode connection. A heater on the length of the rear of the hot plate could raise it to a selected temperature. The hot plate was a Wakefield aluminum chill plate (not liquid cooled), 30 cm by 12.7 cm by 0.635 cm thick with sides. The module had been designed for heat removal from the rear, but heat sink compound would have let it move and slide off the plate; therefore, it was not then used under the *p-i-n* module.

For diode reverse recovery measurement, the circuit in figure 4 had the power supply's positive voltage connected to the cathode and to the load resistor in series with the inductor, initially 1 mH with an iron core. An inductor measured to go through zero inductance at a higher frequency would make less of a possible contribution to ringing or have high impedance; later ones were ferrite. The anode went to the nMOS (*n*-channel metal oxide semiconductor) transistor drain and to the other end of the inductor; the MOS source and the power supply's negative were at ground potential. The power nMOS was Directed Energy/ IXYS Inc. DE475-102N21A rated 1000 V, 21 A, and 30 MHz, adequate if properly heat sinked. A 13-kΩ resistor, later 1.2 MΩ, from gate to source prevented static overvoltage. The 2-cm by 1.85-cm thermally conductive area of the

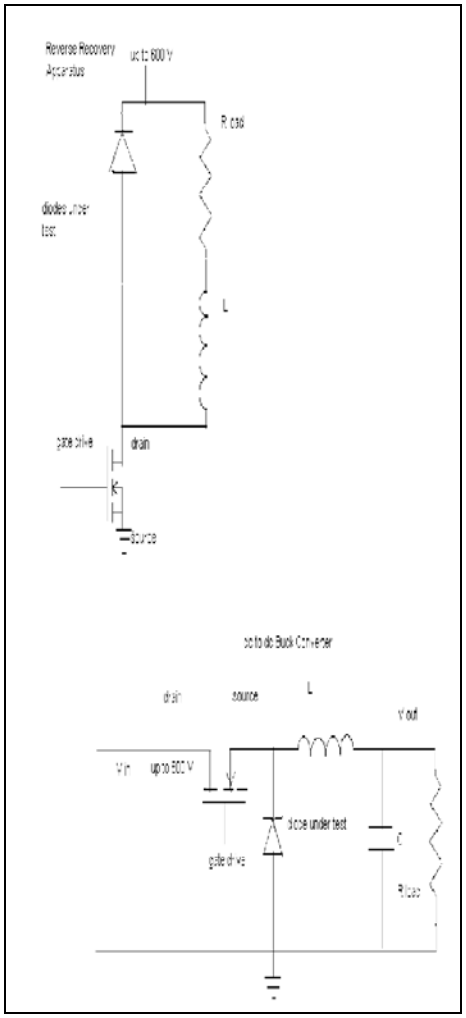

Figure 4. (Upper) circuit for reverse recovery and (lower) circuit for DC-to-DC buck converter.

MOS was initially on an air-coolable heat sink 12 cm by 5 cm by 1.1 cm high with 10 fins; it rises by natural convection, 5.3 °C/W and at 250 linear feet/minute 2.2 °C/W.

By module2, the gate-to-source voltage was wired to a different source tab than was the drain-to-source voltage. The signal generator had a 100-ns rise time and fall time. Simple hard switching was performed; its stresses should have been within the specifications for the SiC diodes. When the MOS was pulsed on for 588 μs, the inductor current increased to near its steady state $V_{\text{supply}}/R_{\text{load}}$; then the MOS was turned off for about 4.7 μs. The slight decrease of current in the inductor as $\exp(-R_{\text{load}}\, t/L)$ developed across the inductor a voltage forward biasing the diode. The inductor current free-wheeled in the forward direction through the diode and through R_{load}. Then the MOS

was pulsed on again for 588 μs and the diode reverse recovered to forward current; this current waveform shows reverse recovery. The two brief pulses, when not repeated for a while, did not generate noticeable heat energy in the diode. The main DC power supply had its output voltage stiffened near the diodes by two in-series 1100-μF electrolytic capacitors 550C112T450 with in-parallel two 0.1-μF ceramic capacitors. A Tektronix model TDS[1]5104 digital oscilloscope measured to 1.25 gigasamples/s per each of four channels. Tektronix model TCP[1]202 current probes were rated DC to 50 MHz or 7-ns rise time and had a 17-ns internal delay to the output. Perfluoroalkoxyl Teflon[2] tubing around the conductors to the diodes ensured enough insulation at temperature for the current probes. The differential voltage probe P5205A was rated DC to 100 MHz and 7 pF.

Unlike Si, SiC diode reverse current and reverse recovery charge did not rise much with temperature. A fully reverse-biased diode junction may have added some of the capacitance for minor ringing. In a reverse recovery apparatus, different causes of currents give distinctive shapes of current (*32*); a pure capacitive load is damped oscillation, MOS gate bouncing is lopsided, and reverse recovery has a negative area more constant than oscillating.

The gate drive resistor and thus the fall time of the current were minimized consistent with moderately little ringing. Improvements of apparatus did not seem necessary to obtain data when measurements were taken. Experience showed future efforts where apparatus could be further optimized. A reverse recovery apparatus should be for high power and for high frequency of at least 0.35/(risetime 10% to 90%) or a few tens of megahertz and for JBS diodes higher. At frequencies observed, the current was confined (the skin effect) to near the surface, increasing the resistance and impedance. Off-module connections of stranded wire large enough in diameter for tens of meters at 60 Hz would in retrospect have been replaced by high current traces of wide Cu strip. A HP4194A gain-phase analyzer measured the impedance versus frequency and the frequency at which it went through zero for passive parts like the inductor. The overall layout could carefully route the returning high current to be directly over or under that outgoing current for reduced loop area and inductance. A DC-to-DC converter (*33*) needs "lay out separation of the ground path of output R to output C, the path output C to diode (to inductor), and the path diode to MOS to input. Each has different spectral behavior; each carries high current."

The MOS contacts are aluminum-like 0.78-cm wide drain tab and gate tab and four 0.41-cm source tabs spreading current for acceptably lower impedance. Copper strip connections could be made to them. Current could flow among multiple MOS in parallel

[1]Not an acronym.

[2]Teflon® is a registered trademark of E.I. duPont de Nemours & Co., Inc.

so that each would not fail below 1000 V. For shorter connections, a compact heater must be situated nearby, such as vertically above the circuit board, and a water-cooled plate for MOS and the module must be near the other components. This could be in the middle of the circuit board.

Just before reverse recovery, module2 with negligible heat sinking and 6.9 Ω load at 50 V had in the left diode 0.4 A and the right in parallel 0.8 A; at 100 V, 1 A and 1.45 A; at 150 V, 1.6 A and 2.2 A; at 200 V, 2.1 A and 2.9 A; at 250 V, 3.1 A and 3.4 A; and at 300 V, 4.1 A and 3.8 A, becoming closer but not equal enough. For 75 °C mounting plate and 200 V, the left diode was 2.5 A and right 2.1 A; it was soon remade into module3. For module4 at 450 V and 150 °C, the left diode went from constant 3.4 A to 0 A at -30 V in 28 ns, then to peak –8.48 A at 133 V in 44 ns more, then up to 0 A at a 492-V brief peak in 41 ns more with negligible current tail.

The DC-to-DC buck converter circuit is also in figure 4. To give DC output voltage 1/5 of the DC power input voltage, the clock signal turned the power MOS transistor on for nominally 20% of the time, and the diode reverse recovered then continued to be reverse biased. The inductor current increased. When the MOS was turned off, the slight decrease of current in the inductor developed a voltage across the inductor to put forward bias on the diode, so the inductor current took the available path of forward through the diode (free-wheeling in the closed loop of the inductor and diode). The MOS source voltage was at the DC power input voltage for 2 μs and practically -3 V for 8 μs, changing rapidly between these voltages. The gate voltage was on top of this source voltage, necessitating batteries as a floating power source.

Capacitors stiffening the main DC power supply included two 1100 μF in series. In parallel with these was a 0.1-μF ceramic disc capacitor; its equivalent series resistance was less than 0.1 Ω and its capacitance went through 0 at 2.4 MHz. Between the power supply and ground pins of the IR4427 gate driver was 0.1 μF in parallel with a 0.01-μF ceramic disc; its capacitance went through 0 μF at 10 MHz.

A 2-μF polypropylene pulse capacitor 940C10W2K went through 0 μF at 480 kHz; the DC-to-DC buck converter's output was across one in parallel with two 0.1 μF. The DC-to-DC converter's 500-μH inductor was rated to decrease a slight amount at 7 A, which should have been more, and went through 0 μH at 1.04 MHz. Allowing some for the series impedance of the inductor, the current free-wheeling forward through the diodes saw R_{load} less than 100 Ω so the current decrease as $\exp(-R_{\text{load}}\, t/L)$ would be small during the reverse recovery time of as much as 100 ns. The DC-to-DC buck converter's optocoupler was briefly Agilent A3101 (rated to 0.4 A), with a power supply of two 9-V batteries in series stiffened by a 0.1-μF and two 0.01-μF capacitors.

The DC-to-DC converter was re-arranged onto a custom printed circuit board to reduce stray inductance and to be mechanically portable. Module2 initially was run continually while the supply voltage was manually turned up from 0 V in several seconds, but diode heating was excessive because of the poor heat sinking. On a 75 °C hot plate with the left diode alone at 135 V and 2 A, the thermistor soon reached 100 °C; at 195 V, it soon reached 113 °C, and at 250 V, it soon reached 150 °C. Heat flow dissipated somewhat before reaching the thermistor, so it reached a lower temperature than the chip temperature. Roughly calculating, 3.8 V forward at 4 A gave 15 W; this was dissipated over a SiC chip area 0.14 cm square or 0.02 cm^2 for 750 W/cm^2. Taking thermal conductivity at temperature as 2 W/cm°C meant a 370 °C/cm gradient across thickness 0.063 cm for a rise of 23 °C through the thickness of the chip.

Module2 received a new left chip and was renamed module3. It was operated for just enough cycles (11 then 19) of the 100-kHz pulse to settle toward steady state but not noticeably heat the module. At 400 V, the left diode began at 4 A and ended at 3.6 A (–6.25 A reverse peak); the right began at 4.2 A and decreased faster to end at 3.1 A (–4.9 A reverse peak). A diode on the curve tracer had approximately a 0.2-V knee below the listed forward voltage, above which the current was significant and fitted with the listed resistance. The left forward was fitted as (the slope gave this resistance) 2.8 V + 0.25 Ω, at 3.8 V, 4 A; the right was 2.8 V + 0.31 Ω, at 4.05 V, 4 A. Reverse at 600 V was at most 0.5 μA for each; unacceptable would exceed 10 to 20 μA. Reverse was also fitted with a knee voltage and series resistance.

At 400 V, the left diode had a 4.3 A peak, and the right had a 3.5 A peak and soon blew; the old right diode on the curve tracer at 300 V reverse was a leaky 15 to 20 μA and saw Au beginning to be lost at edge or corner. Cree, Inc., did not adequately passivate the chip top near the edge, so our not-well-cooled chip reached high temperature and Au began to creep back away from the edges. Also we saw melted wires there (see figure 5). The diode was replaced and the module renamed as module4. At the within-rated currents used, the chips' performance otherwise was reasonably durable, unless our wire bonds also melted because of overheating in our module.

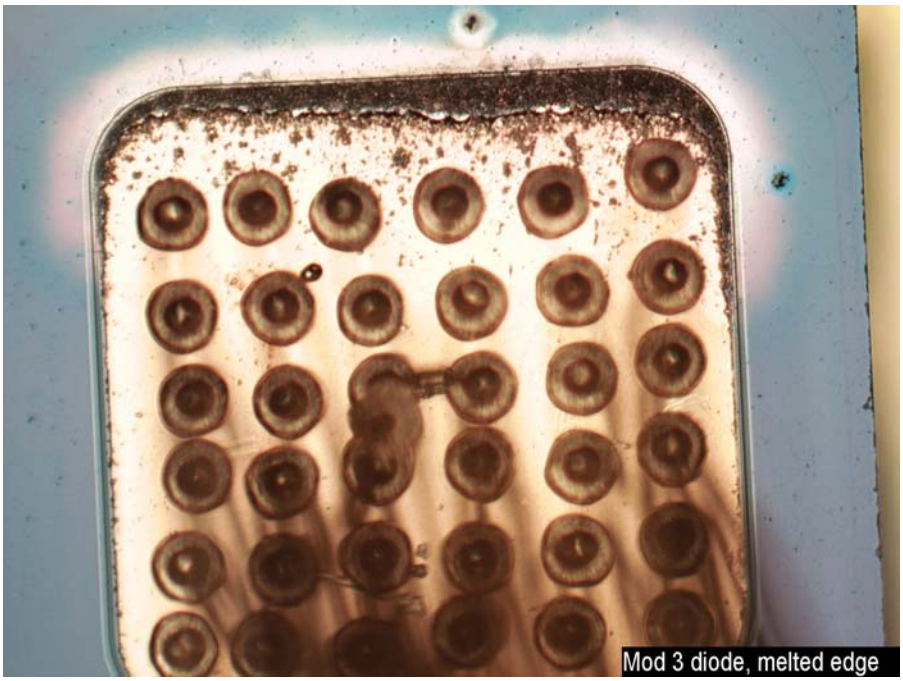

Figure 5. Module3 diode, Au melted from edge.

Module4 was operated for 19 cycles of the DC-to-DC converter, with a 13.7-Ω load at up to 450 V at 25 °C hot plate; then at 450 V, the diodes were 25 °C, 75 °C, 100 °C, and 150 °C at which the left diode had a broad peak of 3.9 A and ended at 3.5 A, and the right had initial peak 3.7 A and decreased to 2.3 A. Current was not shared equally by the diodes; the left forward current initially spiked to at least 2.5× the final value (exchanging the left and right wires attributed this to that diode) and settled by cycle 19. The right initial spike was only twice the final value. Module4 was operated continuously; the MOS transistor with no fan on the circuit board failed in 2 minutes at 350 V.

At 300 V and 83 °C, the left diode current began at 2.2 A, increased to 2.9 A, at 7.7 μs was a final 2.6 A, then in reverse recovery had an -8.4 A peak; the right initial 3 A decreased to final 1.4 A and reverse was -3.4 A peak. The diodes consistently had unequal current and at least the right had an initial spike. The left diode at 500 V reverse leaked 7 μA.

Module4 for brief 19-cycle operation at 400 V was as shown in table 3.

Table 3. Module4 at 400 V.

Forward (A)	Reverse peak (A)	Q_{rr} (nC)	t_{rr} (ns)	Reverse recovery energy (μJ)	Peak (W)
25 °C left 3.2	–5.6	162	64	25 (if 100 kHz 2.5 W)	1600
right 2.3	–3.6	122.8	47.7	14	800
75 °C left 3	–6.4	266	64	44.6	2200
right 2.3	–5	204	67.5	25	1100
100 °C left 2.9	–7.4	319	70.9	55	2500
right 2.4	–5.6	250	73.8	32	1300
150 °C left 2.8	–8	418	87	76	2900
right 2.4	–7.1	418	85	76	2800

Note the Q_{rr} increased to 2.6× and 3.4× from room temperature to these temperatures, the t_{rr} increased to 1.36× and 1.78×, and the reverse peak/forward current ratio increased from 1.75 and 1.56 to 2.9. In this example, the diode performance was not production-worthy but at 150 °C the parameters became closer to equal, and it was not near failing. Unlike Si, the reverse recovery charge and DC reverse leakage current did not increase far more to be out of useful bounds. A few other cases with much worse peaks of reverse current and power could overheat the local junction and possibly lose durability. Continuous operation overheated the MOS and caused high temperature of the diodes; a cooling fan was explored. The left diode at 600 V reverse leaked 10 μA but cooling of the MOS needed more than convection. An 11-cm Papst 4600X fan rated at 20 W was added parallel to the MOS heat sink fins; continuous operation at 300 V made the diodes reach 111 °C in 20 minutes, and at 350 V, they quickly reached 160 °C. The diode junction was obviously at a higher temperature. The left diode reverse on the curve tracer increased to 7 μA curving up at 500 V, so we did not go higher.

A WS81 thermistor was bolted at one side of the MOS so it may have read low. The MOS heat sink's bottom was raised 0.3 cm above the circuit board to be in the air flow. This planar test assembly had non-potted (non-encapsulated) diodes on an AlN module on a non-heated hot plate. Air cooling would remove diode heat from near where it was generated and was mistakenly thought to be effective. Fans considered were ComairRotron Major (235 cubic feet/minute or 0.8-inch static pressure no-flow, 1320 linear feet/minute, 30 W) and Tarzan (350 cfm or 0.8 inch, 1450 lfm, 90 W), and a Dayton centrifugal blower (980 cfm or 1.05 inch, 3500 lfm, 455 W). A ComairRotron Major fan 7 cm from the MOS cooled better with flow angled down 25°.

We photographed the new, lower right diode of module4 (see figure 6).

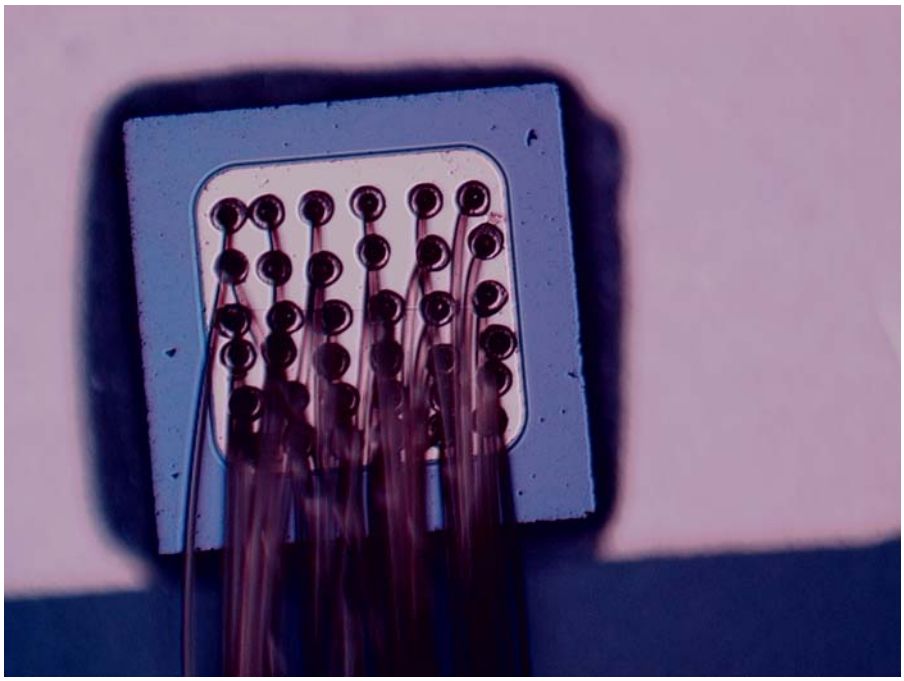

Figure 6. New, lower right diode of module4.

Air cooling was only gradually increased; continuous operation to a few minutes with heat removal by air cooling was used. A module clamped on the hot plate without heat sink compound was not well coupled to its thermal mass. At 300 V one Major fan 7 cm from the MOS and only tangentially on diodes made the MOS 31 °C and diodes 72 °C. At 350 V in 20 minutes, temperatures were MOS 35.5 °C, diodes 90.5 °C and currents left 3.2 A and -8 A peak reverse, right 3.5 A and -3.6 A, total 6.2 A (decreases linearly to 4.6 A at end of forward) and –11.5 A. On the curve tracer, the left reverse at 400 V was 5 μA, at 500 V 5 μA, and at 600 V 14 μA. At 400 V, the diode soon neared 150 °C, so the one Major fan was angled to include the diodes. At 350 V, the MOS was soon 48 °C and the diodes 116 °C; then on the curve tracer, the left reverse at 300 V was 10 μA which was getting worse; the entire experience was that the diodes in reverse were not always stable. During all testing performed, the *p-i-n* diodes had forward curve tracer curves (not in-circuit performance) basically stable and similar, which is necessary for parallel sharing of current or as standard parts.

One Major fan on the MOS and one on the diodes at 300 V gave stable 38 °C MOS and 91 °C diode, at 320 V 37 °C and 106 °C, but at 340 V the diodes sharply increased within 30 seconds to 160 °C. Diodes were acceptable on the curve tracer, then in the DC-to-DC converter would stay at stable temperature, so this degradation apparently went away. These diodes were not stable within claimed specifications; for production quality, the worst case measurements should have parameters with at most 1/3 of the variation usually observed. Reduction of such observed incidents of poor performance to a very

few per million or billion diode hours would be preferable. The old left diode no longer used was measured on the curve tracer as working with little reverse leakage. A Major fan on the MOS and a Tarzan on the diodes gave at 300 V the MOS 32 °C and diodes 66 °C; at 320 V, 34 °C and 71 °C; and at 340 V, 38 °C, and 77 °C. At 300 V and 83 °C, currents for the left diode were 2.2 A initial forward, soon settled to 2.8 A, 2.6 A final, and -8.4 A reverse recovery peak, and for the right were 3 A initial, 1.4 A final 7.7 μsec later, and -3.4 A. At 340 V, the left maximum was 3.4 A and –8.8 A, right was 3.4 A and –3.6 A, total 5.8 A, ending at 4.6 A and –12.5 A. The left at 600 V reverse increased to 9 μA then 14 μA leakage. Even though brief, a peak reverse recovery current notably higher than the forward current meant a power loss undesirably many times larger. A minority of diodes at least sometimes developed this.

Each channel had its vertical sensitivity increased to use most of the oscilloscope's 256 vertical digitization levels over 10.24 graticule divisions. Horizontally, as many as 12,500 continuous sampling points were used, and 1 μs/horizontal division displayed one cycle of operation. The oscilloscope briefly measured and averaged 100 (later 50) sweeps to minimize noise to within digitization error; this was a less successful attempt to measure somewhat accurate forward voltage. Continuous operation at 340 V with diodes 75 °C was recorded. Forward voltage exceeded 19 V for 18.4 ns and 10 V for 53.2 ns; the left diode began at 2.8 A, reached a broad peak of 3.4 A, and ended at 3.05 A; the right diode began at 3.4 A and decayed with 1 μs time constant to end at 1.58 A. The total current began at 6.05 A and ended at 4.6 A. Current sharing in the diodes in parallel was not good in steady state or as a function of time during a cycle in the circuit. Improvement at least in steady state would be required for high volume production and use. Well-behaving SiC diodes and their smaller reverse recovery charge reduced a significant to dominant portion of the diode heat generated. The left diode was -8.6 A peak, Q_{rr} 452 nC, 169 ns, and 22.5 W average; the right diode was -3.5 A, 192 nC, 217.6 ns, and 9.9 W. In the DC-to-DC converter the intervals and power loss during them were as shown in table 4.

Table 4. Contributions to power loss.

Interval	Left during this (W)	Contribution to total (W)	Right during this (W)	Contribution to total (W)
forward I and V	13	10	5.5	6.4
forward I, reverse V	21	0.67	8.3	0.02
reverse I and V (rev rec)	462	7.8	106	2.3
little I, large reverse V	21.2	4.6	5.6	1.2

When peak reverse current increased 2.45×, the contribution to reverse recovery power loss increased by 3.4×. At 375 V with each diode less than 4 A at 83 °C with a Tarzan

fan, the MOS failed at 38 °C after 2 minutes with a Major fan. The diodes were acceptable forward and at 600 V reverse with the left 3 μA, right 0 μA. The MOS heat sink was improved (Wakefield 395-2AB 14 cm by 12.7 cm by 6.35 cm high, 12 fins down, 8 fins up, convection 0.9 °C/W natural, 0.32 °C/W at 500 lfm). More effort prevented the MOS from burning up; on the curve tracer the left forward was 2.8 V + 0.26 Ω, 3.85 V, 4 A; right was 2.8 V + 0.26 Ω, 3.85 V, 4 A; left reverse 500 V <0.5 μA, 600 V, 3.2 μA slightly better; right 620 V <0.5 μA. After the end of this work, the MOS was placed on a water-cooled plate.

We changed batteries to two 12 V in series for abundant long-lasting gate voltage and optocoupler to Agilent HCNW3120 so the MOS reached fully on (rate of rise was controlled to reduce ringing) to minimize its conduction heat loss. The MOS gate was driven through 25 Ω and then later 50 Ω for less ringing. Module was reworked with a new thermistor; the left forward was 2.7 V + 0.28 Ω, at 3.8 V, 4 A; right was 2.8 V + 0.3 Ω, at 4 V, 4 A. The left reverse was at 350 V, 0 μA; at 400 V, 1.5 μA; above 420 V, 18 MΩ slope; 600 V, 10 μA was not the worst; right was 600 V <0.5 μA. Module4 for 350 V quick continuous operation diodes had a peak 190 °C and current ended left 4.3 A and right 2.3 A, reverse peak was left –17.1 A with 80% of diode's energy loss there and right –5.6 A with 50% of diode's loss there.

With a centrifugal blower on the diodes (no heat sink compound, thermal mass of hot plate was not contacted) and a Tarzan on MOS, an averaging of 50 sweeps to minimize noise needed operation for 20 to 30 seconds to stabilize. The diodes at 300 V exceeded 150 °C seen 5 seconds after reduced voltage to 0, and at 350 V exceeded 190 °C or so, which affected them. Even the Dayton blower did not air cool as much as desirable. Curve tracer measured left forward 2.8 V + 0.31 Ω, at 4.05 V, 4 A; right forward 3 V + 0.3 Ω, at 4.2 V, 4 A; the left reverse 420 V + 26 MΩ, at 400 V, 0.5 μA; at 600 V, 7 μA was slightly better, and right reverse 600 V <0.5 μA.

Module4 at 350 V the diodes forward conduction began rising slowly, the left as 4.25(1-exp(t/1 μs)) A and the right as 7exp(-t/2.5 μs) A reaching 2.2 A so current shifted rapidly to the left diode; total current decreased slowly and current sharing was unequal. Left diode had Q_{rr} 1642 nC and t_{rr} 297 ns with 3× the reverse current and 6x the reverse recovery power loss as the right, and right diode had 464 nC and 180 ns. The diodes were definitely further from useful uniformity or reasonably specifiable range at this much higher temperature, but they were durable. We had uncertain explanations for such uneven sharing of *p-i-n* current near reverse recovery. Guesses included effect of previous temperature excursions that exceeded 200 °C and of previous (non-noticed) current excursions that caused that heating, causing perhaps cumulative degradation in 100 kHz switching. More certain were inadequate design of the diode and/or non-uniformity as produced. Parasitic inductance or slightly non-optimized design in our

early test apparatus were perhaps a contribution but not the main cause. Our improvements in cooling and heat sinking and avoidance of temperature spikes were included as realized but sometimes after they were needed.

To increase the voltage rating, a Cotronics silicone thick passivation was coated on the *p-i-n* Module4 front. It adhered but seemingly not strongly; therefore, we avoided any mechanical peeling force on it. The gate signal was put through a HP8112A pulse generator, giving a 10-ns rise time. The gate drive resistor was 50 Ω to reduce ringing to only one 50% overshoot peak of diode reverse voltage, not 16 Ω at 100% or 33 Ω at 64% and two peaks. The resulting 0.28-µs exponential rise (and fall) time constant in gate voltage means the MOS for DC-to-DC buck converter was slower to turn on fully and thus had slightly higher conduction loss. The MOS was cooled with chilled water. To test module4 *p-i-n* with Cotronics passivation, continuous buck converter operation heated the module, so it first operated for many minutes to stabilize the temperature. The rate of current turn-off during the swing from forward to reverse peak, such as from 90% to 10%, is sometimes noted. At 150 °C for 450 V and 12.6 Ω load the picture traces in figure 7 have channel 2 is current 1, channel 3 is current 2, and channel 4 is current 4.

Figure 7. Continuous operation of Cotronics-coated module4 *p-i-n* in DC-to-DC buck converter.

The currents at forward peak/forward ending/reverse peak for diode 1 were 2.0 A broad/1.7 A/-5.4 A, diode 2 were 2.25 A initial/1.2 A/-4.1 A, and diode 4 were 2.7 A broad/2.3 A/-8.3 A, with 620 V peak. At 142 °C for 300 V and 6.4 Ω the peaks for diode 1 were 2.4 A broad/2.1 A/-4.2 A, diode 2 were 3.7 A initial/1.6 A/-4.1 A, and diode 4 were 4.1 A broad/3.8 A/-12.3 A, with 335 V peak. Currents scaled for diode 1 1.2x/1.24x/0.8x, diode 2 1.64x/1.3x/1x, and diode 4 1.5x/1.6x/1.5x, so diode 2 forward and diode 4, in forward and reverse, scaled similarly but the remainder less than average. Again, current sharing by three parallel diodes in two conditions was not dependable and got worse with more total current.

The curve tracer found Cotronics-coated module4 *p-i-n* diodes withstood temperature impressively. The coating definitely worked; forward voltage decreases could have been more equal as shown in table 5.

Table 5. Curve tracer of module4 *p-i-n* diodes.

	Diode	**Forward**	**Reverse**
25 °C	#1	2.8 V + 0.25 Ω	840 V, 5 μA
	#2	2.85 V + 0.24 Ω	1200 V, 1.7 μA
	#4	2.8 V + 0.24 Ω	1200 V, 0.4 μA
150 °C	#1	2.75 V + 0.21 Ω	686 V, 5 μA
	#2	2.75 V + 0.28 Ω	1172 V, 1.2 μA
	#4	2.8 V + 0.24 Ω	1178 V, 2 μA
200 °C or higher	#1	2.66 V + 0.41 Ω	608 V, 6 μA
	#2	2.65 V + 0.4 Ω	1003 V, 6 μA
	#4	2.68 V + 0.42 Ω	1170 V, 5.2 μA
242 °C (measured, may have been exceeded since it had difficulty increasing with heater voltage)	#1	2.42 V + 0.4 Ω	
	#2	2.32 V + 0.43 Ω	
	#4	V + 0.5 Ω	

At the end of this, leads braized at 280 °C eutectic temperature became unattached. The forward voltage decreases were 0.24 V, 0.33 V, and 0.57 V; these varied far too widely for such temperatures. Figure 8 curve tracer measurement represents higher substrate temperatures than was previously used or recommended but the diode still worked.

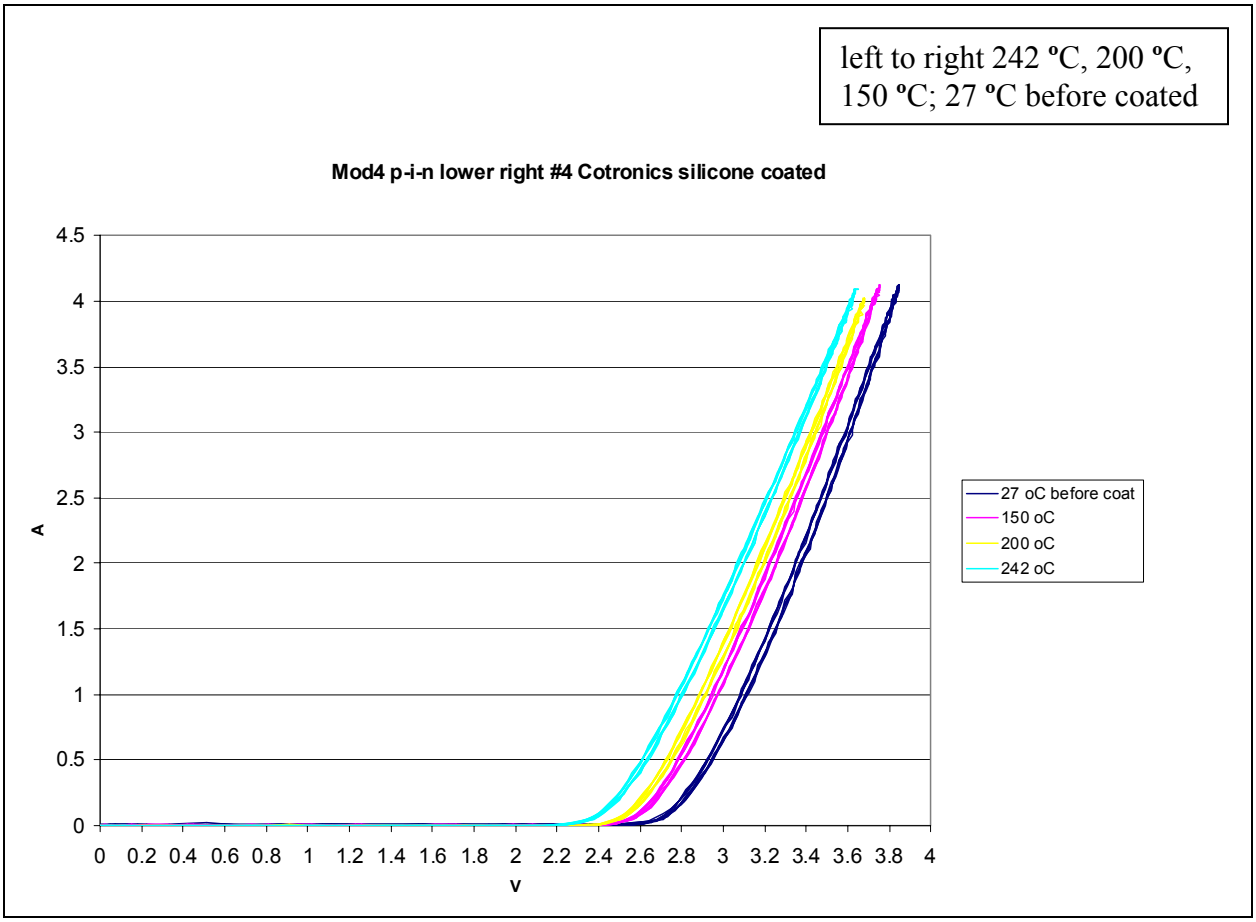

Figure 8. Curve tracer of module4 *p-i-n* #4 lower right Cotronics coated.

5.2 Junction Barrier Schottky Diodes

JBS diodes were rated at 500 V and are the type favored for such voltage. During testing, they always had adequate heat sinking. On the curve tracer, they had a 0.1-V knee below the listed voltage. Module2JBS diode JBS4 was 0.8 V + 0.37 Ω, at 2.29 V, 4 A. The reverse at 300 V was 0.75 μA; at 400 V, 3 μA (we quit at this voltage after these measurements); at 440, V 5 μA; at 500 V, 13 μA; and at 540 V, 30 μA. JBS diode 4 did not later show stress from this. The curve tracer found for all diodes the forward voltage increased and became less equal at 4 A. Module2JBS JBS1 at upper left was initially 2.54 V, JBS2 upper right initially 2.52 V (failed in DC-to-DC converter by 230 V, 1 A), JBS3 lower left initially 2.26 V (failed in DC-to-DC converter by 300 V, 2.3 A), and JBS4 lower right initially 2.29 V. Two worked at the maximum 400 V. After the initial curve-tracer measurement, the diodes were limited to 400 V.

To permit short wires, the circuit board was bolted near the hot plate. Module2JBS was held onto the hot plate by several small (thread 2-56) bolts both at the sides and by clamping its corners under pieces of 0.4-cm Teflon, so it could not slide or be leveraged. This permitted the use of heat sink compound under the module for the designed thermal

conductance and added the hot plate's thermal mass for brief operation. The centrifugal blower was angled down 20° to assist diode cooling. TCP312 current probes rated 100 MHz were used on JBS2, JBS3, and JBS4 since the JBS had much more rapid reverse recovery than a *p-i-n* diode.

The faster reverse recovery of these diodes gave more ringing. This was reduced by shortening wires to the load and from the power supply, changing to a planar load measuring 12.5 Ω + 0.12 μH to tens of MHz, and making the ground point where the anode wires contacted the circuit board. The load units of 50 Ω, 1000 W behaved negligibly inductive at all the frequencies of interest. JBS4 alone at 150 V was 3.2 A forward, at 180 V started at 3.9 A and peaked at 4.19A (we attempted a 4-A limit) with reverse recovery of 14.4 ns and 0.05 nC charge.

In parallel, JBS2 and JBS4 at 180 V gave 1.6 A and 2.2 A. At 200 V in figure 9, the four diodes JBS1 (vertically magnified 2.5× by different scale) channel 1, JBS2 channel 2, JBS3 channel 3 and JBS4 channel 4 obviously did not share current fairly equally at all times. Their currents were always markedly unequal, had different rates of change with time, and shifted the total current among the four. In reverse bias (10% to 38% of horizontal sweep) the top trace was channel 1, then 2, 3 and 4. They started forward conduction at 0.64 A, 1.06 A, 1.25 A, and 1.55 A and ended at 0.66A, 0.6 A, 1.28 A, and 1.1 A. Reverse peaks were –0.6 A, –0.83 A, –0.17 A, and –0.77 A.

Around 250 V (less than 270 V), JBS2 melted its wire bonds and fractured away 80% of volume. These JBS failures were not from damage by testing and showed poor original quality and durability; they withstood less reverse voltage than rated in the DC-to-DC buck converter at a constant reading of 25 °C. On the curve tracer at 4 A, JBS3 at 2.33 V was up 0.07 V from original, JBS1 at 2.64 V was up 0.1 V, and JBS4 at 2.36 V was up 0.07 V; reverse at 400 V was acceptably 3 μA. In the DC-to-DC converter JBS1, JBS3 and JBS4 at 230 V were as shown in table 6.

Figure 9. Diodes JBS1, JBS2, JBS3, and JBS4 in parallel.

Table 6. JBS diodes.

		Start (A)	1 µs later	End (A)	Reverse peak (A)
230 V	JBS1 JBS3 JBS4	1.26 1.76 2.4	1.28 1.9 1.8	1.5 1.7 1.5	-0.92 -0.97 -1.1
270 V The reverse recovery was 24 ns at 12 nC, with JBS4 having a 160-W peak twice that of JBS1 or JBS3.	JBS1 JBS3 JBS4	1.4 is peak 1.9 2.6	1.52 2.25 2.13	1.35 2.03 1.8	-0.95 -1 -1.2
300 V When repeated the sweep blew.	JBS1 JBS3 JBS4 conducting but not displayed	1.6 2.1	1.7 2.6	1.5 2.2	-0.9 -1
300 V	JBS1 JBS4	2.2 3.3	2.2 3.5	1.85 2.8	-1.2 in 16 ns, 11.2 nC -0.61 in 20 ns, 10.6 nC

These were undesirably unequal.

At 300 V, the diodes were working in the first trace picture but JBS3 melted the wire bonds, fractured 1/3 of the top area and 1/6 of bottom, and removed 0.5 cm by 0.3 cm of Au nearby before the second picture and its spreadsheet files were taken. Lifting the module to inspect heat sink compound coverage area may have reduced it but found it was only 2/3 covered and under the diode 3 area was half covered; the module near JBS3 was missing an area of Au larger than a diode. In the DC-to-DC converter, JBS1 and JBS4 at 300 V initially were 2.2 A and 3.5 A, undesirably unmatched currents; 1 μs later 2.2 A and 3.5 A, and ended 1.85 A and 2.8 A; reverse recovery peak was -1.2 A ending in 16 ns with 11.2 nC, and JBS4 was -0.61 A ending in 20 ns with 10.6 nC. On the curve tracer at 4 A JBS1 was 2.99 V up by an excessive 0.66 V, then after storage for 60 minutes became a worse 3.1 V; JBS4 was 2.43 V, up 0.07 V. With forward voltages so uneven and shifting, and current versus time shifting and possibly spiking, testing was halted.

6. Conclusions

These SiC *p-i-n* diodes were not sufficiently uniform to share current equally. They were fairly durable and predictably withstood higher temperature than Si production diodes but were basically not uniform and reliable enough for applications. More equal current sharing at least in DC and preferably during a cycle is needed for high-volume production and use. For example, Module3 at 400 V in the DC-to-DC converter had the left diode began at 4 A and the right at 4.2 A and ended at 3.6 A and 3.1 A (too different and poorly tracking). Also, a better passivation layer over the Au is needed to reduce its deterioration in high temperature excursions. We hope for design responses such as in crystal growth to reduce the literature-reported degradation and triangular defects of SiC.

These SiC JBS diodes had too high a rating of 500 V and 4 A and were not sufficiently uniform or durable. Their beginning curve tracer voltages at 4 A varied undesirably by 0.28 V, which usage increased to 0.67 V; thus, their DC currents in parallel would be less equal. They should have had more equal currents at all times and especially had less difference in variations with time during a DC-to-DC buck converter cycle. Tighter initial voltage distribution at 4 A and better design and screening for the rating would be a first step**.**

A test apparatus must have adequate thermal conductivity in the heat sink, and adequate cooling capacity for thermal control, directly at the device, as for the junction. Air cooling with adequate air flow was, even for the MOS, far from adequate for our needs. The heat flowed through more distance to achieve modest thermal conductance or

thermal mass. Significant and continuous use of the MOS transistor's capacity required a water cooled substrate. The heater must permit short electrical connections to the rest of the apparatus.

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