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Computer Development (SEAC and DYSEAC) at the National Bureau of Standards Washington, D. C.

UNITED STATES DEPARTMENT OF COMMERCE

NATIONAL BUREAU OF STANDARDS

UNITED STATES DEPARTMENT OF COMMERCE • Sinclair Weeks, *Secretary*
NATIONAL BUREAU OF STANDARDS • A. V. Astin, *Director*

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Foreword

Since 1946 the National Bureau of Standards has been active in the general field of electronic digital computers, largely for other agencies of the Government. The Bureau's computer program has been conducted jointly by the Electronics Division and the Applied Mathematics Division. The work of the Electronics Division in Washington has included the development and construction of two computers (SEAC and DYSEAC), components research and development, and various technical and advisory services. The work of the Applied Mathematics Division has included research in numerical analysis of importance in the solution of problems by computers and the design and construction of a computer (SWAC) at the Bureau's Institute for Numerical Analysis in Los Angeles.

This volume presents reports on various aspects of the computer program through 1953, based largely on the work and experience relating to SEAC and DYSEAC. Such topics as systems development, engineering development, design, construction, and maintenance of computer equipment are covered. The introduction summarizes the history of this program in the Electronic Computers Laboratory of the Electronics Division.

A. V. Astin, *Director.*

Contents

Introduction

S. N. Alexander

The development of electronic digital computing machinery at the National Bureau of Standards started in 1946 because of the interest of the Bureau of the Census in the possible use of electronic digital techniques for tabulating purposes. In particular, the Bureau of the Census hoped to attain trial use of an electronic installation in connection with the 1950 decennial census, and the National Bureau of Standards was asked to provide technical guidance and developmental support to this long-range program. Concurrently, NBS was seeking to obtain an electronic digital computer as a scientific instrument for its own use. Immediately following the establishment of these two tasks, a 2-year program for the development of improved components for digital computers was established under the sponsorship of the Office of the Chief of Ordnance, Department of the Army.

The relatively short time schedule desired for the delivery of the two complete machine installations, together with suitable auxiliaries and operational supplies, made it advisable from the outset to seek commercial sources for such equipment. In this way, it seemed possible to compress the research, development, and construction of such equipment into an integrated effort and thereby meet the time schedules. This decision was buttressed by further requirements from the Office of Air Comptroller, Department of the Air Force, and the Army Map Service for similar equipment with comparably short time schedules. NBS agreed to serve as technical agent in monitoring the design, construction, and installation of these machines from two commercial suppliers, while its own laboratories were fully occupied with the component development program.

Because of an unanticipated sequence of technological and contractual difficulties, it became evident early in 1948 that the delivery of complete machine installations would be delayed considerably beyond the target dates. The unexpected difficulties associated with the developmental phases of all such programs, both commercial and university, emphasized the uncertainty of availability of electronic digital computing facilities of any sort. This motivated a request for a "stopgap" installation to serve some of the urgent needs of both the Air Comptroller and NBS during the interim period until full-scale equipment could be obtained from commercial sources within a more realistic time schedule. During the summer of 1948, NBS explored the possibilities of designing and constructing an interim machine that would have sufficient power for general use and yet be simple enough to be constructed in a short time. The feasibility of this program was based on the preceding 2 years of active experience in component development and the availability of the best technology that had been reported by other computer groups, particularly those in the universities.

The original modest objectives for an interim machine were reconsidered toward the end of 1949, when it became evident that the proposed SEAC computer would be the only equipment available to NBS and collaborating Government agencies for at least 2 years. To cope with this altered situation, the plan for the machine was adjusted so that a full-scale installation could be attained by subsequent expansion of an initial nucleus. However, the prime objective was still to have the initial nucleus in operation at the earliest possible date. The resulting machine began useful operation in May 1950, less than 2 years after the start of the program, and SEAC completed nearly a year of scheduled operation for NBS and its collaborators before any other installation was available to them. Furthermore, SEAC was the one installation that was readily available to serve the intermittent computational needs of many other Government agencies, and for over 2 years was used on a round-the-clock basis for the full 7-day week. Even now, after 3 years of regularly scheduled operation, the SEAC is still employed for an extended work week in the solution of problems.

The task of designing a large-scale digital computer such as SEAC from original conception to final realization was, of course, the effort of many minds and the work of many hands. The team chosen for this task encompassed a wide spectrum of talents and skills. The successful completion of SEAC at a time when the availability of such a facility was of urgent importance to the Government was recognized by the Award for Exceptional Service from the Department of Commerce to the

SEAC staff as a group. In addition to this group-citation to the 33 scientists and technicians who contributed to the SEAC accomplishment, particular mention was made of the individual contributions by S. N. Alexander, W. W. Davis, R. D. Elbourn, S. Greenwald, R. C. Haueter, A. L. Leiner, S. Lubkin, C. H. Page, J. L. Pike, R. J. Slutz, and J. R. Sorrells. The early contributions of H. Senf and W. Martin also deserve recognition, even though they did not remain to participate in the completion of SEAC.

As soon as the central nucleus of SEAC was functioning reliably enough to warrant regularly scheduled operations, the program of expansion and additions began. Indeed, the machine became a proving ground for the evolution of advances in computer components, design techniques, and maintenance procedures. The expansion and testing were carried out in the midst of a regular work load of important computing that was tightly scheduled because of priorities. Thus it was necessary to plan carefully in order to meet the requirements for scheduled computation and also include the necessary development work. The fact that these two conflicting objectives were meshed in an effective manner is a compliment to the fine cooperation and management between the scientists and engineers who designed SEAC and the mathematicians who used it.

During this period of expansion, over 90 percent of the time available in a full 168-hour week was effectively scheduled and used for either problem solution, development work, or preventive maintenance. During this period, 83 hours a week were scheduled for problem solution, of which 65 percent was logged as productive time, and 52 hours a week were scheduled for development work. Only 20 percent of the time scheduled for either development work or problem solution was recorded as being ineffective because of machine malfunctions. This is considered a gratifying performance for a pioneering installation, particularly when the difficult tasks of operating and expanding the machine were under way at the same time.

The initial program for expansion was directed primarily at the task of improving the input-output facilities, which resulted in the addition of magnetic wire and magnetic tape units to increase the speed of computation on problems that could not readily be kept within the confines of the 512 words available in the high-speed memory. As more of these magnetic units became available, an external selector panel was added to the machine to permit automatic selection of the desired input-output unit under programmed control of the computer as well as by manual operation of the console switches. This, in turn, made it necessary to design and construct both an inscriber and an outscriber to facilitate the transition between the documents containing the coded problem and the typed sheets giving the results of the computation by the machine. In addition, arrangements were made to permit transfers to and from punched cards which were either the source for data or the final form desired for the solution. Most of the effort in this area was planned and directed by R. J. Slutz, with the able collaboration of S. Greenwald, R. C. Haueter, E. F. Ainsworth, J. L. Pike, L. Cahn, P. R. Westlake, W. H. Bridge, and P. D. Shupe, Jr.

While the input-output system of SEAC was being augmented, steady planning and construction by a group under the leadership of W. W. Davis were also under way for the addition of an experimental electrostatic memory, primarily for trial and evaluation but with the eventual goal of regular service as an additional 512-word high-speed memory. This equipment also served as an exacting evaluation of experimental cathode-ray tubes specifically designed for storage purposes and of testing procedures that were being developed for selecting tubes suitable for operation in the memory.

The central control of the machine also underwent considerable revision and expansion. Some of these changes related to the inclusion of additional machine operations, but the more significant changes related to the inclusion of an automonitor function and a three-address control system, which is described in detail in one of the following papers. These revisions and expansions resulted from suggestions arising out of operational experience and the desire to make the machine more versatile. The detailed planning of these changes was the work of A. L. Leiner, who had been responsible for most of the final system plans for the SEAC nucleus. The physical realization and installation of these new features are a tribute to a combination of careful engineering and patience on the part of R. C. Haueter, S. Greenwald, and P. D. Shupe.

Sporadic performance of the experimental electrostatic memory directed specific attention to the development of an improved cathode-ray tube for storage purposes. By this time, the Bureau had begun the planning of a far more powerful machine than SEAC to be used in the SCOOP program of the

Office of Air Comptroller. This machine definitely required a rapid-access memory, and for this reason the development of both cathode-ray tubes and improved electrostatic storage techniques was pursued vigorously, under A. W. Holt and D. C. Friedman. Meanwhile, other approaches to rapid-access storage were being explored, one of which resulted in the Diode-Capacitor memory system suggested by A. W. Holt and reported in a companion paper.

During the expansion of SEAC and the evaluation of components aimed toward the creation of a SCOOP machine, it became evident that the dynamic circuitry devised for SEAC was susceptible to considerable electronic standardization. In turn, this became the basis for a repetitive physical configuration out of which the high-level pulse circuitry could be assembled. The advantages and possibilities of a standardized package design were realized by R. J. Slutz, and its detailed design and execution were the results of combined efforts of R. P. Witt and R. D. Elbourn.

The computer group at the U. S. Air Force Missile Test Center, Patrick Air Force Base, Cocoa, Florida, collaborated in the mechanical design of the first satisfactory packages, and these were successfully employed in the outscriber that was constructed for SEAC. This packaged design, with some refinements, was used in two computing machines that have recently been completed, one at the Air Force Missile Test Center and the other at the Willow Run Research Center of the University of Michigan. The Bureau revised this package design to incorporate etched circuit techniques. These are the packages that were used in the construction of DYSEAC, a new machine sponsored by the Research and Development Board for the evaluation of a number of organizational and engineering innovations. All three of these machines are based on the circuit techniques and some of the organizational features of SEAC, but they are distinguished one from the other by variations on the SEAC organization that were included to meet specific application requirements.

In order to cover adequately the 5 years of development that stemmed from the SEAC program, the component improvement program, and the subsequent DYSEAC program, the senior personnel of this laboratory have shared the responsibility for reporting on the achievements of the entire group. The authors of any of these particular papers are not necessarily, therefore, the only major contributors to the solution of problems discussed; and many of these authors, with others, have made important contributions to other programs as well as to those on which they are now reporting. Here again, it is important to recognize the team nature of the developmental activity that is being carried on at NBS.

While the detailed planning of the SCOOP computer was deferred in order to identify more clearly its operating characteristics and to have at hand a proved rapid-access memory, the design and construtuion of DYSEAC, which was to result in a complete machine that would serve certain specialized needs and also provide a thorough evaluation of the packaging techniques, was undertaken. Although DYSEAC employs an acoustic memory and a serial arithmetic unit, the basic organization is considerably more sophisticated than that of SEAC, for it contains some of the system features that had been planned for the SCOOP machine. In addition, special features have been incorporated to permit the machine to serve as a tool for experimentation on the handling of large masses of business-type data and for experimentation in using digital equipment in a control system.

The task of planning the organization of DYSEAC and its detailed execution through the preparation of wiring tables was carried out under the direction of A. L. Leiner, with the able collaboration of W. A. Notz, J. L. Smith, A. Weinberger, and W. H. Bridge. The physical realization of the machine involved many original design problems related to the use of packages and a modular type of construction for the chassis. The decision to install DYSEAC in a pair of vans was made after the program was well under way. This added many new mechanical and electrical considerations. The formidable task of constructing DYSEAC was accomplished in approximately 18 months by a team of about 25 people directed by R. P. Witt, ably supported by R. W. Smith, H. P. Belcher, and R. Hand.

One of the major purposes in the SEAC program was to evaluate the reliability and serviceability of techniques that appeared highly promising but were at that time still unproved. Subsequent operating experience has established the soundness of many of the engineering choices that were significant departures from the techniques then current. Operating experience established another important feature: the significant benefits that accrued from using an operating machine as a proving ground for new component and operating techniques. SEAC has served as a valuable focal point that prompted the exchange of ideas among the components researcher, the machine designer, the maintenance engineer, and the user. The DYSEAC holds promise of becoming a comparable source of ideas for further machine development.

1. SEAC

S. Greenwald, S. N. Alexander, and Ruth C. Haueter

1. INTRODUCTION

The first major contribution of the National Bureau of Standards to the development of electronic computing machinery occurred with the completion of the SEAC (Standards Eastern Automatic Computer) in May 1950. This digital machine was the culmination of almost 2 years of intensive design and construction work which was sponsored by the Office of Air Comptroller, Department of the Air Force. The initial objective set during the summer of 1948 was to provide at the earliest possible date a machine of limited computing power that would meet the immediate computational needs of the National Bureau of Standards. This installation would serve as a "stopgap" for the interim period during which full-scale equipment from a commercial source was being completed for delivery to the Government. Toward the end of 1949 this point of view was gradually abandoned, as it became evident that there would be no other equipment available for 2 years or possibly longer. As a result, the ultimate objective was altered so that a full-scale machine could be attained by expansion of the initial nucleus without delaying its completion.

Still another aspect of building an expandable machine was the ability to use it as a proving ground for experimental equipment.

At the present time, after more than 3 years of regularly scheduled operation, SEAC is still actively employed in the solution of problems for both NBS and many Government agencies. What is perhaps more important is that for the initial 2 years of its operation it was the most powerful computer installation readily available to the Government, and consequently was scheduled around-the-clock for a full 7-day week.

Since the machine was first put into operation, a significant fraction of the total time available has been devoted to the engineering work associated with the expansion of SEAC. The magnitude of this effort can be estimated from the fact that the number of vacuum tubes in the system was increased from approximately 750 to 1,300 and the number of germanium diodes from approximately 10,500 to 16,000. This expansion and testing program was carried out in the midst of a regular work load of important computation that was tightly scheduled because of priorities.

A number of circuit and equipment innovations were included in the SEAC program in order to evaluate the reliability and serviceability of techniques that were highly promising but unproved. One example in this area is the extensive use of diode switching. Another is the achieving of a-c coupling by using pulse transformers for highly variable duty factor service. Success with these techniques made practical the use of vacuum tubes as a means of power amplification rather than as gating devices.

At the present, two machines based on a packaged version of the SEAC "transformer-coupled dynamic circuitry" have been completed. One is located at the Air Force Missile Test Center in Florida and the other at the Willow Run Research Center of the University of Michigan. A still further extension of these techniques was employed at the National Bureau of Standards in the construction of the DYSEAC, which is described in a companion paper.

2. OPERATING CHARACTERISTICS

The SEAC is an automatic high-speed digital computer that operates at a 1-Mc pulse repetition rate. The machine is predominately serial in nature and uses the binary number representation. Both instruction words and number words consist of 45 binary digits, which are equivalent to approximately 13 decimal digits. When the machine was first put into operation in May 1950, 11 different types

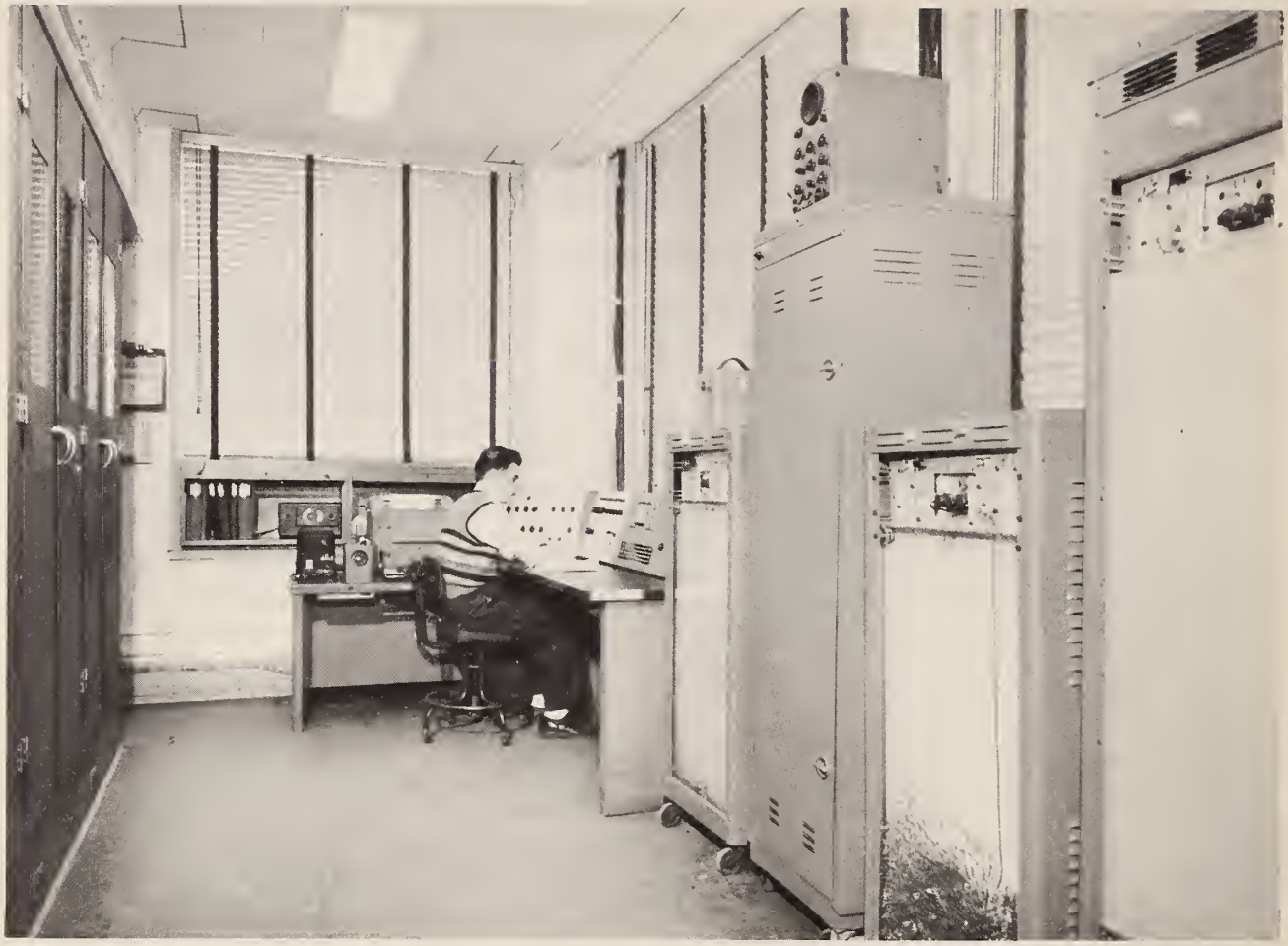

FIGURE 1.1. *SEAC from control console side.*

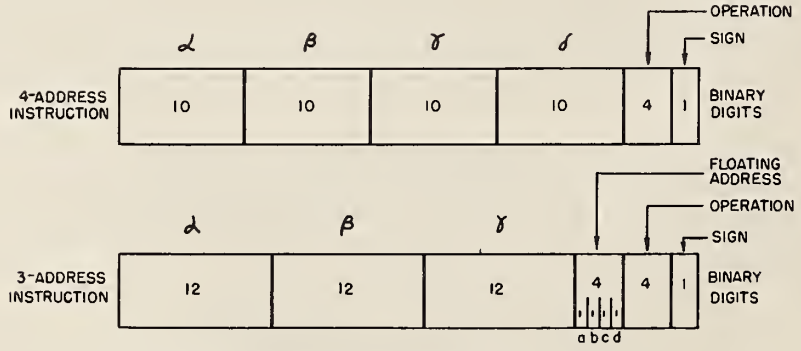

FIGURE 1.2. *Component parts of a SEAC instruction.*

of operations were performed by it: (1) addition, (2) subtraction, (3) multiplication, major part, unrounded, (4) multiplication, major part, rounded, (5) multiplication, minor part, (6) division, (7) comparison, algebraic value, (8) comparison, absolute value, (9) logical transfer, (10) read in, and (11) print out. The instruction words expressed these operations in the four-address mode. The original high-speed memory consisted of 512 words of acoustic delay-line storage, and all of the input-output devices were modified Teletype equipment. The input was from either a tape reader or keyboard, and the output was to either a printer or tape punch.

During the 3 years the machine has been operating, it has been expanded into a far more powerful and convenient tool than its original conception. For example, five additional operations have been incorporated: (1) reverse tape or wire, (2) logical multiplication, (3) base, (4) file counter information, and (5) clear memory cell, bringing to a total of 16 the types of operations available. An experimental Williams type of electrostatic memory has also been added. This stores 512 words in 45 cathode-ray tubes, with parallel access to a complete word in 12 μsec. An alternative instruction system, using the three-address mode of operation has also been installed. By simply setting several switches inside the machine, the computer is set for operation in either the three-address or four-address system.

Magnetic wire and magnetic tape units were added to increase the speed of the computer on problems which require considerable input-output or auxiliary memory capacity. In particular, the magnetic wire handling equipments greatly speed up initial input and final output. Magnetic tape units, both single-and multiple-channel, provide external memory. Figure 1.1, which is a view of the computer from the console side, shows several of these units. Either automatic or manual selection of input-output units is available. Still another feature that has been added by modification of the circuitry is the ability to automatically monitor the operations being performed. When called into use by setting a switch on the console, this feature causes the machine to print out the program-sequence counter information, the instruction being performed, and the result of the operation. This facility is a great convenience, and will be discussed in more detail later.

The component parts of an instruction word in both the four-address and three-address systems are shown in figure 1.2. In the four-address system, the addresses are denoted by the symbols α, β, γ, and δ. Normally, α is the address of the first operand, β the address of the second operand, γ the address of the result of the operation, and δ the address of the next instruction. The instruction also contains a code specifying the type of operation to be performed and a conditional halt control digit in the sign position. An address comprises 10 binary digits, so it can designate one out of 2^{10}, or 1,024, memory cells. This is sufficient for the two SEAC memories. Four binary digits specify the operation to be performed. The 16 different operation codes thus available are now all used. The single binary digit in the sign position indicates whether or not the computer is to halt after performing the operation. In the course of executing one instruction, the control of the computer cycles through four phases, one for each reference to the memory. In a typical operation, address β is referred to in phase 2, α in phase 3, γ in phase 4, and δ in phase 1.

A typical three-address instruction word contains the addresses α and β of the operands and the address γ of the result. The remainder of the word contains floating-address information, the code specifying the type of operation to be performed, and the conditional halt digit. Twelve binary digits are used to specify an address, providing the basis for selection among 4,096 memory cells; four binary digits are used to provide information for the floating address feature. The operation code for the 16 instructions is the same as in the four-address system.

The main difference between the three-and four-address systems is in the designation of the next instruction to be performed. In the four-address system, the instruction contains an explicit statement (δ) designating where the next instruction is located in the memory. In the three-address system, however, there is no such explicit statement. Instead, instructions in this system are automatically sequenced in accordance with a convention, successive instructions being normally located in consecutively numbered memory positions. An exception to this convention is available through the comparison (conditional transfer) operation, whenever the first operand (α) is less than the second operand (β). In this case the result of the comparison leads to what is called a "jump" operation in which the next instruction for both the three-address and four-address systems is chosen from address γ.

The floating address feature allows the programmer to designate any address as either absolute or relative. An absolute address is interpreted in the usual sense, merely as a number identifying a specific memory location. A relative address, however, identifies a position in the memory by specifying its displacement relative to that position from which the instruction word itself was taken. To illustrate, suppose that an instruction located in memory position m specifies that the address of the first operand is number 17 relative. Then the control will take the word in memory location $(m+17)$ and use it as the first operand. If location $(m-17)$ is desired, the complement of 17 is used as the address.

It is possible to use any combination of absolute or relative addresses in an instruction word. Of the four binary digits that supply floating address information, the first three digits, a, b, and c, indicate whether α, β, and γ, respectively, are absolute or relative. The fourth binary digit d tells which of two control counters is to be used during operation in the three-address mode. Counter 0 is normally the operating counter. However, starting with any desired address, counter 1 can be put into operation by a "jump" comparison in which γ is the desired address and binary digit d specifies counter 1. Counter 1 will be the operating counter only so long as d in each following instruction indicates counter 1. As soon as an instruction is reached in which d indicates counter 0, the control automatically returns to counter 0 after performing the instruction.

A typical use of this feature is to code subroutines for counter 1 with floating addresses. The use of floating addresses allows the subroutine to be placed anywhere in the memory automatically. By coding a subroutine for counter 1, a "jump" comparison sends the control to counter 1 at the desired address, and after finishing the subroutine it returns the control automatically to counter 0 at the point in the main program where it left off.

The basic operations of SEAC and their functions are summarized in table 1.

TABLE 1

Name of operation	Description of instruction
Addition	Form the sum of the word in α and the word in β, and write the result in address γ in the memory.
Subtraction	Form the difference α minus β, and write the result in address γ in the memory.
Multiplication, major, unrounded.	Form the product of the word in α and the word in β, and write the major part (unrounded) in address γ in the memory.
Multiplication, major, rounded.	Form the product of the word in α and the word in β, and write the major part (rounded off) in address γ in the memory.
Multiplication, minor	Form the product of the word in α and the word in β, and write the minor part in address γ in the memory.
Division	Form the quotient of the word in β divided by the word in α, and write it in address γ in the memory.
Logical transfer	Write in address γ in the memory those digits of the word in α which correspond to one-digits of the word in β. Leave the word in γ unchanged in those digit positions which correspond to zero-digits in the word in β.
Comparison, algebraic	If the word in α is algebraically greater than or equal to the word in β, take the next instruction from the normal next-instruction address position. (In the four-address system, this is address δ in the memory; in the three-address system, this is the next consecutively numbered address position.) If, however, the word in α is less than the word in β, take the next instruction from address γ in the memory.
Comparison, absolute	Perform algebraic comparison except treat both words as positive.
Read in	If the address number β is odd, read in one word from the selected external unit designated by address number α, and write the data in address γ in the memory; if the address number β is even, read in eight words, and write in the eight addresses beginning with address γ.
Print out	Print out the word in address γ in the memory if the address number β is odd (or the block of eight words beginning with address γ if β is even) onto the selected external unit designated by address number α.

TABLE 1—Continued

Name of operation	Description of instruction
Reverse	Reverse through one word if the address number β is odd (or through eight words if the address number β is even) on the selected external unit designated by address number α.
Logical multiplication	Write the digit-by-digit product of the words in addresses α and β into address γ in the memory.
Base (primarily for four-address system).	If address number α is greater than or equal to address number β, put the number β into the special base-number counter-register and take the next instruction from address δ in the memory. In subsequent instructions, all references to odd-numbered addresses will now be interpreted relative to this constant number β. If address number α is less than address number β, the counter-register is cleared and the next instruction is taken from address γ in the memory.
File	Write the contents of special counter-registers into memory address γ.
Clear	Clear memory address γ.

3. MACHINE ORGANS

An over-all block diagram of SEAC is shown in figure 1.3, in which information paths are shown as solid lines and control paths as dashed lines. Interchanges of information between the Shift Register, the Arithmetic Unit, the Control, and the Mercury Memory are made through the unit called the Bus. The Bus not only provides correct routing of information but correct timing as well. During an input operation, instructions and numbers are read into the Shift Register from one of the input-output units via the Selection Circuits. From the Shift Register there are two possible paths. The digits are transferred either in parallel into the Electrostatic Memory or serially into the Mercury Memory via the Bus. For an output operation, the procedure is the same but the path is reversed. For internal operations, instructions are routed from the Memory to the Control Unit, and numbers are routed between the Memory and the Arithmetic Unit. Transfers are made to and from the Mercury Memory directly through the Bus. Whenever the Electrostatic Memory is used, an additional transfer through the Shift Register is required.

The Arithmetic Unit in SEAC is involved in almost every operation that the computer performs, with the exception of several such as File and Base. Figure 1.4 is a block diagram of the Arithmetic Unit. In the process by which two numbers are added, the first number enters the Arithmetic Unit in phase 2 of the cycle through which the computer sequentially progresses. If the number is positive, it goes through the Input Complementer and Adder into the Accumulator Register. If the number is negative, the Sign Sensing Unit activates the Input Complementer, and the complement of the number is sent to the Accumulator Register. During phase 3, the second number is sent to the Arithmetic Unit. Again it is complemented or not, depending on whether it is negative or positive. The second number is then added to the first number, which has been circulating in the Accumulator Register and is available at the second input to the Adder. In phase 4, the result of the addition is sent via the Output Complementer through the Bus connection to the Memory. If the result is negative, the Sign Determining Unit inserts a binary 1 in the sign position of the number and also activates the Output Complementer.

The process of subtraction is almost identical, the difference being that the effect of the sign of the number from β on the Sign Sensing Unit is reversed. The process for a comparison is similar to that for subtraction. However, no result is transferred to the memory; instead a signal is sent to the Control Unit when α is less than β.

Multiplication is performed in SEAC by repetitive additions, which involve the use of two other registers, the Multiplier and the Multiplicand Registers. In phase 2, β enters the Multiplier Register, and in phase 3, α enters the Multiplicand Register. Multiplication is accomplished by successive additions of the multiplicand to the partial product in the Accumulator Register under the control of the digits of the multiplier. The shifting is accomplished in the Accumulator Register by shortening it one pulse time. Division is also a repetitive process using all three registers,

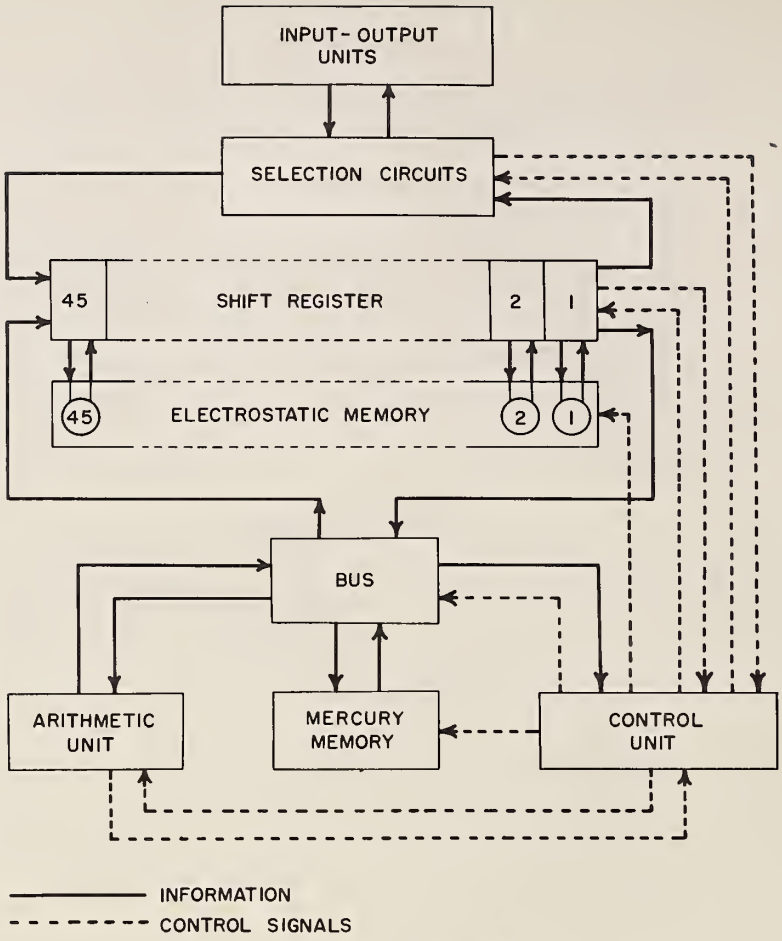

FIGURE 1.3. *Block diagram of SEAC.*

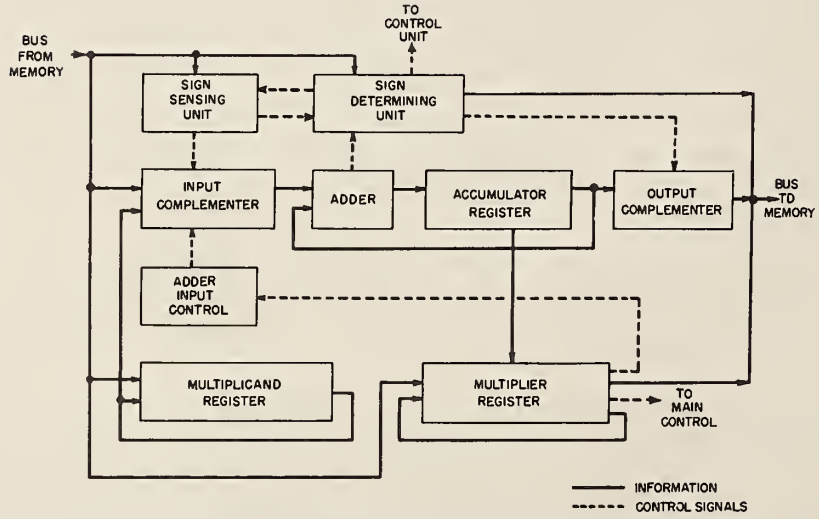

FIGURE 1.4. *Block diagram of Arithmetic Unit.*

with the quotient formed in the Multiplier Register. The nonrestoring method of division is used and consists of successive subtractions or additions of the divisor, according to the sign of the remainder. Physically, the entire Arithmetic Unit occupies only 1 1/4 relay racks. It is interesting to note that this early design for a binary adder, which is used in all computations, employs only three single-cathode vacuum tubes.

The Control Unit is the most complex part of the computer, as may be seen in the simplified block diagram of the control in figure 1.5. This has resulted partially from the experimental nature of the machine and from the continuous expansion it has undergone. One of the major functions of the Control Unit is to decode the instruction to determine (1) the type of operation to be performed, (2) the location of the numbers involved in the operation, and (3) the location of the instruction to be performed next. After the instruction is received from the memory, it circulates in the Instruction Register. The digits representing the operation are decoded in the Staticizer and Decoder, and the appropriate operation lines are activated.

The addresses are selected one at a time in what is called the Address Selector. If the location called for is in the Mercury Memory, the address information is sent to the Mercury Comparator. When the output of the Minor Cycle Counter agrees with the temporal selection portion of the address, the Mercury Comparator sends a signal to the Execute Generator that the desired word is in position to be read out. The Phase Counter is then advanced and the transfer is made. On the other hand, if the location called for is within the 512 words of the Electrostatic Memory, the address is routed into the Electrostatic Control. This Control then determines when the Execute Generator will advance the Phase Counter and when transfer between the Electrostatic Memory and the Shift Register will be made. In three-address operation the information from the selected counter is sent to the Address Selector where it is used to select relative addresses and the location of the next instruction.

The Shift Register Control serves mainly to direct the transfer of information in and out of the Shift Register at the rate acceptable to the Input-Output device in use. The Automonitor Control automatically cycles the computer through the necessary print-outs for each instruction being monitored. The Multiplication Counter counts off the 44 minor cycles (word times) necessary for a multiplication or division and prevents the phase counter from advancing until this portion of the operation is completed. Finally, the Manual Control permits the computer to be started or stopped, or its operation to be modified, by means of switches located on the console.

The Mercury Memory for SEAC is housed in a separate cabinet, which contains the 64 mercury-filled acoustic lines, their associated amplifiers and gating circuits, the selection matrix, and other miscellaneous circuitry. Figure 1.6 shows one side of the cabinet with 32 of the recirculation amplifiers and half of the selection circuitry. As the nominal delay through the lines is 384 μsec, 8 words of 48 digits each are stored in each mercury line. Thus the total capacity of the memory is 512 words.

Because the delay of a mercury line varies somewhat with temperature and yet the whole memory must be kept in step with the crystal-controlled computer clock, it is necessary to maintain all lines at the same constant temperature. A system of aluminum plates and extrusions bonds the 64 mercury-filled glass tubes into a nearly isothermal unit, which is insulated from the outside and is electrically heated and thermostated to 50 $\pm$0.25° C.

Pulses are stored in each line as packets of an 8-Mc carrier. For every binary one there is an associated radio-frequency pulse packet, and for every zero there is a gap. The acoustic output of the line activates a quartz crystal whose electrical output is then transformer-coupled to the input of the recirculation amplifier. The first three tubes serve as a radio-frequency amplifier and detector, with an over-all gain of 50 to 55 db and a center frequency of 8 Mc. The fourth tube in the chain has the function of switching information into or out of the line, as well as that of synchronizing and reshaping. The fifth tube develops the 8-Mc packet of 200-v peak-to-peak amplitude, which is transformer-coupled to the input crystal of the mercury line.

Figure 1.7 shows the general organization of the mercury cabinet. Digital information denoting the mercury line to be selected comes from the Mercury Comparator located in the control section of the machine. An electrical delay line brings these time sequential pulses into positions from which

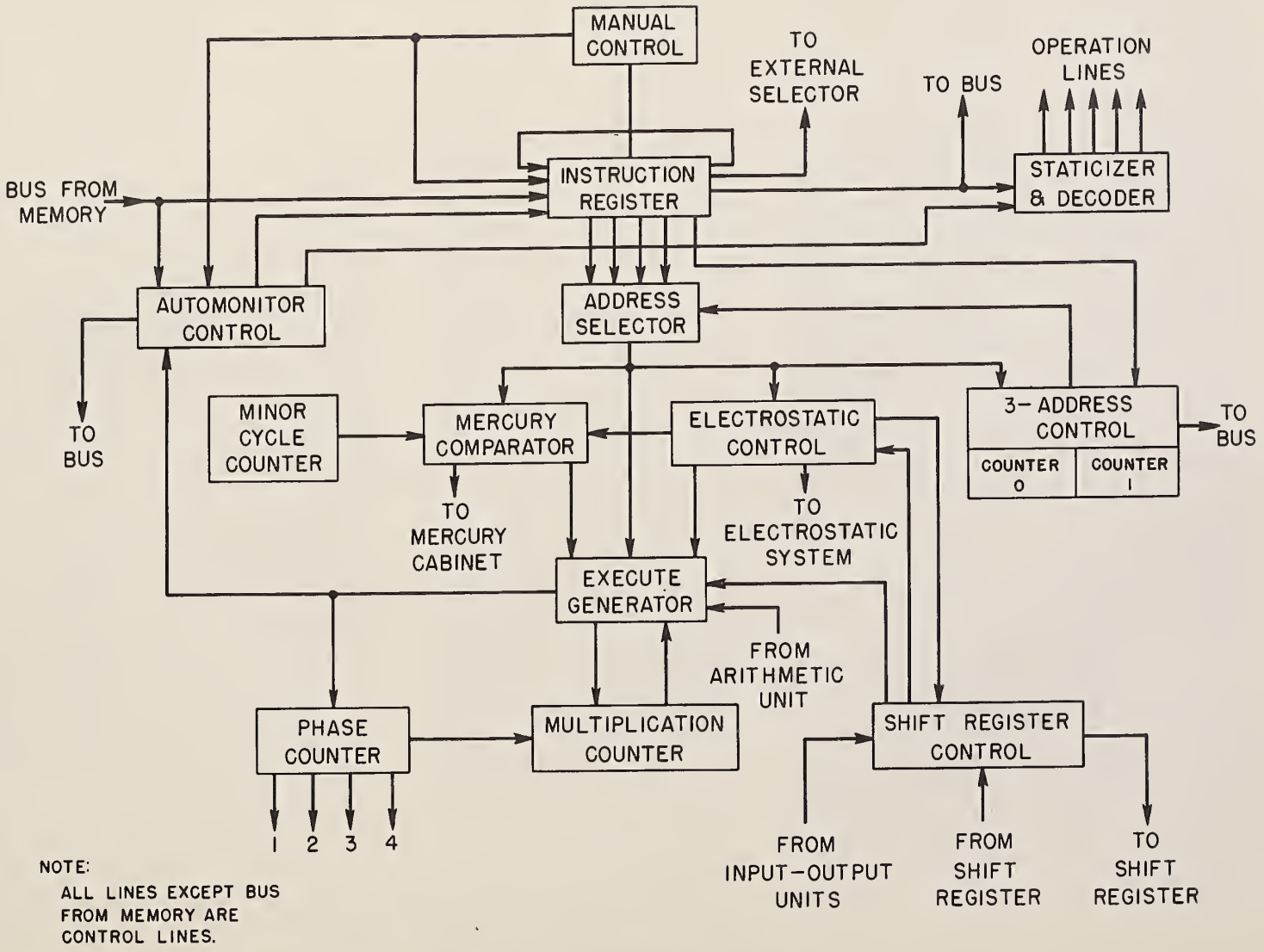

FIGURE 1.5. *Block diagram of Control Unit.*

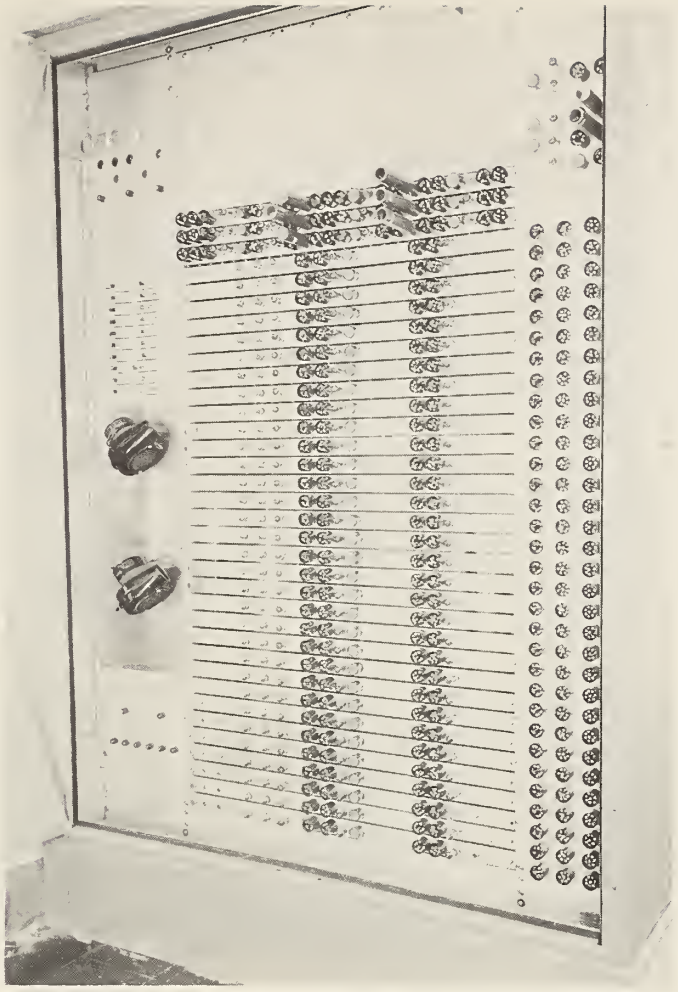

FIGURE 1.6. *Side view of Mercury Memory cabinet.*

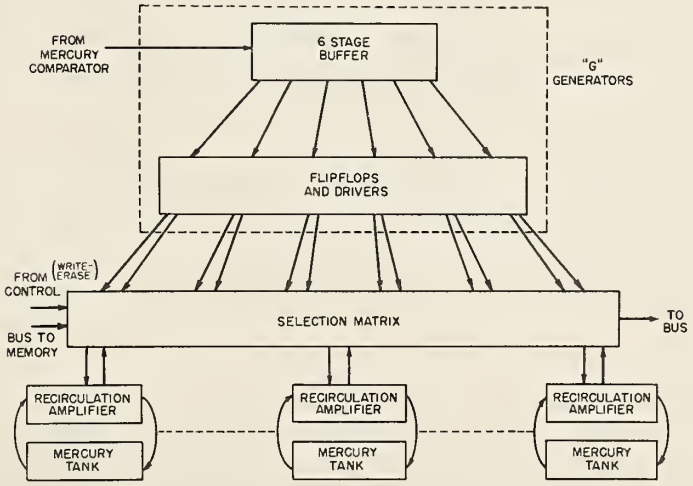

FIGURE 1.7. *Block diagram of the Mercury Memory.*

they can be simultaneously gated into six flip-flops with associated drivers. This portion of the circuitry is called access gating or, more popularly, "G" Generators. The varied combination of six positive and six negative pulse lines from the "G" Generators selects one of the 64 mercury lines that connect with the matrix. When writing into the memory, which is done in phase 4, information appears on the Bus to Memory, from which it is routed to the selected memory line, the old information being simultaneously deleted. In phases 1, 2, and 3, information from the selected address is transmitted via the output mixer of the matrix to the Bus. Information is erased by interrupting the recirculation path only when new information is written in.

As previously mentioned, in addition to the acoustic memory, SEAC also includes a full-scale experimental electrostatic memory. This provides an additional 512 words of storage, effectively increasing the capacity of the machine to 1,024 words. As this memory is arranged to operate in the parallel mode, the access time is considerably decreased, which thereby increases the speed of the machine over that which is possible with the mercury memory. The type of electrostatic storage is that originated by Williams and Kilburn, in which the phosphor surface of a conventional cathode-ray tube is charged to store digital information.

This memory occupies approximately six standard relay racks. Four racks hold the cathode-ray tubes (CRT) plus their associated regeneration amplifiers and gating circuitry. The remaining two racks contain the deflection generators, the counter, and other control circuitry. There are actually 48 CRT positions, but only 45 are employed at any one time. The other three positions are available as spares. Two types of cathode-ray tubes are used for storage, the 5UP1 and the 3KP1. The well-known dot-slide technique is used, in which a dot signifies a binary zero and a dash a binary one.

Figure 1.8 is a block diagram of the electrostatic memory for SEAC, showing the flow of information and the method of control. Numbers or instructions are transferred to the memory along parallel lines from the Shift Register, and this information is stored for as long as it is needed by a continuous process of regeneration, which takes place with the aid of the regeneration amplifiers. At any given time the location of the electron beam in the CRT is determined by the digital information in the Staticizer, which can be loaded from either the Address Register or the Regeneration Counter. The Staticizer sends out pulses of about 7-μsec duration. These pulses are sent to the Deflection Generators where they are decoded and converted to CRT deflection signals having very accurately derived voltage levels. All 48 CRT's are deflected in parallel, and the actions of turning the beam on and strobing the output signal of the amplifier are also performed simultaneously for all CRT positions.

The Operations Generator provides the proper "turn-on" signals to the CRT grids for both dot and dash conditions. It also provides a strobe pulse to the amplifier and a "twitch" signal to the Deflection Generators. The Synchronizer dispatches signals to the other units to insure that the correct sequence of pulses takes place and, furthermore, that these actions are synchronous with the rest of the machine.

When the electrostatic memory is being used, a read or write action can take place as frequently as every 48 microseconds. Of this time, only 12 μsec is actually required for the action, so the remaining time is always used to accomplish three regenerations.

The Shift Register and its Control comprise two full racks of equipment, which are shown in figure 1.9. Its size and complexity are due to its many functions. First, it acts as an intermediary, or buffer, storage between the input-output equipment and the serial acoustic memory. In connection with input-output operations, it also has the functions of digit counting, word counting, and word inversion. Further, the Shift Register acts as a register for the electrostatic memory, which operates in the parallel mode, and serves to provide the transfer to and from the serial representation in the rest of SEAC. In connection with the electrostatic memory, it also helps perform the logical transfer operation.

Figure 1.10 is a simplified diagram of the Shift Register showing how it connects to both memories. It will be noted that the register consists of 48 flip-flops arranged in a closed loop. Shifting may be done only to the right, as indicated by the arrows. During an input operation, the highest order of the number comes in first and is sent to stage 46. This digit then undergoes a

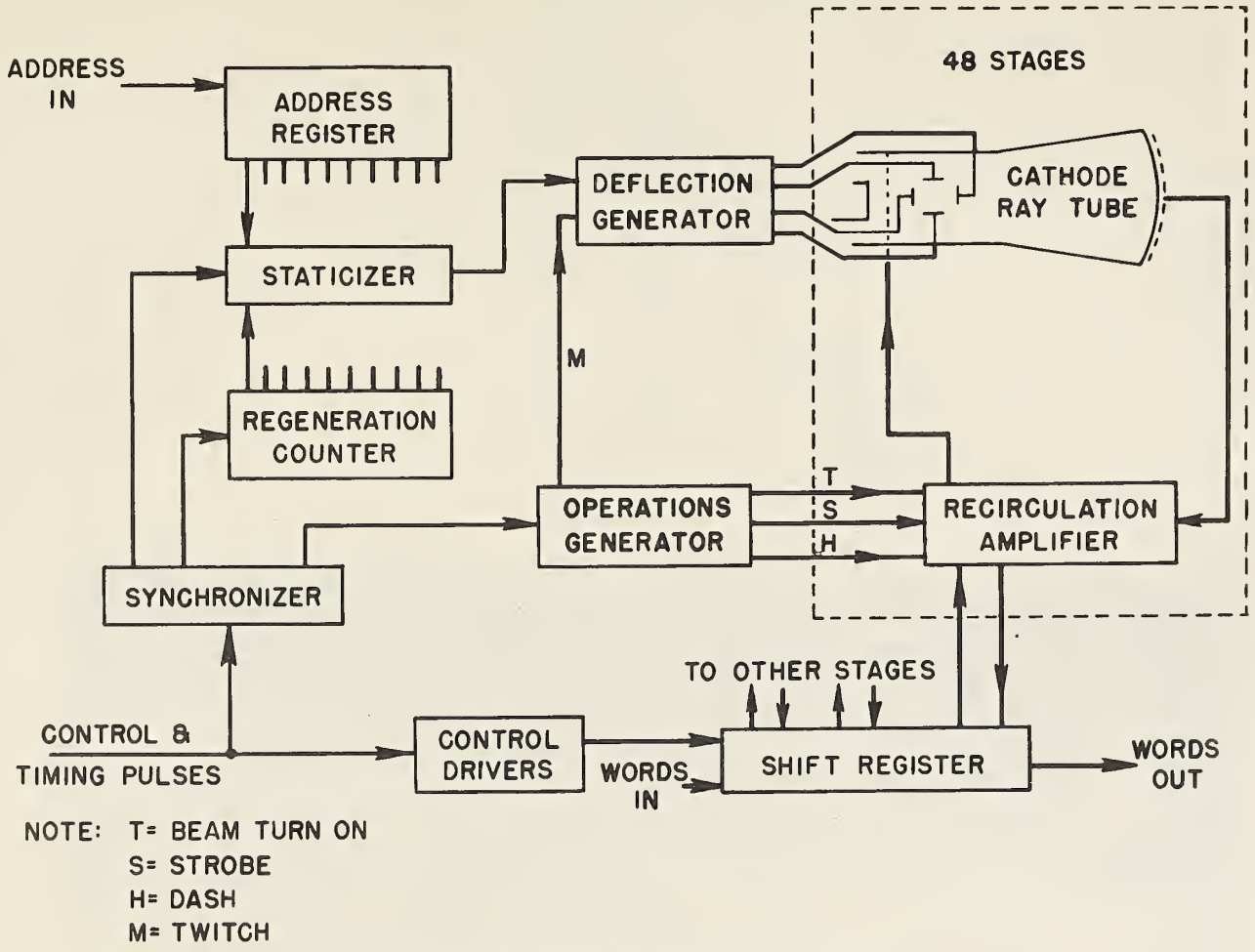

FIGURE 1.8. *Block diagram of the Electrostatic Memory.*

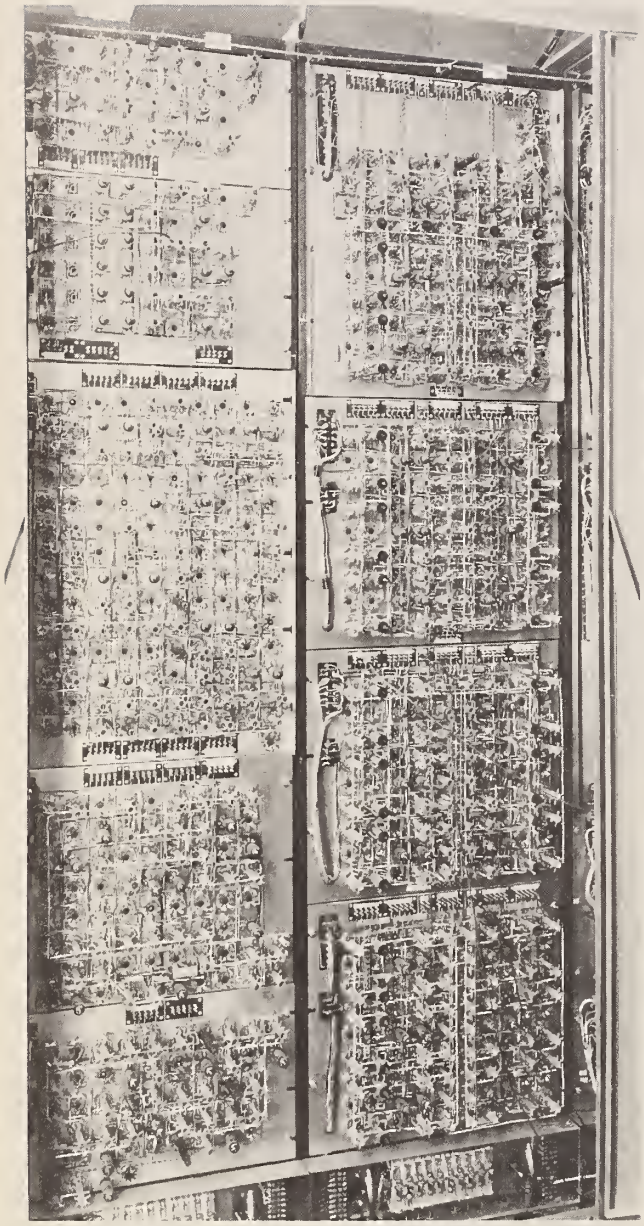

FIGURE 1.9. *Shift Register and Shift Register Control.*

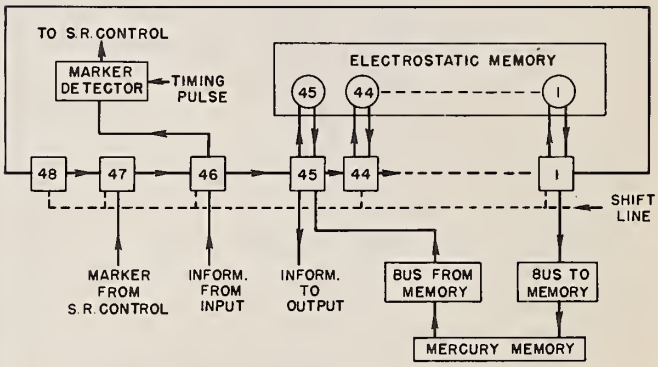

FIGURE 1.10. *Block diagram of Shift Register.*

series of right shifts, until it ends up in stage 47. Then the second highest order digit is inserted in stage 46, and again a series of right shifts takes place. This process continues until the entire number has entered the Shift Register. When the number is in position, a marker pulse signals the end of operation. At this time the number is shifted serially from stage 1 of the Shift Register into the memory at a one-megacycle rate.

During an output operation, the reverse process takes place. The number is shifted rapidly into the register through stage 45. Then, one digit at a time is sent to the appropriate tape, wire, or teletype unit via stage 45. The end of operation is again signalled by the marker pulse.

The Input-Output equipment used in SEAC is fully covered in a separate article. However, some salient facts pertaining to each type of equipment may be of general interest. The Teletype equipment operates at six characters per second, where each character represents four binary digits. This gives an equivalent speed of two seconds per word. Because of this low speed, Teletype is used primarily for manual operations, for which it is a very convenient means for printing out or inserting information in any memory location. The wire units, which employ cartridge loading, are used mainly for initial input and final output from the computer. The time required to fill the mercury memory from the wire input is about 12 sec, including the time for manual manipulations. The tape units developed at NBS for external storage use no reels and are single channel only. These units will hold up to 24,000 words on a 1,200-ft tape. Recently a multichannel tape unit was added to SEAC. Both types of tape units have extremely rapid acceleration, starting and stopping in less than 5 msec. This characteristic makes them especially valuable for external storage.

The Input-Output Selector (upper half of fig. 1.11) consists of the manual switches and the circuitry that are necessary to select one or more units for an input or an output operation. The system permits selection from among 10 different units. A unit may be selected automatically by inserting the proper information in the input or output instruction. The five binary digits that contain the necessary coding enter the Selection Register, as indicated in figure 1.12. The outputs of the register energize at least one selector relay (shown at the top of the diagram) by means of the Selection Gates and Automatic Selection Switches. These multicontact relays switch the necessary signals to control reading and writing on the unit. An input or an output instruction, of course, contains a code to designate a particular input-output unit; however, by means of manual switches on the Input-Output Selector one can establish any correspondence desired between the codes and the actual devices. This feature is especially useful when a new code is being checked or when one of the units happens to be inoperable.

The function of the Comparator is to determine when the input-output unit called for is different from the one previously chosen. Only in this situation is the computer halted momentarily while the necessary relays are energized. Automatic selection can be overridden by any of the manual selection switches. There are three of these switches, one for manual input operations, one for manual output operations, and one for direct selection during computation.

There are a number of auxiliary units physically separate from SEAC that allow the slow work of preparing input programs and data and that of printing the output results to be accomplished without losing valuable computing time. Teletype keypunches and reperforators are used to prepare the initial punched paper tape. An inscriber transfers the information from the punched tape onto magnetic wire for rapid computer input and automatically inserts the proper spacing between blocks of information. An outscriber takes the output data printed onto wire by the computer and produces a punched paper tape. This unit takes its information from a continuously moving wire, performs the necessary operations of counting and recognizing each binary digit, punches the paper tape, and checks for errors in the transcription to the wire as well as errors in its own operation. Additional equipment produces printed copy and/or punched cards from the tape punched by the outscriber.

Besides the fundamental requirements of starting and stopping the machine, the SEAC control console has many facilities that enable the operator to follow the course of the problem, print out any desired information, and make any changes that might be required. Only a few steps are required to put a new problem into the computer. These are clearing the control and memory, selecting the desired input unit, and pressing the start button. To perform a manual print out, the machine must first be halted by throwing the Run-Halt switch. The Computer then halts after performing the present instruction. The Print-Out switch is then positioned to allow the operator to print out either

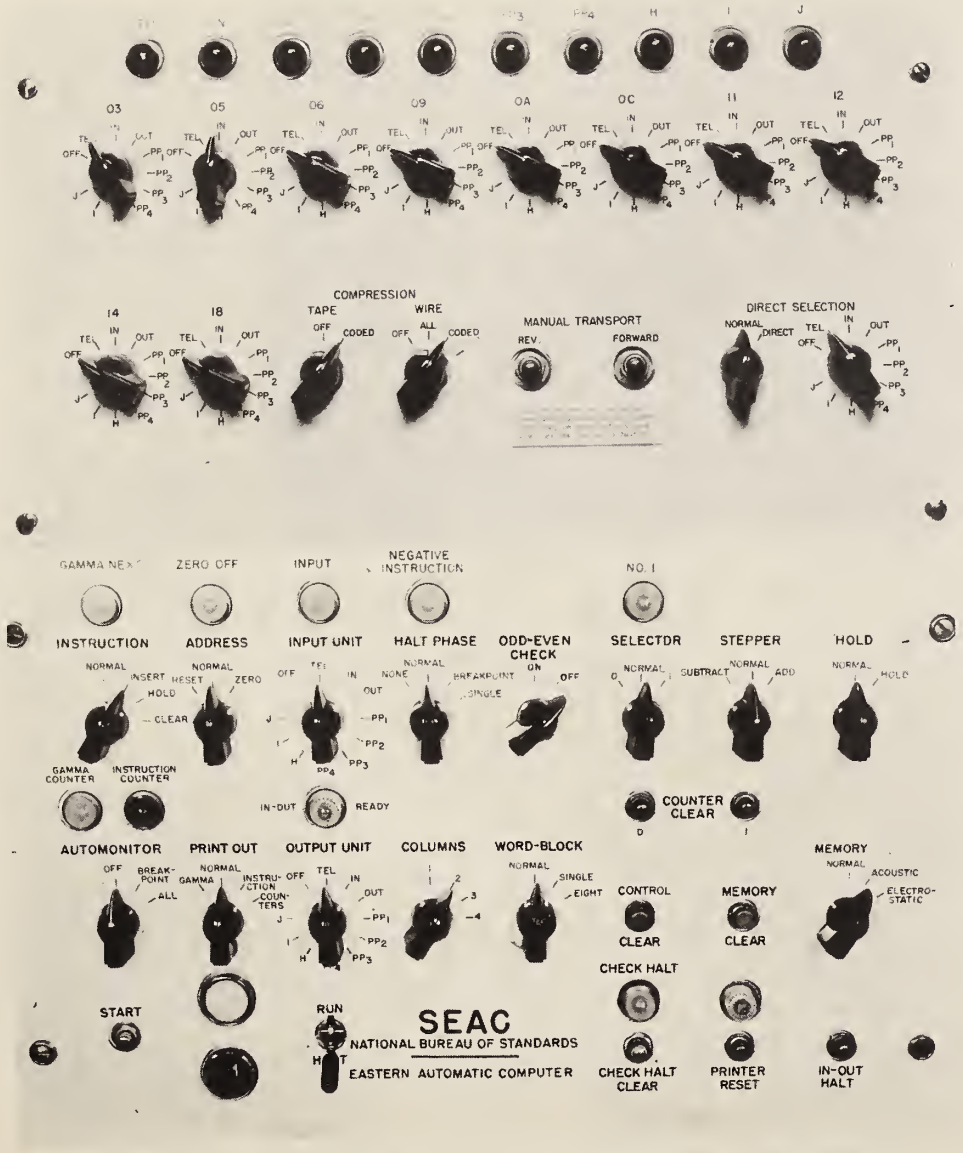

FIGURE 1.11. *Input-Output Selector panel and Manual Control Panel (bottom).*

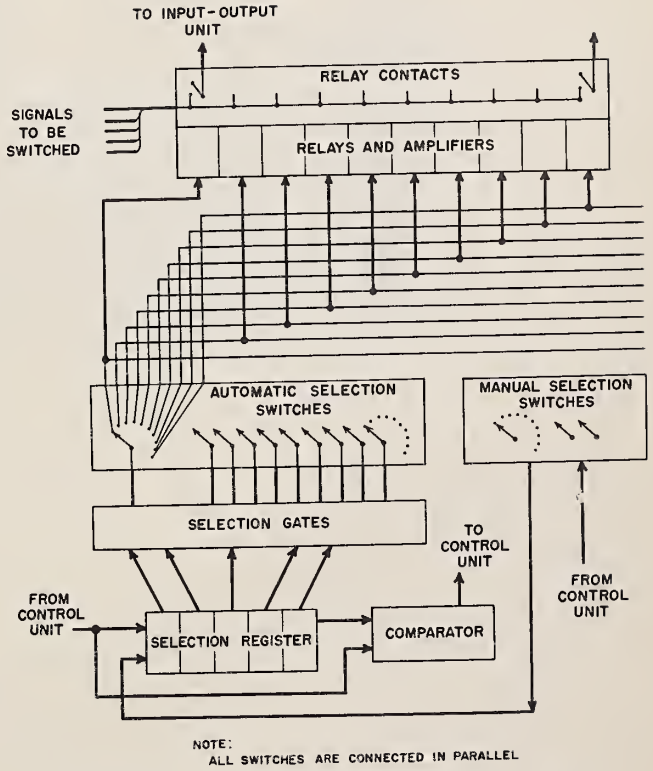

FIGURE 1.12. *Block diagram of Input-Output Selector.*

the instruction just performed, the result of the instruction, or the counter contents. The manual output selector switch allows the operator to select any unit, but the one usually chosen is Teletype.

To insert a word into any specified memory location, first the machine must be halted and the Instruction switch thrown to INSERT. When the Start button is pushed, an input instruction in which γ is the specified location is read into the first cell of the memory from the unit selected by the Input Selector Switch. Again the unit selected is usually Teletype. The Instruction switch is now set back to normal, the Start button pushed once more, and the operation completed. The memory Selector switch permits computation to be carried out in either the Electrostatic or Mercury Memory without a change in coding. In the Normal position of the switch, both memories are in use. The preceding discussion is by no means an exhaustive treatment of the switches and manual control operations available, but mentions briefly those most frequently used.

4. CIRCUITRY AND SYMBOLS

The circuitry of SEAC follows a rather uniform pattern throughout most of the central computer, with the exception, of course, of recirculation amplifiers, magnetic tape amplifiers, and the like. This pattern consists of diodes and resistors for gating, a beam power tube for amplification, and a transformer for coupling to subsequent stages. By intensive engineering of a single type of circuit, a high degree of reliability was achieved and subsequent design, testing, and maintenance were simplified.

Figure 1.13 shows a typical gating stage, of which there are numerous variations. Certain facts about the gating should be pointed out. The diode structure is three gates deep, or-and-or. Up to five inputs are allowed to each gate before the resistor values must be changed; however, this condition occurs in very few locations. The resistors are computed to allow a minimum rise of 100 v/μsec during any part of the pulse excursion. The diodes drawn in a horizontal direction carry pulse information; those drawn in a vertical direction are the clampers. It will be noticed that the gate output, which connects to the grid of the amplifier, is connected to a -5-v clamping diode. As the middle of the gate employs a -8-v clamping diode, a 3-v disconnect is obtained across the final or-gate. This is important in preventing noise from producing spurious signals. An additional disconnect of 2 v is achieved by connecting the positive output of the transformer to -10 v. Negative inputs to and-gates that are used for inhibition omit the initial or-gate, and the position of the -8-v clamping diodes is shifted to prevent them from drawing excessive current.

The single vacuum tube in the stage, tube type 6AN5, has no gating function. Its purpose is power amplification only. The 6AN5 is a miniature beam power tube with some excellent characteristics for this kind of computer service. Its pertinent characteristics are enumerated as follows:

Input capacitance	9.0	$\mu\mu$f.
Output capacitance	4.8	$\mu\mu$f.
Transconductance	8000	μmhos.
Filament rating	0.45 amp at 6.3 v.	

The cathode material is passive nickel, which apparently prevents the formation of interface. In the unpulsed condition the tube stands by with a current of at least 1 ma. The clamping diode to +2 v and a small resistor in the cathode circuit help keep the dissipations of the control and screen grids within ratings.

The transformer used for coupling has several advantages. It provides impedance matching between tube and load, it enables a single stage to transmit either positive or negative pulses, and it avoids the difficulties involved in dc coupling. A step-down ratio of either 5 to 1 or 7 to 1 is used in most SEAC circuits. In any case, the equivalent load presented to the tube is such as to cause the tube to bottom, i.e., to operate below the knee of the $e_p - i_p$ curve. This kind of operation results in almost uniform voltage output even though tubes with 2 to 1 variation in current capabilities are plugged into the same circuit. The cores of the pulse transformers in SEAC are grain-oriented silicon iron in 0.001-inch thick laminations.

As SEAC is a synchronous machine, it requires precise timing pulses to all its circuits to keep the various parts of the machine in step. This is accomplished by the use of a 1-Mc master clock

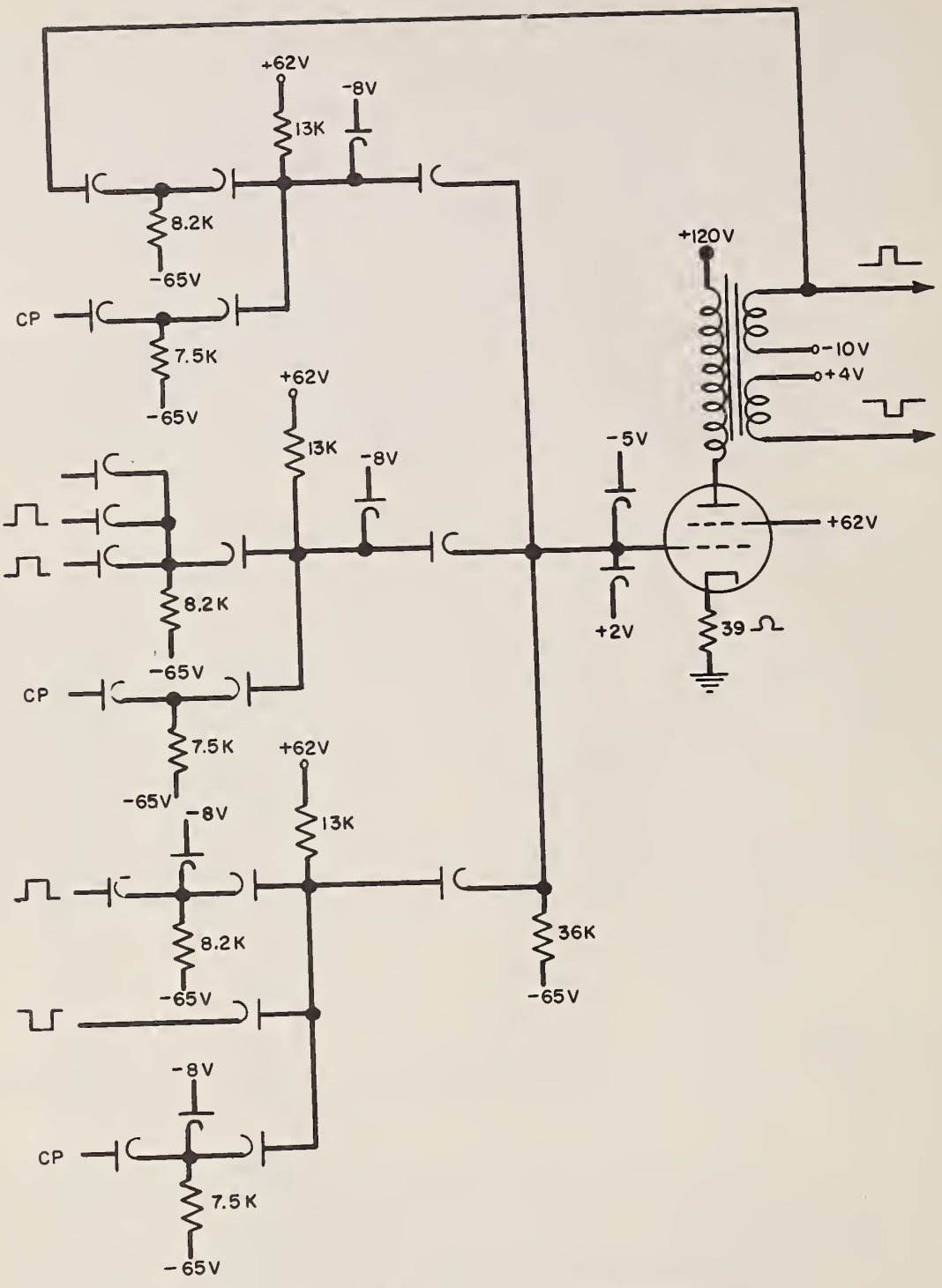

FIGURE 1.13. *Circuit of typical SEAC stage.*

which resembles a small radio-frequency transmitter. The clock signals are not distributed as rectangular pulses or half sine waves, as might be expected, but are full sine waves. There are definite advantages in using sine-wave distribution from the viewpoint of generation at high power levels, distribution without excessive pulse deterioration, and ease of phase shifting to produce the same precise timing in all parts of the computer. As the clock signal passes through the gating structure, only the trapezoidal center portion reaches the grid of the tube. These clock pulses are slightly under one-half microsecond at the top of the gating level. Although the computer could have been designed with a clock having only a single phase, the clock signals are actually distributed in three phases 120 degrees apart, which are named CP_1, CP_2, and CP_3. Because of the slight time delay in each SEAC stage and the overlap of successive clock phases, it is possible to send the output of a stage clocked with CP_1, for example, into the input of a stage clocked with CP_2 without the use of delay lines. Furthermore, three stages of gating may be done with only a 1-μsec delay. This is especially helpful in those parts of the machine where the time available to accomplish the necessary number of logical operations is limited. Figure 1.13 shows how the clock pulse is inserted into each and-gate.

A problem closely related to that of timing is that of pulse reshaping, so that the input signal on the amplifier grid is essentially a clock pulse. This may be accomplished by making sure that the incoming signals to any stage overlap both the leading and trailing edges of the particular clock phase used. As the incoming pulses will certainly be no broader than the clock pulses that produced them, delay lines may be used to achieve the necessary overlap. The method known as regeneration, which was devised shortly before the computer construction program began, accomplishes the same result without delay lines. All that is necessary in this method is that the pulses into a stage overlap the leading edge of the clock pulse. The positive output of the transformer is fed back as one of the inputs of the stage, and thus the pulse is held up until the trailing edge of the clock terminates it. The regeneration line is shown near the top of figure 1.13.

Electrical delay lines play several important roles in the computer. They are utilized in connecting stages where the clock phases are not consecutive; where a circulating register of any given length is required, e.g., the one-word Instruction Register; and where a pulse requires broadening, such as when a negative signal is used in an and-gate for inhibition.

The type of delay line used most generally in SEAC is of the continuous-wound design with an external ground shield. Lines of two different impedances are used: 1,350 ohms into a single gate and 800 ohms into two gates. The type of line used offers several advantages in this kind of computer service, viz., small space requirements, ability to be cut to exact value, satisfactory rise time for half-microsecond pulses, low temperature coefficient, and low attenuation. Delay line lengths in the computer vary from as little as 0.11 to 5.10 μsec.

One of the most frequently used circuits in any digital computer is the familiar Eccles-Jordan flip-flop. Its counterpart in the SEAC type of circuitry is called the dynamic flip-flop. This is not a flip-flop in the usual sense. Whereas the output of a conventional circuit has one of two d-c levels, the dynamic flip-flop output is considered to be in the "one" state when its output is a series of half-microsecond pulses and in the "zero" state when in the unpulsed condition.

The regular gating stage can be connected so as to become a dynamic flip-flop by returning the positive output of the transformer to the input through a delay line. By making the delay around the loop 1 μsec, there will be produced a continuous train of pulses until turned off. Only two and-gates plus a regeneration gate are required. The first gate can turn on the flip-flop with a single pulse, and the second gate serves as the recirculation path. The latter gate must also contain an inhibitor input to turn off the stage when desired.

Although the functions of a given chassis can be traced by using a detailed circuit diagram, this is often extremely arduous because of the maze of signal leads, resistors, tubes, and the like. A set of easy-to-follow symbols was developed during the preliminary period of computer design. These are shown in figure 1.14. As a tube is always associated with a transformer, a single symbol is used to denote both. A small circle indicates a negative output. Gates are symbolized by a closed semicircle, with the arc indicating the output side, thus eliminating the necessity for an arrow. And-gates are distinguished from or-gates by allowing the input lines to come up to the semicircle in the first case and through the semicircle in the second case. Negative pulse inputs

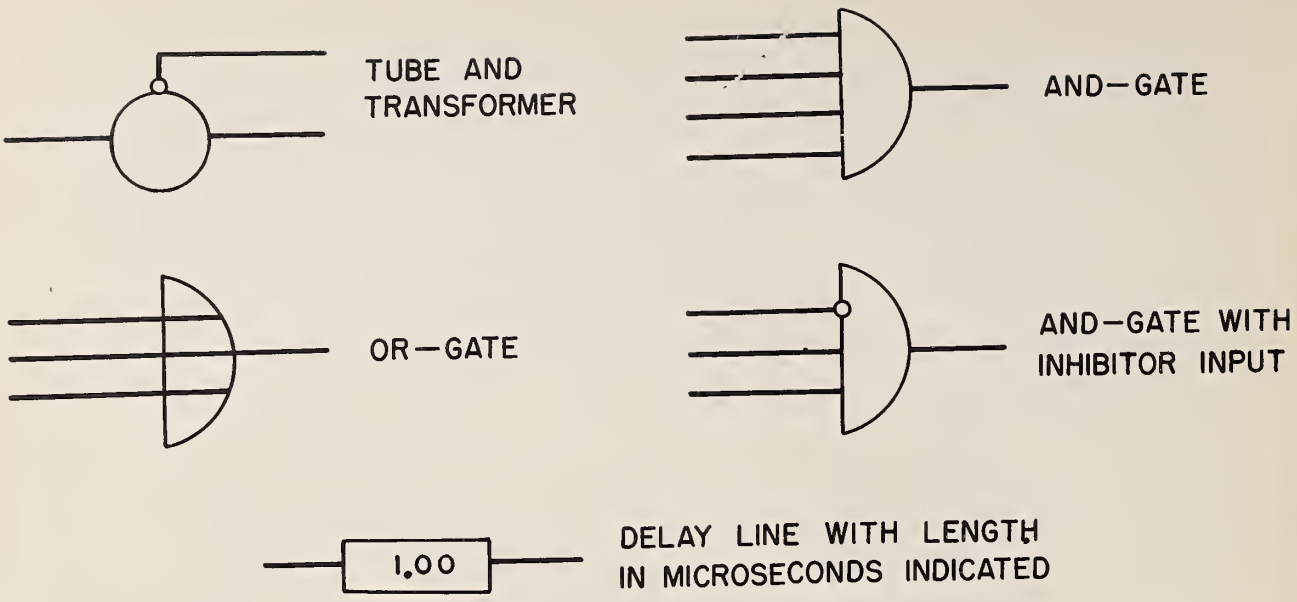

FIGURE 1.14. *Logical symbols used in SEAC.*

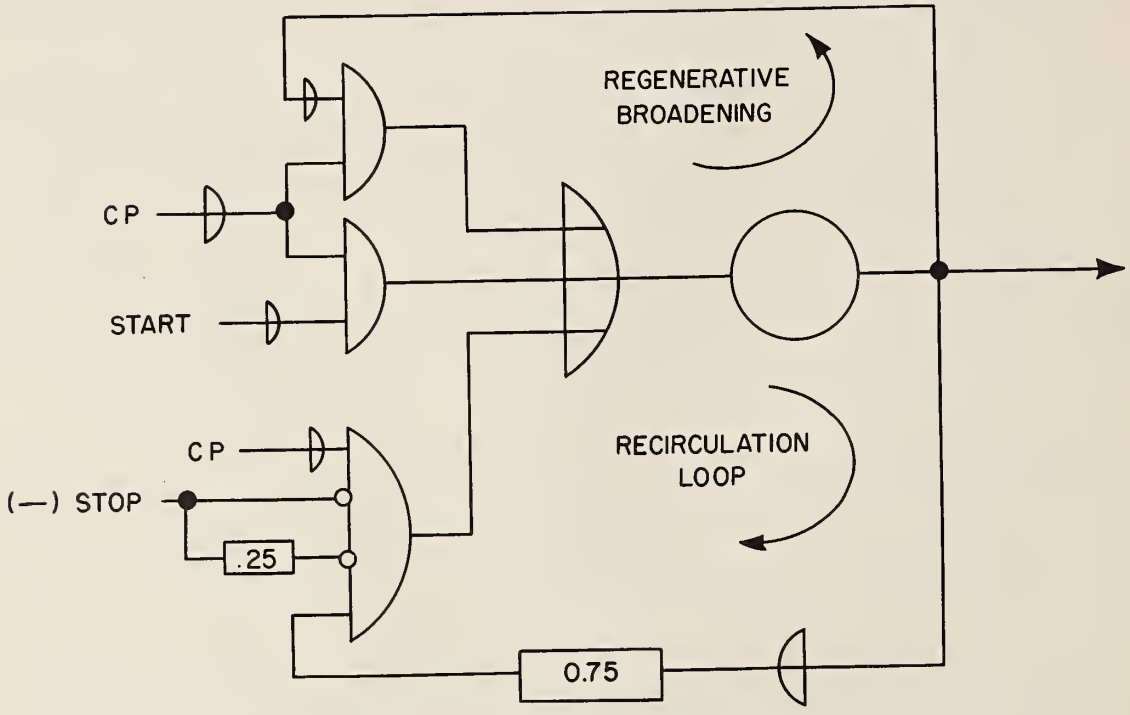

FIGURE 1.15. *Logical diagram of dynamic flip-flop.*

are again indicated by a small circle. Delay lines are symbolized by rectangles with the actual delay period indicated in the box. Figure 1.15 shows how these symbols are used in the logical diagram of the dynamic flip-flop just described.

Several advantages, some very obvious, have resulted from the use of a uniform circuit design. The fact that it allowed concentrated effort on a single type of stage has already been mentioned. Another advantage is that only one tube type is used, and tube selection is based on a single wide specification. The acceptable limits on plate current are 25 to 50 ma, with zero grid bias and +62 v on the screen and plate. These limits apply when checked with 5.7 v on the filament, as well as with 6.3 v. A tube is also rejected if there is an abnormal plate current variation when checked at the two filament voltage levels.

All diodes in SEAC are subject to the same specification, which, for initial installation, permits only 250-μa back current at 40 v and 2 v forward drop at 20 ma. Before a diode is removed the back current may increase to 500 μa.

It is possible to use unshielded wiring for distances up to 40 or 50 ft without encountering trouble from noise, because of the low effective impedance of the circuits. When the stage is pulsed, the tube-transformer combination presents a very low impedance. During the nonpulsed condition, it is the forward resistance of the −8-v clamping diode that furnishes the low impedance.

5. PHYSICAL CONSTRUCTION

Some of the over-all aspects of the physical construction of SEAC may be of general interest. The frame of the computer consists of two rows of nine standard relay racks (18 in all) with a walkway between. This arrangement does not include the mercury memory and the input-output equipment. When the computer was first put into operation, many of the racks were unfilled. This fitted in with the experimental nature of the machine and allowed for the expansion that was contemplated. At the present time the racks are completely filled by the additions that have since been made. On the interior, all plug-in components are easily accessible as are the interconnections between chassis. On the exterior, all chassis wiring, resistors, and tubes are also readily available. Thus any point on any chassis can be easily inspected either visually or electrically by means of oscilloscope or voltmeter. The accessibility is such that much of the early modification of circuits was done with the chassis in place.

Each relay rack has, on the average, four chassis of varying size. Filament and d-c power are made available at the bottom of each rack, where each line is fused individually. Power is transmitted from one chassis to another merely by plugging each chassis into the one below it.

The three-phase clock system is distributed in very much the same manner as the d-c power. Phasing controls and shaping circuits are provided on each rack for the individual clock phases. The shaping circuits are parallel L-C combinations located at both top and bottom of the rack to help maintain proper sine-wave form.

All signal outputs which must be sent from one chassis to another, are first terminated on a connector strip made especially for this purpose. This terminal strip is a rectangular piece of thin Bakelite on which are mounted pins similar to those used on an octal base, except that they are made available on both sides. For interchassis wiring, flexible insulated wire is used. Small female connectors that fit the pins on the terminal strip are mounted on either end.

Although the mechanical arrangement of components is not the same for all SEAC chassis and reflects the change in ideas that occurred during construction, the majority follow certain practices. Figure 1.16 shows both sides of a typical chassis. It will be noticed that tubes, resistors, and wiring are all located on one side, and the other components are on the other side. Everything except resistors and wiring is plug-in and is easily replaced.

The chassis are essentially two dimensional, although the use of turrets and plug-in components gives a certain amount of depth to the construction. This is achieved without any appreciable loss of accessibility, which is one of the main advantages of the two dimensional layout. Placing tubes and resistors on one side of the chassis and all other components on the other side separates the

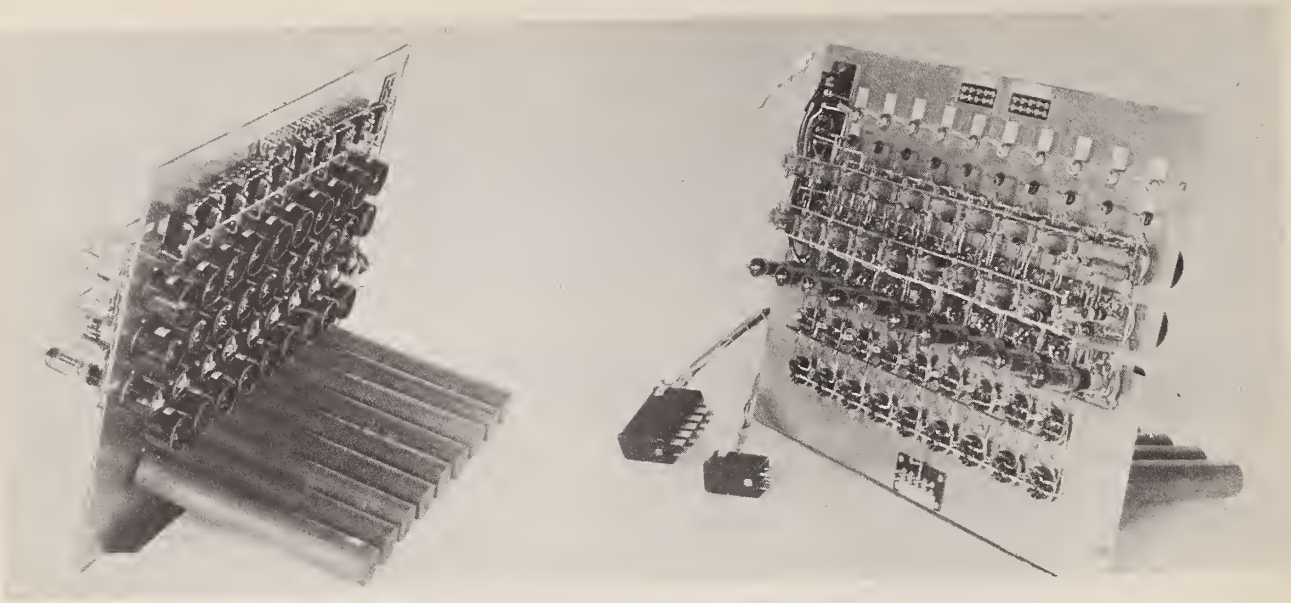

FIGURE 1.16. *Both sides of typical chassis.*

FIGURE 1.17. *Typical plug-in units.*

principal heat-generating elements from the heat-sensitive components, the most sensitive of which are the germanium diodes.

The plug-in components consist mainly of pulse transformers, electrical delay lines, and germanium diodes. Their construction is similar in that all use octal tube bases with solder-dipped connections. In figure 1.16 the first, second, and fourth rows are the diode clusters mounted in octal tube bases. The components in the third row are pulse transformers mounted in similar tube bases. The bottom row contains plug-in delay lines. These are made from a long length of delay line cut into sections of approximately the right length, which are then tailored to the desired value. When the electrical length of the delay line is not more than about 2 μsec, the line can be mounted in an octal tube base and covered with a protective Bakelite tube. Longer lengths of line are coiled in aluminum containers for mounting on the chassis. A more detailed view of typical plug-in units is shown in figure 1.17. The diode clusters, which comprise the majority of the plug in units, consist of from 4 to 7 germanium diodes connected in a variety of ways. By restricting the number of diodes in a cluster to seven, each diode can be checked individually in the unit. As there are over 20 different types, there is sufficient choice to permit the straightforward layout of gating circuitry. When a cluster is rejected from the machine because of diode deterioration, the cluster is salvaged and only the bad diode (or diodes) is replaced.

Depending on their use, transformers are made with several different primary inductances and primary-to-secondary turns ratios. Originally, transformers were potted with a high-temperature wax compound, but later they were bracket-mounted to permit air cooling.

6. OPERATING PERFORMANCE

During most of its 3 years of operation thus far, SEAC has been in use 24 hours a day, 7 days a week. Regularly scheduled computation comprises the bulk of the 168-hour week, with smaller amounts given to routine maintenance and experimental engineering. During routine maintenance periods a continuing check of tubes and diodes is made such that all tubes are checked every 3 months and all diodes every 6 months. In addition, a system of marginal checking is used in which several of the more sensitive gating voltages are shifted up and down. Simultaneously, standard test routines are run and the point at which failure occurs is noted. Any poor tolerances that show up are investigated further. Several other items that are checked during the weekly maintenance period are (1) phasing of 1-Mc clock on each rack, (2) mechanical adjustment of Teletype equipment, (3) gain of Mercury Memory recirculation amplifiers, (4) condition of magnetic tapes.

A fair-sized library of routines has been accumulated for checking the Mercury Memory and various specific machine operations. However, except when unusual difficulties arise, use of two standard test routines is sufficient. One of these checks the memory for its ability to store several different pulse patterns; the other checks the ability of the Arithmetic Unit to perform the various operations. When an error occurs in either routine, the operator can usually diagnose the trouble by analyzing the information printed out.

In a machine as complex as any of the modern digital computers, the operator should be given, in procedure or machine facilities, any aid possible in checking codes and running problems. One of the procedures that has been used to great advantage with SEAC is summing of the memory. For example, after every read-in from magnetic wire, the machine is used to sum the information read-in, after which the sum is compared with the known correct ones. This enables the operator to know immediately whether or not the information has been correctly transferred into the memory.

The use of the sign in the instruction code to halt the computer has already been described. By manipulating one of the switches on the control console, the halt action can be modified in such a way as to help the operator check new codes. On one switch position the machine halts on all negative instructions, on the second position the machine halts only on negative print instructions, and on the third position the machine ignores all coded halts. If the operator uses negative instructions at strategic points (breakpoints), he can more quickly check the accuracy of his coding. Once the code is proved, he can then eliminate these breakpoints merely by throwing a switch without any necessity for changing his code.

Another valuable operator aid is the automonitor feature. The action of printing out the instruction, the result of the operation, and the counter contents is particularly useful when checking out a new code. The operator can set the automonitor switch so that all instructions are monitored or so that only negative instructions are monitored. If a code does not work the first time it is tried, the operator can automonitor the breakpoint instructions. By examining the information printed out, he can determine between what two points in the code the trouble occurred. He can then monitor all instructions between the two points and thus determine the exact point at which the program is in error.

The speed of various arithmetic operations in SEAC is given in table 2. This is arranged by acoustic and electrostatic memories.

TABLE 2

Operation	Time for complete operation, including access time (in milliseconds)			
	Acoustic memory			Electrostatic memory
	max	min	avg	
Addition	1.54	0.19	0.86	0.24
Subtraction	1.54	.19	.86	.24
Comparison	1.20	.19	.70	.19
a. Algebraic.				
b. Absolute.				
Logical transfer	1.54	.19	.86	.24
Logical multiplication	1.54	.19	.86	.24
Multiplication	3.65	2.30	2.98	2.35
a. Major part, unrounded.				
b. Major part, rounded.				
c. Minor part.				
Division	3.65	2.30	2.98	2.35
Base	1.20	.19	.70	.19
File	.86	.19	.52	.24
Clear	1.54	.19	.86	.24

An article on SEAC would be incomplete without some mention of the computation performed since the machine went into operation. During the past 3 years, hundreds of problems covering a wide range of applications have been run on SEAC. A list of broad categories of problems with a few examples in each category follows:

1. Mathematics and statistics:
   Table of Jacobi elliptic functions for real arguments.
   Solution of partial differential equations by Monte Carlo method.
   Generation of optimum sampling plans for the Bureau of the Census.

2. Physics problems:
   Crystal structure.
   Relative abundance of the elements.
   Wave functions for helium atom and for lithium atom.

3. Engineering problems:
   Optical system design.
   Synchrotron design.
   Starting transient in a class C oscillator.
   Transient stresses in aircraft structures.
   Plastic deformation of eccentric columns.

4. Business management and economic problems:
   Problems related to Air Force program planning.
   Problems related to social security accounting procedures.

5. Problems of a security classified nature for the Atomic Energy Commission and the Armed Forces.

2. Dynamic Circuitry Techniques Used in SEAC and DYSEAC

R. D. Elbourn and R. P. Witt

1. INTRODUCTION

Development of the digital computer pulse circuitry to be described began in 1948 with the decision to build the Standards Eastern Automatic Computer, SEAC [1][1]. The functional plan of SEAC was derived from that of the EDVAC built by the Moore School of the University of Pennsylvania. It operates in the serial mode at a 1-Mc pulse-repetition rate. Since the completion of SEAC this circuitry has been improved in reliability and efficiency and has been packaged into just two types of etched-circuit plug-in packages, which are used in the NBS computer, DYSEAC [2].

The first of the decisions that fixed the characteristics of this circuitry was to adopt the serial mode of operation at a 1-Mc repetition rate, as was being used in the EDVAC built by the Moore School of the University of Pennsylvania. The next was to minimize the number of tubes by performing all the logical operations of "and," "or," and "not" between pulses in circuits comprised of germanium diodes and resistors. Such diode circuits were suggested in a preliminary report on UNIVAC by the Eckert-Mauchly Computer Corporation and were described with variations by T. C. Chen [3] in early reports on EDVAC.

To extend the life of the diodes, back voltages were kept low by restricting the amplitude of pulses from 10 to 20 v. On the other hand, complex cascades of diode logic circuits require considerably more driving current than vacuum-tube circuits. Thus there were presented loads of much lower impedance level than vacuum tubes can drive efficiently. An obvious solution was to use small step-down pulse transformers such as had been extensively studied at the Massachusetts Institute of Technology [4]. However, there remained the problem of achieving uniform shape and timing of pulses at the high- but variable-duty cycle that occurs in a serial-type machine.

In addition to supplying large pulse currents at low voltage, the use of pulse transformers has these advantages: 1. Eliminating d-c coupling permits all tubes to operate from the same supply voltages. 2. All tubes can operate with positive pulses on the grid, i.e., no inverter stages are required, because with two secondaries each transformer can supply both positive pulses for normal signals and negative pulses for inhibiting. 3. Performance of a-c-coupled pulse-amplifier stages is less critical of tubes, because it depends on only their incremental characteristics.

The disadvantages of transformer coupling stem chiefly from the fact that during a pulse the magnetic flux in the transformer core must increase in direct proportion to the voltage-time area of the pulse, and a corresponding magnetizing current is required in addition to the load current. Then after the pulse, to bring the flux and the magnetizing current down again to their original values, an equal but negative voltage-time area is required. In other words, a negative-going backswing transient must follow each pulse. This limits the maximum duty cycle of pulses to about one-half, so that the speed of the computer is only one-half of what it would be with the same rise time and tolerances if the pulse-envelope or nonreturn-to-zero system could be used. However, this inefficiency is more than compensated for by the greater power that a tube can deliver with a transformer. There do remain, however, some variations in pulse shape and timing due to variations in magnetizing current between the first and later pulses of a train.

In EDVAC the one-word registers needed in the arithmetic and control units are dynamically circulating loops comprised of electrical delay lines, repeater amplifiers, and clocking gates. This scheme is also used in SEAC because it requires fewer tubes than do static flip-flop registers. The logical reduction of this idea to storing an individual pulse in a one-pulse-time circulating loop called a dynamic flip-flop was suggested in the preliminary report on the UNIVAC. The dynamic

[1] Figures in brackets indicate the literature references at the end of this paper.

flip-flop completely replaced the Eccles-Jordan type in SEAC, because it uses only one tube and can drive a number of external gates without additional amplification. These decisions resulted in a 1-Mc repetition rate digital computer circuitry that has basic uniformity in design and clean separation in function: All logical operations are done by diode-resistor circuits, all incidental storage is done by electrical delay lines, and all amplification is done by transformer-coupled pulse amplifiers of a standardized design using only one type of tube.

Since the construction of SEAC, the circuitry has been improved (1) by increasing the positive grid drive, the plate supply voltage, and the turns ratio to obtain more power output; (2) by changing the 1-Mc clock signal from 3-phase to 4-phase to improve timing tolerances; and (3) by substituting a smaller more efficient transformer using a ferrite core [5]. Many features of this circuitry were later adopted by the Moore School in the design of MSAC. Further improvement was achieved by studying the SEAC circuits to find an efficient way to divide them into a few standard plug-in packages. A group at the Air Force Missile Test Center, Patrick Air Force Base, Florida, and another at the Willow Run Research Center of the University of Michigan have each built computers using these packages. More recently the circuitry has been incorporated into etched-circuit dip-soldered packages of just two types. One contains diode gates and buffers with a tube and transformer. The other contains lengths of electrical delay line and suitable terminating circuits.

Although this paper will describe only the vacuum-tube version, it is of interest to note that J. H. Felker has adapted the principles of this circuitry for use with transistors [6]. He retained the configuration of the diode and delay circuits, the repetition rate, and even the impedance levels, but he was able to reduce the levels of voltage and current by a factor of about 10 and to reduce the physical dimensions accordingly.

2. THE TUBE PACKAGE

A tube package contains a tube and transformer, five and-gates, an or-gate for feeding the output of the gates to the grid of the tube, an output buffer to permit the transformer to drive the gates of subsequent packages, and six spare diodes, which may be connected to provide additional inputs to the gates as required. The circuit is shown in figure 2.1. In the normal or quiescent condition of no pulses, the diodes of the gates are conducting because their input terminals are held at slightly below −8 v by being connected to the positive output terminals of preceding packages. Each positive output terminal is held just below −8 v by its −8-v limiting diodes, which are kept conducting by pull-down resistors to −65 v. With the output terminals of the and-gates at about −8 v, the diodes in the or-gate are nonconducting because a limiting diode prevents the 39K (39 kilohm) resistor from pulling the grid down much below −5 v. The 3-v back bias on the or-gate diodes protects the grid from noise such as cross-talk on long leads between packages or variations in forward drop across the −8-v limiting diodes. To achieve the same protection by grid cutoff would require more bias and hence larger pulses, much of which would be wasted in charging the grid capacitance through a region of very low transconductance.

If one compares the direction of low resistance of the diodes in and-gates and in or-gates, it will be apparent that the output voltage of an and-gate approximates its *lowest* input voltage; whereas, the output voltage of an or-gate approaches its *highest* input voltage. Therefore, an or-gate performs the logical "or" function because it will transmit a positive pulse applied to any of its input terminals. On the other hand, an and-gate performs the logical "and" function because it can transmit a positive pulse only when all of its input terminals are pulsed positively.

The choice of resistance values depends upon current requirements, which are calculated by working back from the grid. At the end of a pulse, when the or-gate diodes have all cut off but the grid is still at +2 v, the 39K resistor must pull the grid down by discharging all the parasitic capacitance of the grid circuit. This capacitance is 19 $\mu\mu$f, and a speed of at least 75 v/μsec is required under the most unfavorable combination of 5-percent tolerances on both supply voltages and resistances. At the leading edge of a pulse the 10K resistor in a gate is able to overcome the 39K resistor and to pull the grid up at 75 v/μsec under the worst combination of 5-percent tolerances and with 19-$\mu\mu$f capacitance on the and-gate junction. This includes the capacitance of connecting spare diodes as additional inputs to the gate. At the top of a pulse the 10K resistor supplies grid current required to obtain maximum output from the tube, but the limiting diode connected to +2 v prevents excessive grid current which would occur when two or more and-gates operate simultaneously.

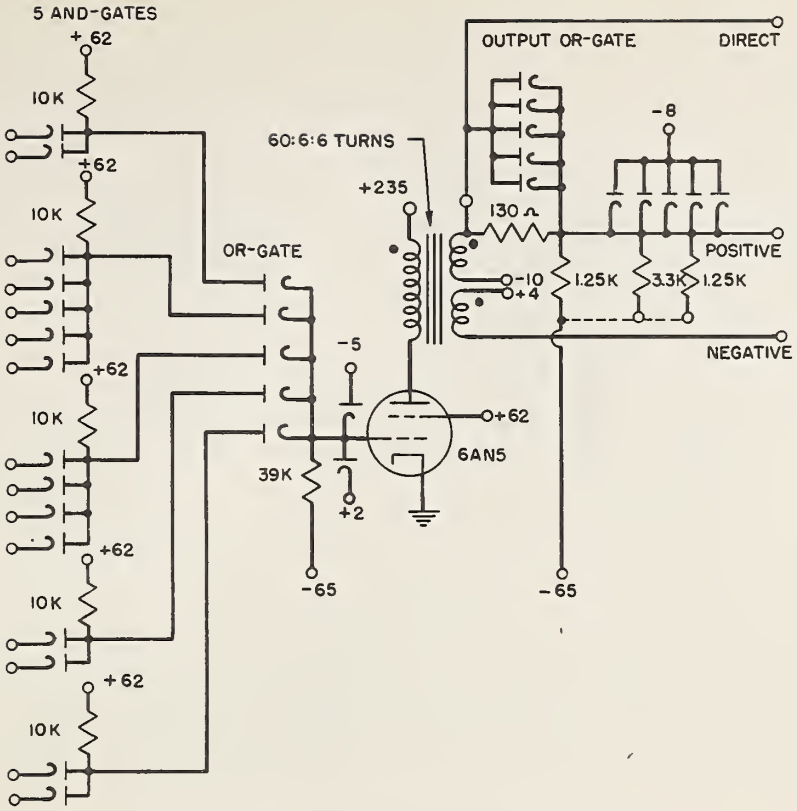

FIGURE 2.1. *Circuit diagram of the tube package.*

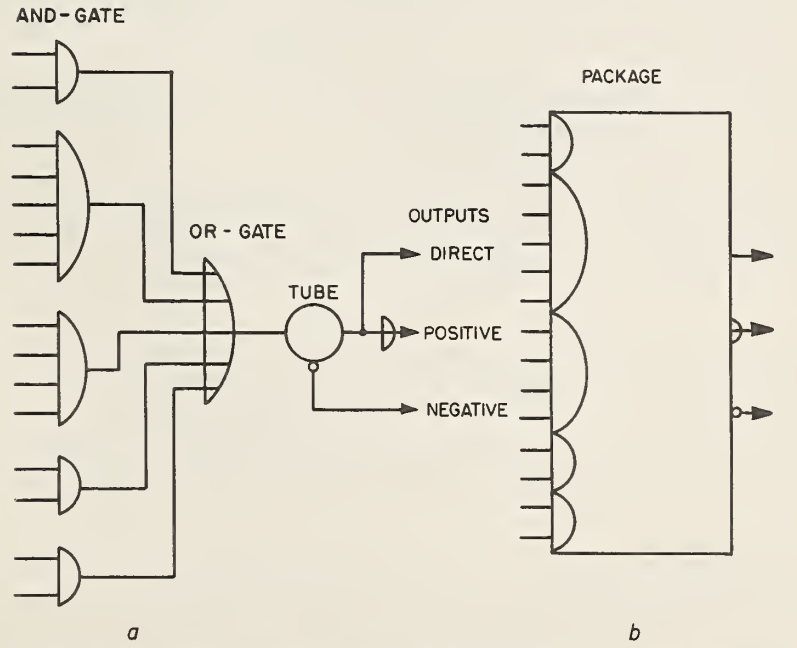

FIGURE 2.2. *Logical diagram symbols for the circuit of the tube package.*
(a) In SEAC notation, (b) in simplified notation.

A diode and-gate imposes quite unusual requirements upon the sources that drive it. When a source pulses positively, its gate diode simply cuts off so that practically no current flows. But when a source is *not* pulsing, it must actively exert its veto power by drawing through its gate diode whatever current is necessary to hold the potential of the and-gate down to about -8 v. Only when *all* the inputs to a gate go positive simultaneously should the 10K resistor be permitted to pull up the output voltage of the gate and, through conduction of its or-gate diode, to transmit a positive pulse to the grid. Whenever some but not all of the inputs to an and-gate are pulsed, the remaining unpulsed inputs must suddenly accept with little change in voltage a different proportion of the current supplied by the 10K resistor; therefore, a low dynamic impedance is required. By themselves, a tube and transformer are not a suitable source, because when not pulsed they may present as much as 300-ohm impedance at 1 Mc. The required low dynamic impedance is achieved by the forward conductance of the -8 v limiting diodes in the output or-gate.

To keep them conducting, even when all other sources pulse, the pulldown resistors that return to -65 v must draw more current than can be supplied by the 10K resistors in all the and-gates connected to the output or-gate. Because the positive pulse secondary of the transformer returns to -10 v, the series diodes in the output or-gate are cut off so that none of this current is trapped in the high dynamic impedance of the transformer. When the tube is turned on, a 20-v pulse appears at the secondary of the transformer, the series diodes conduct, and the transformer supplies the current taken by the resistors to -65 v. Three resistors are provided to permit the load on the positive output to be adjusted to the number of and-gates actually to be driven. Each 1.25K resistor can hold down five gates and the 3.3K resistor can hold down two. The rest of the rated driving capacity of 14 1/2 gates for the package can be used at the negative and the direct outputs. One of the 1.25K resistors is permanently connected to insure that there will be at least enough load to prevent excessive screen dissipation. The 130-ohm resistor that shunts the series diodes of the output or-gate adds no load during a pulse, but it provides somewhat less than critical damping for the negative-going transient that follows a pulse. The combination of the 130-ohm damping resistor and the permanently connected 1.25K resistor is sufficient to prevent the underdamped transient from going above -8 v.

The function of inhibiting an and-gate is accomplished by connecting the negative output of a transformer directly to an input diode of the gate. Because the negative winding returns to +4 v, this diode is normally nonconducting and does not affect the operation of the gate. But whenever a negative pulse is applied to this diode, it becomes the most negative input to the gate and by conducting prevents any positive output at that pulse time. An inhibiting connection does not require an or-gate ahead of it because it carries current only during a pulse, when the tube and transformer present a very low impedance.

The direct output terminal of the transformer is used to drive electrical delay lines and to drive or-gates other than the output or-gate.

For one familiar with Boolean algebra [7] it will be seen that the configuration of diode logic circuits in these packages will allow one to realize any required logical operation. In Boolean algebra "and," "or," and "not" are a complete set of connectives; moreover, the pattern of a set of and-gates feeding one or-gate corresponds to one of the normal forms in which every Boolean proposition can be stated.

For the logical description of computing machines it is certainly desirable to have a more compact symbolism than the complete circuit diagrams. Figure 2.2 shows the circuit of the tube package in a logical symbolism devised when SEAC was designed and also in a briefer symbol appropriate when these packages are used. With the addition of numbers for package location and pin designation, the latter symbol can be the basis of a single-drawing description which can replace logical diagrams, circuit diagrams, and layout charts. Lines carrying negative pulses are marked by a small circle at each end.

Pulses are standardized in shape and timing, and the entire computer is kept in synchronism by making a clock pulse one input to every and-gate. The clock pulses are actually distributed as 1-Mc sine waves at 30- to 45-v peak-to-peak amplitude; however, the effective waveform is just the trapezoidal center slice which lies between the -5- and +2-v grid clipping levels. The delay through a tube and transformer is much less than 1 μsec; in fact, the best timing tolerances are obtained when the clock pulses in successive stages are separated by about 0.25 μsec; therefore, four phases

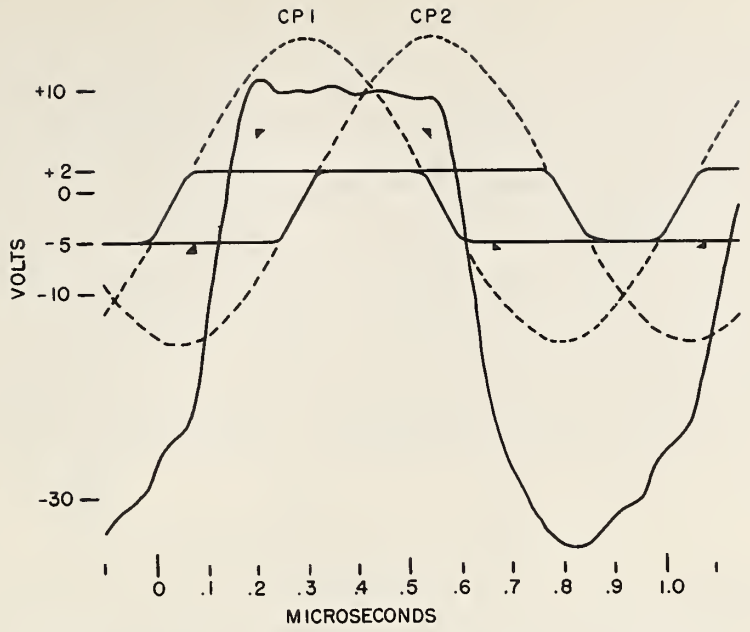

FIGURE 2.3. *Waveform of a typical pulse with the clock pulse from which it was derived and the clock pulse with which it will be reclocked.* Black triangles mark the critical timing limits.

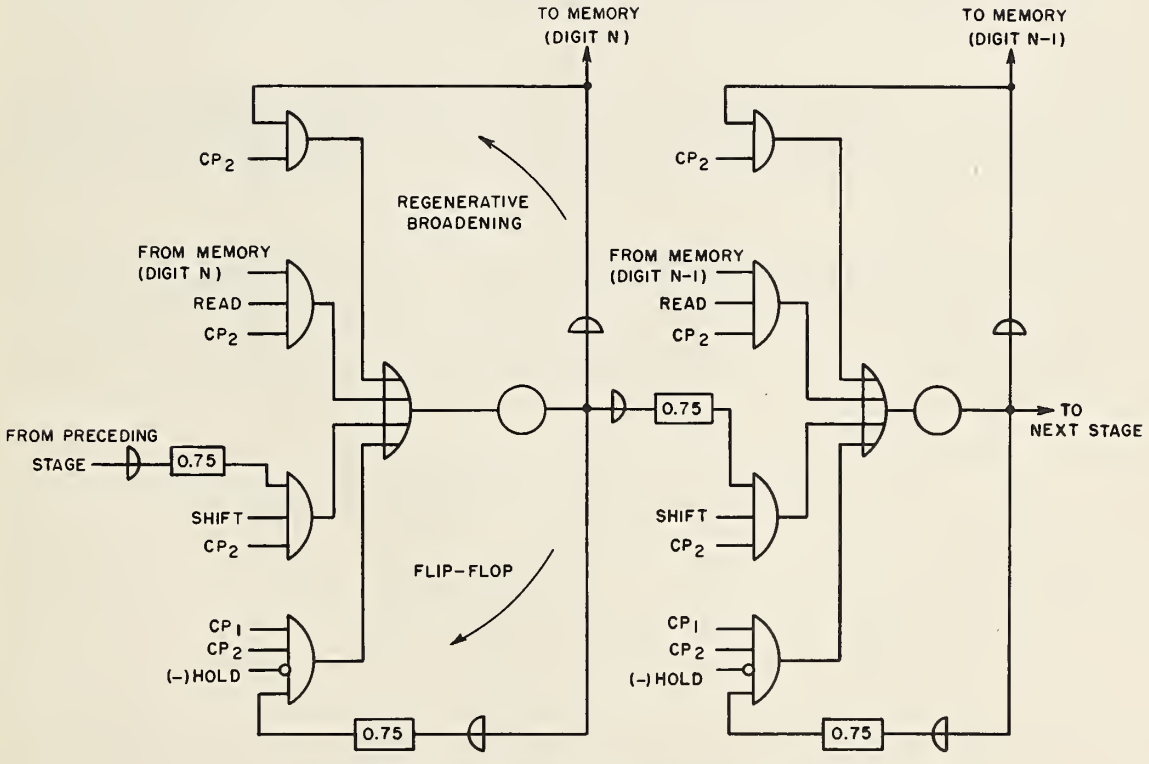

FIGURE 2.4. *Two stages of a typical shifting register.*

of 1-Mc sine waves are used for clock pulses. Figure 2.3 shows the waveform of a typical pulse at the secondary of a transformer. The signal on the grid of that stage was the −5- to +2-v slice of clock phase CP1, while in the next stage the pulse will be gated with clock phase CP2. Notice that the signal pulse does not cover CP2; it cannot because it is too narrow. However, the overlap of the signal pulse with CP2 is sufficient to turn on the next stage; then, once it has been turned on, its own output can be fed back to keep it on until the end of CP2. This trick, called "regenerative broadening," is illustrated in figure 2.4, which shows the logical diagram of two dynamic flip-flops connected together to form part of a shifting register. Either stage may be turned on in one of two ways. The first is by the coincidence of a pulse from the memory and a Read pulse, the second by the coincidence of a pulse from the preceding stage and a Shift pulse. When coincidence does occur the active gate does not rise until such time as the clock pulse CP2 also starts to rise. After the output has risen, the input pulses may fall because the regenerative signal will keep the tube on via the upper gate until the end of CP2. The output signal, delayed 0.75 μsec, arrives at the bottom gate with the next rise of CP2 and so permits the tube to be turned on again. The bottom gate can transmit a signal only during the overlap of CP1 and CP2 (see fig. 2.3). This is wide enough to initiate regeneration but narrow enough to be covered by a negative pulse (−) Hold which can inhibit the bottom gate and so stop circulation in the flip-flop. Other computer circuits are built up in a very similar fashion

3. THE DELAY LINE PACKAGE

An electric delay line is used to enable a transformer to drive a gate which is clocked by a later phase than the next; therefore, only integral multiples of 0.25-μsec delay are required. The problem of reflections from the nonlinear gate loads could be avoided if the characteristic impedance were made so low that the terminating resistance would swamp the nonlinear load of the gate, but this would require a wastefully large driving current. Instead the characteristic impedance is made equal to the pulse voltage divided by the current drawn at the top of a pulse; thus, the line is matched for the main body of a pulse so that only narrow reflections occur during the rise and fall. These are reduced to negligible size by dispersion in transmission and by partial absorption in an input termination.

The type of delay line used was described by Blewett and Rubel [8]. It is built up from the inside out of (1) a core of plastic tubing, (2) a close-wound helix of very fine wire, (3) a sprayed layer of aluminum paint, (4) two layers of Teflon tape, (5) a grounded braid of insulated wires, and (6) a protective cotton serving. Its characteristic impedance is 1,350 ohms, and a 0.25-μsec section is about 5 in. long.

A delay-line package contains one 0.75-μsec section and twelve 0.25 μsec sections along with terminating circuits for five positive pulse lines and for two negative pulse lines. Sections may be connected in series at the socket to obtain other lengths. Figure 2.5 shows the termination circuits connected between a transformer and the line at the input end and between the line and a gate at the output. Spare diodes from a tube package may be connected as shown by dotted lines to form an or-gate between several inputs to a line.

Volt-ampere diagrams in figure 2.6 show how the load-end terminations match the characteristic impedance of the delay line for incident pulses of 16-v amplitude. The terminal voltage and current is a superposition of an incident wave and a reflected wave that must exactly satisfy the terminal resistance conditions. For the incident wave the ratio of voltage to current is just the characteristic impedance, while for the reflected wave it is the negative of this because either the voltage or the current must be reversed by reflection. Dotted lines show the terminal resistance conditions; E_1I_1 denote the incident wave, and E_2I_2 the reflected wave.

For a positive pulse line (fig. 2.6A) the 6.2K resistor returned to −65 v exactly terminates a 16-v incident pulse when the pulse renders the and-gate diode nonconducting. The more obvious termination of a 1.35K resistor to −8 v cannot be used because it would not hold the and-gate down firmly to −8 v whenever there is no pulse on the line.

If an incident pulse arrived when all the other inputs of the and-gate were so positive that the 10K resistor remained connected to the line at the top of the pulse, then a reflected wave E_2I_2 would be produced; however, positive pulses (other than clock pulses) do not rise above +10 v, so

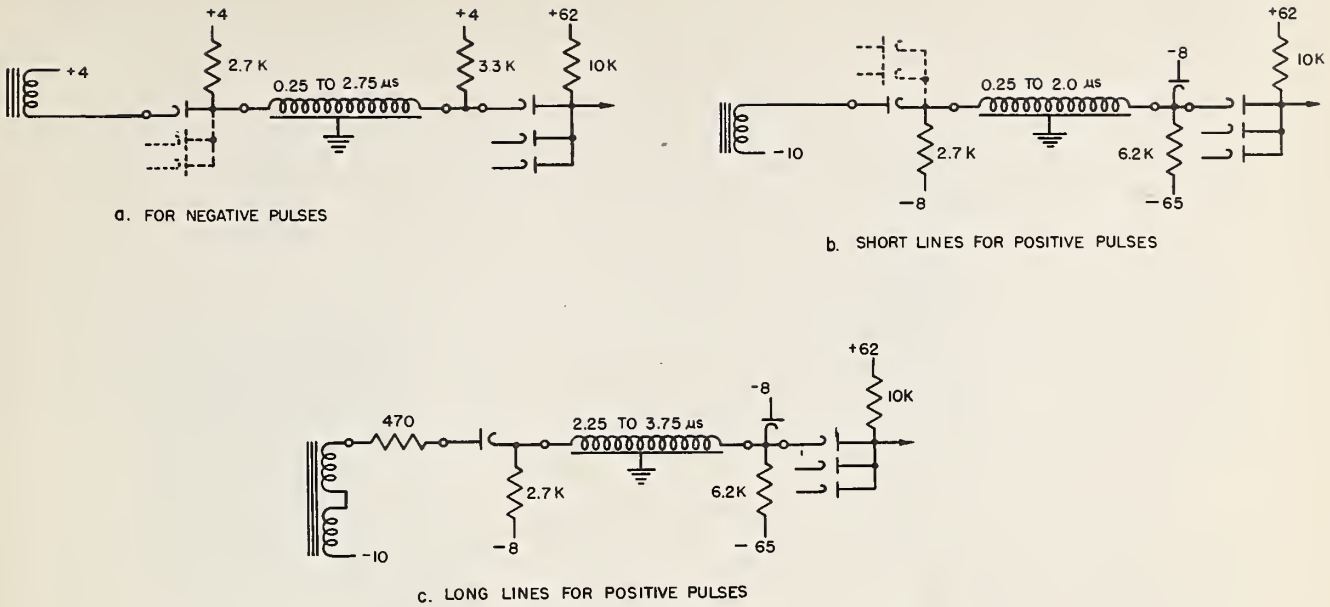

FIGURE 2.5. *Termination circuits for electrical delay lines.*

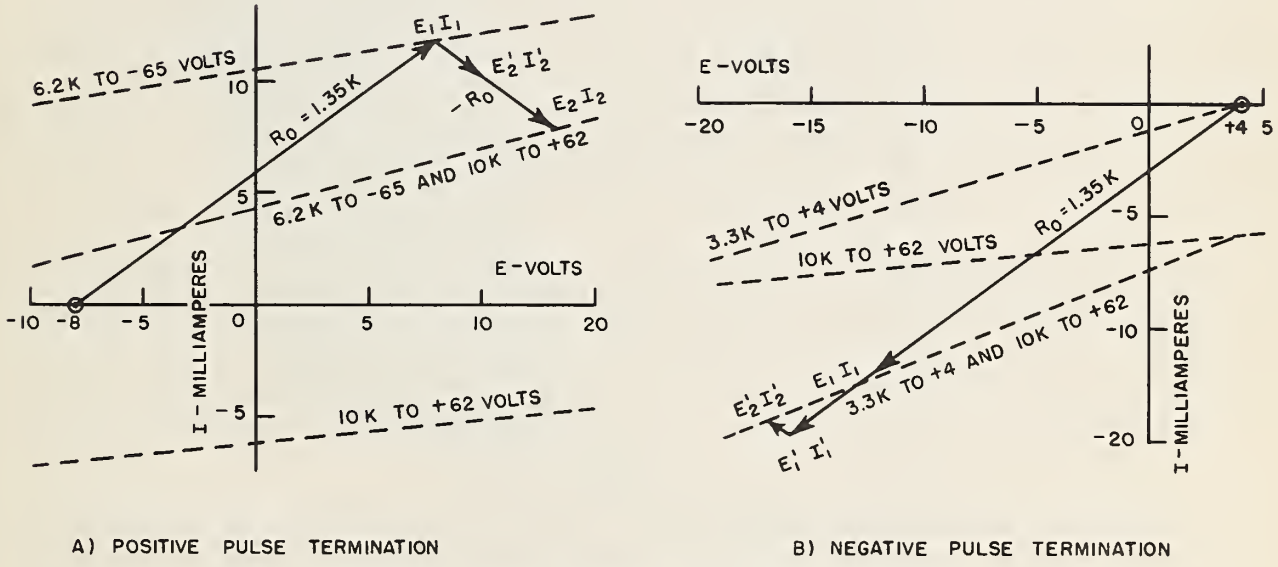

FIGURE 2.6. *Volt-ampere diagrams for delay-line terminations.*

only the smaller reflection $E_2'I_2'$ will be produced. This is comparable in magnitude to the small reflections caused by an incident pulse having more or less than 16-v amplitude because it has suffered more or less attenuation in a longer or shorter delay line than average, or else are caused by variations within the voltage and resistance tolerances.

For a negative pulse line (fig. 2.6B) a 16- to 17-v incident pulse is correctly terminated by the 3.3K and 10K resistors acting together. A 20-v pulse $E_1'I_1'$ will suffer a small reflection $E_2'I_2'$. A somewhat larger reflection is produced if negative pulses from two delay lines arrive simultaneously at the same and-gate and thus have to share the 10K resistor.

The 2.7K resistors in the input terminations absorb enough energy from the small returning reflections to prevent their accumulating seriously in the line, but they do not require as much initial pulse current as would terminations equal to the characteristic impedance of the line. The input diodes disconnect the line from the back-swing transient of the transformer. In long lines the attenuation due to the series resistance of the line (about 1 db/μsec) becomes so great that extra input voltage is required. Connecting both secondaries of the transformer in series gives more than enough voltage, so a 470-ohm series resistor is added to reduce the effective load and to drop the excess voltage, which would produce undesirable reflections.

An output termination intended for a positive line, i.e., a −8-v limiting diode and a 6.2K resistor to −65 v, can be used alternatively as an or-gate between the direct output terminals of several packages and the input of an and-gate, by connecting spare diodes as series input diodes for the or-gate. Two terminations in the delay line package are provided with diodes already attached for this purpose.

4. DESIGN OF THE PULSE AMPLIFIER

The type 6AN5 tube was selected as possessing the best combination of high transconductance, low capacitances, reasonably high current and dissipation ratings, and an efficient heater-cathode structure. Its pertinent characteristics are:

Heater voltage	6.3 v.
Heater current	0.45 amp.
Input capacitance	9.0 $\mu\mu$f.
Output capacitance	5.0 $\mu\mu$f.
Maximum screen dissipation	1.4 w.
Maximum average cathode current	50.0 ma.
Minimum increment of plate current between $E_{c1} = -5$ v and $E_{c1} = +2$ v at $E_p = E_{c2} = 62$ v.	42.0 ma.

The plate dissipation rating is 4.2 w, with 120 v on plate and screen, and 1.7 w with 300 v on plate and screen. In this pulse amplifier the plate dissipation tends to be low because the instantaneous plate voltage is quite low during a pulse. Plate dissipation exceeds 2.0 w in only those tubes which have an unusually large plate current at 5.0-v bias. In service very few heater failures have occurred and no evidence of cathode interface resistance has developed. Some tubes whose heaters were operated at 6.5-v lost emission at about 3,000 hours, but most tubes operated at 6.3 v or below have survived well over 10,000 hours.

Figure 2.7 shows (1) plate-characteristic curves of 6AN5's at grid voltages of −5 and +2, (2) the spread in plate current between high-limit and low-limit tubes, and (3) the load line presented by the output buffer. The reasons for the remarkably low position of the load line and many other design considerations are best explained while following the operation point on the e_p, i_p diagram through a complete pulse cycle.

Before the first pulse the plate is at the supply voltage so the operating point is at *A*. If the grid is turned on suddenly, the plate current quickly rises to *B* and must both supply the load and charge all the parasitic capacitances to bring the plate voltage down to *C* and finally to *D*. Now, a high ratio of primary to secondary turns on the transformer will give a high ratio of secondary to primary current, but it will also require a high primary voltage to give the required secondary voltage; therefore, more of the plate current will go into the plate capacitance rather than

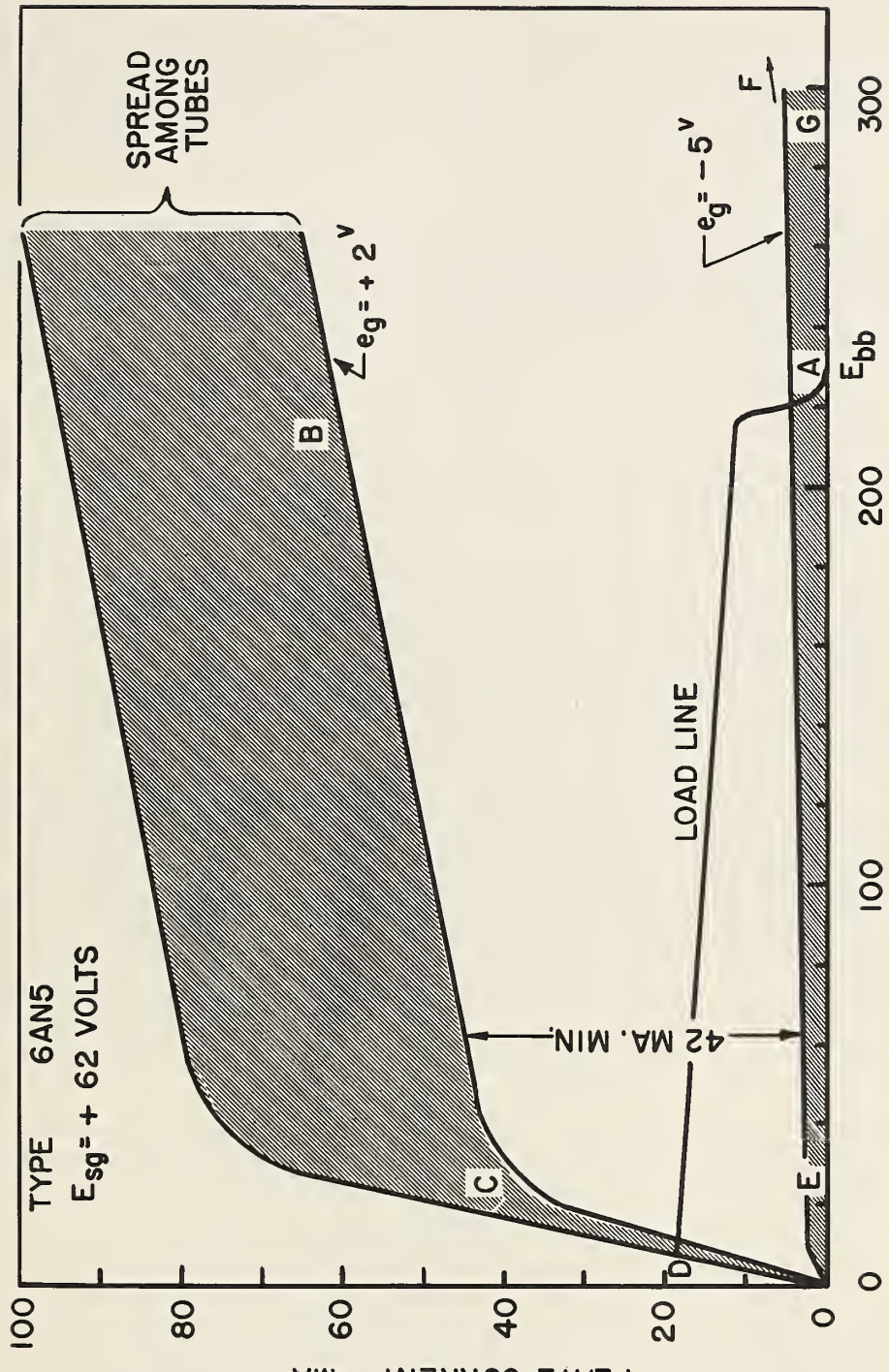

FIGURE 2.7. *Plate characteristics curves with load line.*

into the primary of the transformer. So there is a problem of finding the turns ratio, N, which will give the most secondary current, I_s, for given plate current, I_p, plate capacitance, C_p, required secondary pulse amplitude, E, and allowed rise time, T. If the currents are taken as the average values during the rise, one may write

$$I_s = N(I_p - NEC_p/T).$$

By equating to zero the derivative of I_s with respect to N, one can find the optimum turns ratio

$$N_{opt} = \frac{I_p T}{2EC_p}.$$

This result is easy to remember because it shows that just half the plate current should be used to charge the plate capacitance. The corresponding secondary current is

$$I_s = \frac{I_p^2 T}{4EC_p}$$

Because the secondary current increases with the square of the plate current, it pays large dividends to drive the grid as positive as the dissipation ratings will allow. In this design the plate capacitance, including socket, wiring, and equivalent primary capacitance of the transformer, is 10 $\mu\mu$f; the required secondary pulse amplitude is 20 v; and the allowed rise time is roughly 0.1 μsec. For a plate current of 40 ma obtained from a low-limit tube with positive-grid drive, the optimum turns ratio is 10 and the secondary current 200 ma. This calculation is admittedly only approximate, since it uses average currents during the rise, and the allowed rise time is determined very differently in practice; nevertheless, experiments confirmed the choice of a 10:1- turns ratio. In addition to the delay of charging the plate capacitance, the output pulse is further delayed about 0.02 μsec by the leakage inductance and the load capacitance.

When the plate voltage reaches knee C, the plate current quickly drops to the intersection with the load line at D. At this point a load of at least one 1.25K resistor in the output or-gate is required to prevent excessive screen dissipation. The steep slope of the plate characteristic in this region provides a very uniform pulse height between high limit and low limit tubes and between first and Nth pulses in a train. The high-frequency ringing seen on top of the pulse in figure 2.3 comes from resonance between the leakage inductance and the load capacitance. Inductance in the -10-v supply lead adds directly to the leakage inductance; therefore, close bypassing is desirable.

As the pulse continues, the transformer requires a magnetizing current that increases as the voltage-time area of the pulse, so the operating point gradually drifts up toward C. To prevent its passing around the knee of a low-limit tube before the end of the pulse requires at least 3 mh open-circuit primary inductance.

At the end of the pulse, when the grid turns off, the plate current drops from C to E, and the magnetizing current and load current combine to discharge the parasitic capacitances rapidly to A. Beyond this point the output pulse swings negative as the operating point moves on toward F, because the magnetizing current continues to excite an oscillation of the open-circuit inductance of the transformer with the plate capacitance. The load capacitance is disconnected by the output or-gate. If this oscillation is not damped, a spurious positive pulse will appear in the next half-cycle. On the other hand, if it is overdamped, the magnetizing current will not be quenched before the next pulse time, and it will subtract from the charging current available at the leading edge. The best compromise is to make the transient slightly underdamped in an effort to bring the magnetizing current to zero at the leading edge of the next pulse. In this type of transient the current passes through zero appreciably before the voltage does, so at the start of the next pulse the operating point may be at G; however, the very large charging current available there charges the plate capacitance to B with very little delay.

Because the open-circuit inductances of the transformers employed vary with a standard deviation of about 6 percent, it is not possible always to make the magnetizing current exactly zero at the

start of the next pulse. If the magnetizing current increases by an amount I during each pulse and is attenuated by a factor k in each interval between, then the magnetizing current at the start of an Nth pulse approaches (as N approaches infinity)

$$((Ik+I)k+I)k+\ldots=\frac{Ik}{1-k}.$$

In the worst case, with the primary open-circuit inductance at its upper limit of 4.5 mh, solution of the R-L-C transient gives $k=0.24$. This leads to an estimate of 5.6 ma for the remaining magnetizing current. Experiments with a low-current tube confirm both the slower rise of an Nth pulse with a high-inductance transformer and the earlier fall at the trailing edge when the inductance is too small.

The foregoing theory is not accurate enough to define a final design; instead it provided a reasonable point of departure and helped to interpret the timing tests, which were the real criteria of the design. The central objects of the timing studies are four critical timing limits marked in figure 2.3 by black triangles. Two of these define an interval over which the pulse at the secondary of the transformer must be above +6 v, and the other two define an interval through which it must be below −6 v. The level of +6 v allows for drop in the series diodes of the output or-gate and for attenuation in delay lines. On one hand, these limits are the results of a paper study of the logic circuits in a computer. All the various possibilities for gating or inhibiting between direct pulses or pulses whose waveforms have been distorted by transmission through delay lines were studied to find just what timing limits would insure correct operation. This requires that the pulse to be gated or inhibited is always properly overlapped and yet that no adjacent pulses are improperly affected.

On the other hand, the timing limits are the result of scaling hundreds of photographs of output pulses obtained under the most unfavorable combinations of the following conditions: First versus Nth pulse, high-current versus low-current tube, maximum versus minimum resistive load, no load capacitance versus 300 $\mu\mu$f, 4.5- versus 3.0-mh primary open-circuit inductance, maximum pull-up current in the and-gates with minimum pull-down current in the or-gate versus the opposite, and 45- versus 30-v peak-to-peak clock pulse amplitude. These two definitions of the critical timing limits allow some give and take through adjustable parameters, so the final design was reached by successive approximations.

At the same time a set of loading restrictions was obtained, of which the most noteworthy follow. The maximum resistive load is the equivalent of 14 1/2 gates in addition to the regenerative broadening connection, which is always present. With this load there may be up to 300 $\mu\mu$f of wiring capacitance. With smaller loads there may be more capacitance until a maximum of 1,000 $\mu\mu$f is reached with nine gate loads or less. A negative input to an and-gate counts as only 0.75 of a gate load, a short delay line as 1.75 gate loads, and a long delay line, which requires double amplitude drive, as six gate loads.

5. THE TRANSFORMER

The transformer is completely enclosed by its two-piece cup core in the form of a short cylinder 9/16 in. in diameter by 5/16 in. high. The core is a magnetic ceramic, specifically, sintered manganese-zinc ferrite with approximately the following properties:

Initial permeability	1,000
Saturation induction	3,400 gauss
Curie temperature	130° C
Resistivity	100 ohm-cm.

Its very low core loss and high effective permeability at 1 Mc, as compared with silicon-iron laminations, are primarily due to its resistivity being over 2 million times higher. While the separate losses are quite difficult to measure or to estimate accurately, one can compute that the total loss in the transformer is probably less than 0.1 w because the temperature rise under steady pulsing measures less than 15° C.

Instead of being wound in layers the three windings are arranged side-by-side in deep narrow slots turned in a circular nylon bobbin. The slots for the 6-turn secondaries are just wide enough

for one wire, hence the turns pile up radially. The slot for the 60-turn primary is 5 to 6 turns wide, thus the primary automatically piles up in an approximately bank-wound arrangement, which gives low distributed capacitance. The primary is placed at one side rather than between the secondaries, so that the inside ends of the primary and secondaries can be kept away from each other. Because the positive pulse output has the more critical timing, it is taken from the nearer secondary, which has the smaller leakage inductance. The windings must be carefully insulated from the core because ferrite is very abrasive and is a good enough conductor to provide a breakdown path between primary and secondary.

The core is assembled with no spacer in the butt joint between the ground surfaces of the halves. When one observes that the total reluctance of the magnetic circuit is equivalent to that of an air gap only 0.0006 in. long in the center leg, one can appreciate the importance of cleanliness and of accurate contact of the ground surfaces. Completed transformers, though apparently held together securely by a screw, fiber washers, and lock washers, showed serious inductance changes with rough handling until the practice of dipping in a hard-setting epoxy resin was adopted.

For acceptance, the open-circuit primary inductance is measured at 250 kc with a Q-meter. Acceptance limits are 3.4 to 4.2 mh, although the timing tests were run at 3.0 and 4.5. The small size and high effective permeability make the stray parameters of the transformer quite small. The capacitance between the primary and the nearer secondary is 3.1 $\mu\mu$f, of which only about one-third is effectively across the primary if the assumption that the pulse voltage varies linearly along the windings is valid. The following table shows various short-circuit inductances measured on a transformer whose primary open-circuit inductance was 3.34 mh. Subscripts 1 and 2 denote terminals of the primary; 3 and 4, terminals of the nearer secondary; and 5 and 6, those of the farther secondary:

L_{12}(34 shorted) = 45 μh.

L_{12}(56 shorted) = 80 μh.

L_{34}(12 shorted) = 0.65 μh.

L_{56}(12 shorted) = 0.97 μh.

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3. DYSEAC

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1. INTRODUCTION

The current trend toward the automatization of industrial and commercial operations is opening new areas of interest in which the techniques developed for digital equipment could be exploited. In particular, the unusual flexibility and speed inherent in these techniques could be utilized for automatizing a number of complex industrial control and supervisory tasks. Unfortunately, exploration of these new areas cannot be undertaken efficiently with existing digital computers because of the strong bias in the design of currently operating equipment toward scientific and engineering tasks. If, however, the internal flexibility of machines of this general type were matched by equally flexible means for keeping them in continual communication with devices external to them, digital computers could be used to advantage both in control systems for industry and in information-processing systems for handling the mass paper work of business.

As an example, before digital computers can be successfully incorporated into the often-predicted "automatic factory" and "automatic office" of the future, such equipment must possess ready means for sending intelligence to and receiving intelligence from a variety of external devices performing many diverse functions. Some of these devices will have to store, tabulate, file, convert, display, and sense information; still other devices will have to actuate mechanisms such as servo equipment in response to signals sent out by the computer as a result of information being processed within it. The computer will have to direct all these devices and coordinate their activities into an ensemble operation. Indeed, to achieve the full effect of an ensemble operation, the system needs to have the characteristics of a generalized feedback loop. That is, the computer must not only exert control over these external devices, but they in turn must be capable of calling for alteration in the course of action of the computer. Such requests enter the computer as special signals or information transfers from the external devices.

This feedback arrangement can be used to introduce human monitoring and selective intervention into the normal operation of the system. In its simplest form, pertinent information is displayed to the human monitor who can elect to respond by actuating other external devices that supply the computer with either new data or instructions. This feature will doubtlessly be a highly significant factor in the efficient exploration of the new areas for which digital techniques appear so promising.

The DYSEAC system was planned with just such requirements in mind and is capable of exploring many of these new areas. The planning of the installation has benefited from the component development and system refinement that has flowed out of three years of steady operation and expansion of the SEAC. This experience is embodied in special design features aimed at providing improved reliability, serviceability, and versatility in the installation. Those special features which relate to the system design of the DYSEAC are described in sections 2, 3, and 4 of this article, and those which relate to the physical installation are described in section 5.

The central core of the DYSEAC is a complete general-purpose high-speed digital computer utilizing the same basic electronic circuit elements as those in SEAC. In the DYSEAC, however, these basic building blocks have been organized into a far more powerful system for controlling and responding to auxiliary external devices. As the supervisory and control tasks for which this machine was planned did not require marked increase in computing speeds, the arithmetic powers of the DYSEAC have been only moderately expanded over those in SEAC by reorganizing the computation-control facilities to carry out new and improved arithmetic operations. Major design emphasis was placed, instead, on versatility of control facilities and on latitude for expansion of the installation.

It was deemed important to provide for future expansion of the high-speed internal storage capacity, in case this becomes important for a particular application. Accordingly, the system has been provided with convenient means for supplementing the initial memory capacity of 512 words with additional storage units up to a total capacity of 4,096 words. A more significant provision for expansion, however, concerns the annexation of a wide variety of specialized external devices.

The kind and extent of the external devices to be added will necessarily depend on the particular application which is being explored. Nearly all tasks need some printing and external storage facilities; hence, the initial installation will have a directly connected electromechanical typewriter and one or more magnetic wire cartridges for speedy loading and unloading of the machine. External storage in the form of magnetic tape equipment is also to be included initially in order to handle the more usual computing and data-processing tasks. More demanding tasks requiring somewhat faster access to a rather large volume of data will probably lead to the annexation of one or more magnetic drum units. Still more extensive problems concerned with means for handling masses of paper work will probably lead to the subsequent addition of experimental magnetic disk memory assemblies and experimental versions of the automatic magnetic file. For the exploration of real-time problems, including simulation and control aspects, it will be necessary to annex input and output converters to permit translation of information back and forth from digital to analog form. For example, digital-to-analog conversion is used when visual display of information stored inside the computer is provided externally by means of special cathode-ray tube devices. This listing of external devices includes only those for which serious attention and development are already in progress.

One further device that may be attached to DYSEAC for special experiments is SEAC itself. As the two machines employ the same digital language, this attachment can easily be made through their regular input-output terminals. By use of a coordinated pair of programs, the two machines can be made to work together in common harness on a number of interesting and potentially useful tasks. Indeed, this mode of operation can, by the application of available technology, be extended to a widely dispersed group of information-processing machines that are interconnected by means of a communication network. With suitable feedback facilities and correlated processing programs these machines could even engage in cooperative tasks for which the supervisory functions are transferred back and forth, as the need arises, among the several machines in the network. These new approaches to the problem of automatizing industrial and commercial operations are reasonable extrapolations of current trends and can be expected to lead to practical results if vigorously pursued.

2. SYSTEM FEATURES

The system specifications for DYSEAC are summarized briefly in table 1. Although some of these specifications are similar to those in SEAC or are expansions of SEAC counterparts, many

TABLE 1. DYSEAC system specifications

General operating characteristics:	
Basic repetition rate	One megacycle per second.
Data representation	Binary system; serial mode of representation.
Word length	Forty-four binary numerical digits plus one sign digit.
Instruction system	Three-address system in which a typical instruction word specifies the 12-digit address of first operand (α), second operand (β), and result of operation (γ). Successive instructions are generally located in consecutively numbered memory locations.
Memory	Mercury acoustic delay lines containing eight words each, with a maximum access time of 384 μsec. Minimum capacity: 512 words, stored in a 64-line cabinet; maximum capacity: 4,096 words, stored in eight such cabinets. Automatic parity-digit check of storage accuracy.

TABLE 1. DYSEAC system specifications—Con.

Performance rates of basic operations (including average access time to the memory):

Addition	0.9 msec.	
Subtraction	0.9 msec.	
Accumulate-and-overflow-check	0.7 msec.	
Accumulate-and-store	0.9 msec.	
Summation	0.8 msec.	(plus 0.05 msec. per word).
Multiplication, major (rounded)	3.0 msec.	
Multiplication, minor	3.0 msec.	
Division	3.0 msec.	
Shift	1.1 msec.	(for half-word-length shifts).
Justify	2.0 msec.	(for half word-length shifts).
Logical transfer	0.9 msec.	
Comparison, algebraic	0.7 msec.	
Comparison, absolute	0.7 msec.	
File, unconditional	0.4 msec.	
Breakpoint-file	0.4 msec.	
Input-output	0.3 msec.	(internal program time only).

Special operating features:

Internal program-control features	Dual counter-registers for program sequencing. Base-address and relative-address option.
Joint internal-external control features.	Manual-monitor facilities. Breakpoint-file option. Input-output program-jump option.

are entirely new. Most significant of the new provisions are the Special Operating Features listed at the end of the table. These features are designed to facilitate communication between the DYSEAC and the outside world (i.e., between the machine and the persons operating it or the external devices subsidiary to it) and enable impromptu interchanges of information to occur between them at any time on a completely unscheduled basis. Furthermore, such interchanges can be instigated by either the machine or the outside world, or by both acting jointly.

There are three general properties which give the DYSEAC this versatility:

(1) External-transfer operations, which transfer information between the machine and the external devices, are performed concurrently with internal computing operations; moreover, these transfers can refer directly to any area of the internal memory without restriction as to location or size.

(2) The pace at which the work program is carried out within the machine can be automatically adjusted to the possibly irregular pace at which the external transfer operations are taking place. That is, whenever it is necessary for the internal and external programs to proceed precisely in step with each other, the machine can manage to keep the slower-moving external program abreast of the high-speed internal program by forcing the latter either to halt or to change its course temporarily. This self-regulation property enables optimum use to be made of the concurrent input-output ability of DYSEAC on jobs which require considerable transfer of information into and out of the machine, or which involve searching through voluminous magnetic files.

(3) The work program can be interrupted whenever necessary, and a wide variety of special orders can be interpolated into the program either by the operator of the machine or by the external devices. This interruption property enables the machine to cope with unscheduled job assignments which originate, with little or no advance notice, in external events occurring beyond the supervision of the machine and which must be executed as soon as possible for real-time applications such as air-traffic control.

It should be noted that these three properties, by their combined presence, create a fourth property of considerable power. That is, acting in concert, they enable the machine to be employed effectively as a control element in a generalized feedback loop.

These over-all properties are derived principally from three special operating features of the Program Control, the Input-Output Control, and the Manual-Monitor facilities in the DYSEAC, all

of which will be described briefly in the following sections. A more complete description is contained in the appendix to this paper.

The term "manual-monitor" has been coined to describe five types of operations which are either initiated manually by the machine operator, who for example presses a push-button, or else are initiated by the machine itself under conditions which are specified by means of external switch settings. The former is referred to as a manual operation, and the latter is called a monitor operation because the machine must monitor its internal program to determine precisely when the operation should be performed. The type of operation to be performed as well as the conditions under which it is to be performed are specified by means of external switch settings.

Manual-monitor operations can readily be specified and initiated by external devices as well as by human operators. Furthermore, since all of the external switch settings control only d-c voltages, the external devices can even be remote from the machine itself and they can from a distance (connected to it via ordinary electrical transmission lines) exercise supervisory control over the internal program of the machine.

The five types of manual-monitor operations that can be performed are (1) loading operations, which load new information into specified portions of the machine such as various memory locations and storage registers; (2) print-out operations, which print out the contents of these memory locations and storage registers; (3) insert-in-the-program operations, in which a new instruction is interpolated into the internal program between the items of the scheduled instruction sequence; (4) change-in-the-program operations, in which an entirely new sequence of instructions is substituted for the scheduled instruction sequence; and (5) halt-the-program orders, with warning signal. Various combinations of these five types of operations also can be performed. For example, the machine can be told to perform a compound operation such as the following one which involves both loading and insert-in-the-program operations: Load the entire memory, and take the next instruction from memory location X. (X represents an arbitrary address number previously entered into the machine via the operator's keyboard or from an input unit.)

Monitor operations are performed by the machine whenever the conditions specified by the external switch settings occur in the course of the program. These conditions can be chosen from among a wide variety of program occurrences, e.g., every time the program refers to a new instruction or makes a reference to the memory, any time the program refers to an instruction to which a special monitor symbol is attached, any time the program refers to a Comparison (branch) instruction which results in the selection of either one of the two alternative next instructions, any time the program refers to a location in the memory which matches some specified address number or which falls within certain specified limits, and any combination of these or other special conditions.

By pairing a particular type of manual-monitor operation with a selected set of conditions, a wide variety of special operations can easily be specified and performed. Among the simpler of these are the following examples. (1) Every word written into or read from the memory at each step of the program can be printed out. (2) The contents of a specified memory location can be printed out whenever and as soon as the memory location is referred to in the course of the program, with the option of halting the program at that time if desired. Neither of these operations requires the preparation of any special routine. (3) Various fixed memory addresses or groups of fixed addresses may be continually printed out even while computation is proceeding.

For every manual-monitor operation, the external switches are set to specify not only the type of operation to be performed and the conditions under which it is to be performed, but also the storage places which are to be involved. These storage places can be chosen from a long list of available locations in the high-speed internal memory and from among five different storage registers in the machine. The memory locations may be designated in a variety of ways: either in the usual way, as an address number, or indirectly as an address specified by the current instruction, or as the address scheduled for next reference in the course of the program. These indirect ways are an advantage to the user of the machine who can, for example, direct the machine to print out the result of each operation without knowing (or being required to specify) the address in which each result is to be found.

Thus, by means of the external switches, certain storage areas within the machine may be utilized by devices remote from it. These remotely located devices can direct that information in certain areas of the memory of the machine be transmitted to them. Similarly, they can arrange to insert new information into various portions of the memory. In this way, at the option of either the external devices or the machine program, or both acting jointly, the DYSEAC can share with these remote devices its high-speed memory and consequently every other part of its internal computing and external storage facilities.

This feature makes it possible for two or more full-scale computers (such as SEAC and DYSEAC) to be harnessed together and work in mutual cooperation on a common task. Each member of such an interconnected group of separate computers is free at any time to initiate and dispatch special control orders to any of its partners in the system. As a consequence, the supervisory control over the common task may initially be loosely distributed throughout the system and then temporarily concentrated in one computer, or even passed rapidly from one machine to the other as the need arises.

Further aspects of the control interrelationships available in DYSEAC will be discussed subsequently, after the other Special Operating Features in the machine have been described.

Two other special operating features of the DYSEAC are *Breakpoint-File*, which is a program-control operation, and *Program-Jump*, which is an input-output control operation, Before describing these operations, it will be necessary to outline the program-sequencing features of the machine.

The sequence of instructions which specifies the work program for the machine is normally a consecutive one; i.e., consecutively executed instructions are normally located in consecutively numbered address-locations in the memory. Means for interrupting this consecutive sequencing of instructions and for initiating a new sequence are provided by a variety of choice instructions and counter-setting instructions. (See Comparison and File operations, respectively, in table 2, which describes all of the instructions available in DYSEAC.) The user of the machine, viz., the programmer, has the facility not only of initiating new instruction sequences at any time but also of choosing between two possible alternative sequences. He may, if he wishes, interleave two distinct sequences, periodically jumping from one to the other in an arbitrary manner. This facility is made possible by a scheme which provides two separate counter-registers for program sequencing, each of which holds an address-number. The address-number in either counter-register may be chosen as the address of the next instruction to be performed [1].[1]

The address-numbers in these two counter-registers can also be used for another distinctly different purpose, namely, as *base-points*. That is, at the option of the programmer, the address-number in either counter may be used as a base-point, or origin, for those address-numbers in subsequent instructions which the programmer has designated as *relative* addresses. In other words, if address-number X is designated as a relative address in an instruction, the memory location referred to is no longer X but a new location displaced from X by the number stored in the chosen counter. For example, if the chosen counter contains the number C, then whenever address X is designated as a relative address in an instruction, the memory location referred to is (X + C).

In utilizing this counter-register and relative-address facility, the programmer may elect to follow either of two methods. The first method makes use of a *fixed* base-point, which the programmer modifies only occasionally as the program proceeds. The second method makes use of a *floating* base-point, which is the address of the instruction-word itself and therefore progresses constantly. With this second method, the memory locations of the operands referred to in the program may be specified relative to the location of the instruction word even when that location is not known at the time the program is being planned.

The Breakpoint-File operation can now be described. As indicated in table 2, the control counter-registers can be reset by means of the two types of file operations: File (unconditional) or Breakpoint-File. These two operations allow the programmer to set either control-counter to any arbitrary value, specified either in an absolute manner or relative to its current setting. Since the contents of these counter-registers specify the memory location of the next instruction to be performed, the File operations may readily be used to initiate entirely new branches in the program.

[1] Figures in brackets indicate the literature references on page 57.

TABLE 2. Description of DYSEAC basic operations

Name of operation	Description of instruction
Addition	Form the sum of the word in α and the word in β, and write the result in address γ in the memory.
Subtraction	Form the difference α minus β, and write the result in address γ in the memory.
Accumulate-and-Overflow-Check.	Form the sum of the word in α and the word in β plus the contents of the arithmetic accumulator register. If the sum does not overflow, store the result in the accumulator and proceed to the normal next instruction; if the indicated sum does produce an overflow, however, leave the previous contents of the accumulator unchanged and take the next instruction from address γ in the memory.
Accumulate-and-Store	Form the difference α minus β, add the contents of the arithmetic accumulator register to it, and write the sum in address γ in the memory. Then clear the accumulator.
Summation	Form the sum of the words located in consecutive address locations running from β through α, inclusive, and write the sum in address γ in the memory.
Multiplication, major, rounded.	Form the product of the word in α and the word in β, and write the major part (rounded off) in address γ in the memory and in the arithmetic accumulator register.
Multiplication, minor	Form the product of the word in α and the word in β, and write the minor part in address γ in the memory. Also write the major product, unrounded (with proper sign), into the arithmetic accumulator register.
Division	Form the quotient of the word in β divided by word in α, and write it in address γ in the memory. Also write the remainder into the arithmetic accumulator register with the sign of the dividend.
Shift	Shift the word in α according to the code indicated in the word located in address β in the memory, and write the result into address γ in the memory. The seven numerical digits on the extreme right of the word in memory location β indicate the number of binary places the word is to be shifted and the direction of the shift (left or right).
Justify	Determine the number N satisfying the following inequalities: $[\beta] \leqq [\alpha] 2^N < 2[\beta]$. Write this number with proper sign into the seven digit positions on the extreme right of the word in address γ without altering its other digits in any way. Note: $[\beta]$ means absolute value of the word in address β in the memory, and $[\alpha]$ means absolute value of the word in address α in the memory.
Logical transfer	Write in address γ in the memory those digits of the word in α which correspond to one-digits in the word in β. Leave the word in γ unchanged in those digit positions which correspond to zero-digits in the word in β.
Comparison, algebraic	If the word in α is algebraically greater than or equal to the word in β, take the next instruction from the normal consecutive address position. If, however, the word in α is less than the word in β, take the next instruction from address γ in the memory.
Comparison, absolute	This instruction is similar to algebraic comparison, differing from it only in that the indicated inequalities pertain to the absolute values of the numbers indicated.
File, unconditional	Write the contents of the control counter-register (and certain other control data) in address β in the memory; reset specified counter to γ address-number; adopt contents of specified counter as relative-address base-point in subsequent operations.
Breakpoint-File	This instruction is similar to unconditional file except that it requires the setting of an external Breakpoint-File switch to indicate that its activation is desired. If the switch is not so set, the instruction is passed over without effect.
Input-Output	Load (or print-out) the designated area in the high-speed internal memory from (or to) the designated area in the external storage or input-output unit. After initiating the operation, the program proceeds immediately to the next scheduled instruction. When the external operation is completed, execute program-jump if so indicated.

Furthermore, since these operations cause a complete record of the status of the program to be written into the memory just prior to starting a new branch in the program, the abandoned branch can be resumed without difficulty later on, if desired.

The Breakpoint-File operation has the same characteristics as the File (unconditional) operation except for one important additional feature. It requires the setting of an external switch to indicate that Breakpoint-File activation is desired. If this external switch is not so set, the Breakpoint-File instruction is passed over without any effect on the machine. Therefore, by locating Breakpoint-File instructions throughout the program at strategic points, the course of the program can be changed at these points merely by the turn of a switch. This feature provides a simple and powerful means whereby the course of the internal activities of the machine can be controlled by the external environment.

Before considering the third special operating feature of DYSEAC, namely the Input-Output Program-Jump operation, a typical input-output operation in which information is transferred between an external device and the high-speed memory of the machine will be described. It might be noted again that any consecutive areas of the memory in DYSEAC, ranging in size from a single word to the entire memory, can be loaded or printed out even while a program of computation is proceeding. Automatic interlocks are provided to guard against inadvertent attempts to use a memory location for conflicting purposes. For example, if a print-out order is given, the machine is automatically prevented from writing into any memory location affected by the print-out order until the word in that location has been printed out.

A typical input-output operation proceeds in the following manner. First the machine selects the particular external device or unit with which communication is desired. The code number signifying this unit is specified in the input-output instruction. In the second step of the process, the machine runs through a specified number of words or blocks of words on the selected unit, the starting point being the word lying nearest the reading heads for the magnetic wire or tape units, and a fixed origin on the periphery for the magnetic drums. For other types of applications, this step may be used to introduce a variable delay. In the third step of the process, which begins after the requisite number of words has been counted out, the transfer of words between the external unit and the internal high-speed memory takes place. The transfers commence with the numerically smallest address in the indicated block of words and proceed in consecutive order until the numerically highest address is reached, thereby concluding the operation.

Each input-output instruction not only specifies the particular external unit which is involved in the transfer of information and states whether the transfer is to be a Load or a Print-out operation, but also indicates where the information is to be found and to what destination it is to be transferred. Finally, the instruction indicates whether or not a Program-Jump operation is desired after completion of the input-output operation. If a program-jump is desired, then a signal is produced after the input-output operation is completed which causes the program to jump, i.e., the counter-register being used as the source of the next instruction is temporarily abandoned, and the instruction word in the address location specified by the other counter-register is executed in its stead.

This program-jumping feature is useful in many situations. For most applications which make use of concurrent loading or printing-out of the high-speed memory while computations are proceeding, the precise length of time required to complete the external operation is either indeterminate or else quite difficult to predict. A typical example of an instance of this type occurs when it is necessary to hunt for a particular word or group of words in an unknown location on a long magnetic tape reel, where a word can be identified as one of the desired type only after it has been read into the machine and subjected to an analysis of its characteristics. Since efficiency requires that information be read into the high-speed memory in fairly large blocks, it is desirable during the comparatively slow procedure of reading in the information to make use of the ability of the system to proceed concurrently on other independent phases of the program. By means of the input-output program-jumping feature, the programmer is able to direct that these other independent phases of the program be allowed to proceed uninterrupted until the specified loading of the information is completed and that as soon as the loading is completed, the program should jump to an alternative specified routine which is designed to analyze the newly received information and to decide whether or not to retain it or to continue hunting on the tape.

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An analogous need arises when it is desired to check the accuracy of information printed out on the external medium by reading the information back into the machine and comparing it with its original source. A process of this sort would require a Print instruction followed by a Load instruction. In order to avoid having the program stand by while the print-out operation is being completed, the programmer can arrange for other internal operations to be carried out concurrently which would be interrupted only when the print-out operation is concluded, at which time the Load instruction would be initiated.

More generally, the Program-Jump facility provides a means by which the machine can order an external unit to carry out an assigned task and at the same time periodically report back its progress in carrying out the task so that the machine can maintain the closest possible check on the external operation and redirect it properly as the need arises.

After effecting a program-jump, the new program that is initiated may, as soon as its final instruction is performed, cause the machine to resume the interrupted program where it left off, if the programmer so desires. An automatic interlock relieves the programmer of the burden of having to estimate precisely how long a time will be required for the original input-output operation to be completed and insures that all the steps in the program will be carried out in their proper sequences. The system is so designed that the order which appears first in the program must be satisfied before any subsequent conflicting order can be carried out.

In concluding the discussion of the special operating features of DYSEAC, it should be noted that the various interruption facilities which have been described are based on mutual cooperation between the machine and the external devices subsidiary to it, and do not reflect merely a simple master-slave relationship. With the Breakpoint-File feature for example, the external device which operates the Breakpoint-File switch initiates the request for the branching action, but the actual execution of the operation must await confirmation of the request by the machine, i.e., the occurrence of a Breakpoint-File instruction in its program. In the case of the Input-Output Program-Jump, on the other hand, the initiation of the request originates in the internal program (via an Input-Output instruction containing a jump-order symbol), while the actual execution does not take place until the external device returns the proper signal, signifying termination of the operation. The third variety of internal-external action, the manual-monitor type, exhibits aspects of both types of control relationship. For the simple manual operations, the external unit (or the operator) exercises full control over both the initiation and execution of the request, e.g., by push-button. For the monitor operations, however, the request can be considered as initiated externally (by turning breakpoint-choice switches) but the actual execution of the operation does not occur until the requested conditions arise in the course of the internal program.

These varied internal-external joint-control relationships are summarized in table 3. For each of the special operating features (Breakpoint-File, Program-Jump, and Manual-Monitor operations), table 3 indicates whether an internal or external source initiates the request for the operation and whether an internal or external source decides to execute the operation. This same information is

TABLE 3. Internal-external joint-control properties of DYSEAC special features

	Source which describes operation	Source which initiates operation	Source which decides to execute operation
Special operation:			
Breakpoint-File operation	Internal	External	Internal.
Input-Output Program-Jump feature	--do	Internal	External.
Manual operation	External	External	do.
Monitor operation	--do	--do	Internal.
Conventional operation:			
New instruction brought in from input unit by program.	External	Internal	Internal.

also given for the more conventional method of control, which consists of calling new instruction words into the memory of the machine by means of a programmed input instruction. It is evident that the control interrelationships provided by the special features of DYSEAC are distinctly different for each special operation and that equivalent control versatility cannot be achieved by the more conventional program method. Indeed, the foregoing special features were incorporated into DYSEAC only because the joint-control properties needed for its intended applications could not be secured satisfactorily otherwise, even by the use of special or complex internal programming procedures.

3. OVER-ALL FUNCTIONAL ORGANIZATION

The over-all functional organization of the DYSEAC is indicated in the block diagram of figure 3.1, which shows the major communication routes and control relationships in the system.

The High-Speed Memory shown in the center receives and distributes to the other units the information (numerical and instruction) to which the most rapid access is needed for carrying out the work-program of the machine. The memory communicates principally with five major units of the system. Of these, two are concerned primarily with internal processing affairs and three with external relations. A continuous flow of digital information may be maintained simultaneously between the memory and the inward-looking and outward-looking types of units. The latter types, which serve to communicate with the external devices represented on the left side of the block diagram, include the Input-Output Buffer, the External Selector, the Concurrent Input-Output Control, the Display Staticizer, and the Serializer.

The function of the Input-Output Buffer is to transmit information at the proper repetition rates from the external unit to the internal memory during an input operation, and in the reverse direction during an output operation. The buffer receives words from the memory at the normal 1-Mc internal repetition rate and then transmits them out digit-wise at the proper measured rate appropriate to the external unit. The external unit itself (via the External Selector) specifies the word format and repetition rate appropriate to it. Provision is made in the Input-Output Buffer for handling information in various forms, e.g., in a single-channel serial form for magnetic wire units, in serial-parallel 4-channel or 6-channel form for magnetic tape units or Flexowriter, and in fully parallel 45-channel form for magnetic drum. A wide variety of other formats is also available if needed. The initial range of repetition rate may be up to 16 kc (single channel). If higher rates are desired in the future, an additional buffer storage register may be added to the system.

The External Selector is a high-speed electronic switching device which selects the external unit with which an input-output operation is to be performed. It provides the signal required to operate the proper multichannel electromechanical relay or other device which completes the circuit connections for the lines carrying both the digital information and the control signals needed to operate the external unit. The design of the External Selector has been chosen so as to be readily expandible whenever additional external units become available. The initial model contains provision for selecting among up to 48 distinct external mechanical relay switches, but it can be expanded, with about an equal amount of additional equipment, to be capable of handling up to 256 distinct information channels, such as individual parallel magnetic-drum channels or high-capacity magnetic filing systems.

The External Selector accomplishes its switching function by a process of scanning successive switching channels in synchronism with a counter located in the Input-Output Control Unit, starting from a fixed origin. As a result, a gradation of electronic switching access times is available, ranging from a minimum of about 25 μsec for the channel closest to the origin to a maximum of about 6 msec for the last channel of an expanded 256-channel model. This wide range of switching speed can be matched to the operating rates of the external devices themselves, e.g., the first 20 channels, whose average access time is 0.25 msec, might be chosen to communicate with high-speed external units capable of reacting in 1 to 2 msec, while the last 200 channels, whose average access time is about 4 msec, switch with speeds compatible with the average rotational access time of a 3,600-rpm magnetic drum. A feedback checking feature is provided in the External Selector for insuring that one and only one channel is selected and that it is the channel requested by the Input-Output Control Unit.

The Concurrent Input-Output Control has the function of regulating the detailed progress of all input-output operations requested in the course of the internal program. It directs the flow of traffic between the memory and the Input-Output Buffer, and between the Input-Output Buffer and the External Selector. It instructs the External Selector to step along to the proper switch channel, checks that contact is made with the desired unit, and signals the Input-Output Buffer to proceed to accept digits either from the external unit during an input operation or from the high-speed memory during an output operation. It receives signals from the Input-Output Buffer as each complete word is transferred, and it not only keeps count of the total number of words handled, but also keeps track of which address in the high-speed memory contains the word currently to be transferred. This information is transmitted to the Memory Address Switches at the proper time.

In the comparatively unlikely event that both the Input-Output Buffer and some internal unit should simultaneously demand access to the high-speed memory, the Concurrent Input-Output Control resolves the conflict by according temporary priority to the external operation [2]. Likewise, it referees conflicts or inconsistencies between the internal program and the progress of external operations. It also notifies the Program Control unit at the termination of an input-output operation so that the program-jump may take place. Its other functions include regulation of the memory error-seeking scan process and the Summation operation.

The Display Staticizer and the Serializer are input and output organs adapted especially for real-time operations. The Display Staticizer is a register storing 28 bits statically in parallel for controlling, for example, a digital-to-analog converter that provides deflection voltages for CRT visual displays. The register is loaded periodically, cycling through a chosen group of words in the high-speed memory. The size of this group, one to 32 words, and its location in the memory are adjustable manually. The cycling process proceeds through the specified area independent of the internal program and in no way interferes with the use of the area by any other units, such as Arithmetic Unit or Input-Output Buffer.

The Serializer unit is provided for continuous real-time external input devices. This unit can accept one full word of 45 bits delivered in parallel in the form of asynchronous pulses from an external unit (minimum pulse duration about 50 μsec) and can transmit the word in synchronized normal serial form to any other units of the system capable of reading words out of the high-speed memory. The Serializer, however, can provide words to the other units at about 4 1/2 times the average access rate of the acoustic memory.

The Arithmetic Unit (lower right-hand corner of fig. 3.1) carries out a group of 13 arithmetic or choice operations. Arithmetic results are written directly into the high-speed memory, and control signals specifying the outcome of the discrimination operations are sent directly to the Program-Sequencing and Control Unit where they serve to modify the choice of memory location from which the next instruction is to be read. A third route of communication to the Input-Output Buffer, labelled "special word transfers," represents the facility of loading or printing out the contents of the arithmetic accumulator register directly via the Flexowriter or magnetic input-output units.

The remaining unit in direct communication with the high-speed memory is the Instruction Register. Instruction words are transferred one at a time, as needed, from the memory into the Instruction Register. From this unit, pieces of information contained in different segments of the instruction-word pattern are selected by the Program Control Unit and transmitted to various other internal units throughout the system. From the Program Control Unit, digital address codes pertaining to each phase of each operation are sent to the Memory Address Switches in order to make the specified memory locations available to the Arithmetic Unit and Instruction Register at the proper time. This information is made available to the Concurrent Input-Output Control at the same time for checking against possible conflict with current input-output operations. Furthermore, whenever an input-output instruction is received in the Instruction Register, the Program Control routes it immediately to the Input-Output Control Unit and proceeds to call a new instruction word out of the high-speed memory. Finally, during the File-type operations, various items of program-control information can be written out of the Program-Control Units directly into the memory. This same information can also be transferred into or out of the system via the external input-output units over the indicated special-word-transfer path to the Input-Output Buffer.

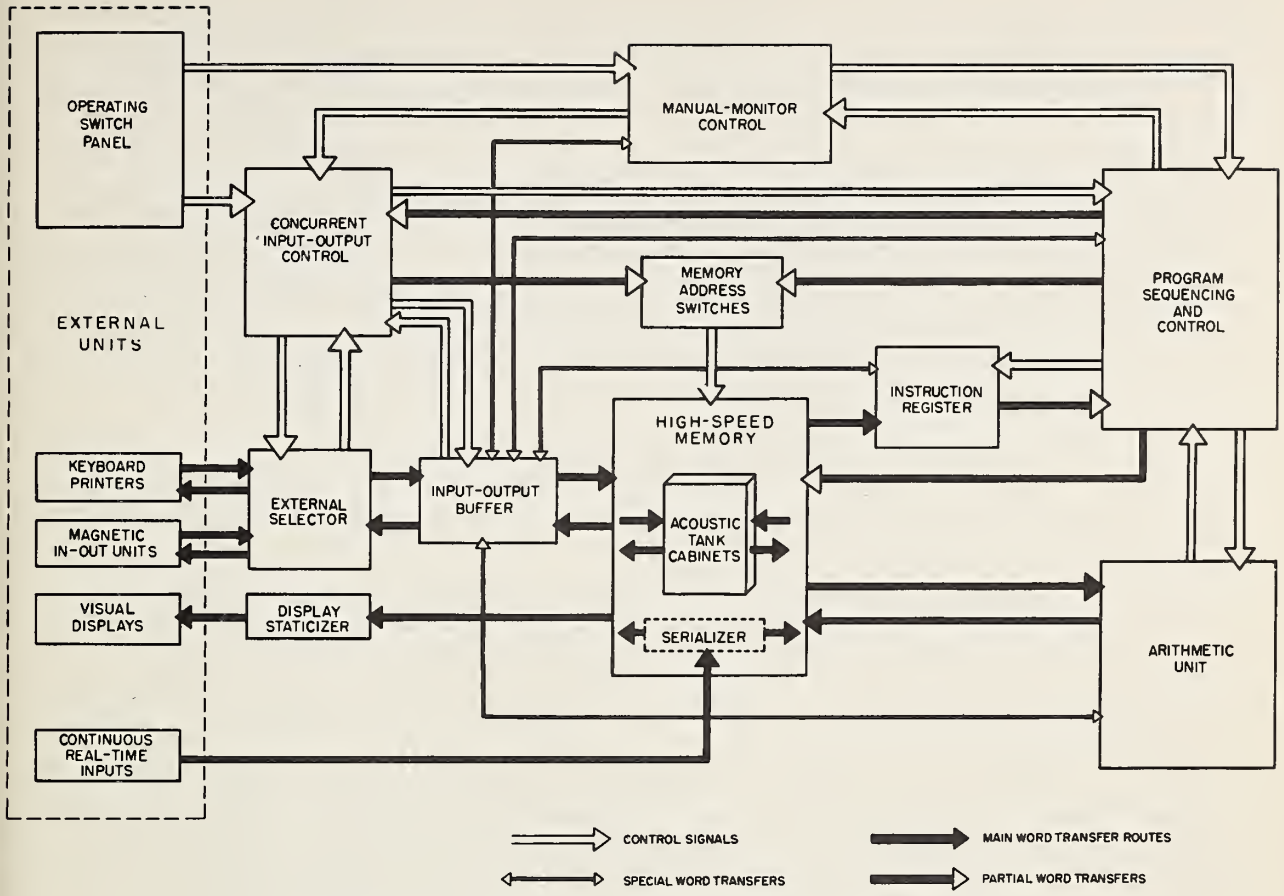

FIGURE 3.1. *Overall functional organization of the DYSEAC system.*

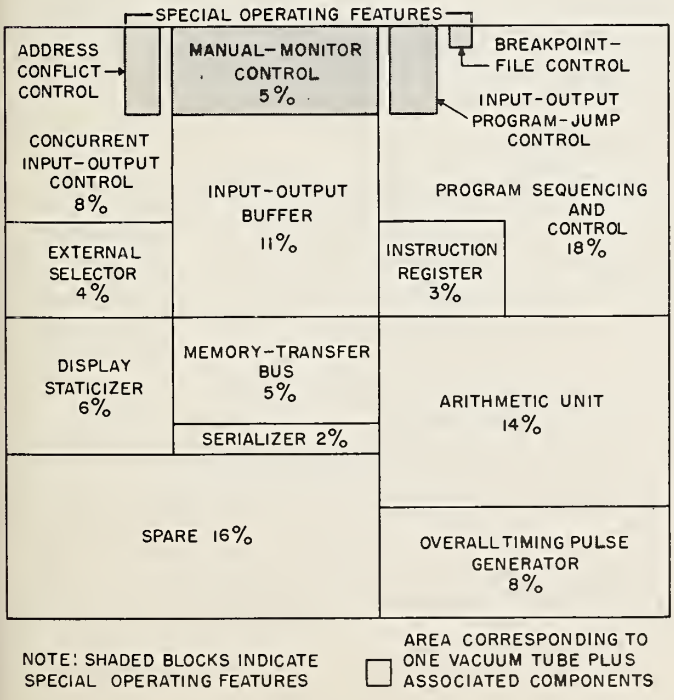

FIGURE 3.2. *Proportion of space required for DYSEAC special operating features.*

The last major unit to be noted is the Manual-Monitor Control. This unit is responsible for regulating and synchronizing the carrying out of joint internal-external operations. Its major functions are (1) to interpret the breakpoint conditions received from the external Operating Switch Panel, (2) to observe the progress of the internal program and recognize when the specified breakpoint conditions arise, and (3) to deliver signals temporarily halting the internal program, if necessary, setting up the required special-word-transfer routes, and initiating the specified interpolated internal or external operation.

The proportion of physical space required by the equipment for carrying out the joint internal-external control operations of DYSEAC is indicated graphically in figure 3.2. The areas marked off on this chart have been made directly proportional to the number of physical packages required for realizing the various functional units just described, exclusive of the memory. It can be seen that the equipment for performing Manual-Monitor operations, Breakpoint-File operations, and Input-Output address-conflict and program-jump operations (shaded areas on the chart) constitute only about 6 percent of this total. Also, about 16 percent of the total physical space available, labelled "spare" on the chart, has been left unused and can be utilized for annexation of other internal computing or control units if so desired.

4. OPERATING CAPABILITIES

As a result of its special features, the DYSEAC possesses three versatile operating properties which may be summarized as follows:

(1) The external devices harnessed to the machine can gain access at any time to all or to any part of the internal memory without disrupting the internal computing program. Moreover, practically continuous input-output access to certain special parts of the internal memory is available for the use of specialized external units needing faster-than-average access, e.g., units which provide continuous visual displays for the operator or which produce certain manual or automatic control signals for the computer.

(2) The DYSEAC can operate with a wide variety of input-output devices ranging from electromechanical typewriters through magnetic storage devices to analog-digital converters associated with different types of sensing devices and servomechanisms. Some of these devices deal with detailed digitalized data at magnetic recording rates. For these, the system contains facilities for accepting and transmitting data at a variety of repetition rates and word formats.

(3) Whenever necessary, the progress of the internal program can be regulated, scaled, and synchronized by events occurring beyond the supervision of the machine. Because of this ability of the machine to turn its attention to any of its wide family of subsidiary devices and to interrupt or redirect its over-all program in order to assist or manage them, DYSEAC can be used for investigating many diverse areas of potential application ranging from the simulation and control of links in a data-communication network to the high-speed processing of business data.

As an example of a potential application which requires such capabilities, consider an installation engaged in the automatic processing of business accounts and records. In an application of this sort the main task of the computer might be the routine processing of monthly accounts. The data to be processed would be withdrawn automatically by the machine from the external magnetically recorded files [3], would then be properly combined with newer data, and finally the up-to-date information would be returned to the files. Even while these operations are progressing automatically, however, the contents of the files would need to be available to the clerical staff of the office for inserting occasional corrections or revisions of data, or for answering scattered spot requests for information. Moreover, in some cases, the computing services of the machine would be needed for carrying out special minor processing tasks on the data being withdrawn from the files in this manner. At the same time, batteries of printers might be systematically going through the files and routinely printing out those portions for which the monthly processing was already complete. Similarly, the routine entry of new data, such as sales records, into the portions of the files not yet reached for processing might be going on.

Obviously, it would be highly desirable to be able to carry out any of these several operations at will, with as little disruption as possible either to each other or to the main task. Because of

the unforeseeability of some of the operations (such as the spot requests for information) or the uncertain or variable operating rates of some of the external devices (such as mechanical printers) although the *nature* of the functions may be prearranged and suitable instructions may be prepared and inserted into the machine in advance, the exact *time* for their actual initiation or the *sequence* of their execution can not in any way be precisely scheduled in advance. In order to operate efficiently, therefore, the machine should be able *on a completely intermittent and unscheduled basis* to share both its program-control and its internal storage facilities with its external subsidiary devices and human operators.

As a second example of a potential application which requires these capabilities, consider an installation engaged in the control of air traffic at an airport terminal. For this application, the human operator can be coupled to the machine system (1) through the medium of a visual display device which exhibits graphically the numerical data stored inside the internal memory and (2) by means of a battery of manual control switches capable of inserting new numerical data or certain new control commands into the machine. The numerical data displayed by the machine represent in real time a map of the predicted traffic patterns in the neighborhood of an airport, e.g., the predicted locations, based on latest scheduling information, of all aircraft inside a certain area. The human operator can, by means of the manual input-controls, enter newer data into the machine as the information becomes available, interrogate the machine for more detailed information concerning certain individual flights as the need arises, and instruct the machine to exhibit the effect to be expected from issuing revised flight-control orders. In the latter case, parts of the internal information of the machine must be presented to the operator in a rather complex pictorial form in order to be meaningful to him. Applications of this sort, like the previous one, require a constant interchange of intelligence between the computer and its operator, and between the computer and other devices.

A third type of potential application involves the utilization of automatic computers for the control of automatic machinery, a first step toward the so-called automatic factory. Here, the main tasks of the computer involve first, storing the prearranged procedure of series of steps that are to be taken by the automatic machinery which is carrying out the manufacturing process; second, sensing the progress of the machines or the results of their activity on the product being produced; third, after a complex analysis or comparison of the desired end result with the observed result, determining the appropriate next step to be taken; and finally, issuing appropriate signals which will tend to guide the external tools or regulators in a preferred direction. In the latter case, the computer not only is performing many of the functions already described but also is acting as an element in a feed-fack control loop.

Because the DYSEAC has all of these control capabilities, it can be a highly effective tool for exploring any of these diverse areas of potential application. A particular area will naturally require the annexation of terminal devices specific to the nature of the task; yet there need be little or no alteration in DYSEAC itself in order to conduct meaningful investigations directed toward the planning of equipment specially designed for specific tasks.

5. INSTALLATION LAYOUT

In the course of the planning for certain types of control system experiments, it became evident that considerable advantage would accrue if DYSEAC could be moved to the actual operating site. The packaged modular form of the machine, to be described later, readily lends itself to a compact and sturdy construction suitable for transportable service. Accordingly, the program was altered and appropriate structural modifications were incorporated so that the machine could be installed in a trailer van.

In order to provide adequate accessibility to all equipment for both engineering and maintenance purposes and to provide as much space as feasible for operating personnel and such special external equipment as might be required for control experiments, the complete installation is housed in two trailer vans. As can be seen in figure 3.3, the van is of drop frame construction and has a total length of 40 ft, is 8 ft wide, and has an over-all height of 12 ft. The louvered apertures at the rear of the van are a part of the air-intake and exhaust systems for the air-conditioning system. Although the walls and overhead of the van are fully insulated, there are still usable internal dimensions of 31 by 7 by 9 ft behind the drop and a total space of 2,400 ft^3 is available.

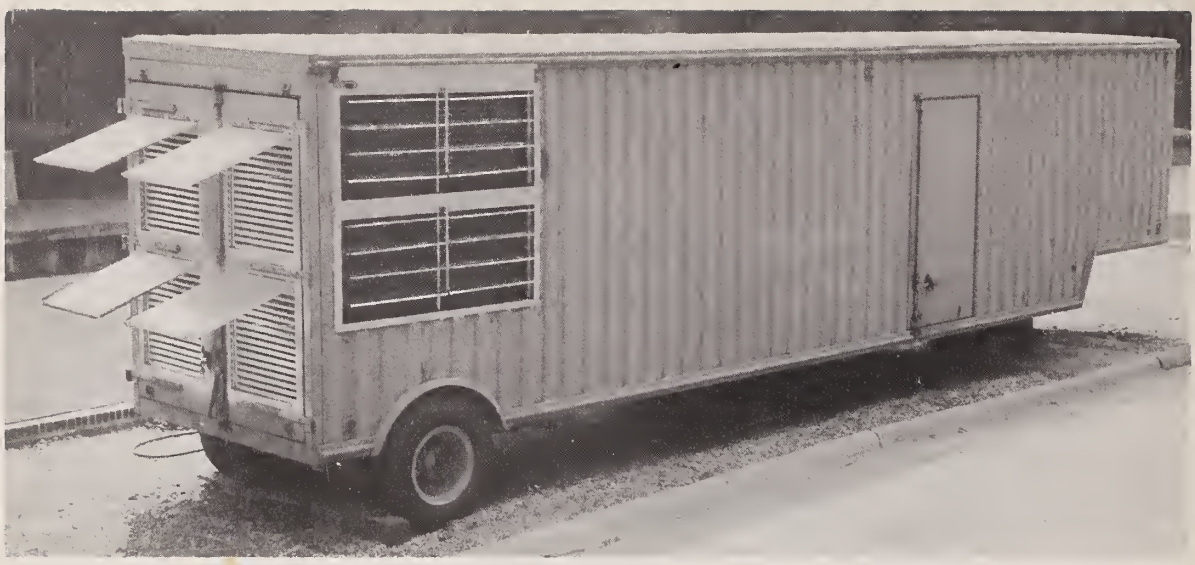

FIGURE 3.3. *Van No. 1, containing the DYSEAC control center and computer including the mercury memory.*

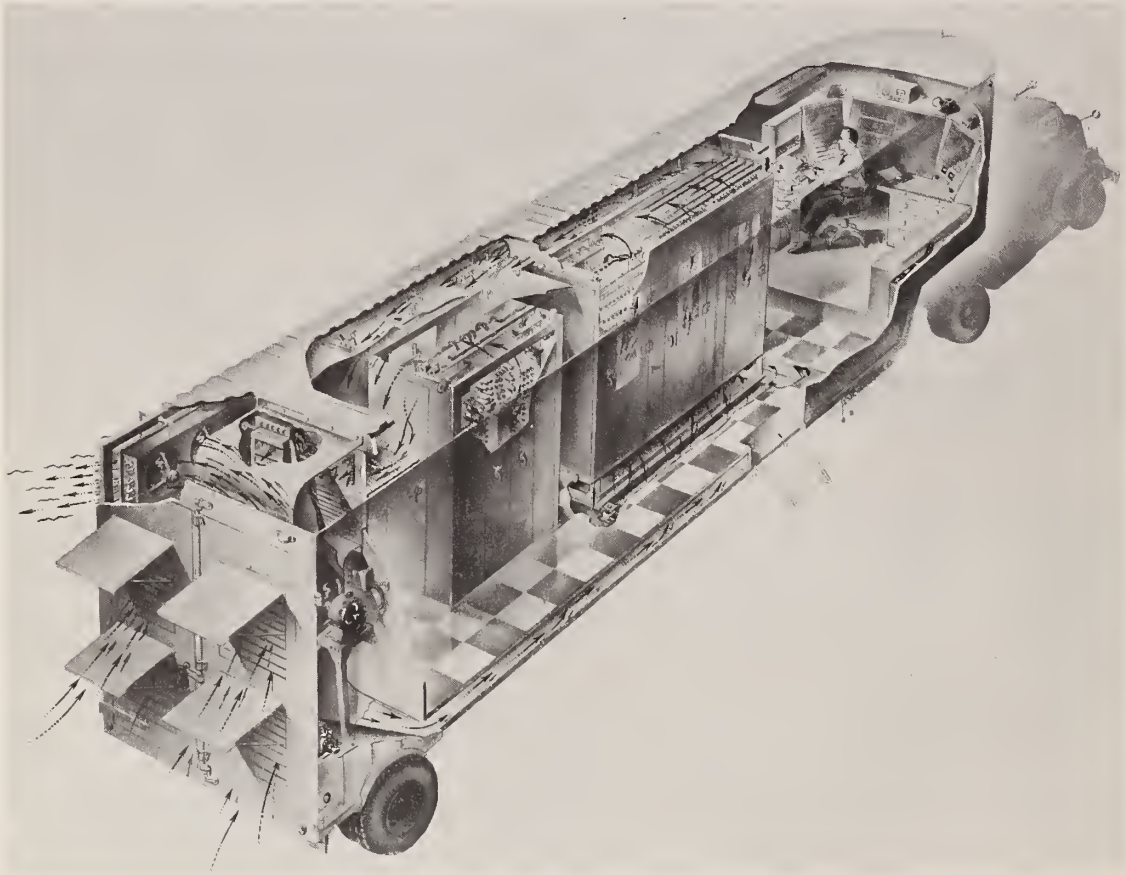

FIGURE 3.4. *Sectional drawing of computer van.*

The arrangement of equipment in the computer van is that shown in the sectional drawing in figure 3.4. Starting at the left, the first 8 ft is occupied by a four-unit air-conditioning plant, which has been purposely located over the wheels to carry the weight, and provides a total capacity of 12 refrigeration-tons. Next in order is the cabinet for the acoustic memory, which is mounted on its own isolated platform to minimize the transmission of shock and vibration during transit. Since this unit was patterned closely after the one used with SEAC, it requires access to all four sides for maintenance purposes and consequently had to be housed separately from the cabinet that encloses the computer proper.

The computer cabinet contains three oversized relay racks of welded frame design. These racks are bolted together to form a single structure which is given added rigidity by using the cabinet panels to absorb the shearing forces. The computer cabinet is also mounted on its own isolated platform to minimize the transmission of shock and vibration during transit. Both the memory cabinet and the computer cabinet are braced during transit by tie bars that cross from their upper corners to the floor, but these are removed when in a fixed location. Finally, the control console and the operator's station are located on the step just forward of the drop in the frame. A small amount of space on the step is reserved on each side of the van so that input-output devices such as magnetic tapes and a magnetic drum can be added to the installation when needed.

The second van is an integral part of the DYSEAC installation, since it contains both the facilities for maintenance and the entire d-c power supply system. The latter has seven separate power supplies; four main supplies, two bias supplies, and one high-voltage supply, all of which are located on the step to utilize this low-ceiling area. The main supplies are rated for a combined output of 10 kw and provide the following voltages: +235, +120, −62, and −65 v. These supplies use selenium stack rectifiers and each has a magnetic amplifier regulator.

An air-conditioning system using two of the standard units is installed at the rear of the second van. Its purpose is to make the interior space suitable for use by personnel under high ambient conditions in the field while all doors are secured so that the special equipment installed in the van can be protected from dirt and moisture. Further, to provide warmth in winter, electrical strip heaters are installed in the air flow systems of both vans. Storage space for spare parts and maintenance equipment is provided at the rear of the van in the remaining space alongside the two air-conditioning units. The central portion of the van presently serves as a general-purpose area in which field maintenance and repair operations can be carried on. However, most of the available 1,500 ft^3 is intended for housing the specialized auxiliary equipment that might be needed during a particular set of experiments or field trials.

The entire DYSEAC installation is designed to be energized from standard three-phase 208-v power distribution system. The computer proper dissipates a total of 12 kw and in order to provide for the necessary voltage regulation and rectification losses, a 20-kva input is needed. The air-conditioning equipment in both vans requires another 35 kva, which includes an allowance for the high currents drawn during starting. Additional capacity beyond this minimum of 55 kva will be needed to provide for the expansion of the installation through the addition of input-output equipment and the special auxiliary equipment. Ample margin for expansion is available if the DYSEAC installation is supplied from the military power vehicle which carries two 50-kw Diesel-driven alternators. Thus, DYSEAC could operate as an independent installation in an isolated field location by the addition of this power vehicle.

The large-signal pulse circuitry used in DYSEAC is based on improved versions of electronic techniques that were developed for use in SEAC. These techniques and their operating characteristics are fully described in a companion paper [4]. The relatively low "impedence levels" in the SEAC circuitry that resulted from the use of a step-down transformer, fast diode gating circuits, and appropriate diode clamping and clipping techniques gave an unexpected measure of protection against pickup due to cross-talk and stray noise. This characteristic permitted unusual freedom in the routing and grouping of signal wires in SEAC and was exploited fully in designing a compact modular plug-in structure for the DYSEAC. The circuitry has gone through three stages of packaging development and is now contained in two basic types of packages, which are pictured in figure 3.5.

The tube and gating package is shown at the right and the delay and termination package is shown at the left. Both packages are designed around an aluminum frame and a pair of side boards, each of

which is attached to a 30-pin half-plug. When assembled, the package is 7 in. in over-all height, 3 1/2 in. in width, and 1 inch thick, and it holds the two half-plugs firmly in position so that they can be plugged into a single 60-pin socket. The split-plug construction facilitates manufacture and permits disassembly for access to the components, which are mounted on the internal faces of each side board. The etched circuit wiring on the external face of each side board is arranged so that the same dip-solder operation that solders the components to the etched wiring also solders the terminals of the wiring to the 30 pins of the half-plug.

The output pulse from any tube package can be observed at a pin-jack on the front end of the package, so that a package whose output is faulty can usually be identified without removing or disturbing anything. At the plug end a relatively large number of pins have been provided so that many of the circuit paths can be completed only through interconnections that are to be made at the base of the plug. The proper circuit paths have been left uncompleted so that every component within the package can be tested in an unambiguous manner entirely through the terminals provided on the package. By so doing, it becomes entirely feasible to design both static and dynamic testing equipment for quickly determining whether any of the 50 components that may be contained in a package are out of tolerance. This can be accomplished without disassembly of the package and without specific knowledge of the detailed wiring of the package. It is hoped that these features in the package design will contribute toward the simplification of maintenance procedures in the DYSEAC.

The temperature sensitivity of some of the components in the tube package requires that special attention be given to their position within the package. The tube and gating resistors have a combined dissipation that can be as high as 17 w, which corresponds to the relatively high figure of 0.8 w/in.^{3} Because the operating characteristics of the germanium diodes are very sensitive to an increase in ambient temperature, it was necessary to provide forced ventilation through the package. In order to minimize the ventilation requirements, it was decided to place all of the diodes in an upstream location with respect to the flow of air through the package. As can be seen in figure 3.5, there is a circular opening in the side of the aluminum frame near the plug which admits air to the package so that it flows first over the diodes. The cooling air then flows past the ferrite cored transformer, whose characteristics can shift slightly with temperature. Next the air flows over the gating resistors, then past the 6AN5 tube, and finally exhausts through another circular opening located on the top of the aluminum frame just above the tube position. It was experimentally determined that an air flow of 3 ft^3/min was sufficient to hold the temperature rise to less than 25° F above the ambient. Similar openings are present in the frame of the delay-line package to provide cooling for the resistors in the termination circuits.

The task of conveniently supplying air to the individual packages to a considerable extent determined the type of construction that was used for the chassis. The chassis were planned to be modular mechanical units that could be used almost everywhere in the computer. A typical chassis loaded with packages is shown in an oblique view in figure 3.6. The chassis is designed around the two long flat air ducts that can be clearly seen in figure 3.6. The sockets for the packages are located so that packages can be pushed against both sides of each air duct. The chassis width was chosen to accommodate 20 packages in each row, giving a total of 80 packages for a complete chassis. A series of easily removed clamp bars, one of which can be seen across the center of the chassis, hold the packages securely in place during transit and the wedge-shaped cross section of the clamp bar assures proper mating for the plug of each package with the socket mounted on the chassis. The clamp bar serves the additional function of firmly seating the air inlet opening of the package against the rubber-grommeted hole that is provided on either side of the air duct as shown in figure 3.7. The size of grommeted hole is small enough to throttle the flow from the air duct to such an extent that when one or more packages are removed the air supply to the remaining packages is not significantly changed.

On the back of the chassis, mounted just behind the air duct, is a bus-distribution system which brings the one-megacycle clock signals and the dc power to the sockets for the packages. As shown in figure 3.7, the top four buses distribute the four-phase clock pulse signals. The dc voltages are distributed on the ten buses which are located above and below the bakelite board which supports the entire distribution system. Power is brought into each chassis through an individual plug mounted at the side, and for the purpose of marginal checking through the use of variable voltages, this plug can be energized from a separate power supply. All signals going between packages within

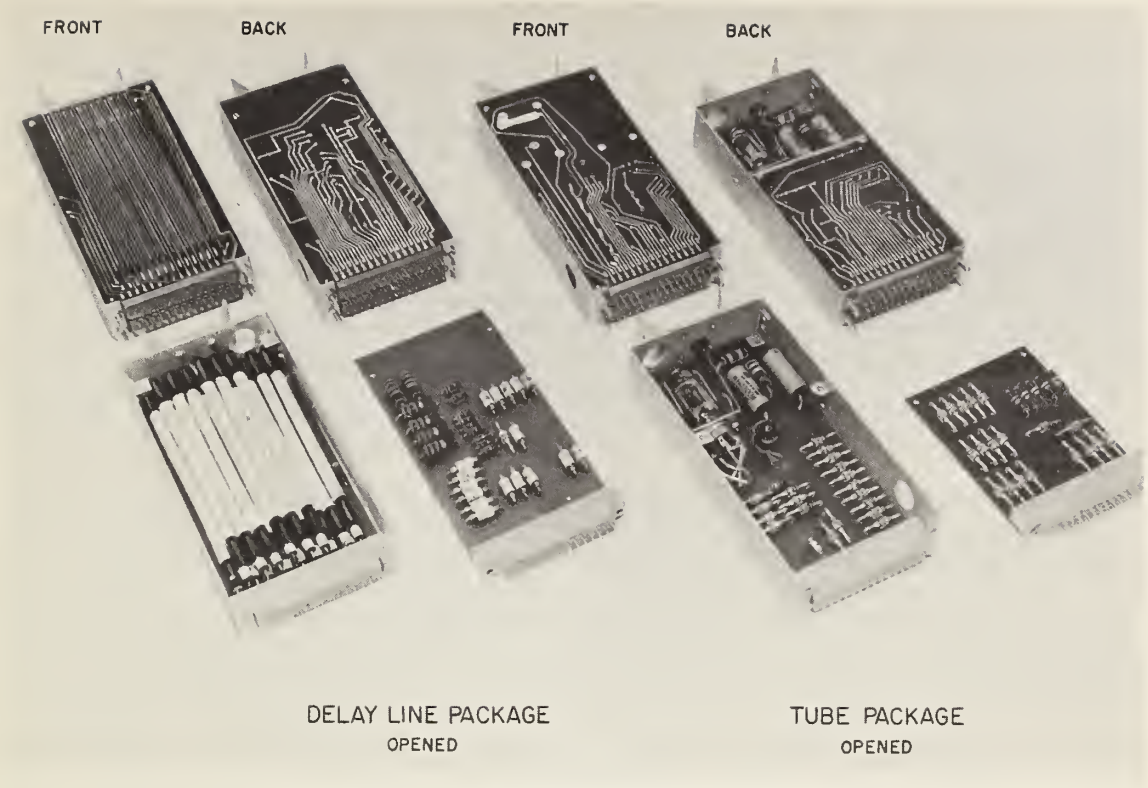

FIGURE 3.5. *The two basic packages used in DYSEAC.*

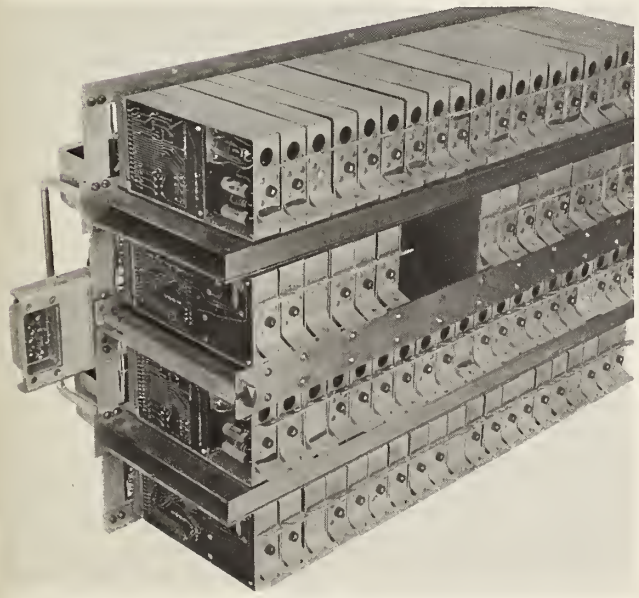

FIGURE 3.6. *Oblique view of typical DYSEAC chassis.*

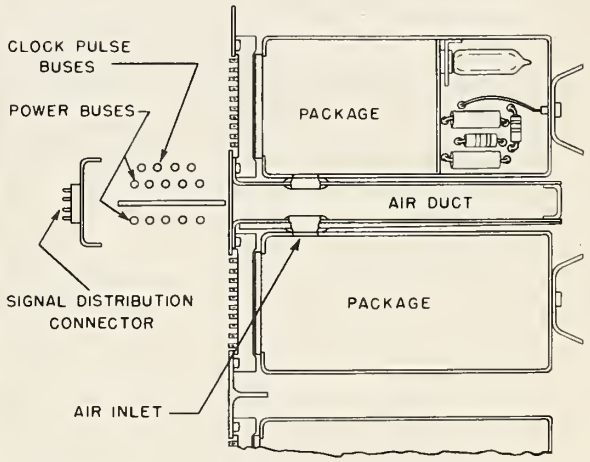

FIGURE 3.7. *Diagram of package arrangement in DYSEAC chassis.*

the same chassis are wired permanently into place. All signals going between chassis are brought out to the signal distribution connector, which is composed of a number of 35-pin plugs. During the initial operation of the machine, individual pin-to-pin connections were made with push-on leads of a hooded construction. The eventual purpose is to consolidate the interchassis connections into groups which terminate in 35-pin sockets that mate with the plugs of the signal distribution connectors. Since several spare package positions were left on most chassis to allow for simple modification and limited expansion, this step was purposely deferred until the signal distribution has become completely stabilized.

Considerations in the design for the rack were about equally divided between the supply of air to the chassis and the distribution of power and signals throughout the rack. Each rack is arranged to hold four chassis. The chassis slide into position between two large vertical air ducts. In so doing, the ends of the two air ducts of each chassis fit into long rectangular openings that are present in the sides of the vertical air ducts. The size of these rectangular openings is chosen small enough with respect to the cross section of the vertical duct so that the removal of one or more complete chassis from a rack will not dangerously diminish the supply of air to the remaining chassis in the rack.

Three such racks are housed within the computer cabinet. The blower in the air-conditioning system forces cool air to flow along the false floor on which the entire computer cabinet stands. The air flows up the vertical ducts and out along the air ducts of each chassis and passes through the individual packages, which then exhaust into the space enclosed by the computer cabinet. The air return of the air-conditioning system draws off this exhaust air and causes it to flow through the personnel space in the van and then back into the cooling system. The memory cabinet is ventilated similarly by admitting air from beneath the false floor and exhausting it above the false ceiling.

Each rack contains four power transformers to supply the filament power. These transformers are to minimize the difference in voltage at the sockets of the vacuum tubes in the several chassis. All voltages for each chassis are individually fused and have their own bypasses located on the rack structure. In order to reduce the effects of inductance in the d-c supply leads, bypassing is provided on both sides of each chassis. These racks contain 524 tube packages and 251 delay line packages. There are about 400 additional amplifier stages in the mercury memory and in the input-output system.

The input-output system for DYSEAC has been planned to have considerable versatility and is arranged to be readily expandible with a minimum alteration of the central computing equipment which has already been installed. This feature is particularly important in order that the specialized equipment needed for control-type experiments and for experiments in the mass processing of business-type data can be readily annexed to the installation. A particular example of a specialized item that is applicable to both experiments is the notched-disk magnetic memory [5], which is now nearing completion.

The initial installation, however, is limited to fairly simple input-output equipment of the sort now in regular operation with SEAC. A magnetic wire cartridge unit is available for use, and space for the installation of additional units is available on the console. These units can be loaded with sufficient magnetic wire to store up to 20,000 words and have a transfer rate of 100 words per second. Because the start-stop time is approximately one second, these units are intended for block loading and unloading, where the start-stop time is not an important consideration. The console is provided with an electromechanical typewriter that is directly connected with the computer. Transfers into the machine at the rate of 10 characters per second can be entered either from the keyboard or the punched paper tape reader. The computer can be programmed to print directly on the typewriter or punch a paper tape. When the input characters are organized into a base-16 code, the machine word than consists of 11 numerical characters followed by an algebraic sign and a space, giving a transfer rate of 1.3 seconds per word. On the other hand, when the input characters are organized into an alphanumeric code, the machine word contains 7 alphanumeric characters, giving a transfer rate of 0.7 second per word.

One of the console panels contains approximately 90 switches, which are a very specialized type of input-output equipment needed in using the Manual-Monitor and Program-Jump features of the

machine. In order to give the operator command over all of the input-output devices and the computer, it was necessary to run several hundred interconnecting leads between the computer rack and the console and the console base, which contains a bank of specialized bias and filter circuits that are associated with the various switches of the console.

There have been a number of problems associated with the design of a machine having such novel operating features and located in the rather unfamiliar environment provided by a trailer van, which led to several design choices which have not yet been fully evaluated. A particular example is the task of reinforcing the mercury acoustic memory in which the mercury is contained in Pyrex glass tubing. A number of laboratory tests were employed to guide design alterations but at the present time there is no operational experience to indicate how complete the protection has been against shock and vibration. Since the sensitive elements of the acoustic memory can be removed and stowed in special bins during transit, the success of this protection was not a prime consideration for the present program. If sufficient time had been available, the acoustic memory would have been redesigned to employ the now available quartz block acoustic paths. Such a design should not only be more serviceable for field application but would also be considerably more compact and could be assembled directly with the computer proper.

Finally, there are a number of design features intended to minimize the problems of maintenance and supply for digital equipment at a distance from the normal conveniences of the laboratory environment. Particular reference is made to the package construction which is planned for simple and rapid testing and replacement. As soon as the results of the evaluation tests are at hand, it is planned to report the results in the appropriate technical journals.

The Electronic Computers Laboratory was fortunate in having the consulting assistance of the NBS Heating and Air Conditioning group and a competent contractor in the development of the compact, transportable air-conditioning equipment installed in the two vans.

6. REFERENCES

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[4] R. D. Elbourn and R. P. Witt, Dynamic circuitry techniques used in NBS computers, paper 2 of this Circular.

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7. APPENDIX

7.1. Comparison with the SEAC

Operations. Of the 16 types of operations performed by the DYSEAC, five types are the same as those in the SEAC, five types represent variations or expansions of their SEAC counterparts, and six are either entirely new or completely revised. In the latter class are the two Accumulation instructions and the Summation, Justify, and high-speed Shift operations which have been provided to facilitate coding and to speed up the performance of various arithmetic and data-handling processes. In the expanded class of operations, the facility for providing both major and minor products (or both quotient and remainder) in little more than a single multiplication (or division) time should be noted. Improved base-point and relative-address arrangements have also been provided. All of these arithmetic, processing, and program-control operations are described in sections 7.3 and 7.4. The input-output features of the DYSEAC, representing a completely new departure from the SEAC

system, are described in section 7.5; and the manual-monitoring facilities, also representing an important departure from the SEAC system, are described in section 7.6.

Pulse Codes for Representing Information. Like the SEAC, the DYSEAC operates on a minor cycle of 48 μsec and employs a pure binary word representation consisting of 44 binary numerical digits plus one sign digit. Numbers are expressed in the form of absolute value plus algebraic sign. The sign (+) is represented by 0, and the sign (−) is represented by 1. For details on the word-format, see table 4.

DYSEAC also employs a three-address instruction system, that is, each instruction word contains three address-numbers denoted as alpha, beta, and gamma, which in most cases have the following significance: Alpha denotes the location (in the acoustic memory) of the first operand, beta denotes the location of the second operand, and gamma denotes the location to which the result is to be sent. Each address-number referring to these locations is represented, within the instruction word, by a 12-digit binary number sequence composed of three parts:

1. The smallest three digits indicate the position of the word in the tank, i.e., the timing number (0 to 7).

2. The next six digits are the binary representation of the tank number within the cabinet of 64 tanks (0 to 63).

3. The largest three digits designate which one of the eight possible cabinets is referred to (0 to 7).

These three combined parts form the binary representation of the address-number (0 to 4,095), successive numbers generally indicating adjacent locations in the same tank. Successive instructions are generally located in consecutively numbered memory locations.

The total information content of an instruction word is distributed as follows:

12 digits contain the address *alpha*,
12 digits contain the address *beta*,
12 digits contain the address *gamma*,
4 digits contain relative-address and program-sequencing information (described in table 6),
4 digits contain the code-symbol specifying the type of operation to be performed,
1 digit contains a monitor signal (whose utilization is described in section 7.6), and
1 digit is a check digit (whose utilization is described in section 7.2).

TABLE 4. Word-format (internal)

Each instruction word contains—		
Binary digits	Digit position in word[a]	Content
1 bit	P-46	Check digit.
12 bits	P-45 through P-34	Address alpha.
12 bits	P-33 through P-22	Address beta.
12 bits	P-21 through P-10	Address gamma.
4 bits	P-9 through P-6	Relative-address and program-sequencing information.
4 bits	P-5 through P-2	Operation code-symbol.
1 bit	P-1	Monitor signal.
46 bits total		
Each number word contains—		
1 bit	P-46	Check digit.
44 bits	P-45 through P-2	Numerical digits.
1 bit	P-1	Algebraic sign digit.
46 bits total		

[a] The successive binary digit positions in a word are denoted by P-1, P-2, . . . , P-46, counting from right to left (least significant to most significant).

7.2. Checking features

Like SEAC, the new machine contains provision for automatically checking the performance of the high-speed memory. The design of this checking feature is based on observed experience of the operating reliability of the acoustic delay-line memory used with SEAC. Its inclusion is based on the premise, supported by SEAC experience, that the faults most commonly encountered with this type of memory are those which result in an occasional picking up or dropping of a single binary digit in some part of the memory. The checking feature in DYSEAC is designed to guard against the possibility that such errors may pass by undetected.

The system operates on the principle of inserting a single odd-even check digit at the end of each word as it is being written into the memory. This check digit, which is chosen so as to make an *odd* number of the total sum of the one-digits appearing in each word, occupies the P-46 digit position of the word and is not susceptible to manipulation by the arithmetic (or other program) instructions. The consistency of each word stored in the memory is checked by a special detecting device which causes a halt (with appropriate warning signal) whenever a word is observed which fails to pass the odd-number checking test.

This error-detecting device can detect an error under any of the following circumstances:

1. Whenever a defective word is read out of the memory or is found to occupy a memory location which is about to be written into.

2. Whenever a defective word is observed in a memory tank during the period prior to the minor cycle in which the particular address sought for becomes available.

3. Approximately once every second or so, at which time the program is temporarily halted for about 25 msec and the entire memory is scanned from beginning to end in search of a defective word.

In all cases, the halt and error-signal indications occur in time to prevent the execution of any further instructions. For example, when a memory location containing a defective word is written into, the halt occurs immediately after the writing has taken place and before a new instruction has been selected.

Manual controls are provided to aid in locating the address that contains the defective word (see section 7.6.). Whenever a defective word is printed out on the supervisory printer, a characteristic error-indication character replaces the customary sign-indication character at the right-hand end of the word.

Although intended primarily for application in connection with the mercury acoustic delay-line memory, the checking equipment is in no way restricted or limited to this type of memory and may be utilized equally well in connection with any other type suited for annexation to this machine.

7.3. Arithmetic and Processing Operations

Five addition-type operations are provided, namely, Addition (normal), Subtraction, Accumulate-and-Overflow-Check, Accumulate-and-Store, and Summation. These operations are described in detail in the following paragraphs.

Addition, normal (code symbol, 2). This is the usual algebraic addition operation, like the one used in SEAC. The instruction reads "Form the sum of the word in alpha and the word in beta, and write the result in address gamma."

Subtraction (code symbol, 1). The instruction reads "Form the difference of the word in alpha minus the word in beta, and write the result in address gamma." No provision is made in either this operation or the preceding one for checking against the occurrence of overflow.

Accumulate-and-Overflow-check (code symbol, 4). This operation and the following operation are intended for use in situations where the accumulation of the sum of a long list of numbers is desired, or in situations where it is particularly difficult to predict the occurrence of overflow. It combines the characteristics of both an arithmetic operation and a choice operation. Both instructions involve the use of an arithmetic register for the purpose of accumulating a partial sum.

This register is referred to as the *arithmetic accumulator register*, or simply the *accumulator*. The instruction reads "Form the sum of the word in alpha and the word in beta plus the contents of the accumulator, and, if the sum does not overflow, store the result in the accumulator, and proceed to the normal next instruction. If the indicated sum does produce an overflow, however, leave the previous contents of the accumulator unchanged and take the next instruction from address gamma in the memory." For rules governing the clearing of the accumulator, see paragraph below. Note that this operation does not involve the writing of any information into the memory.

Using the Accumulate-and-Overflow-Check instruction, lists of numbers may be summed at least twice as fast as is possible by means of the normal addition operation, because a single instruction allows two items rather than only one to be added to the accumulated partial sum.

Accumulate-and-Store (code symbol, 5). This instruction permits writing of the contents of the accumulator register into the memory. It is used for terminating a series of Accumulation-and-Overflow-Check operations. It does not in itself provide any check against overflow.

The instruction reads "Form the difference of the word in alpha minus the word in beta, add the contents of the accumulator to the result, and write the sum into memory address gamma. Then clear the accumulator."

This instruction is also used for clearing the accumulator prior to starting an accumulation sequence. Another use occurs during double-precision operations or when division remainders are desired. These are described in the paragraphs dealing with Multiplication and Division.

The rules governing the modification of the accumulator contents and the effect of the accumulator contents on the various operations are summarized in table 5. Notice that the accumulator contents affect (or are affected by) only five out of the total of 16 instruction types. This fact contributes considerably to the power and flexibility with which these accumulation features can be used, because it allows the coder to interleave those accumulation instructions that actually add the successive items to the partial sum with other instructions, such as normal additions, comparisons, and logical transfers, which can be used for modifying addresses in some of the instruction words, keeping independent tallies, and so forth.

Notice also that this operation involves the difference (alpha minus beta) rather than the sum (alpha plus beta), as in the preceding operation. This feature is intended to facilitate the process of writing the contents of the accumulator, unmodified, into the memory. To accomplish this, the coder need only write the same arbitrary number for both of the addresses alpha and beta in the instruction word. This may be desirable for the final step in the accumulation process, if the coder fears the possibility that the addition of the last two items may cause an overflow.

TABLE 5. Summary of rules governing use of accumulator

Instructions not affecting (and not affected by) contents of accumulator	Instructions affecting contents of accumulator	Modified contents
Addition Subtraction. Summation. Shift. Justify. Logical Transfer. Comparison (algebraic). Comparison (absolute). File (unconditional). Breakpoint File. Input-Output.	Accumulate-and-Overflow-Check[a]---- Accumulate-and-Store[a]---------- Multiplication, major (rounded)--- Multiplication, minor---------- Division----------	Partial sum. Zero. Major product (rounded). Major product (unrounded). Remainder.

[a] Except for these two accumulation operations, the previous contents of the accumulator do not affect the *result* of the operation.

Summation (code symbol, 3). This operation permits the extremely rapid summation of large blocks of words located in consecutively numbered address positions in the memory. The instruction reads "Form the sum of the words located in consecutive address locations running from beta through alpha, inclusive, and write the sum in address gamma in the memory." For this operation, address beta is ordinarily numerically less than address alpha. If this condition is not observed, however, the sum of the words in addresses beta and beta-plus-one is produced.

No provision is made in this operation for checking against overflow. In carrying out certain programs of checking procedures, however, which involve forming the sums of large groups of words, the occurrence of overflow is generally not material. It must be remembered that when overflow does occur, the sum obtained may be in one of two ambiguous forms, $(4-x,-x)$, depending upon the order and the grouping in which the words were summed. The equivalence of these two forms may be established, however, by checking the fact that their difference, as computed by a Subtraction operation, is numerically equal to zero.

Summation operations and input-output operations do not proceed concurrently. If a Summation instruction is given while an input-output operation is in progress, the program is temporarily halted until the input-output operation has been completed.

Major multiplication, rounded (code symbol, A). This operation produces a rounded-off major product. The binary point in both of the operands and in the result is located two binary positions from the left-hand end of the word (i.e., between P-44 and P-43). In other words, the largest magnitude that these numbers can reach is slightly less than four. The instruction reads "Form the product of the word in alpha and the word in beta, and write it, rounded off, in address gamma in the memory and in the accumulator."

Rounding-off is accomplished by adding a unit in the first rejected position on the right-hand end of the product and allowing the resultant carrys, if any, to propagate. Means for securing the major product unrounded are described under minor multiplication.

The time required for all multiplication-division types of operations is 44 minor cycles longer than for an addition operation.

Minor multiplication (code symbol, B). This instruction produces the minor product. The instruction reads "Form the minor product of the word in alpha and the word in beta and write the result in address gamma in the memory." The location of the binary point in this operation is the same for the words in alpha and beta as in the preceding operation. The result, however, is positioned so that the least significant digit in the porduct is located in the extreme right-hand numerical position in the word, namely, the P-2 position. An alternative interpretation of the binary point positions would be that the binary point for both of the factors and for the product is located at the extreme right-hand end of the words (that is, all of the words are integers).

Whenever a minor Multiplication instruction is performed, the major product, unrounded (with proper sign), is written into the arithmetic accumulator register. If such an operation is followed by an Accumulate-and-Store instruction, the major product may be written into the memory in considerably less than the usual multiplication time. It should be noted that the right-most two binary digits of the major product and the left-most two binary digits of the minor product are identical.

Division (code symbol, C). By means of the Division operation, both the quotient and the remainder may be obtained rapidly. The instruction reads "Form the quotient of the word in beta divided by word in alpha, and write it in address gamma in the memory." The positions of the binary point in this operation are the same as for the major Multiplication operation described above. The quotient is not rounded off, and the process is carried out in such a way that the quotient may be in error by being numerically too small as a result of the lack of rounding off. Whenever a Division operation is performed, the remainder is written into the arithmetic accumulator register with proper sign, namely, the sign of the dividend. The remainder is never numerically greater than the divisor times two to the minus 42 power. The remainder may be rapidly written into the memory by means of an Accumulate-and-Store instruction, as described previously.

Shift (code symbol, 8). By means of this operation, words may be shifted an arbitrary number of places either to the left or to the right in considerably less than a Multiplication or Division

time. The instruction reads "Shift the word in alpha according to the code indicated in the word located in address beta in the memory, and write the result in, address gamma in the memory." The six numerical digits P-2 through P-7 of the word in memory location beta indicate the number of binary places the word is to be shifted; the P-1, or sign digit, indicates the direction of the shift, i.e., for left-shift positive and for right-shift negative. In other words, the digits P-1 through P-7 indicate the power of two by which the word in alpha is to be multiplied without round-off. The sign of the shifted word is transferred unchanged.

The time required for a shift operation is a function of the number of places shifted, and ranges from 1 minor cycle to 12 minor cycles (average 6.5 minor cycles) longer than an addition operation.

Justify (code symbol, 9). The Justify operation provides the coder with a convenient means for carrying out floating binary point operations, or other operations requiring frequent readjustment of scaling factors. The instruction reads "Determine the number N satisfying the following inequalities:

$$(\beta) \leq (\alpha)2^N < 2(\beta); \qquad -63 \leq N \leq 63,$$

and write this number with proper sign into the digits P-1 through P-7 of the word in address gamma without in any way altering its other digits." (β) and (α) mean "absolute value of words in memory addresses β and α, respectively. By choosing (β) equal to a power of 2, this operation can be used to determine the number of places that the word in alpha must be shifted in order to make its most significant binary digit coincide with the most significant binary digit of the word in beta. Note that the result of a Justify operation is written into the memory in such a way as to make it possible to use it immediately as the beta operand in a subsequent Shift operation which will cause the shifted word to be lined up with some designated comparand in the manner described by the first inequality above.

When either or both of the operands in a Justify instruction are equal to zero, the result produced is $N=63$, as indicated in hexadecimal notation in the following table:

Alpha	Beta	Gamma
Zero---------	Not zero----	3F+
Not zero-----	Zero--------	3F−
Zero---------	--do--------	3F−

The time required for a Justify operation is a function of the value of N produced and averages $N+2.5$ minor cycles longer than an addition operation.

Logical Transfer (code symbol, D). The logical transfer instruction is similar to its counterpart in SEAC. The instruction reads "Write in address gamma in the memory those digits of the word in alpha which correspond to one-digits in the word in beta. Leave the word in gamma unchanged in those digit positions which correspond to zero-digits in the word in beta." This operation permits segments of one word to be transplanted into another word. Also, it contains as special cases the processes of logical multiplication and logical addition.

7.4. Program-Control Operations

Program-sequencing. As in the three-address control system in SEAC, two distinct counter-registers are provided, for program sequencing, which allow the programmer to choose between two possible alternative sequences of instructions at any time. That is, he may (if he wishes) interleave two distinct sequences, periodically jumping from one to the other in an arbitrary manner. These counter-registers are designated as counter No. 0 and counter No. 1, respectively. Each counter holds a 12-binary-digit address. The coder may select the address in either counter as the

address of the next instruction to be performed. The counter from which the address of the next instruction is to be taken is indicated by the P-6 or "d" digit in the instruction being currently executed. (See table 4 for the format of an instruction word.) In other words, this d-digit in every instruction indicates the source of the address of the instruction immediately to follow. Execution of this process may be temporarily suspended, however, by means of a program-jumping feature available in connection with input-output operations, which is described in section 7.5.

Comparison, algebraic (code symbol, 6). By means of this instruction, either of the counter registers may be reset and a new program sequence initiated, starting at the new address setting. The instruction reads "If the word in alpha is algebraically greater than or equal to the word in beta, take the next instruction from the normal consecutive address position. If, however, the word in alpha is less than the word in beta, take the next instruction from address gamma and reset the counter specified by the P-6 (d-digit) to gamma." Note that the indicated inequalities pertain to the algebraic magnitudes of the numbers.

Comparison, absolute (code symbol, 7). This instruction is similar to the Comparison (algebraic) described in the preceding paragraph, differing from it only in that the indicated inequalities pertain to the *absolute* values of the numbers indicated.

Overflow-check (code symbol,4). The Accumulation-and-Overflow check operation described in section 7.3. may be used as a choice-type operation as well as an arithmetic-type operation. Paraphrasing the previous description of this operation, it becomes: "If the addition of the word in alpha and the word in beta to the contents of the accumulator causes an overflow, take the next instruction from address gamma in the memory and reset the counter specified by the P-6 (d-digit) to gamma. Otherwise, take the normal next instruction."

Relative addresses. The numbers written in the address segments of an instruction word may be interpreted in either of two ways, namely, as absolute addresses or as relative addresses. The intended interpretation is indicated by a set of code digits in each instruction word (see table 3). A code digit 0 indicates an absolute address, and a code digit 1 indicates a relative address.

An absolute address is interpreted merely as a number identifying a specific fixed memory location. A relative address, however, identifies a position in the memory by specifying its displacement relative to a certain address number that is stored in one of the special counter-registers. That is, if the counter-register in question contains the number C, then whenever an address number A is written in an instruction word *along with a relative designation,* the memory location A plus C is referred to. The value of C may range from 0 to $2^{12}-1$, and the effect of negative displacements can be secured by using the complement, modulo 2^{12}, of the displacement desired.

Either of the two available counter-registers (No. 0 or No. 1) can be used in this fashion. The File instructions, which are described on the next page, govern the adoption of either counter for relative address purposes and the insertion of the desired base number, C. After either counter is adopted for this purpose, it remains adopted until a countermanding File instruction is given. The following terminology is used in the subsequent discussion:

Relative counter, or adopted counter, refers to the counter-register holding the number to which alpha, beta, or gamma is relative. (Chosen by means of File instructions.)

Instruction counter refers to the counter-register holding the address from which the next instruction is scheduled to be taken. (Chosen by means of d-digit in each instruction word.)

As a result of the dual counter-register system, two different general methods of applying the relative address facility are available. The first method makes use of a *fixed* base number, or base point, from which the address in the instruction word is used to indicate the relative displacement of the memory location referred to. In this type of application, the counter adopted for relative (Adopted Counter) and the counter used for program sequencing (Instruction Counter) are different. For example, suppose counter No. 0 is chosen as the Instruction Counter and counter No. 1 is the Adopted Counter. Since counter No. 0 is the Instruction Counter (i.e., all the instructions are written with the d-digit equal to zero), the counter reading is generally increased by unity after each instruction is executed. The contents of counter No. 1, however, since it is not being used

TABLE 6. Relative-address information and program-sequencing information

Binary digits	Digit position in word	Contents
a-digit--------	P-9----------	Indicates whether *alpha* is an absolute or relative address.[a]
b-digit--------	P-8----------	Indicates whether *beta* is an absolute or relative address.
c-digit--------	P-7----------	Indicates whether *gamma* is an absolute or relative address.
d-digit--------	P-6----------	Indicates which counter register contains the address of the next instruction.
Total: 4 bits		

[a]Except for the operations Input-Output (see table 10), File and Breakpoint (see table 8).

for program sequencing, can be left unchanged. Thus all operands in the instruction being executed can remain relative to a fixed point.

From time to time, the contents of the adopted counter (No. 1) may be modified as the occasion arises. After each such modification, which requires only a single instruction word, all of the operands referred to in the set of instructions being executed are automatically selected from a new block of memory locations. This type of procedure is particularly valuable when large numbers of identical operations need to be performed on successive words, or groups of words, systematically arranged in the memory. Examples of this sort arise in matrix operations, a typical example being the multiplication of two matrices.

The second type of application of the relative address feature involves the use of a *floating* base point, rather than a fixed one. This floating base point is the address of the instruction word itself. Under this scheme, the adopted relative counter and the instruction counter are the same. With this procedure, the memory locations of the operands referred to may be indicated relative to the instruction word even when the address in which the instruction word is located is not known to the coder at the time the program is being written. This feature is particularly valuable in permitting the preparation of standardized subroutines in an invariant form that is independent of the actual memory locations into which the subroutines will ultimately be inserted.

A counter-register is adopted as a relative counter by means of one of the counter-setting and filing operations, namely, File (unconditional) or Breakpoint File, which are described below.

File, unconditional (code symbol, F). These counter-setting and filing operations permit the programmer to (1) adopt either given counter as the relative counter, (2) reset this counter to a new reading, and (3) record the old setting of the counter in the memory along with various other useful information. The File (F) instruction reads "Write the file record (indicated in table 7 below) into the memory location specified by address beta in this File instruction word. (Format of the File instruction word is indicated in table 8.) Then adopt the counter specified by the P-9 digit of File instruction word for relative references. Finally, reset this counter according to the setting indicated in the gamma segment of the File instruction word."

After a counter-register is set by means of a File instruction, its contents remain fixed until either (1) reset by another File instruction or (2) referred to as the source of the address of a next-instruction. As a general rule, whenever a given counter-register is referred to as the source of a next-instruction address, the counter reading does not receive its unit advance until after the current instruction has been executed and its result has been written in the memory. Exception is made to this rule only in the case of the P-45 through P-34 digits of the file-record, in order to record the address of the scheduled next-instruction. If a counter has not been used as the source of a next-instruction address since it was last adopted or reset, this fact is indicated in the P-3 or P-4 digit of the file-record.

TABLE 7. File-record: Information written into the memory as a result of a File instruction (F or E)

Information	Contained in digit position—
Address of scheduled next instruction	P-45 through P-34
New counter reading, after resetting	P-33 through P-22
Prior counter-reading, plus the number in the alpha segment of the File instruction word.	P-21 through P-10
File instruction word a-digit	P-9
File instruction word b-digit	P-8
File instruction word c-digit	P-7
File instruction word d-digit	P-6
Which counter was previously adopted (No. 0 or No. 1)	P-5
About counter No. 0 (If this counter has not been used as a next-instruction address source since it was last adopted or reset, the P-4 digit is 1; if it has been so used, the P-4 digit is 0.)	P-4
About counter No. 1 (If this counter has not been used as a next-instruction address source since it was last adopted or reset, the P-3 digit is 1; if it has been so used, the P-3 digit is 0.)	P-3
About the previous instruction (Whether the d-digit of the previous instruction was a 0 or a 1.)	P-2
About the counter not being adopted (If this counter is at present being reserved for an Input-Output program jump[a], the P-1 digit is 1; if not, the P-1 digit is 0.)	P-1

[a] For a discussion of Input-Output program jumps, see section 7.5.

The File instruction word, which is not to be confused with the resulting file-record, has the same general format as the other types of instruction words (cf. tables 4 and 8) but the significance of some of the digit positions is different.

TABLE 8. Word-format of file instructions

Digits	Word segment	Contents
P-45 through P-34	Alpha	Contains the displacement constant to be added to prior counter reading in order to produce P-10 through P-21 of file-record.
P-33 through P-22	Beta	Contains the memory address, absolute or relative,[a] into which the file-record is to be written.
P-21 through P-10	Gamma	Contains the new setting for counter, either absolute or relative.[b]
P-9	a-digit	Indicates which counter to file and reset (No. 0 or No. 1).
P-8	b-digit	Indicates whether beta is absolute (0) or relative (1).[a]
P-7	c-digit	Indicates whether gamma is absolute (0) or relative (1).[b]
P-6	d-digit	Indicates which counter is the source of the next-instruction (No. 0 or No. 1).
P-5 through P-2	Operation symbol	Contains the file-operation code symbol.
P-1	Monitor signal	Either 0 or 1.

[a] For beta, relative to previously adopted counter.

[b] For gamma, relative to newly adopted counter, indicated by a-digit.

Some examples of several typical uses of the file instruction and the resultant file-record written into the memory are contained in table 9.

TABLE 9. Typical uses of the file instruction

Example	Purpose of instruction	P-digits	Contents of file instruction	Contents of file-record
1-------	File both counter readings in address X; the No. 0 counter to be retained as the instruction counter; the No. 1 counter to be retained as the adopted counter.	45—34	0	Counter No. 0, advanced.
		33—22	X	Counter No. 1.
		21—10	0	Counter No. 1.
		9	1	1
		8	0	0
		7	1	1
		6	0	0
2-------	File both counter readings in address X; the No. 1 counter to be retained as the instruction counter; the No. 0 counter to be retained as the adopted counter.	45—34	0	Counter No. 1, advanced.
		33—22	X	Counter No. 0.
		21—10	0	Counter No. 0.
		9	0	0
		8	0	0
		7	1	1
		6	1	1
3-------	File in memory address X the address for the present instruction (counter No. 0) reduced by Y (to be interpreted later as the location of the instruction initiating another iteration of program); the No. 0 counter to be retained unchanged as the adopted counter; the next-instruction address to be taken from counter No. 1.	45—34	$2^{12}-Y$	Counter No. 1.
		33—22	X	Counter No. 0.
		21—10	0	Counter No. 0 minus Y.
		9	0	0
		8	0	0
		7	1	1
		6	1	1
4-------	Reset counter No. 1 to equal X; and take the next instruction from X.	45—34	0	X
		33—22	Unused address	X
		21—10	X	Previous setting of No. 1.
		9	1	1
		8	0	0
		7	0	0
		6	1	1
5-------	Advance counter No. 1 by X units and adopt it for relative references purposes; take next-instruction address from counter No. 0.	45—34	0	Counter No. 0.
		33—22	Unused address	Counter No. 1, advanced X.
		21—10	X	Counter No. 1, before advance.
		9	1	1
		8	0	0
		7	1	1
		6	0	0

Breakpoint File (code symbol, E). The Breakpoint File instruction provides an operation which is exactly similar to the unconditional File instruction (F) except that it requires the setting of an external switch to indicate that its activation is desired. If the external switch is not so set, Breakpoint File instructions are passed over in the program without causing the prescribed alteration in counter readings, etc., or writing into the memory. The next instruction is selected according to the usual rules, i.e., from the next consecutive address.

The Breakpoint File instruction is intended to facilitate the carrying out of program monitoring operations such as are required in the initial debugging of a new program. For example, the programmer can insert Breakpoint File instructions liberally throughout the program, arranging them in such a way as to cause program jumps leading to interpolated automonitoring routines. The automonitoring (or program analysis) routines can be composed in the widest conceivable variety. The initial trial running of a program may then be carried out with the Breakpoint operations activated whenever the need for automonitoring appears to arise. For the normal running of a program, the Breakpoint File instructions can be rapidly passed over without causing any significant loss of time. From a slightly different point of view, the Breakpoint File may be used to cause a given program to be carried out in either of two previously specified ways depending upon the setting of the external selection switch. This feature may be used in applications analogous to those described in section 7.6.

The unconditional File and Breakpoint File operations do not refer to addresses alpha or gamma in the memory, thereby avoiding the access time which would otherwise be required for these operations.

7.5. Input-Output Transfer Operations

Load and Print instructions (code symbol, 0). In using this system, the programmer can arrange to load or print out any consecutive series of memory locations ranging in size from a single word to the entire memory, even while a program of computation is proceeding. Automatic interlocks are provided in the event that the programmer inadvertently attempts to use any memory location in an inconsistent manner in this respect.

The types of input-output operations have been chosen so as to be readily applicable for use with input-output units of widely varying types and characteristics, such as (1) a collection of magnetic wire or tape drives, (2) one or more magnetic drum storage units, (3) mechanical keyboard and printing devices such as Flexowriter, and (4) special analog-type input or display devices.

The format of an input-output instruction word is indicated in table 10. The alpha segment of the instruction word is used to specify (1) the type of operation, i.e., Load or Print, (2) the type of unit, such as tape unit or drum unit, (3) the direction of motion of the unit, if relevant, (4) the running distance or location of the initial word sought for on the external unit, and (5) the code identifying the particular unit or channel desired. The gamma address segment in the instruction word specifies the initial address in the high-speed memory, and the beta address segment indicates the final address in the high-speed memory between which the transfers are to be made. For transfers to take place, the designated final address beta must be numerically greater than or equal to the designated initial address gamma. If this condition is not satisfied, no transfer of information takes place, and the instruction becomes merely an order to move the designated unit a specified distance in a given direction, and could be used for rereeling tape drives, and so forth.

TABLE 10. Word-format of a typical input-output instruction (for tape or wire unit and drum unit)

Digits	Word segment	Contents
P-45	Alpha	Indicates type of operation: Load (0), or Print (1).
P-44	--do	Indicates type of unit: Tape (0), or Drum (1).
P-43 through P-34	--do	Indicates location of information on unit. On drum: The quadrant of drum is indicated by P-43 through P-42, and the drum channel is indicated by P-41 through P-34. On tape: The direction of motion of the tape unit, forward (0) or reverse (1), is indicated by P-43. The running distance in this direction is indicated by P-42 through P-38. The number of the tape unit is indicated by P-37 through P-34.
P-33 through P-22	Beta	Indicates the final address in the high-speed memory to (or from) which information is to be transferred.
P-21 through P-10	Gamma	Indicates the initial address in the high-speed memory to (or from) which information is to be transferred.
P-9	a-digit	Indicates program-jump: (If a program jump is desired after completion of the input-output operation, P-9 is a 1; if no such jump is desired, P-9 is a 0.)
P-8 through P-7	b, c-digit	Indicates whether beta and gamma are relative or absolute.
P-6	d-digit	Indicates counter containing address of next instruction.
P-5 through P-2	Operation symbol	Contains code symbol for input-output operation, (0).
P-1	Monitor signal	See section 7.6.

Concurrent regulation interlocks. As mentioned previously, automatic interlocks are provided as safeguards against inadvertent attempts to use a given memory location for two inconsistent purposes. For example, after initiating a Load operation the machine is not allowed to read from or write into any memory location affected by the Load instruction until the pending memory-loading operation has taken place in that particular location. Similarly, after a Print instruction has been given, the machine is not permitted to write into any location affected by the print-out order until the word in that location has been printed out. Whenever necessary, these automatic interlocks temporarily

halt the computing program, but only for the minimum time needed to insure that these conditions are fulfilled. For example, if an instruction specifies that memory addresses 000 through 500 be loaded and that the next instruction be taken from address 010, the program will proceed to the next instruction immediately after address 010 has been loaded, even though the remaining 490 words have not yet been entered into the other memory locations. The interlock will be called into play again only in the event that premature reference to any other of the first 501 words is attempted.

Automatic interlocks are also provided against the contingency that the program calls for an additional input-output operation before a previously ordered input-output operation has been completed. In this event, the program halts temporarily, waits until the preceding operation is completed, and then proceeds in the usual fashion to carry out the second instruction.

Program-jumping feature. For many applications which make use of concurrent loading or printing out of the high-speed memory while computations are proceeding, the precise length of time required to complete the input-output operation is either indeterminate or else quite difficult to predict. A typical example of an instance of this type occurs when it is necessary to hunt for a particular word or group of words located in an unknown location on a long magnetic tape reel—where a word can be identified as one of the desired type only after it has been read into the computer and subjected to an analysis of its characteristics. Since efficiency requires that information be read into the high-speed memory in fairly large blocks, it is desirable (while the comparatively slow procedure of reading-in the information is taking place) to make use of the ability of the system to proceed on other independent phases of the program. By means of the special input-output program-jumping feature, the programmer is able to direct that these other concurrent independent phases of the program be allowed to proceed uninterrupted until the specified loading operation shall have been completed, and that, as soon as the loading is completed, the program shall jump to an alternative specified routine which is designed to carry out the identification analysis upon the newly received information and to decide whether to retain it or to continue hunting on the tape.

Program jumps of this sort are directed by means of the P-6 and P-9 digits in the instruction word. More explicitly, the P-6 digit (d-digit) of each instruction word specifies the counter-register (No. 0 or No. 1) which contains the address of the instruction to be executed immediately after completion of the current instruction. If the d-digit is 0, the address of the next instruction is contained in counter No. 0; if the d-digit is 1, the source of the next instruction is contained in counter No. 1. When the current instruction is an input-output order (which generally specifies a lengthy external operation) and the programmer desires, prior to its completion, to proceed with the next instruction and other internal operations which can be carried out while the lengthy external operation is being executed, then the P-9 digit (a-digit) of the current instruction word is written equal to 1. In effect the programmer, at the time that he orders the input-output unit to perform a specified task, this includes in the order a request for the production of a signal when the task is completed. This signal, received from the input-output control, causes the program to jump; i.e., the counter register then being used as the source of the next instruction is temporarily abandoned, and the instruction word in the address location stored in the *other* counter register is executed in its stead.

TABLE 11. Summary of program-jump rules

Input-output instruction	Source of immediate next instruction	Source of next instruction after input-output operation is completed
d-digit equals 0 and a-digit equals 1	Counter No. 0	Counter No. 1.
d-digit equals 1 and a-digit equals 1	Counter No. 1	Counter No. 0.
If the a-digit equals 0, no program jump occurs, and after completion of the input-output operation the next instruction is selected in the usual way by the instruction word being executed at that time.		

After effecting a program jump, the new program that is initiated by the substitute instruction may, if the programmer so desires, be written with a constant d-digit in all of the instructions except the final one. As a result, as soon as the final instruction is executed, the program will return to the instruction located in the memory address stored in the temporarily abandoned counter-register and resume the interrupted program where it left off. It should be noted that the programmer need make no provision for explicitly recording or determining the address at which the interrupted program is to be resumed. This address will automatically be held unchanged in the temporarily abandoned counter-register.

After the program has encountered an input-output instruction with the a-digit equal to 1 (which, in effect, indicates that the programmer wishes to preserve the address in the control counter-register for future reference), any premature attempt to alter the contents of this register by means of a counter resetting instruction (or any instruction whose d-digit specifies the reserved counter) will result in the program being halted temporarily until the input-output operation in question has been completed and the originally directed program-jump is ready to be made. This automatic interlock relieves the programmer of the burden of having to estimate precisely how long a time will be required for the input-output operation to be completed and insures that all the desired steps in the program will be carried out in their proper sequence. The system is so designed that the order which appears first in the program must be satisfied before any subsequent conflicting order can be carried out.

7.6. Manual-Monitor Operations

Under the general heading of *manual-monitor operations* are included all those operations which are either initiated manually by the machine operator, who for example, presses a push-button, or are initiated by the program itself under conditions which are specified by means of external switch settings. The former is called a manual operation, and the latter is referred to as a monitor operation because the machine must monitor its internal program to determine precisely when the operation should be performed. In both cases, the exact nature of the operation to be performed and the storage places to be involved are specified by means of external switch settings.

Types of Manual-monitor operations. The types of manual-monitor operations which may be performed fall into five main classes, namely, (1) loading operations, which load new information into specified portions of the machine such as various memory locations and storage registers, (2) print-out operations, which print out the contents of these storage locations inside the machine, (3) insert-in-the-program operations, in which a new instruction is interpolated into the internal program between the items of the programmed instruction sequence, (4) change-in-the-program operations, in which a new sequence of instructions is substituted for the scheduled instruction sequence, and (5) halt-the-program orders, with warning signal. A list of the various storage locations inside the machine to which some or all of these types of manual-monitor operations may be made to pertain is indicated in table 12.

TABLE 12. Storage location directly accessible by means of manual-monitor operations

Memory locations
1. Address 000.
2. Addresses 000 through 007, inclusive.
3. Addresses 000 through 00F, inclusive.
4. Addresses 000 through 017, inclusive.
5. Addresses 000 through 01F, inclusive.
6. Addresses 000 through end,[a] inclusive.
7. Address alpha indicated in the current instruction word.
8. Address beta indicated in the current instruction word.
9. Address gamma indicated in the current instruction word.
10. Address scheduled for next reference by the current instruction word.
11. Address stored in Counter-register No. 0.

[a] "end" denotes largest available address number in memory.

TABLE 12. Storage locations directly accessible by means of manual-monitor operations—Con.

Memory locations—Con.
12. Address stored in Counter-Register No. 1.
13. Address stored in Address Storage Register (ASR).[b]
14.- 20. Similar to items 7 through 13 above, except that all eight addresses in the tank in which the indicated word is located are included.
21. Addresses 000 through ASR.
22. Addresses ASR through end, inclusive.
23. Addresses ASR through 007, inclusive.
24. Addresses ASR through 00F, inclusive.
25. Addresses ASR through 017, inclusive.
26. Addresses ASR through 01F, inclusive.
Storage Registers
27. Instruction Register.
28. Arithmetic Accumulator Register.
29. Counter-Register No. 0.
30. Counter-Register No. 1.
31. Address Storage Register (ASR).

[b] ASR denotes the address number stored in the Address Storage Register.

Conditions for initiating monitor operations. Monitor operations are performed by the machine whenever the conditions specified by the external switch settings occur in the course of the internal program. These conditions can be chosen from among a wide variety of program occurrences. For example, the operator may indicate that the monitor process is to be initiated by any one or more of the following conditions:

1. Every time the program refers to a new instruction.
2. Every time the program makes a reference to the memory.
3. Any time the program refers to an instruction to which a negative sign (P-1 equal to 1) is attached.
4. Any time the program refers to a Comparison instruction which results in the selection of the normal consecutive next instruction.
5. Any time the program refers to a Comparison instruction which results in the selection of the jump alternative next instruction stored in address gamma.
6. Any time the program refers to an address which exactly matches the 12-binary-digit address number stored in the special Address Storage Register (ASR) provided for this purpose.
7. The same as item 6, except that only the nine most significant digits are matched.
8. Any time the program refers to an address lying within some indicated one (or more) of the eight possible memory cabinets.
9. Any time a memory-error indication appears (see section 7.2.).
10. Any time an overflow occurs as the result of an Accumulate-and-Overflow-Check instruction.
11. Various other special conditions.

It will be noted that item 8 permits the three left-hand binary digits of each address to be used as special code keys that signify the various classes of occasions on which a monitor operation might be desired. This feature is still applicable even if the full 4,096-word complement of memory locations is not actually provided. For example, if only a single 512-word cabinet of memory is in operation, these code digits are capable of expressing seven classes of automonitor-initiating conditions.

Applications of manual-monitor system. Under section 7.4. describing the Breakpoint File operation, it was noted that the initiation of automonitoring routines could be controlled by means of the external switch which is provided for activating Breakpoint File instructions, provided such instructions had been inserted in the program in the proper strategic places. In the event that these Breakpoint File instructions have not been inserted in the program, the third type of monitor

operation (insert-in-the-program) can be used for the same purpose. For example, one of the possible operations of this type can interpolate the word in address 000 as the next instruction in place of the scheduled next instruction in the program, without in any way altering any counter resetting or other operations which the preceding instruction had caused to be carried out. The word in address 000 would be chosen so as to cause the contents of the counter-registers to be filed in designated memory locations and would then initiate a prepared program of automonitor analysis. (This program might, for example, include printing out the address of the instruction previously executed, the instruction word itself, various of the operands, or the result of the instruction. The initiation of this program could be made dependent upon conditions involving the type of instruction, the characteristics of the addresses involved, or the operands themselves. When the desired information has been printed out, the program would cause the control to be reset to the condition that had existed before the automonitor routine was started and would cuase the next regularly scheduled instruction to be selected.

Among other simpler operations which can easily be performed, the following may be noted: Various fixed addresses or groups of fixed addresses may be continually printed out even while the computation is proceeding. Since these operations are initiated by means of external switches which control only d-c voltages, operations of this type might well be initiated by mechanical devices remote from the computer itself. In other words, these remote external devices can direct that various sections of the computer's memory be made available to them. Similarly, they can direct that various sections of the computer's memory be loaded. Thus the computer can be said to share its high-speed memory (and consequently any other part of its internal computing or external storage facilities) with these remote devices, at the option of either the external devices or the computation program, or both, jointly.

7.7. Summary

As the foregoing outline of the DYSEAC system has shown, this machine is capable of carrying out (1) a balanced set of internal arithmetic and program-control operations, (2) a group of external input-output operations which can proceed simultaneously with the internal computing operations and, at the option of the programmer, can be automatically interlocked with them in such a way as to intermesh the sequencing of internal and external operations, and (3) an extended repertoire of manual and monitoring operations by means of which a wide variety of special input-output or program-branching operations may be interpolated at any time into the previously prepared program instructions. These latter two features, acting in concert, make the internal storage facilities of the machine available to the outside world without appreciably interfering with the internal computations; also they permit unscheduled interchanges of data and program information to take place between the machine and the outside world at the instigation of either, independently, or of both, cooperatively. This communication between the machine and the outside can be readily maintained whether the outside communicant is another automatic device or a human operator.

4. System Design of the SEAC and DYSEAC

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1. INTRODUCTION

In the course of developing comprehensive system plans for the SEAC and DYSEAC, certain standard methods and procedures were evolved for producing a large-scale system design. These standard procedures, including first the development of system specifications, then the development of functional plans, and finally the development of wiring plans, are described in this paper. Some of the problems encountered in formulating the specifications and system plans are also discussed [1][1].

The flow of development generally followed in creating such large-scale computers is charted in figure 4.1. As indicated, two sets of factors (which can be considered as the initial boundary conditions of the system-design problem) affect the choice of system features for a machine: first, the set of factors related to the intended use of the machine, and second, those related to the type of components or "building blocks" with which the machine is to be constructed. Because these two sets of factors are basically unrelated to each other, they often present contradictory requirements. For example, a proposed machine feature may appear ideal when evaluated solely in terms of the intended use of the machine but may entail an unacceptable engineering risk when evaluated in terms of component reliability and cost. The necessity for effecting compromises and avoiding conflicts of this kind between the rival claims of operational effectiveness and engineering reliability and economy strongly influenced the system designs of the SEAC and DYSEAC.

As is also indicated in figure 4.1, the principal machine components whose properties profoundly influenced the system design of these computers were the internal memory units, the external communication units, and the internal switching and small-scale storage circuitry. The internal memory units included an acoustic delay-line memory and an electrostatic Williams' tube memory. The external communication units included such devices as mechanical keyboard-printers, magnetic recording units, special cathode ray tube display devices, input converters for translating analog information to digital form, and digitally-actuated output mechanisms. The internal high-speed switching and storage circuitry included the following fundamental digital elements for controlling pulse signals: (1) The *and-gate*, with or without an inhibition input, and the *or-gate* were the fundamental elements utilized for combining or switching pulse signals. Groups of these gates are assembled with an amplifying tube and pulse transformer to make a *pulse repeater*. This pulse repeater carries out the logical switching functions of the gates included in it and also amplifies and restandardizes the signals going through it. (2) The so-called *dynamic flip-flop* was the fundamental bistable device utilized for providing one-bit storage. This device is composed of a pulse repeater and a *delay line* connected to form a closed loop around which a single pulse can be kept circulating repeatedly with a recirculation period of exactly one pulse-repetition cycle.

These elements were used uniformly throughout the SEAC and DYSEAC both for word generation and for central functional control purposes. No other basic elements were used in the internal system. In figure 4.2, items 1 through 6 illustrate these fundamental elements and the symbols adopted for representing them. Table 3 explains their mode of operation.

From these basic elements, small composite units were developed for carrying out typical simple processing operations according to the rules of binary arithmetic. For example, comparators, counters, decoders, complementers, adders, storage and shifting registers were developed. Such units are illustrated in figure 4.2, items 7 through 16. Using these small composite units, larger subsystems were then organized for carrying out more complex arithmetic and control operations such as the arithmetic operations of multiplication and division, or the control operation of selecting

[1] Figures in brackets indicate the literature references on page 92.

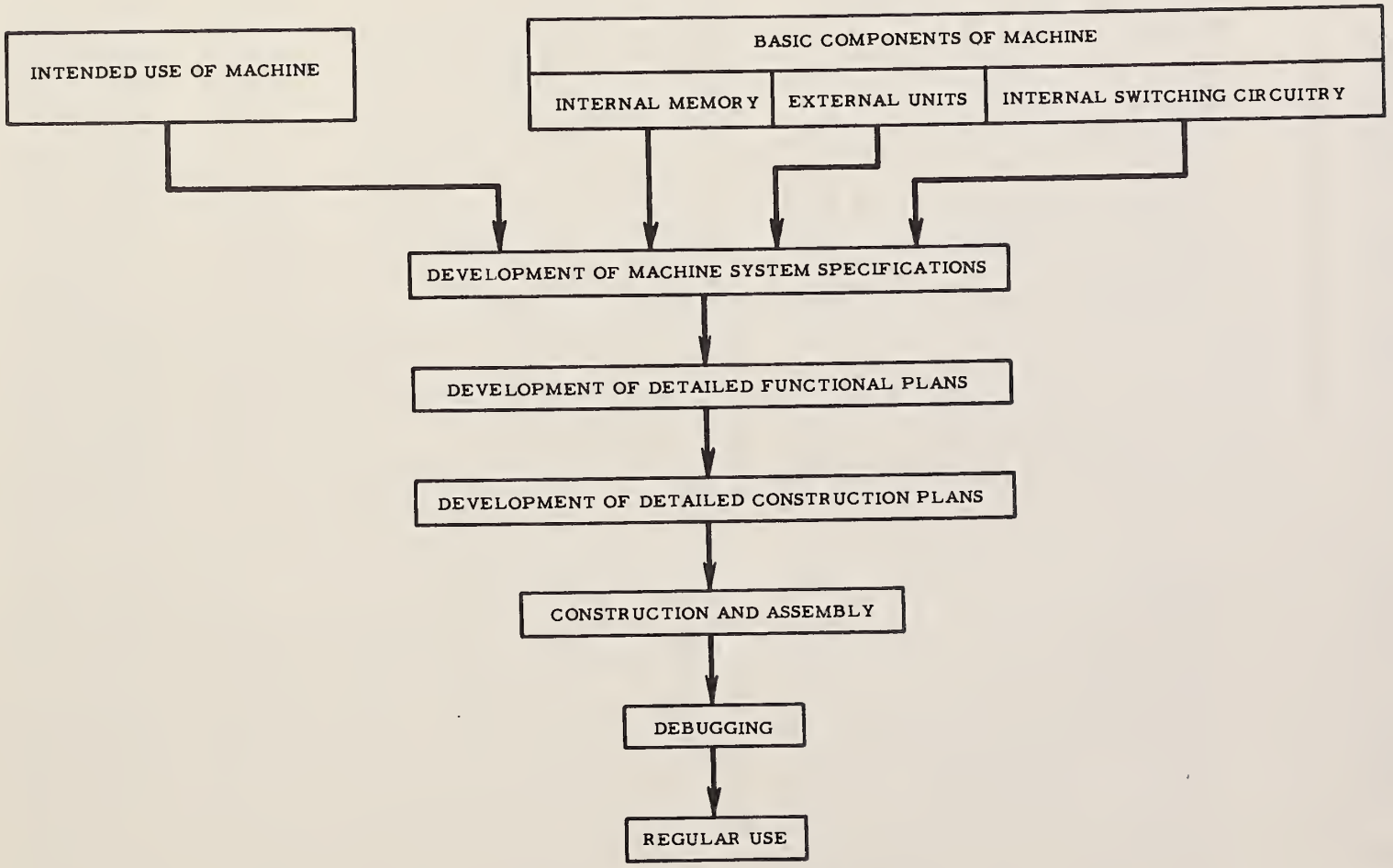

FIGURE 4.1. *Computer development flow chart.*

a word from a designated memory location. Table 4 lists some typical operations for which such subsystems were developed.

These composite units and subsystems provided a set of basic techniques by means of which computations could be performed on digital data and complex procedures could be employed for integrating large masses of unorganized information. Once devised, they served as a storehouse of building blocks and organization schemes from which more comprehensive full-scale systems could be developed. In this way, they provided the means for fashioning automatic supervisory control facilities capable of directing large families of external devices carrying out complex tasks.

2. DEVELOPMENT OF SYSTEM SPECIFICATIONS

In developing system specifications for the SEAC and DYSEAC, an effort was made to specify a balanced system in which each component part was organized to do only what it needed to do and no more. Such a system usually contains the fewest possible parts and consequently is more economical to construct, debug, and maintain. As the characteristics of the principal memory, switching, and external communication units to be incorporated into the system were widely varied, the problem of achieving an effective balance between these units arose. A major boundary condition to the problem was imposed by the engineering decision to use a mercury acoustic delay-line memory for high-speed storage. The access speed characteristic of this type of memory governed the choice of computing speeds for the switching units and input-output speeds for the external communication units. More specifically, a purely serial arithmetic unit was chosen instead of (for example) a serial-parallel or fully parallel unit because in the acoustic memory the recirculation period of 384 μsec for an 8-word recirculating tank increases the time required to read a word into or out of the memory by seven-sixteenths of this period, on the average, which is 168 μsec. For the four references to the memory required in most SEAC and DYSEAC arithmetic operations, this lengthens the time needed to execute an operation by 672 μsec. As the actual basic computing time required to carry out the four sequential steps of a complete addition operation, using simple and efficient serial techniques, is only 192 μsec, obviously not much over-all gain in speed would be achieved by reducing the arithmetic computing time unless a corresponding reduction could be effected in the memory access time. Table 1 shows the average times for execution of the various types of arithmetic operations performed by SEAC and DYSEAC and the portion of these times occupied by memory access waits.

TABLE 1. Average rates for certain SEAC and DYSEAC operations

Operation	Performance rate in SEAC	Performance rate in DYSEAC	Percentage of time occupied by memory access waits
	msec	*msec*	%
Addition, subtraction, logical transfer	0.9	0.9	78
Multiplication, division	3.0	3.0	23
Comparison	0.7	0.7	72
Shift (half-word shift)	----------	1.1	61
Justify (half-word shift)	----------	2.0	33
Summation (per word, for 100 words)	----------	0.06	12

From this table it will be noted that addition times and multiplication times are the same for DYSEAC as for SEAC—the speed ratio being about 3:1 for executing these operations. If, as is the case in many computational problems, additions occur about three times as often as multiplications, the speed-up achieved in the over-all execution time of a problem by striking out a given percentage of the operations in the program is the same regardless of whether the operations eliminated are additions or multiplications or a mixture of both. In this rough sense, the speed ratios may be said to be balanced. Actually, the occurrence of multiplication in solving a problem on DYSEAC will be rather less than with SEAC because of the newly added high-speed Shift and Justify operations by which many procedures requiring one complete multiplication time with SEAC can be done much more rapidly with DYSEAC.

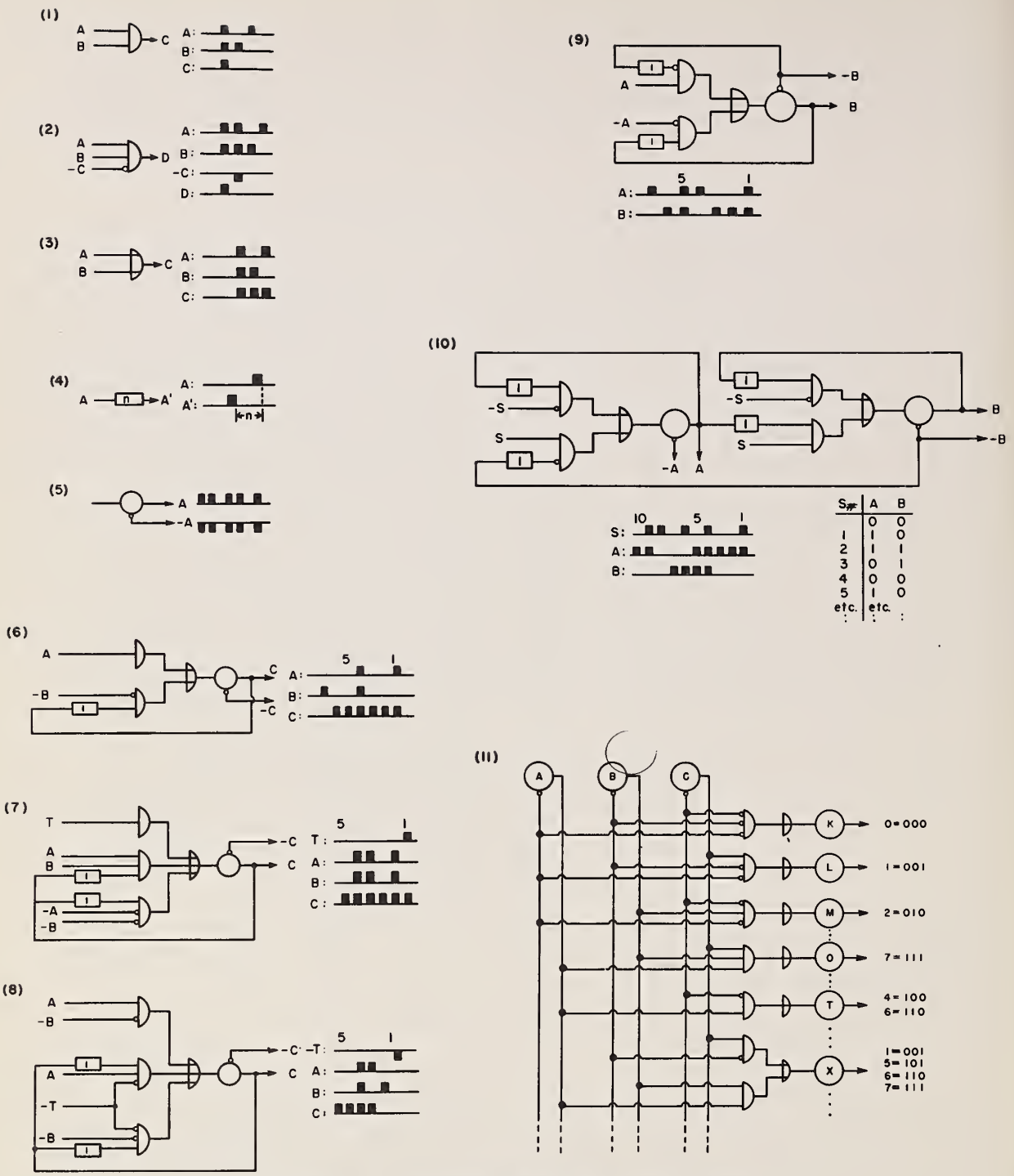

FIGURE 4.2. *Fundamental elements for computer systems.*
(See table 3 for explanation)

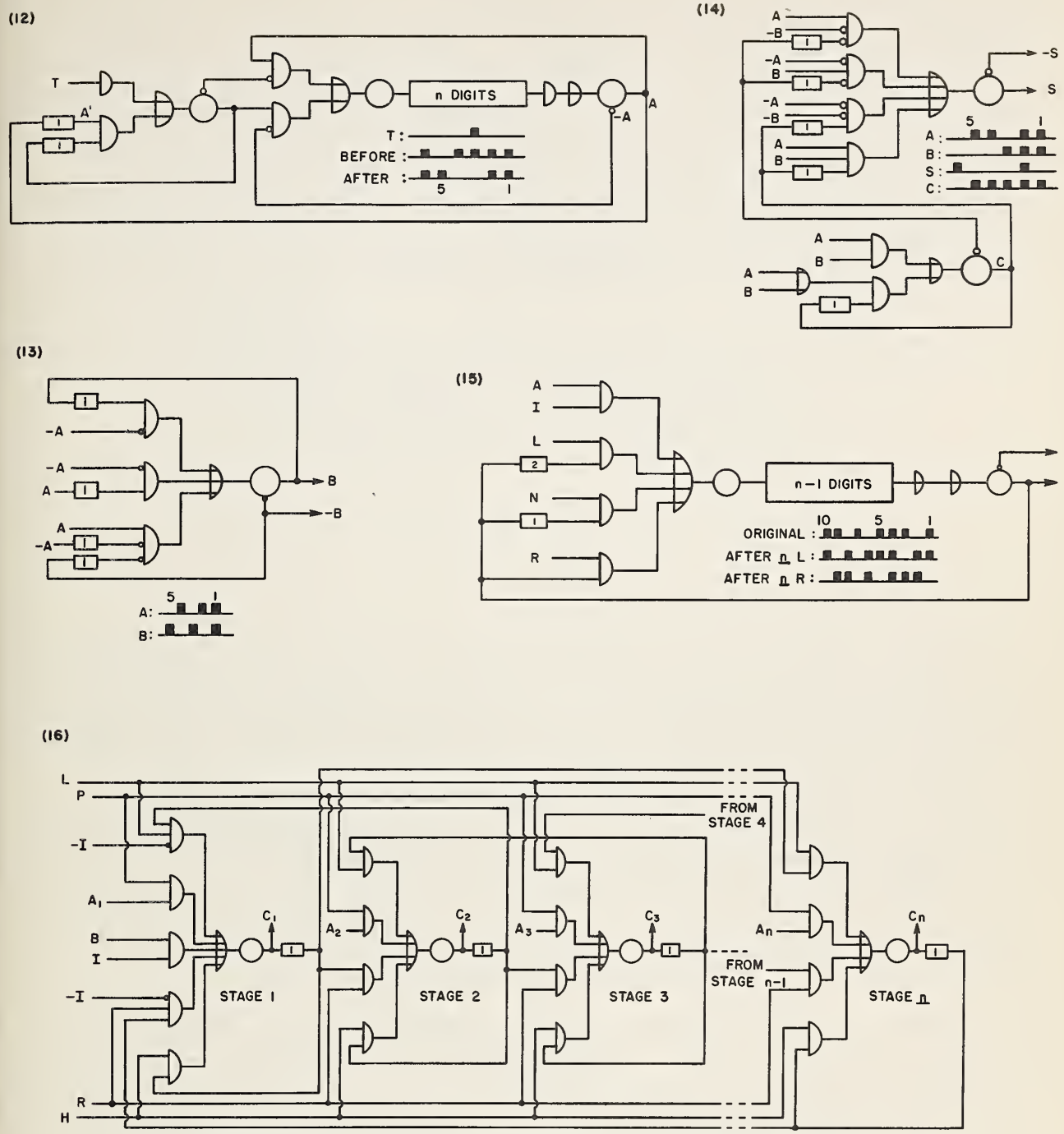

FIGURE 4.2. *Fundamental elements for computer systems*—Continued
(See table 3 for explanation)

Turning now to the balance between computing rates and input-output rates, table 2 shows the time required to transfer a word between the high-speed memory and an external unit operating at the pulse-repetition rates associated with conventional magnetic recording units. As the time required to execute an average instruction is of the order of a msec, it takes four to six times as long to transfer a given instruction word from a typical external magnetic unit into the high-speed memory as it takes to execute it after it has been stored within the machine. Ordinarily, associated with each instruction there are from one to four words of input-output, namely, at least the instruction word itself and possibly any or all of the operands and the result. Therefore, the total input-output time required to transmit these data in and out of the machine would not ordinarily be greater than roughly two dozen instruction-execution times. If each instruction is executed about this many times after it has been inserted into the machine, then the internal processing and external transfers will, in the long run, occupy roughly the same amount of time. In the case of DYSEAC, where computing and input-output transfers can proceed concurrently, the over-all time taken to solve a problem will be equal to the time required for the longer of these two processes.

TABLE 2. Rates for input-output operations with magnetic recording units, averaged over 512 words

Pulse rate of external wire or tape unit	Time to transfer one word between external unit and DYSEAC memory
kc	*msec*
4	12.8
8	6.8
12	4.8
16	3.8

It appears, therefore, that for a high-speed memory of the present acoustic delay line type, little benefit would accrue from increasing these input-output rates unless the problem being solved involves extensive hunting along the wire or tape in search of particular words. If the nature of the application requires such hunting procedures, then a better-balanced system could be obtained by increasing the over-all input-output rate in direct proportion to the average number of words which must be searched through in order to find a desired word.

Other major problems were encountered in formulating system specifications for the SEAC. On the one hand these specifications had to be kept to a minimum so that the machine could be completed at the earliest possible date for interim use; and on the other hand the specifications had to include provision for expanding this interim machine, both internally and externally, by the annexation of advanced high-speed internal memory equipment and external input-output equipment as they became available. Neither the developmental time-scale nor the operating properties of these new components could be precisely defined at the time the specifications had to be drawn up. Furthermore, the future uses of the machine could not be precisely defined either.

Fortunately, at the time the development of the DYSEAC was undertaken the situation was quite different. Even though the range of application and method of use intended for the DYSEAC are broader and more varied than for SEAC, it was possible to define them more precisely at the start of the program. Consequently the DYSEAC system could be organized more effectively than the SEAC; and though both machines contain the same relative proportions of equipment for carrying out communication, control, and processing functions (see fig. 4.3) the DYSEAC is able to provide considerably more powerful operating features using the same amount of equipment. These operating features and their relation to the intended use of the machine are described in the DYSEAC article.

After the problems related to the intended uses of the machines and to the operating characteristics of the principal component parts had been defined and evaluated, and before the final system specifications were formulated, several other analytical studies were carried out. For example, coding studies were conducted to determine optimum internal programming specifications, i.e., what the format and content of the number and instruction words should be, what the program-sequencing procedures should be, what arithmetic and control operations should be included in the system, and other related questions. As a result of such studies, the approximate number of instructions and

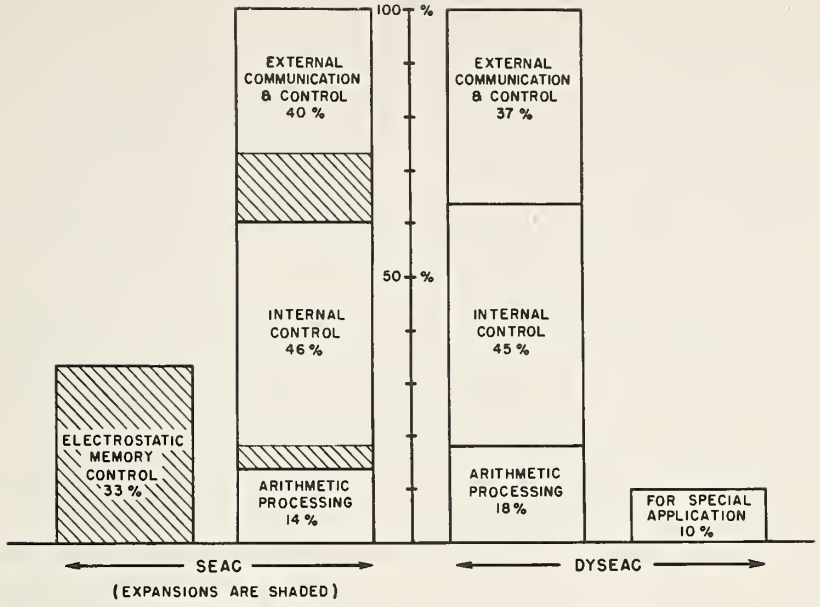

FIGURE 4.3. *Proportion of equipment for performing major functions in SEAC and DYSEAC systems.*

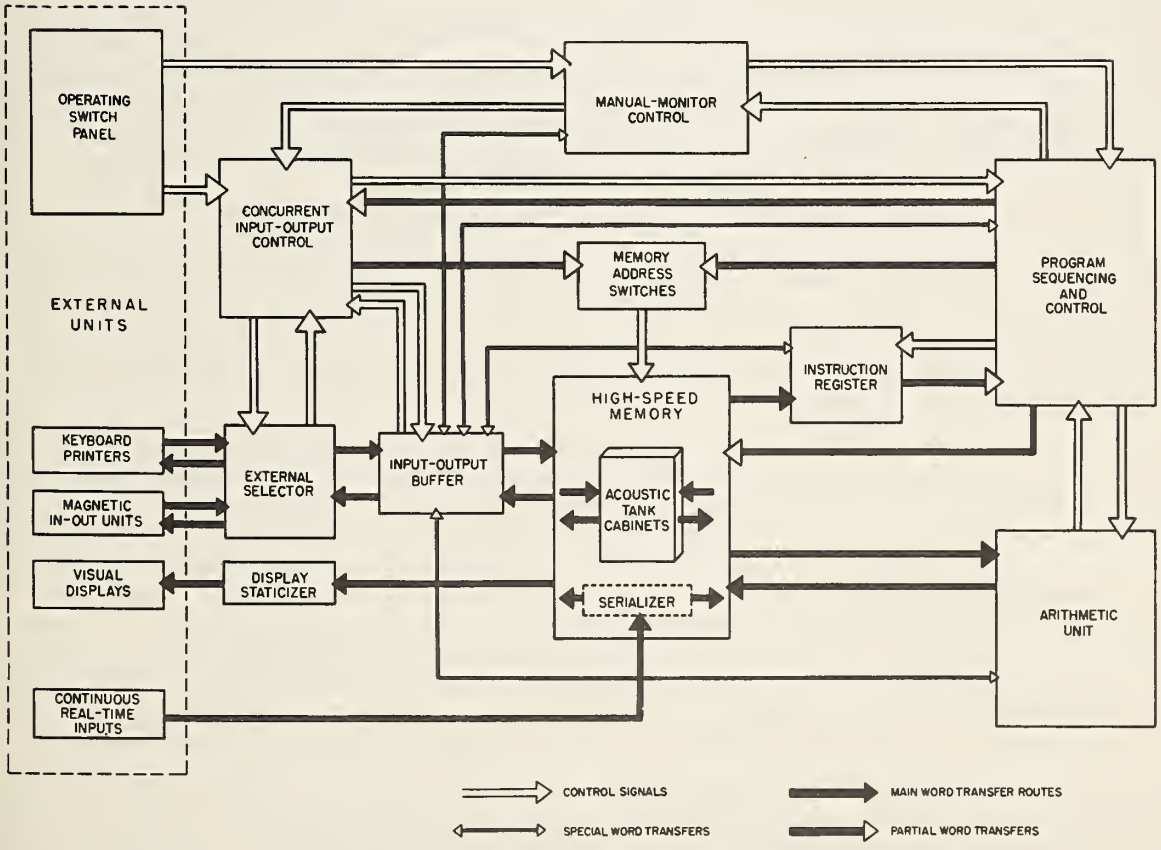

FIGURE 4.4. *Block diagram of DYSEAC.*

memory cells needed for solving various problems can be established, as well as the frequency of access to various classes of words, over-all solution times, etc. These data are in turn useful for carrying out further analyses aimed at determining the relationship between the problem-solving capacity of the system and the equipment cost. For example, by relating the unit cost and access time of various types of storage equipment with the relative frequency of use of the various classes of words involved in the program, the most economical choice of proportions for each type of storage device needed to perform the problem at a given over-all speed can be determined.

It should be noted that a strong interdependence exists between decisions made as a result of these various considerations. In designing SEAC, for example, the decision to provide for the incorporation of an additional parallel memory as well as the initial serial memory exerted a profound effect on the design of two apparently unrelated parts of the system, namely, the input-output buffering system and the program-sequencing system. The parallel memory was coupled to the otherwise serial machine by means of a staticizing shift register capable of communicating with the parallel memory in a simultaneous broadside fashion from all of its register cells and with the serial units in a step-by-step serial fashion through a single register cell. The flexible serial-parallel conversion abilities of this device together with its ability to operate over a wide range of shift speeds led to its adoption as the input-output pick-up register for the system [2]. On the other hand, the DYSEAC, which does not require this sort of facility for staticizing information, uses the more economical circulating electrical delay-line storage technique for its pick-up register. This register, although purely serial in operation, can be loaded with up to 45 binary digits delivered from an external input device via 45 distinct channels in a broadside fashion.

A second effect of the decision to provide for a parallel memory on SEAC relates to the program-sequencing system. Initially, the memory capacity of the machine was less than 1,024 words, and therefore address numbers of 10 bits each were adequate. Hence, an instruction word containing four addresses of 10 bits each could be used. When it became necessary to provide for expansion of the initial memory capacity up to as much as 4,096 words, extra space was needed in the instruction word to represent numbers in excess of 1,024. To make room for the longer address code designation, therefore, without extending the length of the instruction word, a three-address instruction word of 12 bits per address was adopted as an optional alternative to the four-address instruction word. Along with this three-address designation, a consecutive-number scheme for sequencing instructions was used. This scheme in turn facilitated the adoption of a floating relative-address scheme for program sequencing [3]. These examples illustrate how design decisions affecting a single unit of the system were propagated and made themselves felt throughout the remainder of the system.

3. DEVELOPMENT OF DETAILED FUNCTIONAL PLANS

The previous decisions defining the over-all system specifications for the computer to a great extent implicitly determined the general nature of the over-all blocks or major units in the system as well as their control inter-relationships and principal information-transfer routes. At this stage of development, the system is usually represented by the familiar block diagram composed of simple labelled boxes interconnected by means of directional lines (see fig. 4.4).

The next step in the evolution of the system design was to break each of these large blocks into smaller blocks, according to the functions suggested by the general operating specifications. For example, an arithmetic unit might be broken into boxes representing an adder and some storage registers whose number and characteristics depended on the operating specifications. A control unit might be broken into boxes representing subunits whose functions are, for example, the selection, acquisition, and distribution of information from the memory to other parts of the computer, or the issuing of control signals to the arithmetic unit that direct it through certain motions that are required in order to perform a given arithmetic operation. At this stage of development, definite rules regarding the cause-effect relationships among all the basic units became fixed. Also, the time delays imposed by the information processing, that is, the speeds at which signals can make their way through the various blocks, had to be estimated and upper and lower limits specified.

Because the system being designed was centrally synchronous, over-all timing considerations now came to the fore. To use a rough analogy, all the units and subunits had to be so designed that they could be geared together and perfectly meshed. The next step, therefore, was to investigate and specify definitively the exact timing inter-relationships which must exist among all of the

major units in order to insure that transfer of data and control signals among them can take place in proper sequence. This step is necessary in order to force the *time* sequence of the passage of signals from one unit to the next to correspond to the desired *cause-effect* sequence through which the units are functionally related to each other. This process is sometimes referred to as "closing the timing loops." For example, with a synchronous machine using a circulating delay line memory, one of the major timing loops to be closed is the so-called memory-to-arithmetic-unit-to-memory loop. Closing this loop means establishing that a pulse read out of a memory location into the arithmetic unit can pass through the arithmetic unit and arrive back at the memory in time to be rewritten into the memory at exactly the proper instant. The proper instant for this rewriting is determined by the requirement that, when the pulse is read out of the memory at a later time, it will emerge from the memory at an instant which is precisely an integral number of word-transfer cycles after the instant at which it emerged on the previous occasion.

Once the major timing loops were closed, it became possible to establish a fixed over-all timing schedule for the system as a whole. That is to say, a definitive pulse-time "time-table" was adopted for most of the major units which communicate with each other and for the over-all timing-pulse generators whose functions are to furnish signals commonly used by all the other units. From this point on, every remaining unit and subunit in the system had to be so designed that it would be capable of performing its functions entirely within the confines of the fixed time schedules adopted for the over-all timing signals.

It is advantageous to establish these fixed over-all time schedules at an early stage of the design program, because this facilitates dividing up the detailed work on the various major units among a team of several designers. So long as each designer adheres to the established timing "boundary conditions," the detailed design of each unit can be carried ahead separately with less fear of drastic reaction from developments in the design of other units. This sharing of design responsibility is feasible, however, only if the timing schedules are fixed at the outset and left unchanged.

In carrying ahead the design of each unit and subunit, the next step was to convert the logical cause-effect relationships which must exist within and among the various subunits into space-time relationships. The cause-effect relationships may be expressed by well-known algorithms for the case of an arithmetic unit, while for a control unit the description of the relationships may take the form of specially devised tables of procedural rules and process flow diagrams. Whatever their form, these cause-effect relationships may be reduced to stylized logical statements; for this purpose the notation of Boolean algebra often provides a convenient shorthand. In order to convert the cause-effect relationships to space-time relationships it was necessary, first, to select fundamental building blocks capable of executing the required functional relationships on incoming pulse signals, and, second, to determine the proper time at which these signals should be transmitted between the individual input and outputs of each building block.

This work was carried out with the aid of *process block diagrams*, an example of which is shown in figure 4.5. These diagrams consist mainly of simple inter-connected rectangular blocks labelled with descriptive titles designating the general logical relationships that they bear toward each other. Each block represents a specific type of subunit drawn from a list of semistandardized prototype units designed to perform various common functions. Typical examples of such units are the comparators, counters, adders, registers, etc., described in the Introduction. From this collection of prototypes, a functional unit specially suited to any particular situation could usually be devised merely by making simple modifications of the standard prototype model.

The manner in which each building block fitted into a unit to perform its system function was further specified by prescribing the times at which it was to be turned on or off by each connected clock. At first, the entire unit was laid out in blocks with timing signals indicated only approximately. As the design process proceeded, the necessary timing specifications became more precisely definable, and the specific timing pulses and exact delay-line lengths needed in order to insure proper time meshing of all the gating stages could be specified.

The next step, which overlapped the previous one to some extent, was to prepare so-called *functional diagrams*, using the symbols illustrated in items 1 through 5 of figure 4.2. Although basically only five varieties are used, these are sufficient to determine implicitly every physical component of the machine. The internal details of each block on the process block diagrams were worked

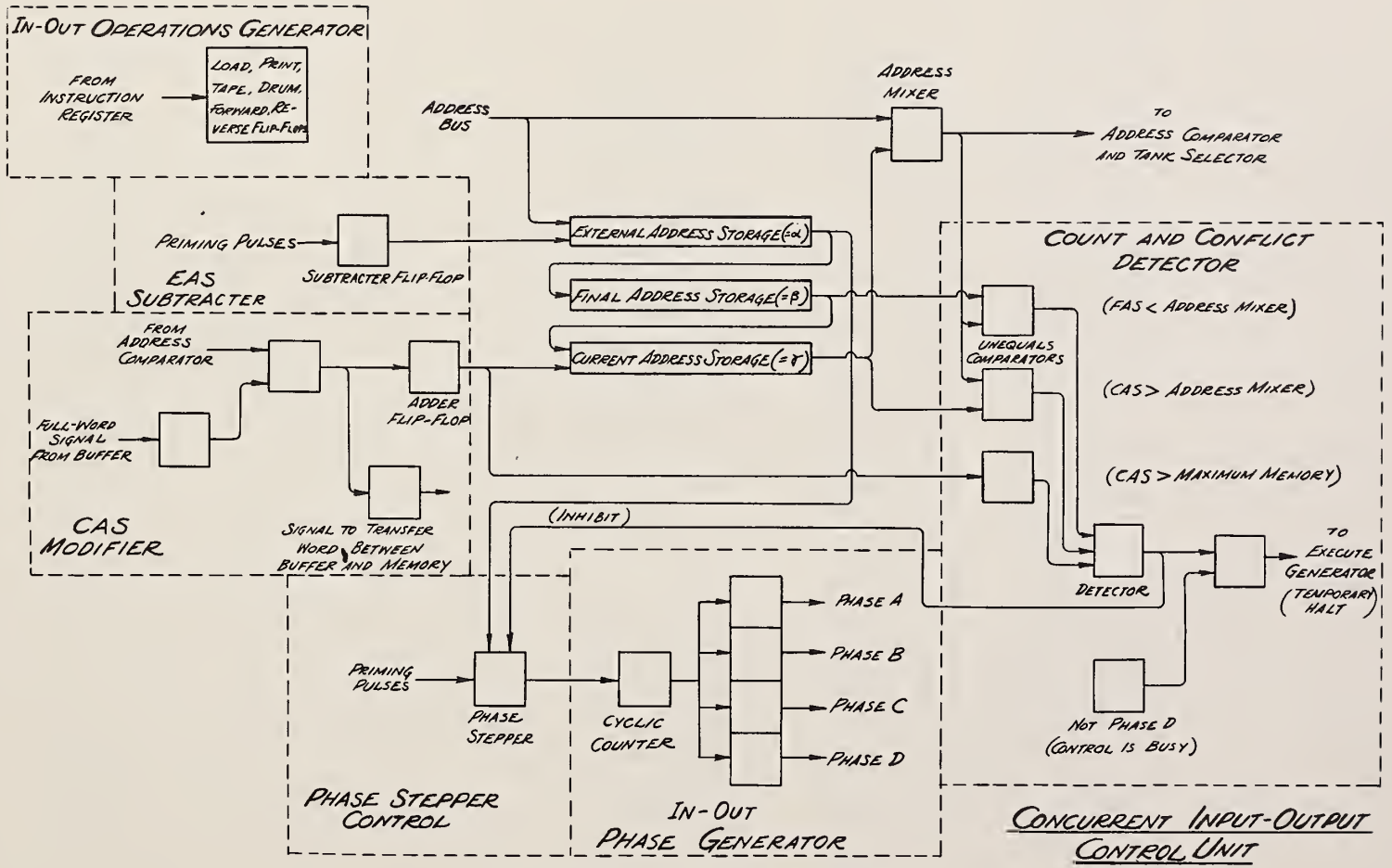

FIGURE 4.5. *Example of a process block diagram.*

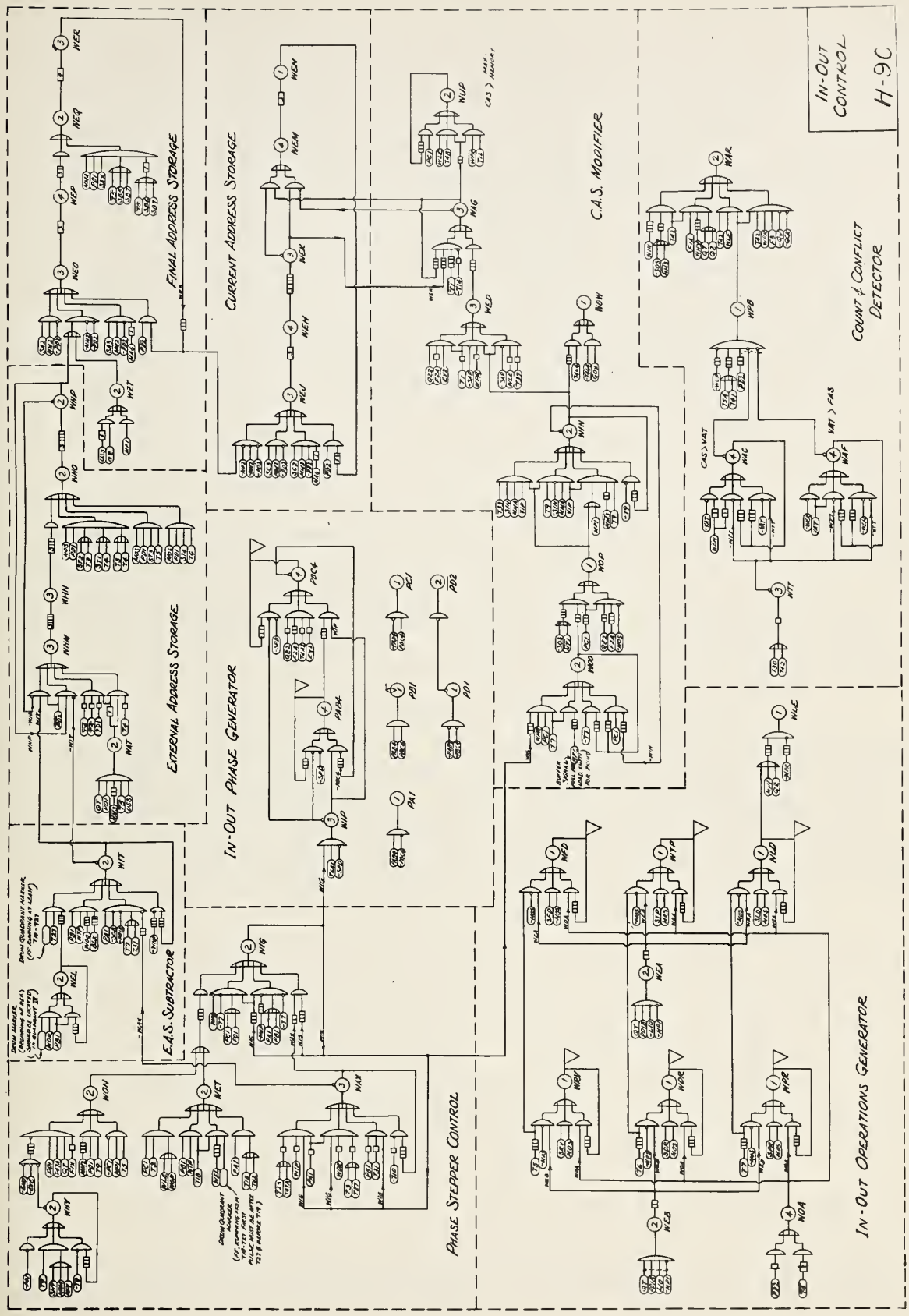

FIGURE 4.6. *Example of a functional diagram.*

out in terms of these symbols and recorded on the functional diagrams (see fig. 4.6). As noted above, this procedure consisted largely of expanding, modifying, and combining these fundamental elements so as to fit them to the special case at hand. The manipulative techniques of Boolean algebra were occasionally found helpful at this point for reducing gating configurations to standard form or for checking the equivalence of alternative circuit arrangements. Each tube stage was assigned a unique designation (usually a three-letter symbol), which serves to identify the signals that the stage emits. As the stages became meshed together, numbers specifying the entry and exit times of the signals for each gate, delay line, and tube were recorded. In designing SEAC, tolerances on these quantities were calculated nominally to the nearest 0.01 μsec. With DYSEAC, however, because all components were standardized, it was sufficiently precise to record the timing on the functional diagram only to the nearest nominal quarter of a microsecond.

In the process of preparing the functional design, an effort was made to minimize the number of components utilized, particularly with respect to tubes, next with respect to delay lines, and finally with respect to diodes. The choice of the most economical and efficient arrangement for the functional elements depended quite strongly, however, on such factors as the size and content of the physical packages into which the electronic components are grouped and on their electronic operating specifications. Factors which affected the choice of optimum forms on the functional layouts were, for example, (1) the maximum permissible stray capacitance that is introduced as a result of extended lead lengths, and (2) the limitations on the maximum load that can be drawn from a tube. Functional layouts, therefore, even though they depict no electronic components explicitly, still must be designed with careful regard for the specific physical components by which they are later to be realized.

Another type of interaction between successive stages of the development program may occur after the functional design is partially or even fully completed. At this stage the designer may find that the operating capabilities of the machine can be usefully expanded by making minor design rearrangements which team up the same facilities in new combinations. In this way, additional operating features can often be provided at little or no additional equipment cost. This feedback from functional design to system specifications can produce significant over-all improvements when close coordination is maintained between the two activities.

4. TRANSLATION TO DETAILED WIRING PLANS

After the functional plans had been completed, the evolution of the design proceeded toward the preparation of the detailed working plans from which the actual electric wiring of components could be carried out. The form that these wiring plans took for each machine depended strongly on the physical packaging methods employed for holding the electronic components on the chassis, and on the fabrication procedures followed in wiring up the soldered connections. Although extensive use was made of plug-in component packages in both SEAC and DYSEAC, the nature of the packages and the fabrication techniques used in both cases were so dissimilar that the types of wiring plans prepared for the two machines had to be radically different.

In the SEAC, because fabrication and wiring were carried out by skilled technicians who were capable of reading circuit diagrams, it was possible to use conventional wiring diagrams containing the usual electronic symbols for tubes, transformers, delay lines, resistors, and germanium diodes. In this machine, transformers and electric delay lines up to 2 μsec were packaged in individual plug-in units, but diodes were packaged in groups, electrically isolated from each other and usable in logically unrelated circuits. Over 20 distinct types of these diode packages were used, each package containing generally from 4 to 7 diodes connected in various standard configurations. After the circuit diagram for each chassis was completed, therefore, the diodes indicated on it had to be put through a so-called "clusterizing" process, in which groups of diodes on the diagram were classified according to the different types of standard configurations to which they corresponded. Each such group was then surrounded by boundary lines and the enclosed area, designated according to its type, was assigned a socket location on the chassis. This clusterized circuit diagram was used by the wiring technicians in wiring up the chassis.

In the DYSEAC, however, a completely different form of component packaging was employed [4]. (Each DYSEAC etched-plate tube package contains not only a tube-transformer unit but also preassembled and-gates and or-gates which can be associated with the tube. Also included are supplementary

free components by means of which these standard preassembled gates can be expanded or additional gates incorporated.) Furthermore, a considerable portion of the actual chassis wiring work was carried out by relatively inexperienced technicians who were not expected to cope with the type of circuit diagrams used for SEAC. As a result, sets of working plans were drawn up for DYSEAC which explicitly listed the precise socket and pin identification numbers of each of the approximately 10,000 pairs of socket pins in the machine between which soldered connections were to be made. In order to produce these, a method was employed which involved the preparation of three distinct types of working plans, namely, *packaging diagrams*, *chassis charts*, and *wiring tables*.

The packaging diagram was prepared by using the functional diagram as a guide. For each tube stage appearing on the functional diagram, a rectangular package symbol was entered on the packaging diagram (see fig. 4.7). The next step was to transcribe to the *inside* of the package symbol all of the gating appearing on the functional diagram which fell within the category of standard built-in types preassembled inside the package. Following this, the nonstandard gating structures which were not of the preassembled types (that is, types which required the use of supplementary free diodes or other components) were transcribed from the functional diagram and entered *outside* the package symbols. Finally, components and connections required for circuitry reasons and not appearing on the functional diagram were entered. Thus the information on the packaging diagram is more complete than on the functional diagram in that it represents all the connections which must be made on the chassis sockets.

By means of the packaging diagram it was possible to determine the total number of packages that were required for all the gating stages and delay lines. After this was done, each package was assigned to a specific socket position on the chassis; a certain small percentage of sockets were left unoccupied to serve as spares. All assignments were recorded on a chassis chart, which is a pictorial representation of an actual chassis (see fig. 4.8). The assigning of package positions was done with a view toward minimizing both the total number and length of intra-chassis wires between the sockets and the length of interchassis patch-cord.

As the next step, the available components in each package were assigned to perform the required internal functions for that particular package. The pin numbers associated with each component as it was assigned were written on the packaging diagram in such a manner that every functional signal input or signal output terminal on the package is explicitly identified as being connected so a particular pin.

A careful inventory of the components used in each and every package was kept on the chassis chart as each component was assigned. By means of this inventory the designer could know at all times throughout the process exactly how many components of every type were still available near any region of the chassis. At the end of the process of assigning components, there was usually a slight surplus of components of all types left on the chassis. If an overdraft of components occurred, however, a spare socket could be utilized to provide the needed components. Out of a total of about 21,000 diodes used in DYSEAC etched circuit packages, approximately 22 percent are surplus; of the 3,800 delay-line segments (0.25 μsec), about 10 percent are unused.

Next, the signal distribution between packages on the chassis was indicated by writing on the packaging diagram the socket number and pin number of the signal sources which were to be connected to the components that were previously assigned as the destinations of these signals. After this had been done for the complete chassis, the interchassis signal distribution was indicated. This wiring between chassis is done by patch-cords which connect to pins of special plugs that are mounted on bridges above the various chassis. A package input or output that communicates directly with some other chassis was labelled on the packaging diagram with its local bridge socket number and pin number. On the chassis chart the notation appended to the bridge socket and pin was the unique functional symbol (usually three letters) identifying the particular tube package on the packaging drawing.

The preparation of the packaging diagrams and the chassis charts were preliminaries to the last step which was the ultimate goal, viz., the preparation of a set of wiring tables which enabled technicians to wire up the chassis (see fig. 4.9). The wiring tables consist essentially of columned pages whose entries are numbered serially corresponding to the 60 pins on a socket. Each column corresponds to a particular socket and is labelled accordingly. For example, a column headed 68A

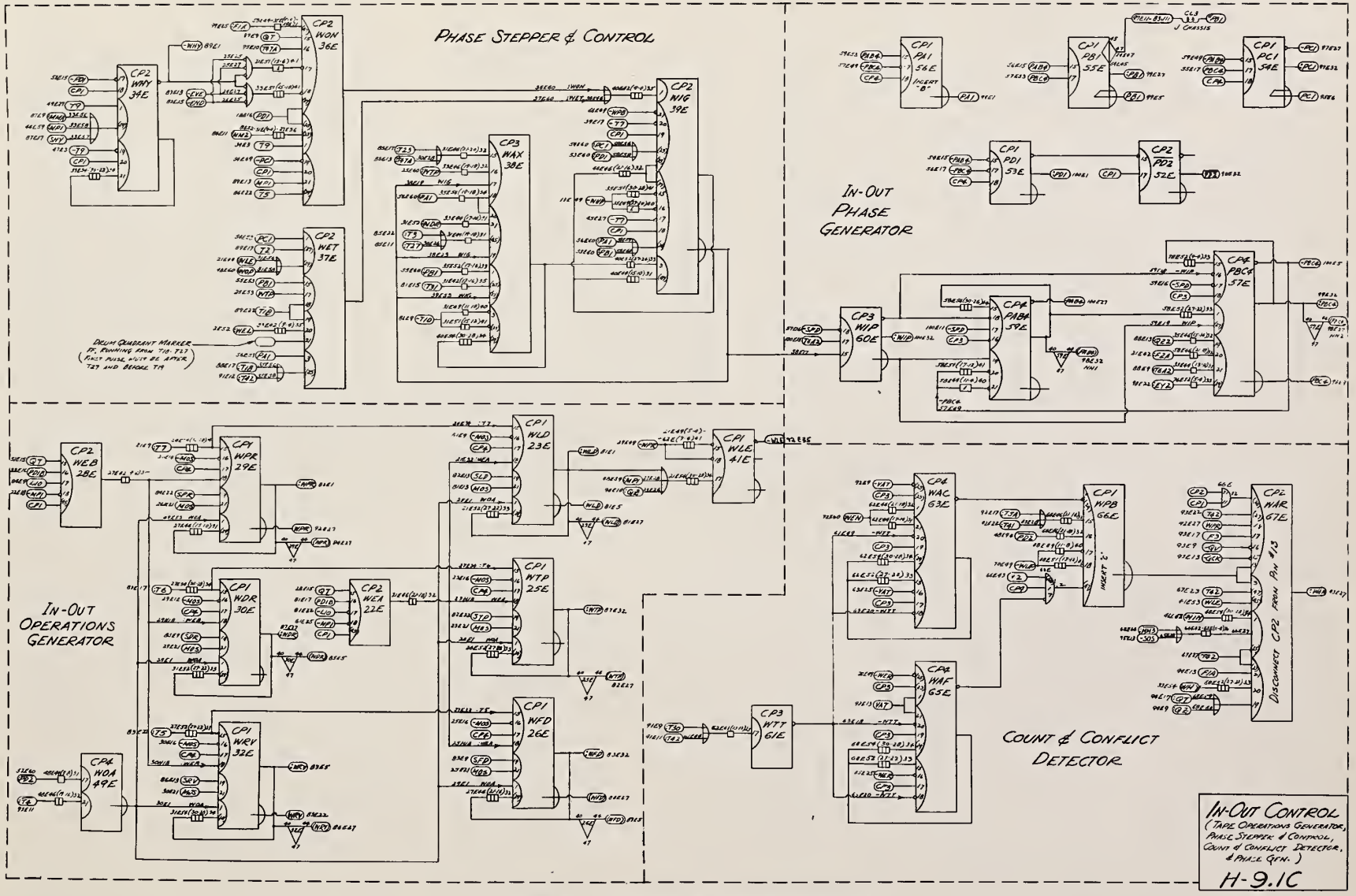

FIGURE 4.7. *Example of a packaging diagram.*

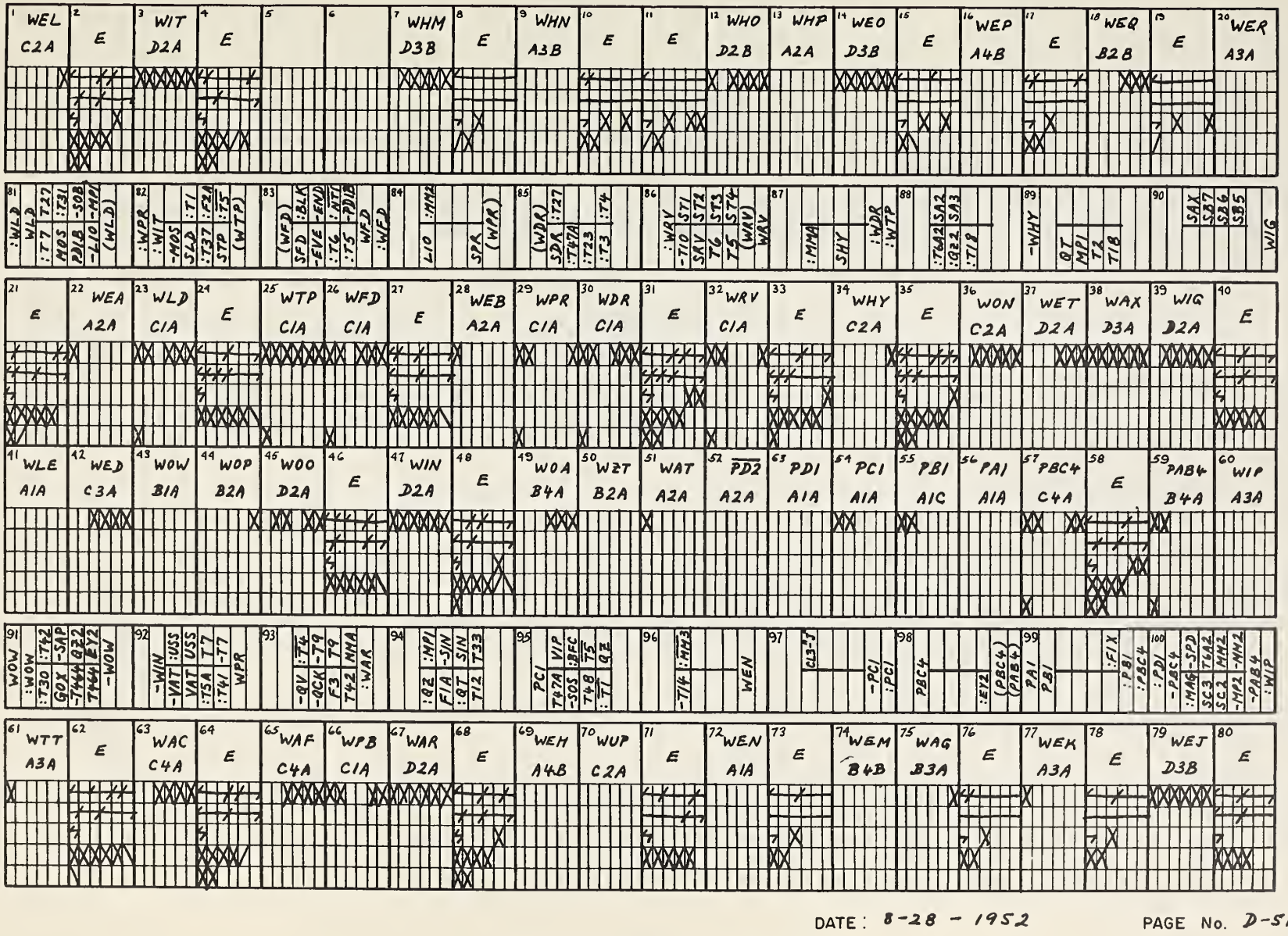

FIGURE 4.8. *Example of a chassis chart.*

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25E TUBE		WTP C1A		26E TUBE		WFD C1A		27E LINE				28E TUBE		WEB A2A	
26D1	23D1		1	29D1	95D1						1				
(J30)			2	(J30)							2				
			3								3				
			4					46C7			4	(J44)			
			5					11C53			5				
			6					(35)			6				
			7					( )			7				
			8								8				
			9					(C43)			9				
			10					(C31)			10				
			11					( )			11				
			12								12				
			13					( )			13				
			14								14				
27H34			15	27H33				(C45)			15	53D15	22D15		
23F16	26F16	44F21	16	26F16	29F16			(C32)			16	22D16			
NC4			17	NC4				( )			17	84D9			
23H18	26H18		18	25H18							18	22F18			
82D22			19	83D9				( )			19				
			20								20				
23D21	26D21		21	25D21	29D21			(C47)			21				
			22					(T43)			22				
24C9			23					( )			23				
95D14			24								24				
83F15	26F25		25	25F25				( )			25				
(F28)			26	(F28)							26				
83F13	26F27		27	25F27				(T53)			27				
(F26)	21F50		28	(F26)	39F50			(T34)			28				
24H33			29	27H32							29				
(J2)			30	(J2)				(T55)			30				
			31					(C10)	29H29		31				
			32					(C16)	26H29		32				
			33					(T22)	26H15	32H15	33				
			34					(T28)	25H15	30H15	34				
			35					(6)	29H18		35				
			36					31C4	36H23		36				
			37								37				
			38								38				
(L45)			39	(L45)							39				
(C52)			40	(C52)							40				
			41								41				
			42					28C60			42				
			43					(C9)			43				
82L27	NN4		44	83L5	NN5			29C60	24C42		44	(J4)			
(L39)	( )		45	(L39)	( )			(C15)			45	NC1			
			46					26C60	83C32		46				
(W56)			47	(W56)				(C21)			47				
			48								48				
			49								49				
			50								50				
			51								51				
(C40)			52	(C40)				83T22			52				
3D20	37D17		53	83D27				(T27)			53				
			54					83T17			54				
			55					(T30)			55				
(W47)			56	(W47)							56				
			57								57				
			58								58				
			59								59				
24C52	33C46		60	27C46							60	27C42			

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FIGURE 4.9. *Example of a wiring table.*

means the information entered in that column pertains to the 68th socket in chassis A. The package type is also indicated in the heading. Each item in the column pertains to a particular pin on that socket, and the entry made for each item specifies some other pin to which it is to be connected. The entries are in the form number-letter-number, specifying respectively the socket serial number, the type of signal (such as direct positive output, negative output, delayed signal), and the pin position in the socket. To help guard against errors a double entry system was employed, whereby each length of wire was represented by an entry for both of the pins that it connects. If a pin was to be connected to more than one other pin, the appropriate number of entries were made for each item.

Technicians receiving copies of the wiring tables did the wiring on all the chassis, following the wiring tables implicitly. The power wiring and other standardized wiring was done according to standard instructions appropriate to whichever of the five possible package types was specified in each column heading. The total wiring table record for the connections between the etched circuit packages of DYSEAC occupies about 270 pages (8 by 10 in.) and specifies approximately 20,000 soldered pin connections.

5. CONCLUSION

In the development of a large-scale computer, system-design work occupies the middle ground between electronic engineering and operations analysis of the intended application. The final system design must be practicable to construct with available building blocks and current fabrication techniques, and must also be capable of satisfying the ultimate user's needs. In working out design problems concerned with reconciling these two requirements, standard methods of attack which would be generally or universally applicable probably are not obtainable. On the other hand, design problems concerned with the development of functional and construction plans, rather than with the development of system specifications, probably would provide a fruitful field for research into generally applicable procedural methods. In particular, problems which might benefit from such research are those concerned with (1) analyzing and synthesizing the complex logical relationships existing in large-scale systems and (2) translating such relationships into explicit wiring plans. With respect to the first class of problem, it should be noted that although methods of mathematical logic such as Boolean algebra have been found useful and effective in handling certain types of system design problems, the scope of their utility to date has been strictly limited to problems of comparatively minor importance in the system design work at this laboratory. With respect to the second class of problem, a very promising possibility appears to lie in the idea of using digital computers themselves to carry out the processes involved in compiling wiring plans. These detailed and tedious processes of recording, classifying, rearranging, keeping inventories, and the like, are in fact feasible tasks for present-day machines. Furthermore, in the future the tasks of the computer might not need to be limited to the production of just the wiring tables prescribing the locations of the various parts of soldering lugs between which connections are to be made. With the development of methods for forming wiring interconnections out of prefabricated standard interchangeable parts, and with the increasing use of mechanized assembly techniques in the manufacture of electronic equipment, it is possible that the computer may one day also be utilized in fabricating the actual equipment. That is, as the final wiring data could be produced within the computer, possibly it could also produce mechanical patterns (e.g., punched paper cards or tape) suitable for governing the selection and positioning of the prefabricated parts out of which the interpin connectors might be formed. In this way, the somewhat dramatic concept of setting a computer to build a computer might well be brought nearer to realization.

TABLE 3. Explanation of figure 4.2

Individual pulses occurring successively in a pulse train are shown pictorially in the order *right to left*. A pulse represents a 1-digit; the absence of a pulse represents a 0-digit.

Item on figure	Name	Mode of operation
1------	And-gate----------	A pulse appears at C if and only if pulses occur on A and B simultaneously. More than two inputs may be used.
2------	And-gate with inhibition input.	A pulse appears at D if and only if pulses occur on A and B simultaneously and no pulse occurs on C.

TABLE 3. Explanation of figure 4.2—Continued

Item on figure	Name	Mode of operation
3	Or-gate	A pulse appears at C if a pulse occurs on either A or $\bar{B}$, or both. More than two inputs may be used.
4	Delay-line	A pulse occurring at A appears at A′ after the span of time *n* microseconds.
5	Amplifying tube and two-pole transformer output.	The output at A consists of positive-going pulses; at −A, negative-going pulses. There is always a one-to-one correspondence between A and −A.
6	Basic flip-flop	The flip-flop is turned *on* (i.e., emits continuous pulses at C) beginning with the first pulse of A, and is turned *off* (emits no pulses) beginning with the first pulse of B which is not accompanied by a pulse of A.
7	Equality comparator	T is a priming pulse occurring before the first pulses on A and B that are to be compared. After the last pulses of the trains A and B have appeared, C emits a pulse if and only if pulse trains A and B are identical.
8	Inequality comparator.	T is a clearing pulse that occurs at or before the first pulses on A and B that are to be compared. After the last pulses of A and B have appeared, C emits a pulse if and only if the binary number represented by A is greater than that represented by B. The digits of A and B occur in order of increasing significance.
9	Binary counter	B emits continuous pulses beginning when an odd number of pulses have occurred on A, but B emits no pulses when an even number of pulses have occurred on A.
10	Two-stage cyclic counter.	Stepping pulses occur on S. With both stages off, the first S turns on A. If A is on and B is off, the next S turns on B. If A and B are on, the next S turns off A. If A is off and B is on, the next S turns off B, etc.
11	Matrix decoder	Let the pulses (or no pulses) emitted by A, B, and C at any instant represent a 3-binary-digit number, ABC. Examples of decoding are: M emits a pulse if and only if ABC = 2; T emits a pulse if ABC = 4 or 6. Such matrices are readily expandable so as to decode larger numbers of digits and in a wider variety of ways.
12	Add-1 counter	T is a priming pulse whose timing determines the power of 2 to be added to the n-binary-digit number contained in the delay-line register. Starting at the time of T, all digits of the original pulse train are inverted (1 becomes 0, 0 becomes 1) up to and including the first 0. The digits occur in order of increasing significance. If A′ is from −A instead of A, the device subtracts 1.
13	Two's complementer.	All digits of A up to and including the first 1 emerge from B unchanged, but all succeeding digits of A after the first 1 are inverted. Digits occur in the order of increasing significance.
14	Adder	A and B carry pulse trains that represent two binary numbers to be added. The output S is the pulse train that represents the sum of A and B. The carry digits are at C. All digits occur in order of increasing significance.
15	Recirculating delay-line register.	This illustrates how an n-binary-digit number contained in such a register may be shifted to the left or right by precession. N, L, R, and I are mutually exclusive control pulses, and in the absence of all others, N is present. N is *normal recirculation*, L is *precess left*, R is *precess right*, and I is *insert*. After a continuous train of *n* L- or R-pulses, the contents have been shifted one pulse position to the left or right with respect to their original positions. Apart from mere shifting, such a precessing register may be used as a pick-up register to collect digits presented on input A at a synchronous but irregular rate, in normal or reverse order, and to arrange them in normal order for distribution as a pulse train. This is done by causing a single I-pulse corresponding in time to each A-digit to be substituted for the first pulse of a train of L-pulses or for the last pulse of a train of R-pulses.

TABLE 3. Explanation of figure 4.2—Continued

Item on figure	Name	Mode of operation
16------	Staticizer---------	This illustrates a different type of pickup register, and it also shows a method of converting from parallel to serial mode of transfer and vice versa. I is serial-insert control pulses for source B. P is parallel-insert control pulses for sources A_1, A_2, A_3, . . . , A_n, H is *hold* pulses, R is *shift right*, and L is *shift left*. I, P, H, R, and L are mutually exclusive except that I is always accompanied by R or L. In the absence of all others, H is present. A single R-pulse causes the content of each flip-flop to be transferred to the one immediately to the right, and a single L-pulse, to the left. For normal order of B-digits, a single R-pulse is used with each I-pulse, while for reverse order of B-digits a single L-pulse is used instead. A continuous train of R-pulses allows an information pulse train to be inserted or removed from the register in normal serial order. A single P-pulse inserts digits from A_1, A_2, A_3, . . . , A_n simultaneously. The parallel outputs are C_1, C_2, C_3, . . . , C_n.

TABLE 4. Examples of typical basic operations in computing systems

Types of operations	Procedures which must be developed for carrying them out
1. *Arithmetic*:	
Addition and subtraction.	Basic addition-subtraction procedures including negative number representation, complementing practices, sign determination of sums, overflow recognition.
Multiplication and division.	Basic multiplication-division procedures including the shifting of numbers in a register, the flow of information between various registers, time sequencing and control of steps required in performing such operations.
Compound operations--	Specialized procedures, formed from combinations of basic procedures, which are needed to achieve higher speeds of operation for special purposes, e.g., extra-rapid accumulation achieved by the DYSEAC Summation operation at up to nine times the normal DYSEAC Addition rate.
2. *Control:*	
Central control operations.	Basic procedures for achieving centralized control functions. (In SEAC and DYSEAC, most control functions are performed by means of suitable combinations of the outputs of only four basic units: a timing generator that provides cyclic recurrent signals for marking off elapsed time within each serial word-cycle, a four-state phase generator whose outputs correspond to each of the four phases of each operation, a phase-stepping unit that advances the phase generator and marks the initial cycle of each phase, and an operations generator that specifies the type of operation being performed.)
Memory-address selection.	Procedures for achieving rapid memory access by means of space-selection switches using matrix decoders for digital address codes, time-selection using counter-timers, and space-voltage analog selection using special digital-to-analog converters.
3. External transfer operations.	Procedures for transferring digital information between internal memory of a computer and low-speed non-synchronous input-output devices [2].
4. External control operation.	Procedures for providing flexible external control over the internal system and for achieving versatile joint control by both internal and external parts of the system acting jointly [5, 6].
5. Program sequencing------	Procedures for sequencing the individual instructions in a program and providing for branching in its execution [3].

6. REFERENCES

[1] A. L. Leiner, W. A. Notz, J. L. Smith, and A. Weinberger, System design of the SEAC and DYSEAC Trans. Inst. Radio Engrs., vol. EC-3, No. 2 (June 1954).

[2] A. L. Leiner, Buffering between input-output and the computer, Review of Input and Output Equipment Used in Computing Systems, Joint AIEE-IRE-ACM Computer Conference, S-53 (March 1953).

[3] A. L. Leiner, Provision for expansion in the SEAC, Mathematical Tables and Other Aids to Computation **36**, 233-237 (October 1951).

[4] R. D. Elbourn and R. P. Witt, Dynamic circuit techniques used in SEAC and DYSEAC, Trans. Inst. Radio Engrs., vol. EC-2, No. 1 (March 1953); Proc. Inst. Radio Engrs. [10] **41** (1953).

[5] A. L. Leiner and S. N. Alexander, System organization of the DYSEAC, Trans. Inst. Radio Engrs., vol. EC-3, No. 1 (March 1954).

[6] A. L. Leiner, System specifications for the DYSEAC, J. Assoc. Computing Machinery **1**, No. 2 (April 1954).

5. High-Speed Memory Development at the National Bureau of Standards

R. J. Slutz, A. W. Holt, R. P. Witt, and D. C. Friedman

1. INTRODUCTION

The problem of obtaining reliable and economical storage of information at high access rates has consistently been one of the most difficult in the field of computer development. During the past several years, the NBS Electronic Computers Laboratory has been active in the development and evaluation of promising memory techniques, particularly the acoustic delay line, the Williams method of cathode-ray storage, and the diode-capacitor system.

When the initial plans for SEAC were being developed in the latter part of 1948, there was no reasonably economical high-speed computer memory system available. However, acoustic delay lines of mercury had been used successfully in radar application, and a memory system based on acoustic delay in mercury was under development for the EDVAC computer at the Moore School of Engineering, University of Pennsylvania. This type of mercury design appeared to be well suited to the immediate need for a reasonably reliable high-speed memory for the NBS Computer.

With the completion of SEAC in early 1950, work was begun on a memory improvement program with the chief objective of increasing the speed of computation through the use of higher speed memories. At this time, the Williams system seemed to be the most promising of the memories under development. This laboratory, as well as other groups in this country, designed a Williams type memory, using the parallel mode of operation, which is basically faster than the original Williams-Kilburn serial system.[1]

A more recent NBS development in the search for rapid-access memories is the diode-capacitor memory.[2] This system was suggested by A. W. Holt and is being developed by a group under his direction. It is a striking example of the inadequately recognized situation that the limiting part of a rapid access memory is not the memory itself but the access. This scheme uses the simplest of storage devices, an ordinary capacitor, and gets its importance from an efficient access scheme in which combinatorial tricks reduce the access circuitry to only a little more than two diodes per bit.

2. THE NBS MERCURY MEMORY

The physical structure of the mercury delay line memory for use with SEAC followed that of the EDVAC memory system with only minor modifications. However, entirely original electronic circuit designs were developed. The system provides memory storage capacity of 512 words, each word requiring 48 pulse times and eight words stored in each of 64 mercury lines.

The delay line used in both the EDVAC and SEAC acoustic memories consists of a mercury-filled Pyrex tube with a quartz crystal at each end to serve as electroacoustical transducers. These quartz crystals are backed up by glass end-cells filled with mercury. The delay line proper is approximately 20 in. long and provides 384 μsec of acoustic delay when operated at 50° C. The central body of mercury used for the transfer of acoustic energy is electrically grounded, and the two backing pools of mercury act as the electric input and output terminals.

The information pulses that are to be stored are energy packets resulting from on-off modulation of an 8-Mc carrier. About 200-v peak-to-peak is applied to the sending crystal, which produces

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[1] F. C. Williams and T. Kilburn, A storage system for use with binary digital computing machines, Proc. IEE (British) part II, **96**, 81-100 (1949).

[2] A. W. Holt, An experimental rapid access memory using diodes and capacitors, Proc. ACM (December 1952).

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acoustic waves whose amplitude nearly causes cavitation. This crystal sets up waves from each face; one travels down the line, and the other is scattered in the end-cell. As the receiving crystal closely matches the acoustic impedance of mercury, most of the energy that reaches it passes through and is scattered in the receiving end-cell. A voltage of several hundred millivolts is created by the receiving crystal.

Although there is a total attenuation of about 60 db between the input and output circuits, only about 3 db are lost in acoustic attenuation in the mercury. One-side-loaded double-tuned coupling transformers are used primarily to provide electrical isolation and incidentally to minimize the attenuation that results from the low resistances necessary to achieve a 4-Mc bandwidth in the face of the comparatively large capacitances of the crystal transducers.

The 60-db attenuation makes special precautions necessary to prevent the acoustically delayed signal from being overwhelmed by direct electric coupling between the end circuits. This coupling results from the impedance of the ground connections to the central mercury column, which is common to both circuits, and is aggravated by the fact that the mercury is contained in glass tanks that permit only restricted contact areas. The wire or ribbon leads used may have a considerable contact resistance with the mercury. A solution to these difficulties was found in the circuit arrangement shown in figure 5.1. Double ground leads, insulated end-cell shields, and floating windings of the coupling transformers permit each end circuit to be a self-contained closed circuit from which almost no current escapes to flow in any common ground path. In this way the direct electric feed-through has been made negligible even when contact resistances have reached the order of thousands of ohms.

Platinum, tungsten, and stainless-steel grounding leads were tested in the original SEAC memory installation, together with 10 variations of cleaning procedures for the glass assemblies. The question of effective treatment of the glass tanks arose because of early speculation that the mercury might become contaminated, but no difficulty from contamination has occurred during the 3 years the SEAC mercury memory has been in use, perhaps because of the circuitry used to prevent electrical feed-through. All delay lines were filled dry rather than by displacement of some other liquid by the mercury. In the 3 years of operation of this computer only two lines have been removed from position. One was removed as soon as it was discovered that its delay differed from the other lines by more than a tenth of a microsecond. The other was unnecessarily removed because of trouble that was subsequently traced to a faulty plug-in connection.

In order to store signals indefinitely in an acoustic delay line, it is necessary to perform the various circuitry functions shown in figure 5.2. These circuits permit a signal introduced into the amplifier to modulate a carrier frequency, which is then sent into the delay line where it is converted into an acoustic signal. After 384 μsec it is picked up from the delay line and amplified, detected back to a video signal, reshaped, retimed, and recirculated back through the delay line. This process may keep on indefinitely or until the computer replaces these pulses with other information.

The input and output of the mercury delay line consists of transformer-coupled circuits which are double-tuned to the basic carrier frequency of 8 Mc and are one-side-loaded only for an over-all bandwidth of approximately 4 Mc. These double-tuned circuits are used primarily for electrical isolation, although they also make increased bandwidth possible. Interstage coupling circuits in the IF amplifier are single-tuned. Because the output of the last IF stage must drive into the relatively low-impedance nonlinear detector, a double-tuned circuit is used for this impedance-matching function. Because the secondary of this tuned circuit is completely floating, a relatively high-impedance voltage-doubler detector could be utilized. This detector feeds into a low-pass filter of approximately 100-ohm impedance.

Following the detector output are a series of germanium diode gates which permit a narrow time sample of the detector output to be taken. This sample is then fed into a transformer-coupled amplifier stage and broadened by regenerative broadening. Because the output of this transformer-coupled stage commences with the time of the narrow interrogation pulse which may be held to a fixed timing relative to the main computer, this circuit serves to resynchronize the delay line information with the computer operating rate. The other diode gates into this stage are used to intercept

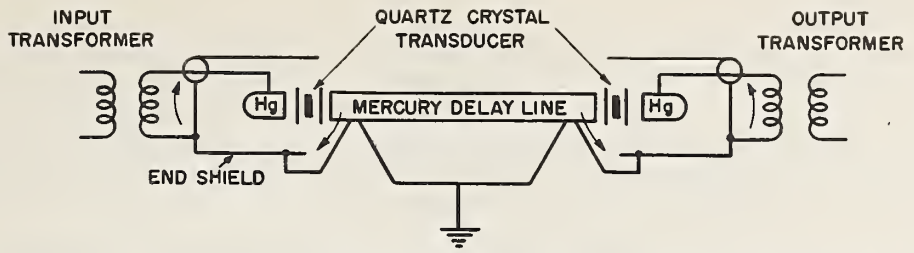

FIGURE 5.1. *Schematic diagram of circuit connections to the acoustic delay line used in NBS mercury memory.*

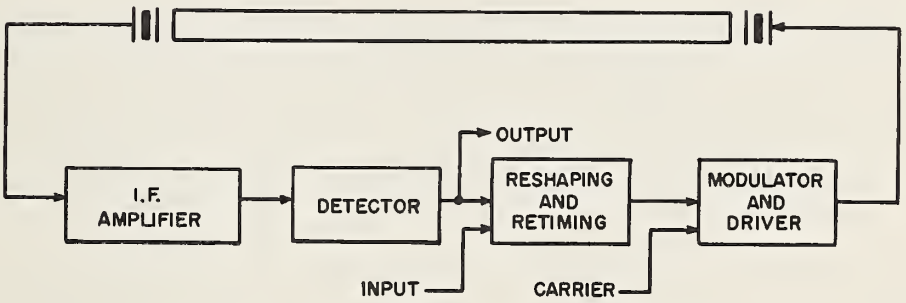

FIGURE 5.2. *Block diagram of the mercury memory system.*

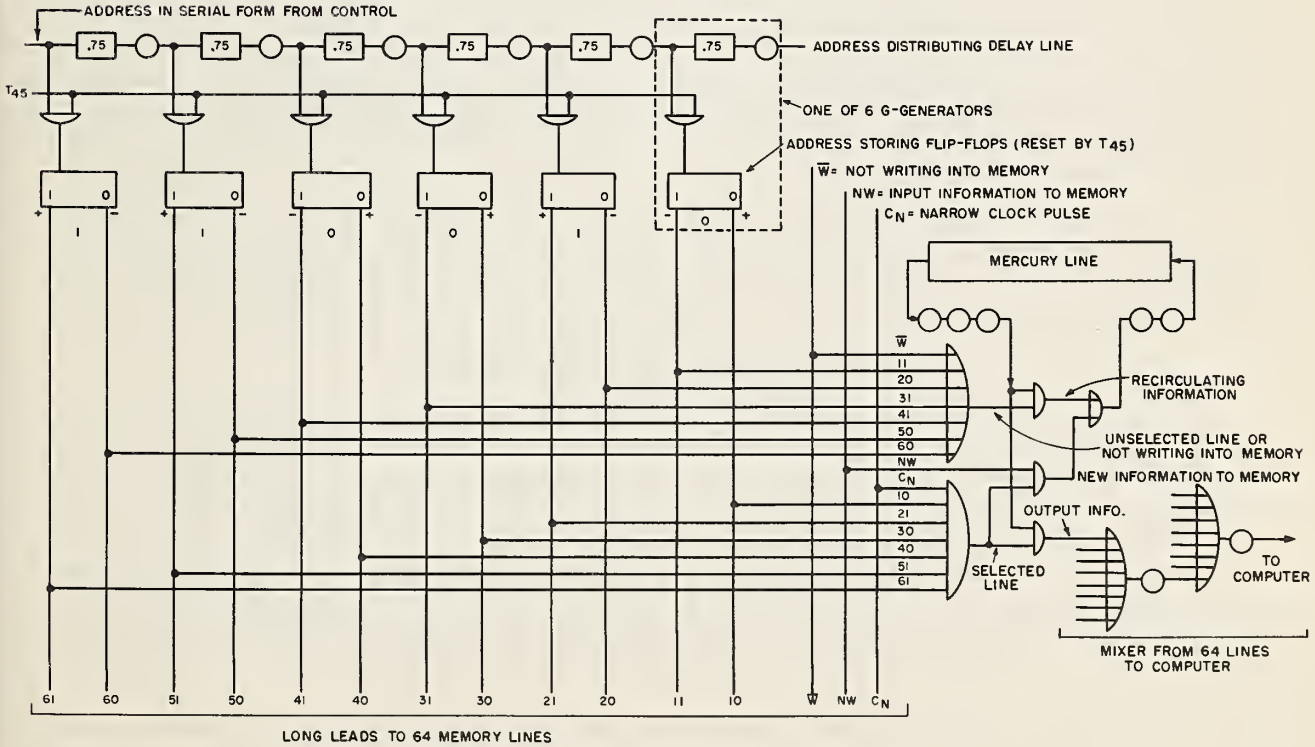

FIGURE 5.3. *Mercury line selection system.*

information that is recirculating in the delay line if a word is to be cleared out in order to insert new information.

The output of the transformer-coupled stage consists of a half-microsecond pulse of very low impedance and approximately 20-v amplitude. This signal is broadened to approximately 0.75 μsec, using distributed electrical delay lines. This signal is then modulated by an 8-Mc carrier signal in a second germanium diode gate which feeds into the driver stage for the mercury delay line. The pulse transformer, all germanium diodes, and the detector circuit are completely plug-in to facilitate maintenance. The amplifier unit as a whole is also plug-in to the main memory cabinet.

Selection of one out of the 64 mercury delay lines in the memory cabinet requires six binary digits, since $2^6=64$. A line may be selected either to read stored information from the memory into the computer, in which case the information is also retained in the memory, or else to write new information from the computer into the memory, in which case the information previously stored there must be cleared out.

The six line selection digits are delivered serially over one wire from the computer to the line selection circuits in the memory cabinet, shown in figure 5.3, where a six-stage distributor line makes them available on six different wires at the time of a pulse called T45. This T45 pulse gates the selection digits into six dynamic flip-flops which have special high-powered output stages to drive the large diode matrix which actually selects a memory line. The signals driving the selection matrix are transformer-coupled and reverse polarity every half microsecond, but all that is significant for selection is their polarity during the narrow clock pulse C_n, which controls the admission and recirculation of information pulses in the mercury memory.

Actually, there are two diode selection matrices driven from the same input leads. One matrix, comprised of or-gates, supplies pulses to every memory line except the selected line in order to gate the previously stored information on around the recirculation path. If the operation is to read from rather than to write into the memory, then circulation must be maintained even in the selected line. This is done by pulses on the line $\overline{W}$ (meaning "not writing"), which is wired into every or-gate.

The other matrix is comprised of and-gates so that it supplies pulses only to the selected memory line. These pulses, timed by C_n, serve to gate information either into or out from the selected memory line.

Three additional information digits are needed to select a particular word of the eight words in a delay line. A counter in the computer records which memory position is currently available at the detector output, and comparison of this counter with the three time-selection digits is used to initiate gating of the desired word.

The memory was considered adequate for use in the transportable DYSEAC computer with only minor structural changes. The same design has been used relatively unchanged by several computer groups throughout the country. Seven models have been constructed with only minor modifications from the original NBS design. Successful operation has been reported from all groups having this memory.

3. CATHODE-RAY TUBE MEMORY

With the decision in 1950 to develop a Williams-type memory, work at the Electronic Computers Laboratory was planned along five major lines: (1) circuitry for a parallel memory system; (2) equipment to determine the suitability of tubes for storage purposes; (3) methods to circumvent the deficiencies of standard cathode-ray tubes; (4) program for improving storage tubes; and (5) development of the theory of Williams-type storage. An early result of the memory improvement program was the construction of a full-scale experimental electrostatic memory of 48 tubes, each storing 512 binary digits of information. This equipment was completed and placed in experimental operation in SEAC by February 1951 and was one of the earliest full-scale Williams-type systems constructed in this country.

In the SEAC Williams memory,[3] each tube is assigned one particular digit of the 45 binary digits making up a word that can be either an instruction or a number. (The other three of the 48 positions in the SEAC word are spares.) All of the digits of one word are assigned the same relative positions in the array of 512 stored spots on each tube. Figure 5.4 is a block diagram of the SEAC electrostatic memory system.

Action during a reading operation is as follows: The address (numerical designation of location) of a word is taken from the Address Register and translated into X and Y coordinates of its location on the tube face by the Staticizer and Deflection Generator. All deflection operations are done in parallel. In 3 μsec, the deflection transients disappear, and the beam is turned on in all tubes for 0.5 μsec (see fig. 5.5). The outputs from the signal plates are amplified and sensed during the STROBE period which occurs within this time. A positive output represents a binary one, and a negative output represents a binary zero. This information is transferred to the Shift Register in parallel, from which it is fed serially to the arithmetic unit or to an output device.

Since the act of reading causes all spots to be written to "zero," the "ones," must be restored. To accomplish this, at the end of the DOT pulse all tubes are provided with a sawtooth deflection pulse which displaces the beam about one spot-diameter. If the output from any tube is positive at STROBE time, the beam is held on by the DASH pulse which occurs during the TWITCH. The spot charged during reading is then discharged by secondaries from under the moving beam and a one is thus restored. If the output of the tube is negative, a zero has been sensed and rewritten during DOT so that no other action is needed. The absence of the positive output prevents the beam from being held on during the TWITCH and the spot is left charged. The total time allowed for this read-write operation is three microseconds. An additional time of 6 μsec is required to allow the staticizer pulse to swing back, making a total operation time of 12 μsec, 3 for deflection, 3 for read and rewrite, and 6 for flyback. Writing is done in similar fashion. The information is stored in the shift register and is used in place of the output of the amplifier to control the holding on of the beam during TWITCH.

Since the charges stored tend to leak away or are discharged by secondary electrons and stray primary electrons during reference to neighboring spots, it is necessary to regenerate (read and rewrite) each word periodically. The operation is the same as consultative reading, except that the source of the address to be rewritten is the regeneration counter rather than the address register, and no information is gated into the shift register. The regeneration counter advances consecutively through the electrostatic storage addresses as each word is regenerated. Since the minimum time to perform an operation in the arithmetic unit of SEAC is 48 μsec, three regenerations can be carried out between each useful consultation. If there is no consultation of the electrostatic memory at the allotted time, an additional regeneration occurs. This may happen when SEAC is using both memory systems and an address in the acoustic memory is called for, or during a long operation such as multiplication.

In operation with SEAC, over 1,500 hr of useful operation have been obtained, but it has never reached the long-term reliability of the SEAC mercury memory.

The problem of supplying storage tubes for a Williams-type system has proved more difficult than was originally anticipated. During the early planning of Williams-type memory systems in this country, standard cathode-ray tubes were expected to provide adequate data storage, and all but one of the currently operating computers which have Williams memories do use standard types of tubes. However, standard tubes which were commercially developed for other purposes have certain limitations when they are used in high-speed memory systems. These limitations include nonuniformity of surface, which causes the blemish problem; interaction between storage locations, which causes the read-around-ratio problem; and interaction between electrodes of the tube, which causes the cross-talk problem.

Performance of the standard type tubes in operating computer memories has not been as good as has been hoped. In order to use these tubes reliably, either the number of bits per tube has had to

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[3] A. W. Holt and W. W. Davis, Computer memory uses conventional C-R tubes, Electronics (December 1953).

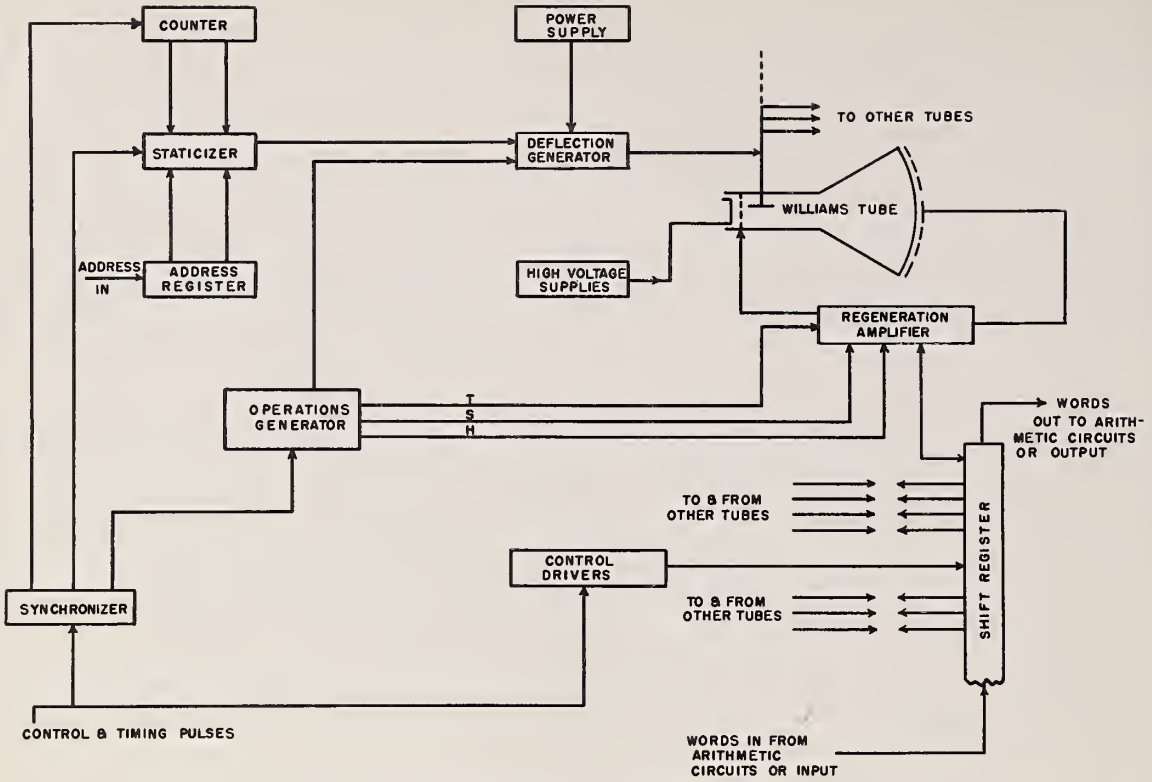

FIGURE 5.4. *Block diagram of electrostatic memory system.*

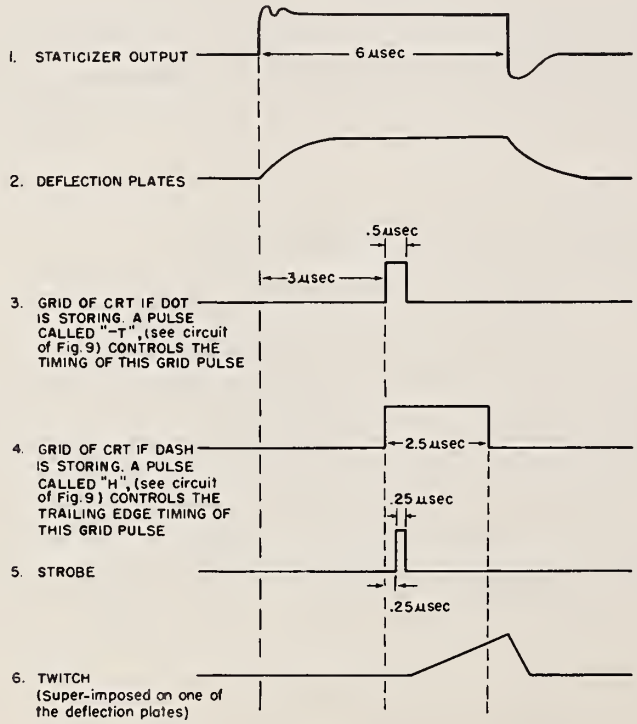

FIGURE 5.5. *Timing cycle: reading, writing, regenerating.*

be reduced below the number originally planned, or the ratio of references to the memory per regeneration has had to be limited. It has also been necessary to reject about four out of every five tubes received in production lots; acceptable tubes are therefore more expensive than had been expected.

Two lines of attack on the problem of improved tubes have been emphasized at the Electronic Computers Laboratory. The first approach was to try to obtain an improved tube which, although special purpose, would nevertheless be less expensive than intricate tubes proposed for other systems of electrostatic storage. The second approach was to try to circumvent the faults of available tubes. Both lines of attack have recently been quite successful.

On of the major problems is the presence of minute areas of low secondary emission ratio on the storage surface of the tubes. These spots are variously called blemishes, flaws, or (in England) phonies. Storage is impossible on these areas, and they must be avoided or the tube must be discarded. Unfortunately, the dodging of blemishes is difficult when many tubes are operated in parallel. In this case, computer operation may become unreliable unless very careful engineering prevents motion of the spot over the face of the tube.

Blemishes appear in about 80 percent of the tubes produced commercially, largely because extreme cleanliness is required to produce blemish-free surfaces. Blemish-free surfaces have been successfully produced in this and other laboratories when care is taken to maintain a high degree of cleanliness. Manufacturers of cathode-ray tubes interested in good surface quality are cooperating in the work of improving the tubes, as shown in table 1.

TABLE 1. Work at commercial tube plants

Manufacturer		Success	Direction of effort	Remarks
A--------	Smaller spot size; improved spot profile; improved deflection defocusing characteristics.	A likely design was produced.	Further testing of this model.	Design originated at NBS Computer Laboratory.
B--------	Smaller spot size; better beam profile.	Tube with half spot size, twice storage capacity of 5UP11.	Possible further testing of this gun in 3-in. bulb.	Finished sample tube delivered one week after initial discussion.
C--------	Over-all improved storage tube.	Final sample tubes were blemish-free at 2KV. Read around ratio was very high compared to that of standard CRT used.	Small-scale of production of further improved tubes, some refinements to be considered.	Work done under BuShips contract. Testing done at many cooperating government laboratories.
D--------	Experimental tubes for surface studies.	Study produced. No exceptional surfaces. Good bulb design for gun-signal plate shielding.	Small production with standard phosphor for tests in SEAC.	For experimental use only. Tube design originated at NBS Computer Laboratory.
E--------	Fine spot, prefocused gun.	----------	----------	In early stages. Work being done under BuShips contract.

The investigation of tube blemishes undertaken at NBS was first directed to the determination of the nature of the blemishes so that some control might be attempted and to correlating the location of these blemishes with the location of physical blemishes in the phosphor. Specially coated plates were checked in a demountable system under a microscope for this purpose. Correlation was low. An attempt to determine the size of a blemish was made by using India ink markings on a glass

plate. It was found that a positive blemish (defect in an area coated with ink) or a negative blemish (spot of ink on a preponderantly glass area) could be identified when one dimension was equal or greater than the beam diameter.

The first method of finding blemishes was to sweep over a rectangle on the face of the tube with a Lissajous pattern produced by sinusoidal X and Y deflection voltages and to apply the same deflection voltages to a monitor tube. The output at the signal plate of the storage tube was amplified and applied to the grid of the monitor. As long as there was no change in the storage surface, the brightness of the monitor was constant. However, when a blemish was struck by the electron beam, it caused a change in brightness on the monitor, and its relative position was marked by a bright or dark spot. The system located the blemishes but did not tell whether they would affect storage. This test was very sensitive but only qualitative.

A test called the Line-of-Dots test was developed at this Laboratory. It was not as sensitive but was able to determine whether a blemish would affect storage. Results of this test correlate very well with the performance of tubes in actual operation, and the test is now used as a specification test by a commercial manufacturer of a developmental Williams tube.

The Line-of-Dots test operates as follows: The beam is turned on and swept across the horizontal axis of the tube under test during the first half of the cycle. During the second half-cycle the beam is swept across the same line, but the beam is turned on only during 10 very short periods. During each one of these short periods the screen on the front of the tube picks up a positive-going signal which is very similar to the usual "dash" signal. These periods are nonsynchronous with the sweep, so that the entire line is interrogated during successive sweeps. When displayed on the vertical axis of a synchronized monitor, the envelope of the dash signals will show a notch or dip at a point where there is a blemish. The block diagram of this equipment is shown in figure 5.6.

Because blemishes afflicted 80 percent of the tubes, attempts were made to remove them. The use of infrared, ultraviolet, and electron bombardment failed to affect them. Rapping with a soft mallet helped to remove some. The best tool seemed to be a spark coil such as that used for checking vacuum leaks. The high-voltage brush discharge across the face of the tube charged the blemish and the surface alike, and the electrostatic repulsion removed many of the blemishes. This method was refined to the extent that 80 percent of a batch of tubes which were treated in this manner were acceptable.

Another aspect of the storage surface problem is the aging of the phosphor during use. A tube which has been in use for some time frequently develops a set of blemishes corresponding to the raster position. These raster burns usually do not affect storage seriously until the tube has had a reasonable life. Los Alamos, however, reports that in MANIAC it is necessary to replace tubes at an undesirable rate because of raster burns. Although our studies of this phenomenon are not complete, it does appear that the difficulty can be prevented by baking the phosphor at higher temperatures than are normally used. This indication has been tentatively confirmed by British work.

The second major difficulty encountered in Williams-type storage is the obliteration of the stored charge at one spot by the splash of the secondary electrons emitted from neighboring spots. The number of consultations of neighboring spots which may be made before regeneration is required is called "read-around ratio," "splash number," or "repetitive consultation number." Low read-around ratio may be improved by one or more of the following methods: by reducing the total number of spots in the tube and separating them further, by systematically forcing sufficient regenerations per useful consultation of the memory, by taking the ratio into account during coding of problems, or by improving the intrinsic properties of the tube in this respect.

Low read-around ratio appears to be mostly a function of gun design. Stray electrons not in the focussed beam, poor current distribution in the beam, and large beam diameter contribute to this effect. It was felt that a relatively small effort to obtain smaller spot size and a more rectangular current profile might result in considerably improved read-around ratios. Indeed, one company (manufacturer B, table 1) provided the laboratory with an improved tube a week after the first consultation. This tube, called the 5lCUPll, had a gun in which the beam was heavily masked. It would store 1,024 bits in SEAC, whereas a 5UPll usually would store only 512. A sample lot of these tubes was produced, but they were unsatisfactory for other reasons, and no more were ordered. However, the original tube was used in SEAC for about 1 1/2 years alongside 3KP and 5UP types.

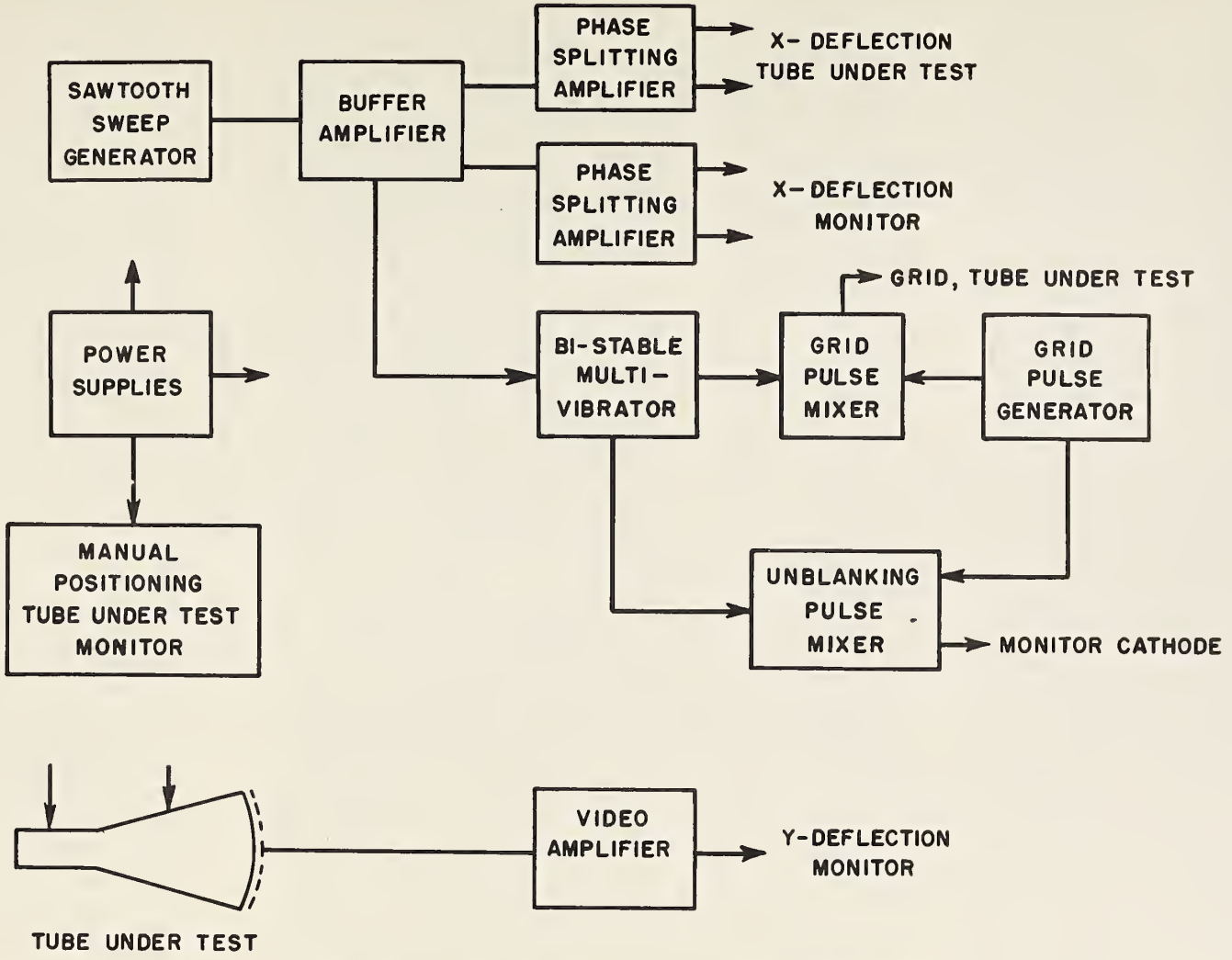

FIGURE 5.6. *Block diagram of line-of-dots blemish test equipment.*

Later the Bureau of Ships approached Manufacturer C to do development work on storage tubes. A contract was let that provided for the production of several trial designs to be followed by small-lot production of the best of these designs. In cooperation with the National Bureau of Standards, which was acting as technical consultant on the contract, the Argonne National Laboratories, the Institute for Advanced Studies, and a commercial laboratory tested these trial tubes. The purpose was twofold; first, to determine the best design of the developmental lot for use in the final sample production, and second, to determine how well the various tests used in the different laboratories agreed among themselves and with operation in a computer. The agreement among the tests in arranging the tubes in order of quality was quite good, considering the variety of test conditions. This order also agreed well with their performance in SEAC.

A second lot of tubes, all alike, are now in process of being tested in digital computers at various laboratories. These computers include ORDVAC at the Ballistics Research Laboratory, Aberdeen Proving Ground; ILLIAC at the University of Illinois; AVIDAC at Argonne National Laboratories; the Institute for Advanced Study's computer; and SEAC. Results to date are very encouraging. On the basis of these results, a conference held at the National Bureau of Standards led to agreement on specifications for a computer tube similar to this lot, and small-scale developmental production of the tube has begun.

This improved tube will have a gun in which the beam is heavily masked. Shielding is carefully designed to decrease the number of stray electrons. Distortion of the beam because of deflection is reduced by reducing the beam diameter in the deflection region and shaping the deflection plates. A storage surface of magnesium tungstate is used because of its good secondary-emission properties and because better control of screening in manufacture is expected. A 3 in. diameter was agreed upon because it was felt little could be gained by going to a larger tube, and considerations of space requirements and of safety favor as small a tube as possible. The specifications are such that no significant blemishes should appear at 2,000-v accelerating voltage, and the read-around ratio should be at least 256 in a field of 1,024 spots.

In the meantime, also under a Bureau of Ships Contract, another company (Manufacturer E) is developing a fine-spot gun with a magnetic fixed focus. The elimination of any electrode or electrode voltage is desirable because it reduces the number of parameters affecting the operation of the gun.

The third major fault with standard cathode-ray tubes when used as storage devices is the cross-talk among elements of the tube and between the signal plate and tube electrodes. For example, in the 3KP-5UP gun a deflection lead serves as a support for the grid cylinder, and the sharply rising grid pulse is capacitively coupled more to this deflection plate than to its mate. If the unbalanced coupled signal is large enough, the spot is in motion during writing or reading, which tends to spoil "dots." Again, the deflection plates in a 3-in. tube are rather near the signal plate. As these are pulsed with rapidly rising pulses of the order of 100 v and the normal signal level is about a millivolt, it is not hard to couple in signals that might cause the amplifier to block or ring so that false data are stored. A study was made of these effects, and it was found that grounding a conductive coating painted on the outside of the tube gave a substantial improvement in tubes without third anodes. A third anode gave the best shielding between gun and signal plate.

4. DIODE- CAPACITOR MEMORY

The basic storage element of the diode-capacitor memory is shown in figure 5.7. The connection E is used for both reading and writing, while the two diodes between A and D are used as a "squeezer" to connect the capacitor to the reading-writing circuits. During holding, both diodes are biased in their back direction. For example, A might be held at −4 v with respect to ground, and D held at +4 v. Then if the capacitor has a charge of, say, 2 v, both diodes will be biased in their back direction, and only small currents will flow into or out of the capacitor. For reading, suppose that both points A and D are forced to ground potential ("squeezed"). This will cause one or the other diode to conduct and a voltage will appear across the resistor R. If C is charged with 2 v of such polarity as to make its lower terminal more negative than its upper terminal, then when the squeeze occurs there will appear at E a pulse of −2 v, which then dies out with the time constant RC. This would be recognized by the reading circuits at E as a binary zero. If the polarity of the charge on C had been in the opposite direction, the squeeze would have produced a positive pulse, which would be recognized as the binary one. Thus the contents of the storage element has been read, but in

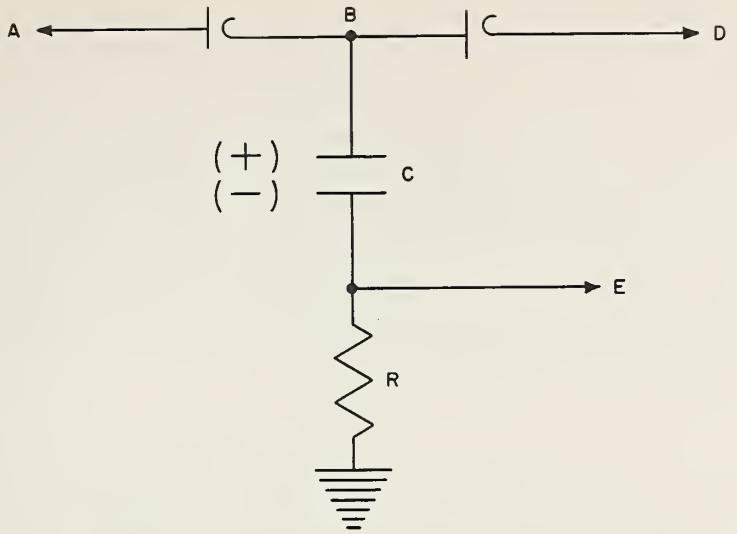

FIGURE 5.7. *Basic circuit of the diode-capacitor memory.*

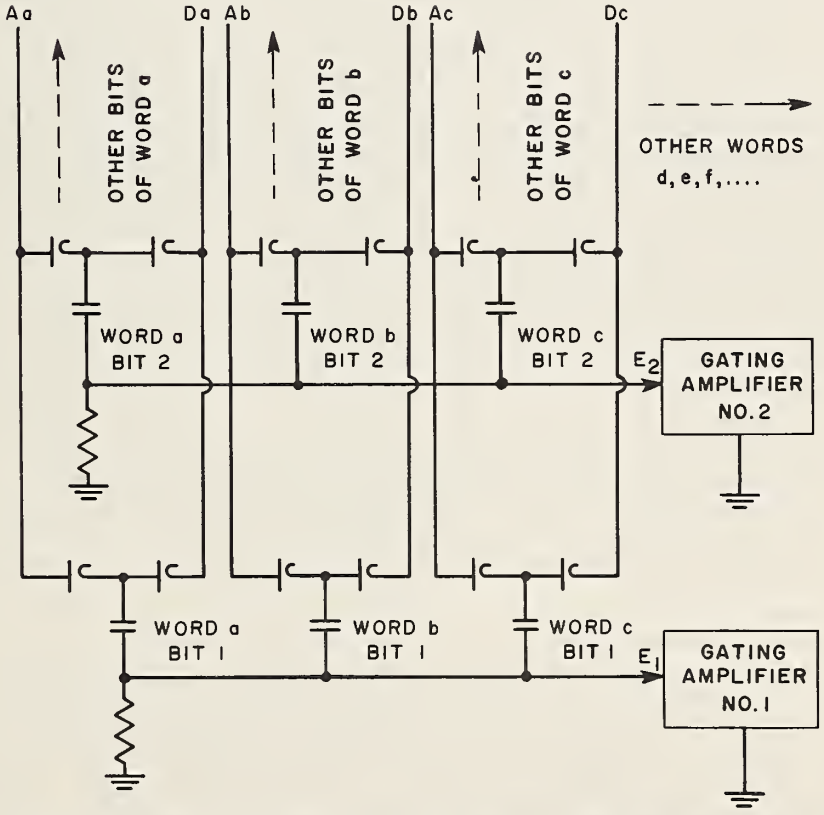

FIGURE 5.8. *Part of a full diode-capacitor memory, showing the manner in which the words, bits and gating amplifiers are interconnected.*

doing so it has been discharged (at least partially) and the information lost from the storage element. The information must be rewritten to continue the storage beyond the reading operation.

In order to write (or rewrite) information it is necessary merely to force the lead E to the desired state during the squeeze and hold it there until the squeeze is over. While A and D are at zero volts, suppose that E is forced to +2 v and held there at least until A and D are returned to their normal voltages of −4 and +4, respectively. Then the capacitor is left with a charge of 2 v, and upon the next squeeze it will produce a positive pulse at E. That is, a one is written. Obviously the opposite is equally possible: forcing E negative until the end of the squeeze will write a zero. Note that once A and D have returned to their normal voltages, the charge on the capacitor will be undisturbed by later changes of E, provided the magnitude of the voltage on E never exceeds 2v. Thus E can have other pulses on it, either positive or negative, and the charge stored on C will remain unaffected because both diodes will remain with backward bias. This is important for organizing many basic storage elements into an efficient memory assembly and is the reason for charging the capacitor to only +2 v while biasing the diodes twice as much.

In the discussion so far the diodes have been implicitly assumed to be ideal, having practically infinite forward conductance and practically zero backward conductance. The effect of finite forward conductance is modest: it will reduce somewhat the output pulse amplitude, and it will determine how long a writing pulse must last to charge the capacitor adequately. The effect of finite backward conductance, however, is critical. During the holding operation relatively long times will elapse, and even minute currents through the diodes will disturb the capacitor charge. The unit would gradually leak toward a condition of no charge on the capacitor, or even a condition in which the sign of the charge is reversed. Therefore, the permissible duration of the holding operation is determined by the rate at which the capacitor charge leaks through the back current of the diodes. Arbitrarily long storage of information is achieved through regeneration. Before the capacitor charge can change to a point where there is danger of losing the information, the memory control circuits read in a routine manner the contents of each cell and rewrite it accordingly.

What is needed at point E, then, is an amplifier which will sense the polarity of E during the early part of the squeeze period, together with a gate structure that will force E to the desired polarity during the latter part of the squeeze period. For reading or regeneration, E is forced to the same polarity that was read; for writing new information the polarity to which E is forced is independent of what was read but is determined by the new information being written. Such a gating amplifier is easy to construct. The amplification required is very modest, since its input is a pulse whose amplitude is of the order of 1 or 2 v. The gating can be accomplished with standard techniques, utilizing 2 or 3 vacuum tubes and several diodes.

An interesting point is that the memory in this form permits the ready incorporation of powerful self-checking features. The input to the gating amplifier is expected to be bipolar. That is, a definite pulse should be received every time a storage element is read. This pulse may be either positive or negative, depending on the information content of the storage element, but it should not be zero. If a signal approaching zero amplitude is received, it is a direct indication that the operation of that particular storage element is marginal. Thus, at the expense of some complication of the gating amplifier, it can be made to recognize three different input levels: acceptably positive, unacceptable, and acceptably negative. An unacceptable input need not, of course, be restricted to being very close to zero. A pulse of anything less than, say, one third of the normal amplitude might be sensed as being unacceptable. This would give a very prompt indication of incipient failure.

In order to achieve acceptable efficiency, it is essential that one such gating amplifier serve many basic storage elements. Figure 5.8 shows how this is done. The busses A and D are made common to all of the bits of a particular computer word, and a particular gating amplifier serves the same bit on each of many words. For 256 words of 40 bits each there might be 256 pairs of leads A and D, and 40 gating amplifiers. For reference to word b, the busses A_b and D_b would be squeezed to zero voltage, while all of the other pairs would be held at their normal values of −4 and +4 v. In this way each gating amplifier receives a pulse from its bit of the selected word, so the word is available in parallel at the gating amplifiers. These amplifiers can then write into this word, or rewrite it, without affecting the other words, since all diodes in the other words remain with backward bias as already described. After the squeezing busses on word b are returned to normal, any

other word may be referred to in the same way. In this way it is possible to have a fully parallel random-access memory. Regeneration is handled by having the memory control intersperse regeneration cycles between the computer access cycles. For the regeneration cycles, the words are read, one after the other, and rewritten to their former state.

At present the quantitative aspects of the regeneration problem appear to be the greatest limitation on this entire memory scheme. As a rough approximation consider the following argument: The rate of discharge of the capacitor during holding is proportional to I_b, where I_b is the back current of the diode at a voltage of about 4 to 6 v. Similarly, the rate of charging during writing and rewriting is proportional to I_f, where I_f is the forward current at something like 0.5 to 1 v. The safe holding time and writing time are inversely proportional to these rates, so the ratio of the permissible holding time to the writing time is I_f/I_b. This ratio of permissible holding time to writing time indicates how many writing operations can be done before it is necessary to come back and rewrite a particular bit. It is an approximate measure of the number of bits that can be served by one gating amplifier. With the inclusion of safety factors, reading time, and possible selection times, this figure comes in the range of about 0.1 (I_f/I_b) to 0.01 (I_f/I_b).

For actual diodes, this means that with the customary germanium whisker diodes, only some 32 to 64 bits can be served by each gating amplifier. It is, of course, possible to have multiple sets of gating amplifiers, but having many such sets would seriously increase the cost of the system. On the other hand, miniature selenium diodes give a much better figure of merit. It would appear possible to operate safely with 256 to 512 bits per amplifier. These diodes have much greater capacitance than the germanium, but the balanced construction of the squeeze circuit overcomes much of the difficulty. An ideal diode for this application is the new silicon junction diode, which has a simple thermally diffused junction. Laboratory models of these diodes have been able to withstand rather less back voltage than the germanium or selenium, but they have a fantastic I_f/I_b ratio. The back voltage that these units will stand is of the order of 20 v, which is entirely acceptable in this memory circuit. On the other hand the ratio I_f/I_b is even greater than some thermionic vacuum diodes. Only two such diodes have so far been available to this laboratory for test (through the courtesy of the Bell Telephone Laboratories), but they formed a basic storage element with writing times of a few microseconds and holding times of two to three seconds. These diodes appear capable of operating in a memory with 10,000 words per amplifier, with safety factors of 10 in the forward direction and 100 in the backward direction. Right now these units are rarities, but there is hope that they will be available in quantity and at reasonable cost in a few years.

A possibility that should be mentioned for the future is the use of capacitors which exhibit strong voltage-charge hysteresis. Such capacitors could be used in this system without requiring tight limits on their characteristics. This system would permit much looser specifications for the capacitors than present alternative proposals for their use. Using them in this system would eliminate the I_f/I_b restriction on the number of memory elements served by each gating amplifier. The specifications for the diodes could also be greatly relaxed, but there would be no decrease in the number of diodes needed.

The system described so far achieves reasonable efficiency for the gating amplifiers but requires a selection circuit capable of squeezing the appropriate pair of buses for a particular word. This could be accomplished by the customary diode matrix, but the usual form of such a matrix has large standby currents. In this memory the squeezing buses require relatively large currents; the resultant selection matrix is feasible but draws large amounts of standby power. To avoid this situation a selection matrix using transformers and diodes is used as shown in figure 5.9. This matrix has no standby power requirement, although it does require more input drivers than would be necessary with a multidimensional diode matrix. For the transformer-diode matrix, 2n inputs are required to select from among n^2 words. The matrix is made up of two sets of crossing buses (X and Y in fig. 5.9). At each crossing a diode and transformer are connected as shown. Normally all of the X buses are held at, say, +10 v, and all of the Y buses are held at −10 v. This puts backward bias on the diodes associated with each transformer, so no current flows through any transformer. If one X bus is dropped to −10 v, still no current will flow; but if simultaneously one of the Y buses is raised to +10 v, then just the one transformer at the crossing of these two buses will receive a signal. If X_2 is lowered to −10 v, and Y_1 raised to +10 v, the transformer secondary connected to buses A_c and D_c will squeeze the voltage on these two buses together. This will select the desired word.

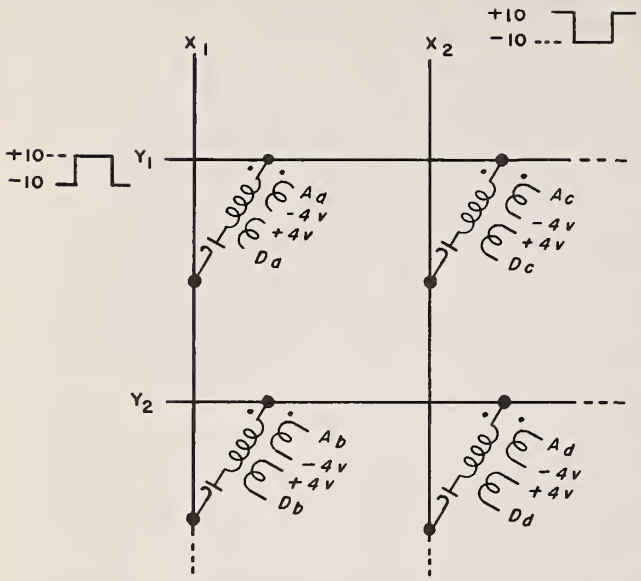

FIGURE 5.9. *A matrix switch using the transformer and-gate.*

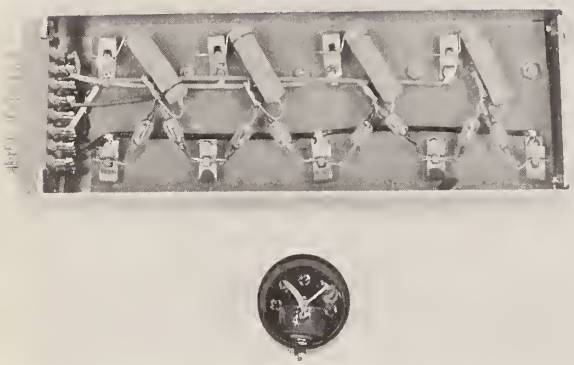

FIGURE 5.11. *Eight-bit memory package and transformer and-gate.*

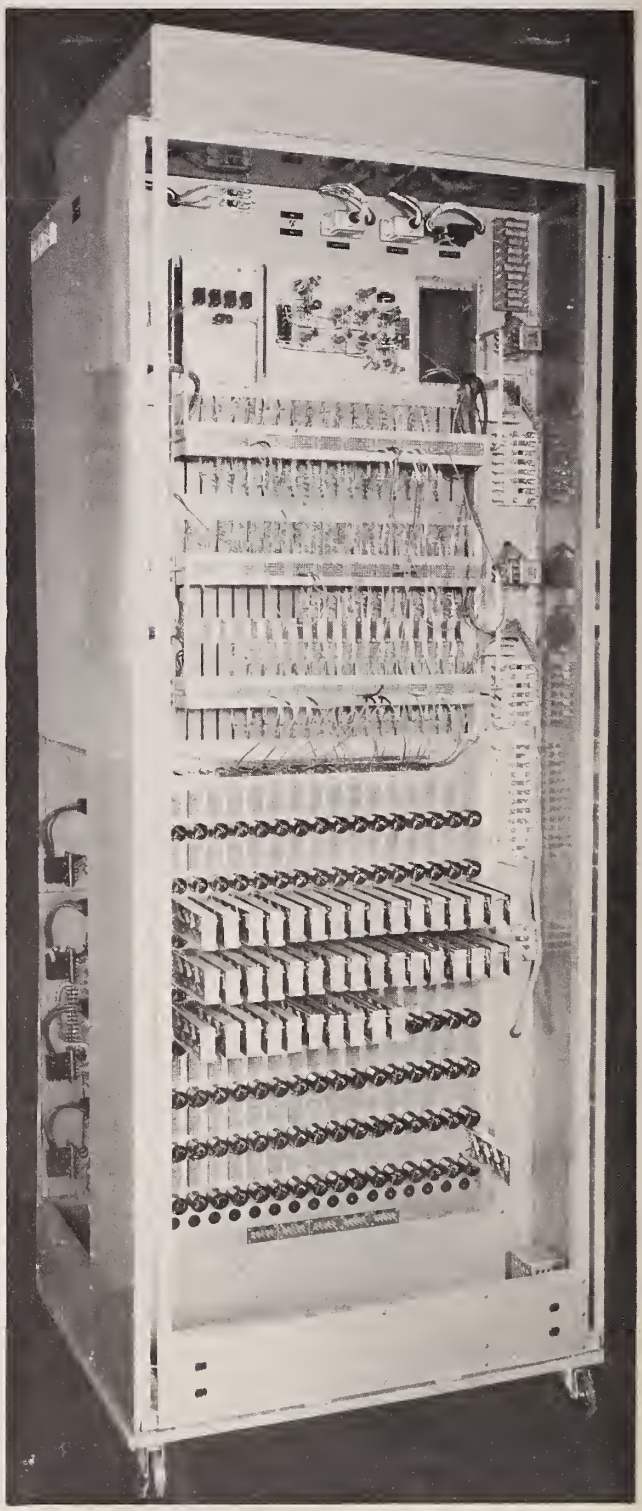

FIGURE 5.10. *Front view of diode-capacitor memory rack.*

After the individual elements of the system were tested, a laboratory model was built containing 16 words of 4 bits each. With this model in its final form several successful lengthy tests of storage were carried out. On five occasions the unit was left running for 3-day periods and found to have the correct information at the end of that time.

Results with the laboratory model have been sufficiently promising to make it desirable to test something more nearly approaching a full memory. A prototype is now in construction which will be attached to the SEAC and tested in the same way that the electrostatic memory prototype has been tested. For the diode-capacitor memory, the unit is designed for a capacity of 256 words of 45 bits each, but only 128 words of 8 bits each are being built as a start. Since the words have only 8 of the customary 45 bits, it will not be possible to operate the SEAC exclusively from this trial memory unit. However, since the SEAC can operate from both the acoustic and the diode-capacitor memories in integrated fashion, it is possible to do extensive testing of the new memory by using test routines stored in the acoustic memory. If all goes well with these tests, the memory will undoubtedly be expanded to a useful size.

Figure 5.10 shows this unit as it is now being assembled, and figure 5.11 is a view of the 8-bit memory package. It will be noticed that very little attention has been paid to compactness in this construction. Quite the opposite, the units have been deliberately separated to permit access to them during experimental runs. Bracketing estimates on a full-scale memory assembly indicate that 1,000 words could be packaged in 20 to 50 ft^3.

In describing the operation of the memory no mention was made of the access rate that can be achieved. That is because the access rate is primarily limited not by the memory elements but by the external circuitry. The characteristics of the diodes in the memory unit determine the ratios that were discussed, but within wide limits the operating rate can be selected by selecting the capacitor size. This generalization becomes more limited if diodes are used which have large capacitances in themselves, such as the selenium diodes, but for low-capacitance diodes the generalization is reasonable. In the experimental equipment being built the active part of the basic cycle will be a 3-μsec period, during which reading and writing occur. This cycle is repeated every 6 μsec, the remaining 3 μsec being used for recovery of the transformers in the selection matrix.

The diode-capacitor memory has several advantages. An especially nice one is that there are no very weak signals or sensitive leads. The minimum signal is of the order of a volt across a few hundred ohms, and all of the selection is truly digital. There are no analog voltages to be derived, and all characteristics of the materials are bounded on only one side. That is, there is no limit on the upper end of the diode characteristic: it does not have to be matched to the other diodes in the circuit. The memory is very rapid, access to random information is possible at well over 100,000 words per second, and it can be very rugged in construction where this is an important attribute.

On the other hand, it has several disadvantages too. A large number of diodes is required for a large memory. A memory of 25,000 bits requires 50,000 diodes, and it is an open question whether 50,000 diodes will give reliable operation even when the design allows them wide tolerances. Still, three years' experience with some 15,000 diodes in SEAC indicate that such operation is not entirely out of line. In addition, schemes have been worked out for rapid maintenance testing of such a large memory by a form of marginal checking which should permit replacement of drifting units before they cause trouble in computing. However, so many individual elements to be assembled will of necessity make for higher fabrication cost. Present estimates indicate that for the same capacity the cost would be approximately twice that of a mercury acoustic memory or a Williams-type electrostatic memory (the units constructed at NBS indicate roughly equal cost for these two types).

It would appear at present as though the proper balance among cost, performance, and serviceability is something that only more experience can indicate. It is hoped that the prototype construction will provide the experience necessary to determine this balance.

5. FACTORS AFFECTING MEMORY DEVELOPMENT

The *reliability* of a memory system is hard to define, since the reliability of a completed piece of equipment is so much a function of the engineering. In this laboratory it is believed that the

simplicity of the device is related in a most fundamental way to the reliability and this concept has proved to be a useful yardstick. Of the three memory systems discussed here, the diode-capacitor is the simplest, the acoustic is median, and the Williams is the most complicated. On the basis of sensitivity to voltage changes and external interference, the diode-capacitor is least sensitive, the acoustic is median, and the Williams is most sensitive. The log book for the acoustic memory in operation with SEAC shows occasional runs of nearly a week without adjustment or complaint from the mathematicians; the longest run on record for the Williams (with SEAC) is 11 hours. The most recent model of diode-capacitor memory has made a run of 269 hours without error in the laboratory. These figures should not be taken as indicative of the limits of reliability, since the engineering is constantly being improved on all these memories.

The *access rate* is more easily defined and is given in terms of the maximum number of randomly selected words per second. These speeds are, of course, variable over a considerable range at the designer's choice. The acoustic memory, being serial, is basically slower than the parallel memories, but it is perhaps inadequately realized today that high computation rates can still be accomplished using the acoustic memory, by careful organization of the machine. How fruitful this approach is, of course, depends greatly on the type of service for which the computer is designed. In SEAC, the acoustic memory is designed to deliver an average of about 6,000 random words per second, but with optimum programming it can deliver about 20,000 words per second. The figure for the Williams memory in SEAC is about 20,000 random words per second, although systems have been built that are as high as 60,000. The basic speed limitation is the amount of current which can be supplied to the storage spot without causing serious interaction between spots; a circuitry problem is to increase the speed of deflection and still maintain accuracy of final point. The model B prototype of the diode-capacitor memory is designed for 80,000 random words per second in laboratory operation and may be converted to 125,000. In operation with SEAC, however, the speed will be 20,000 words per second, since this is the fastest rate at which the machine can accept information. In order to change the speed, one need only change the capacitor; the limits in speed for the diode-capacitor memory are not being pushed as yet.

Figures for the relative cost of these three memories can only be given for the initial installation, although it is apparent that maintenance costs ought to be considered. The price for acoustic memory used in SEAC is about $1.50 per binary digit, including all access circuitry, amplifiers, and hardware. The cost of the Williams memory in SEAC is about the same, although extra engineering features, such as extensive shielding and elaborate power supplies, would raise the cost. The diode-capacitor memory will probably cost in the range of 2 to 4 dollars per bit, more than half of the cost being in the price of diodes.

Briefly comparing the relative size, weight, and ruggedness of these three memory systems, they are all more or less in the same class of size, running between 20 and 100 ft^3 for 50,000 bits of memory proper. Compact etched-circuit designs have been made for the diode-capacitor memory. In weight, the memories are again in about the same class, although the acoustic and Williams need, in general, more mechanical structure. In ruggedness, however, the Williams memory appears to be basically less desirable than the other two systems, since the cathode-ray tube and gun is a relatively fragile device. Under severe vibration the deflection accuracy is almost certain to be adversely affected.

It should be apparent that each of these memories has its own attractive features. It may be, for example, that the Williams will turn out to be most suitable for very high-speed fixed installations, the diode-capacitor most suitable for very high-speed mobile machines, and the acoustic best for serial high-speed general-purpose equipment. Development and evaluation of all these memories are therefore continuing at this laboratory, with the SEAC acting in a most useful capacity as a tool for evaluation.

6. Input-Output Devices for NBS Computers

J. L. Pike and E. F. Ainsworth

1. INTRODUCTION

The SEAC input-output equipment had a modest beginning with modified Teletype equipment which included a tape reader and keyboard for input operations, and a printer and punch for output operations. It was, of course, realized that there was much to be gained by adding magnetic recording devices to speed up the input and output processes, thereby putting the various parts of the machine in better balance. The requirements for this equipment seemed to fall in two classes. In one case data must be temporarily stored outside the computer but re-inserted later in the course of the problem. The other class requires a system of bringing new input to the computer and removing output. While there is an added convenience in having both of these features provided by a common system, the requirements are not entirely compatible. In the case of SEAC it was considered expedient to use separate types of equipment for input-output and overflow memory. The principle was to provide equipment that would make the computer a more useful tool but with emphasis on simplicity and reliability. For these reasons the reel-less tape drive for auxiliary memory was developed at the Electronic Computers Laboratory. Temporarily this was used as high-speed input-output but the reel-less method of tape storage did not provide the desired convenience. A cartridge loading wire recorder mechanism was chosen for high-speed input-output because of the great convenience this provides. The compromise here was in high-speed start-stop performance and the possibility of multichannel recording. In combination these two mechanisms provide a system with the desired characteristics.

To prepare input data, punched paper tape is used as an intermediate step. This makes the wire recording equipment simple as the wire can be moved continuously when the tape information is transcribed to the wire. The paper tape can be easily checked and corrected, eliminating the necessity for error-checking circuits on the keyboard.

2. INPUT PREPARATION

Figure 6.1. shows the complete input-output system in use with SEAC. Units A and B are used to prepare and check the punched tape. These units are Teletype apparatus with modified code and keyboard.

Unit C, called an "inscriber," comprises a punched tape reader, a drive unit for the magnetic recording wire cartridge, and control circuits for automatic transfer of the information from tape to wire. Counters control the tape reader so that the recording is put on the wire in blocks of eight words. Between these recorded blocks enough space is automatically provided to allow the computer sufficient time to acquire its next read-in instruction. Whenever the computer program requires that the wire be stopped and started between blocks, the counter is set to provide a much longer space.

Unit D is a punched-card-to-wire-cartridge converter that is now under construction. A machine (IBM Type 63) which converts punched card data to punched tape is commercially available but none is provided for the NBS computers at present.

3. MACHINE INPUT-OUTPUT

A modified Teletype apparatus (unit E) communicates directly with the computer and is used primarily for troubleshooting the computer or the program. The principle followed in adapting Teletype to SEAC was to avoid any modification to the basic mechanism that would affect its reliability. The code bars were reground and filled in, where necessary, to alter the code. Most of the function

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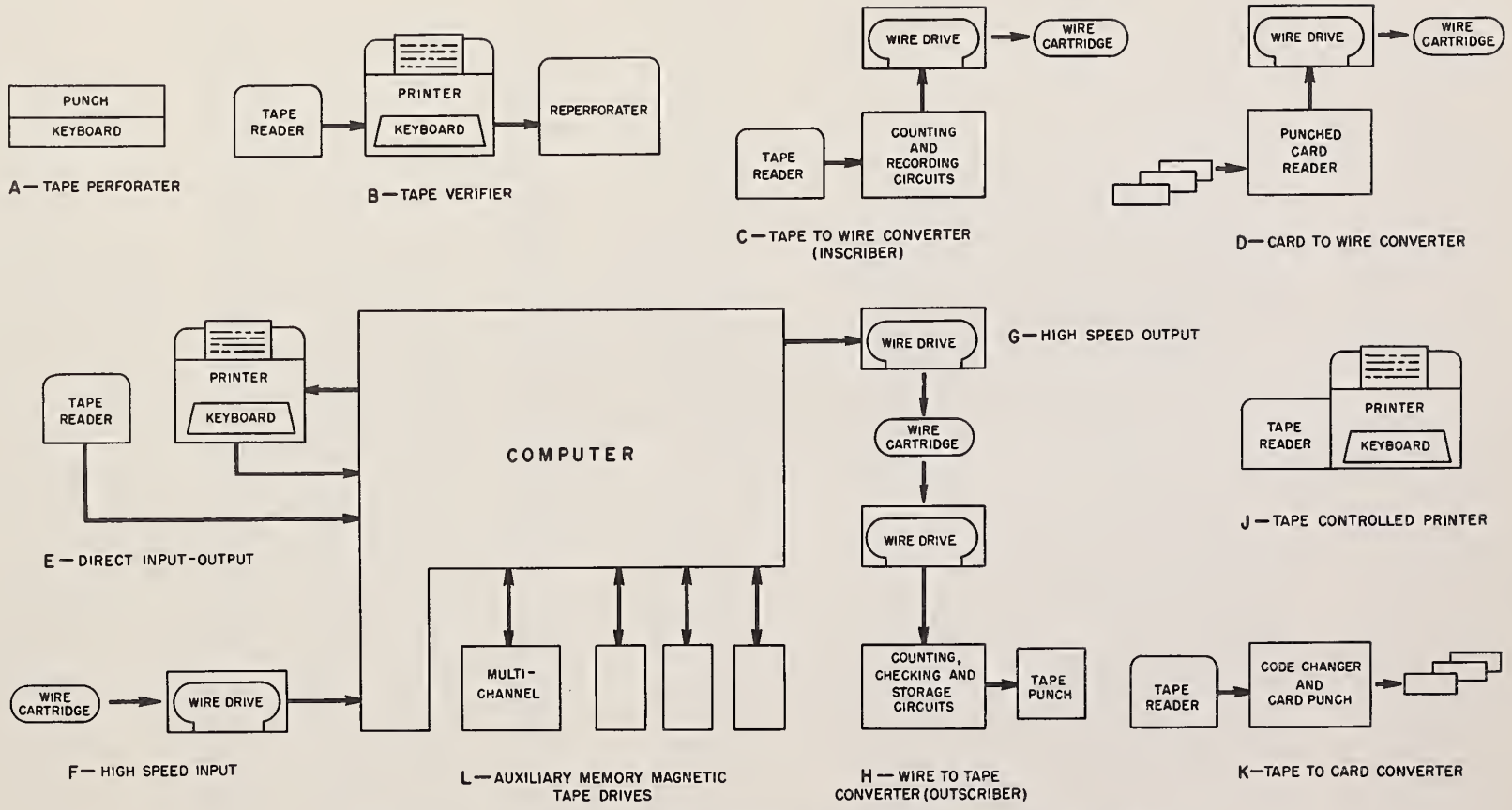

FIGURE 6.1. *Input-output and auxiliary units for the SEAC and DYSEAC systems.*

bars were removed, and those remaining were modified with respect to the code they recognize. A Teletype transmitter-distributor provides the timing signals to the computer for output printing at the standard Teletype rate.

A modified Flexowriter replaces Teletype equipment for DYSEAC input-output. The Flexowriter system comprises a punched paper tape reader and a punch built into an electric typewriter as one complete unit. Its operating rate is slightly higher, 10 characters per second as compared with 6 for Teletype. The Flexowriter also has the added advantage of being easily adapted to give such additional features as upper and lower case letters, 6- or 7-unit code, color change, and tabulating.

Teletype equipment is well suited to serial input-output as it includes distributing and collecting apparatus. The Flexowriter, since it is not designed to be operated over long lines, handles the units in each code character simultaneously on separate lines. In many types of computer circuitry, of course, this is a preferable arrangement. The Teletype machine in use with SEAC for some 3 years has proved quite reliable, and it remains to be seen whether Flexowriter equipment will provide similar reliability.

Unit F is the wire drive that provides high-speed input to the computer. It accepts the cartridge prepared by unit C or D. All of the cartridge loading wire drives in the system are modifications of the mechanism of an office dictating machine. Figure 6.2. shows the input and output wire drives in the SEAC console. The wire is contained on two spools in a closed metal cartridge. This cartridge, shown in figure 6.3., carries a pointer traveling over a replaceable paper scale on which the data recorded on the wire may be labeled. These units can be switched to manual control so that the wire may be positioned to the data desired for input, and then switched to computer control so that when the program calls for input from this particular source it is automatically read in. Typical read-ins require only a few seconds, the speed of the wire being 120 times as fast as when it was recorded from Teletype tape.

A cartridge can contain about 14,000 words, which is enough to load the high-speed memory many times, and is the equivalent of over 7 hours of Teletype tape reading. Many programs may be put on the same cartridge, and a particular one can be located by use of the position indicator on the face of the cartridge. A device useful to the operator is a loudspeaker connected to the wire drive amplifier, which allows information groups to be located exactly. It also seems to give the operator a great deal of satisfaction to be able to hear something going on.

The mechanical part of the office dictating machine was purchased from the manufacturer unwired and without the associated electronic equipment. One modification required for computer input-output use is a change in the motor capstan size to produce the desired speed, in this case 8 ft/sec for both forward and reverse. The auxiliary equipment, units C and H, require a very slow wire speed, less than 1 in./sec, for transferring information to or from punched tape. For this application a second motor with gear train is mounted in line with the regular motor. The shafts are coupled by means of an over-running clutch so that either speed may be obtained by simply switching on the appropriate motor. Another important modification is the replacement of the recording head used in the office machine with a higher quality head. The mounting requires modification to fit the small space available, but this head produces a much cleaner wave form in the recorded pulses.

The cartridges as supplied for office use contain about 1,800 ft of stainless-steel wire (3.75 min at 8 ft/sec). This has been replaced with plated wire, which allows about twice the pulse packing. The recorder mechanism contains two oiled cork disk clutches operated by solenoids to engage the forward and reverse spool driving shafts. These solenoids are wired directly into vacuum-tube control circuits. The clutches require periodic cleaning, oiling, and adjustment to assure their reliable operation.

Considerable trouble has been encountered with the latching system for holding the cartridge into the wire drive mechanism. In many cases the latches became disengaged while the wire was running and allowed the cartridge to jump away from the spool drivers, usually causing the wire to break. Recently, the mechanism for engaging these latches has been modified in such a way as to eliminate this trouble. There is still occasional breakage of wire which is not explained. The plated wire, which gives better recording performance, is somewhat weaker mechanically and more brittle. Considering the great increase in operating efficiency offered by this system, the occasional trouble with

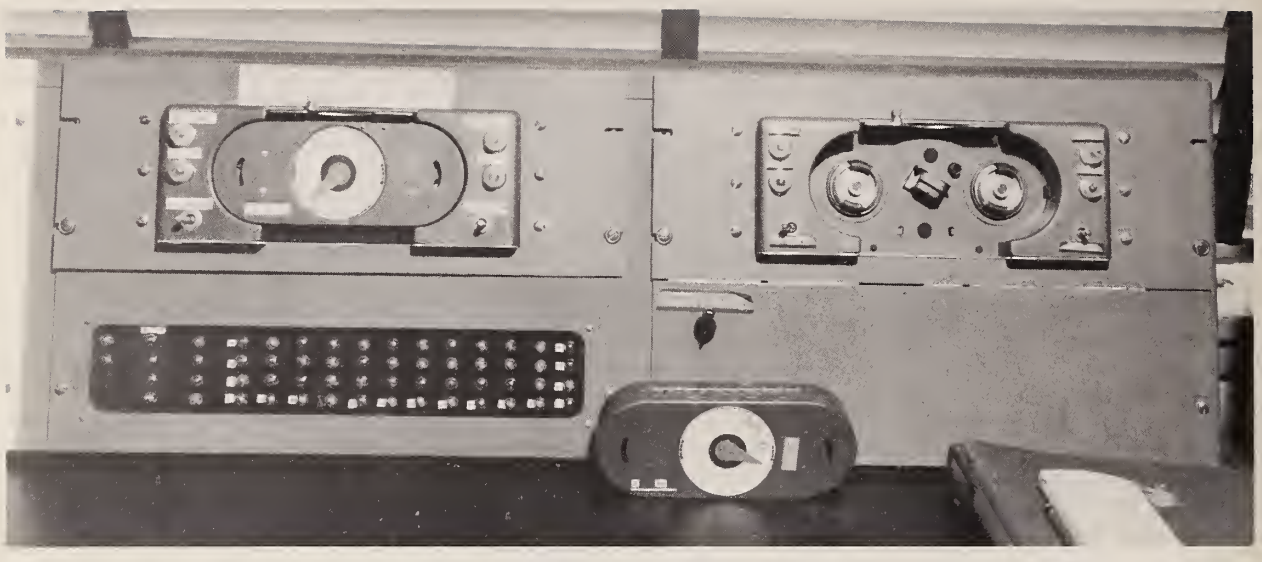

FIGURE 6.2. *SEAC input and output wire drives.*

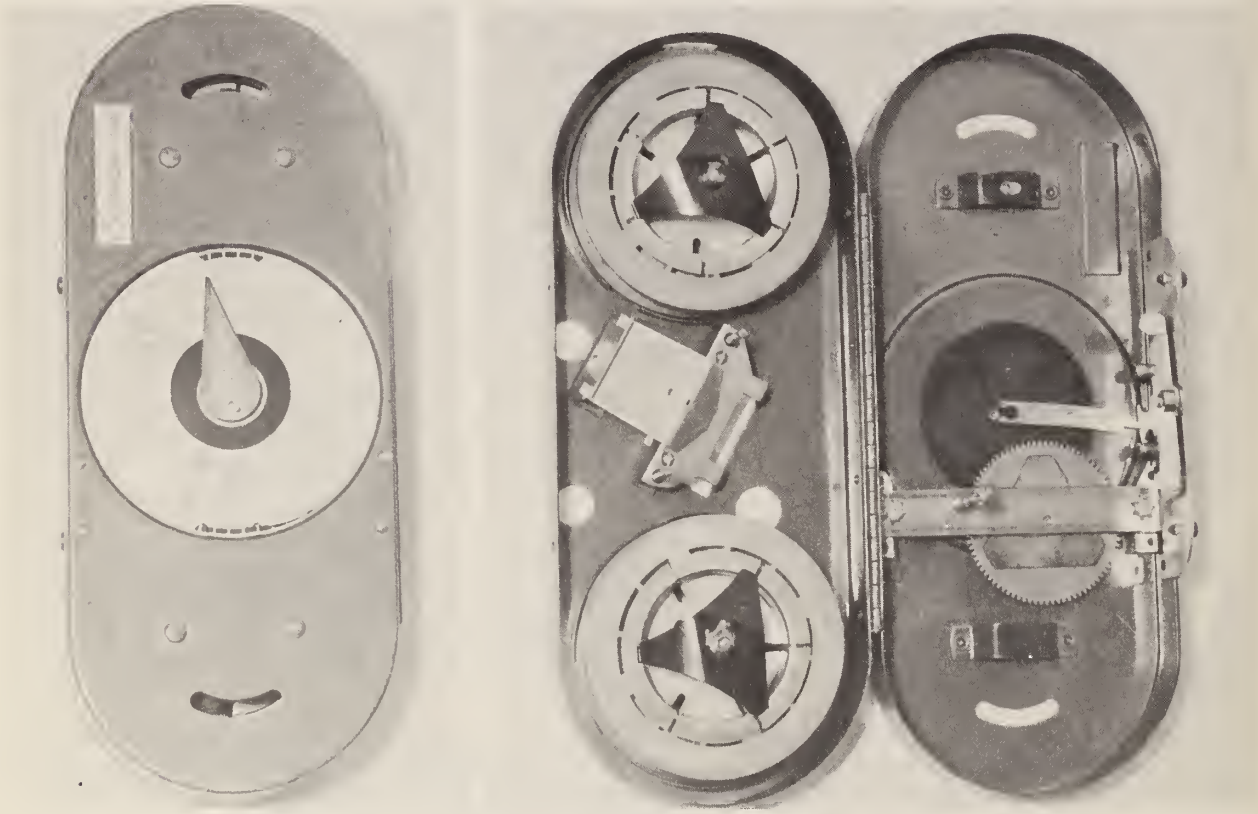

FIGURE 6.3. *Recording wire cartridge.*

FIGURE 6.4. *Magnetic wire to punched tape converter and tape-controlled printer.*

broken wire is tolerable. When the wire does break, the cartridge can be rewound with new wire, or the broken wire can be spliced and used if the spliced area is avoided.

As in the original operating system of the wire recorder, the engagement of the clutch solenoid closes contacts which start the motor. This gives an acceleration to the wire from standstill to full speed in approximately one second. Adequate gaps in the recorded program must, therefore, be provided to allow the wire to reach full operating speed before it enters the information area. This means that it is most efficient to use this device for input or output which requires few stops and starts between long runs of data. The output wire drive (unit G) is identical to the input unit. Both SEAC and DYSEAC have provisions for the use of several input and output wire drives, which may be automatically selected in the program.

4. OUTPUT AUXILIARIES

When a cartridge of wire has been recorded with computer output it is placed in unit H, called the "outscriber."[1] Here the wire is driven continuously at about 1 in./sec, and its information is transferred to a punched paper tape. Since this form of wire drive does not give quick start-stop operation, the use of a printer or card punch directly with the outscriber would require special provision for carriage return or card change. This could be done either by leaving large gaps in the recording at the expense of computer output speed or by providing a huge intermediate storage. The use of punched tape avoids these difficulties. The outscriber includes a shift register which both determines when enough pulses have been received to form a character and stores the information as the count progresses. A second register holds the information being punched as the first register accepts new information. Since the computer prints in blocks, it is easy to sense the gap in the recording between blocks and examine the shift register at this time. If the shift register contains information, an error is indicated and the wire automatically stops. The tape is produced by a Flexowriter punch operating at about 12 characters per second, the rate established by the wire speed and pulse spacing. Wires recorded on the inscriber (unit C) may be checked by reproducing punched tape on the outscriber. A second outscriber, now under construction, is based on the new Teletype punch which will operate at a speed approaching 60 characters per second.

The outscriber and inscriber are both designed to operate with either 4 bit or 6 bit binary coded characters. By using the 6 bit character, alphabetic information can be read in and out of the computer. The code for the letters is chosen so that the alphabet appears in ascending numerical order to facilitate alphabetical sorting. There need be no change in the computing machine to enable it to use both letters and numerals, but the input and output must be interpreted differently.

Punched tape may be converted to page print or punched cards. The printer now in use (unit J) is a modified Flexowriter. This includes a tape reader and electric typewriter operating in SEAC code. In the four-bit base-sixteen code used, the sign can be identified only by its standardized position in the word. A stepping relay counts characters so that at the sign position the code is modified. Another stepping relay counts words to control the carriage return. Figure 6.4. shows the outscriber and printer, units H and J of figure 6.1.

Two machines are provided for converting from punched tape to punched cards (unit K). One machine used a Flexowriter tape reader and relay code changer to operate a card punch (IBM type 24). The second machine is commercially available (IBM type 43) and is used practically unmodified.

5. AUXILIARY MEMORY

The equipment described thus far is concerned with the flow of information to and from the computer. Auxiliary memory requires a different form of external equipment which is provided by magnetic tape drives (fig. 6.1., unit L). A computer such as SEAC has a necessarily limited storage capacity in its internal high-speed memory. With many types of problems this is a serious limitation and requires that information be transmitted out of the computer for storage to be reentered into the computer later in the program. This means that the speed with which the storage and reentering can be accomplished is a major factor in the over-all operating speed. A common technique is to employ

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R. C. Haueter, Auxiliary equipment to SEAC input-output, Review of Input and Output Equipment Used in Computing Systems, Joint AIEE-IRE-ACM Computer Conference, S-53 (March 1953).

high performance servomechanisms to achieve rapid start, stop, and reversal of a magnetic medium in the recording device.

For SEAC a system was devised to solve quickly and economically the problem of overflow memory without the use of servomechanisms. As seen in figure 6.5., the device for moving the magnetic tape comprises a capstan turning continuously and a jam roller which may be moved into contact with the capstan by means of a solenoid. The complete tape drive mounts two of these capstan assemblies rotating in opposite directions with the recording heads between. The tape hangs loosely over the capstans and is accelerated to its running speed, typically 5 or 10 ft/sec, when the jam roller is engaged. The total acceleration time, including the solenoid lag, is about 5 msec. Individual motors (dual-speed hysteresis) drive each capstan and are so mounted as to allow easy replacement by motors of a different speed. The capstans are of smooth stainless steel and give very little friction against the loose tape. The jam roller is simply a small ball bearing with a nylon tire pressed on it. The solenoid which moves the jam roller about 0.010 in. is adapted from the coil of a short telephone type relay.

The units now in use with SEAC employ single-channel bipolar recording with a-c erase on 1/4-in. tape. The tape is stored in a "tank" where it falls in random loops from the capstan as seen in figure 6.6. This tank is formed by the space between two plates separated by slightly more than the tape width. Separate tanks are used to receive the tape from each capstan, with the ends of the tape prevented from passing through the mechanism. There is no tendency for the tape to twist parallel to the faces of the tank and therefore no opportunity for snarls to form in the tape. The SEAC units can be operated with up to 3,600 ft of tape in a tank 19 in. wide and 3 ft high. A single tank may be used with the tape spliced into a continuous loop, but the use of more than about 400 ft in this way has proved difficult. The use of wider tape and multichannel systems is entirely feasible. At the present time the tapes are run at 5 ft/sec and recorded at 110 pulses per inch. The tapes have been run satisfactorily at 10 and 15 ft/sec, but at the present time the SEAC cannot handle pulses as fast as these speeds would present them. The amount of information that can be put on a tape depends on the manner in which it is recorded. When it is required that the tape be able to stop between blocks of information, enough blank space must be provided for it to do so. This space is provided in the recording operation by delaying the recording until the tape has had time to move sufficiently. At most, SEAC can record or read eight words per instruction. If the program calls for more than eight words at a time, there is no point in leaving the blank space every eight words. Only enough space is needed to allow the machine to compute the next read-in instruction. The system is designed so that the programmer may state in the instruction whether he wants the longer space provided or not. Recording without these spaces is called "compressed" recording. Using the compressed recording 12,000 words can be recorded on a 600-ft tape; uncompressed, 8,000 words. The same compressed recording system is used on the output wire units, where the long start-stop time makes it even more effective.

One trouble encountered in the use of these reel-less tape drives came from the strong tendency of the tape (acetate base) to acquire an electrostatic charge as it passed through the drive mechanism. Such a charge can be strong enough to cause the tape to stick to the tank near the top until it backs up into the mechanism and is damaged by a sharp fold. This trouble is completely eliminated by the use of a tape now available with an evaporated aluminum film on the back surface. If Lucite is used for the tank, it must also be treated to prevent the accumulation of static charges on its surface.

Another problem arises from the presence of flaws in the magnetic tape. Commercially available tape has many small imperfections in the magnetic oxide coating which are quite undetectable in ordinary audio work but which cause loss of one or more digits of information in pulse work. With multichannel apparatus there are several systems for avoiding these flaws, but since we are operating a single-channel system, an attempt was made to improve the tape surface mechanically. The Electronic Computers Laboratory developed a technique that is quite effective in eliminating flaws from ordinary tape. The serious flaws are caused by nodules of the oxide that project above the normal surface and lift the tape away from the head. They may be removed by passing the tape surface across a properly shaped scraping blade. This technique has been successful only with the product of one manufacturer, since the physical characteristics of the flaws vary with the manufacturing method.

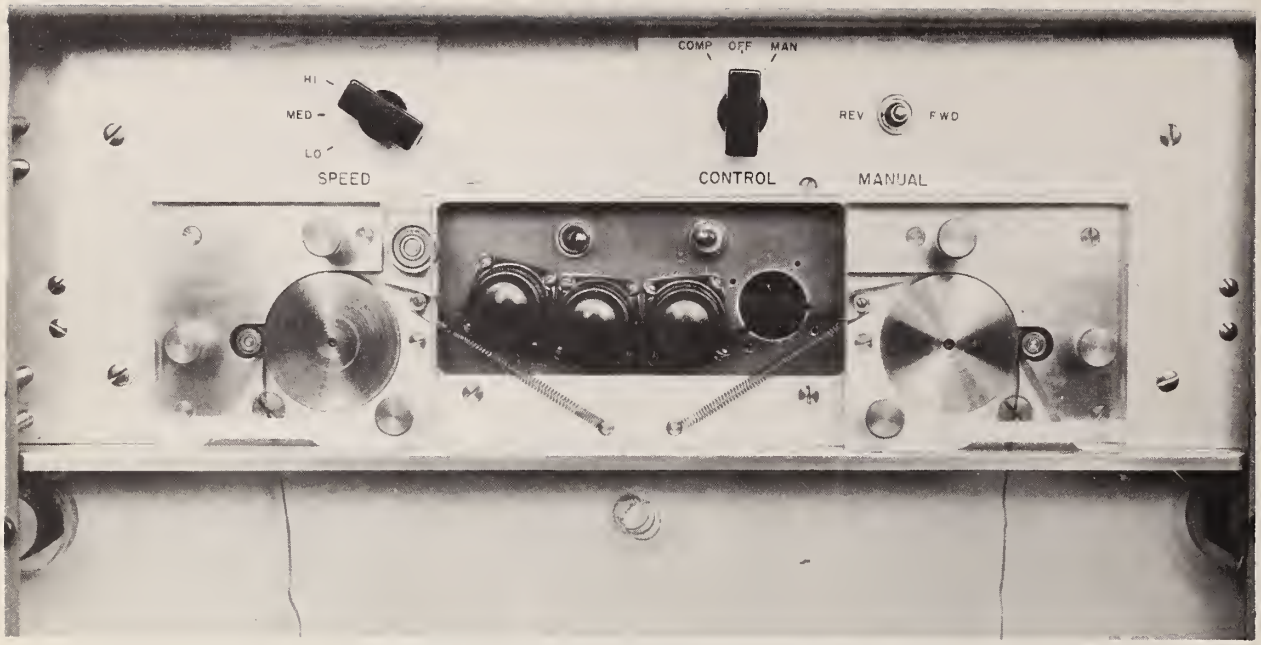

FIGURE 6.5. *Tape drive capstan and jam roller.*

FIGURE 6.6. *Auxiliary memory tape drive.*

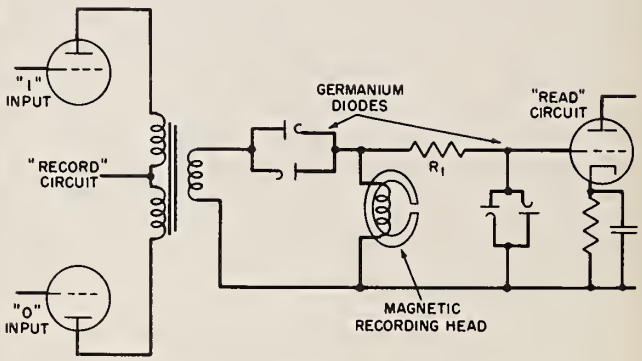

FIGURE 6.7. *Recording and reading circuit.*

A third difficulty arises from the use of plastic tape with this storage method. If a 1,200 ft tape is left immobile in the tank for a day or so, it develops kinks at the loops which will cause the tape to jump away from the recording head at the light pressure that is preferable. If the pressure pad is tightened to eliminate this trouble, it causes increased wear on the tapes and heads. A fair compromise may be made by using only about 600 ft of tape in a tank. If a base material of improved resilience is developed, an increase in storage volume will be facilitated. The simplification derived from avoiding the reel inertia problem is paid for by inconvenience in changing tape. This is quite tolerable when the device is used only as an auxiliary memory.

A completely different type of tape drive is the multichannel Raytheon unit. The mechanism used with SEAC is very nearly a stock model made by the Raytheon Manufacturing Company. It has six heads across 1/2-in.-wide tape and moves the tape at 45.5 in./sec. The mechanism employs a high-speed electromagnetic friction disk brake system applied through a differential to give high-speed performance to the capstan. The tape is stored on servo-controlled reels. A low-inertia moving frame carries several idlers that store a loop of tape, and the position of this frame provides the reel servo input.

As used with SEAC, one of the channels is a synchronizing or marker channel. It contains a digit for every place in the information channels where a digit may be recorded. Synchronizing digits are placed on the tape once and not changed thereafter. At the present time we use about 80 digits per inch.

The other five channels are used as information channels. Information is printed on or read from only one channel at a time inasmuch as SEAC is not wired to receive more than one channel. Since the position of information digits is determined by the position of the synchronizing pulses, information digits are always at specific places on the information channels. This makes erasing unnecessary as new information may be superimposed on the old. Recording is always to saturation, so that writing a digit of the same polarity as the one last recorded at this spot has no effect, but writing one of opposite polarity will change the magnetic ondition of the tape at this point to saturation in the other direction.

Another advantage of having the synchronizing digits permanently recorded is that flaws on the tape can be avoided. If synchronizing digits are placed only where there are good recording spots on all channels, then only these good parts of the tape will be used. One of the ways this may be accomplished is as follows: The channel which is selected for synchronizing is printed with pulses at the packing rate to be used in the final condition. Next, the second channel is printed by reading from the synchronizing channel to actuate the print circuits. The reading amplifier gain is reduced so that no marginal pulses are accepted and only fully normal pulses will cause printing. Thus, the second channel will contain pulses only when there are good recording spots in the synchronizing channel. The process is repeated, with the third channel being printed from the second, and so on until all channels have been recorded. Now the last channel contains pulses only where there are good recording spots in all other channels. The synchronizing channel is erased and reprinted from the last channel so that it now contains pulses only where there are flawless recording spots in all channels.

A unique system is used to connect the magnetic recording head. The head is not switched but remains connected to both the reading and recording circuits at all times, as shown in figure 6.7. The nonlinearity of the diodes and the great difference in signal level between that developed across the secondary of the print transformer during printing and that developed across and head during reading are the basis of this circuit. At the low level of signals developed across the head during reading, the diodes present a high impedance to either polarity. The series diodes therefore prevent the transformer secondary from shunting the head with a low impedance. The resistance R1 must be small compared to the low-level resistance of the diodes in the grid circuit, so that a large part of the voltage developed across the head will appear at the grid of the amplifier.

During printing the diodes present a low resistance to signals of the greater amplitude. As their resistance is low compared with the impedance of the head, the series diodes do not appreciably attenuate the signal to the head. It is desirable to have the resistance R1 high compared with the grid-circuit diode resistance at the print signal level so that only a small part of the print

signal will appear at the read amplifier. It is also desirable for the resistance to be large as it will limit the amount of current that flows in the grid circuit.

Another application of the nonlinearity characteristic of diodes is in the synchronizing channel amplifier. This channel must be read while printing is carried on in other channels. The signal pickup from printing in an adjacent channel is about 50 times that of the actual snychronizing signal. Diodes are put in the grid return circuits of some stages of the amplifier where this lower impedance for the larger signals will cause the amplifier to have less gain for the unwanted pickup.

Two of the channels have been connected so that the forward direction for them is reverse for the other channels. In effect, this gives an endless loop of any length up to four tape lengths. Time for reversing is saved on problems where the same information must be read several times. At the time of writing, this unit has been in operation with SEAC for about 6 months and has proved quite satisfactory.

At present the input-output and auxiliary equipments give more maintenance trouble than those parts of the computer which use electronic components. This is partly because of the tendency to operate the mechanical devices near their top speed in an attempt to more nearly match the requirements of the computer. The volume of data handled by computer equipment suggests that more development of mechanical accessories is necessary in order to achieve long life as well as high speed and reliability.

7. Operational Experience With SEAC

J. H. Wright, P. D. Shupe, Jr., and J. W. Cooper

1. INTRODUCTION

SEAC, the NBS Eastern Automatic Computer, has been operated for 23,793 hours since its completion and initial operation in May 1950.[1] Operation was sufficiently successful to result in an operating schedule of 24-hours-a-day, 7-days-a-week, beginning in October 1950. Of the available 168 hours a week, machine time during the ensuing year was divided almost evenly between scheduled problem solution and engineering development. During the second year the engineering groups were allowed only about 25 percent of the total available time.

During problem solution SEAC is operated by the mathematician or coder whose problem is being solved. An engineer or qualified technician is always in attendance during machine operation to assist the operator and to repair the machine in case of machine failure. In a typical month's operation, SEAC has been employed on as many as 50 different unrelated problems from almost all fields of science. The time required for running a problem on the machine varies from a few minutes to many hours, depending upon the nature of the problem and its complexity.

Two of the items listed as single projects have actually been very large, with many ramifications. Together, they have used 57 percent of the 11,000 hours "good time," i.e., scheduled time exclusive of engineering developments, maintenance, or outages between September 1, 1950, and May 1, 1953. These two projects are the theoretical linear programming work for the Office of the Air Comptroller (which sponsored construction of the SEAC) and the work for the Atomic Energy Commission.

In the remaining 43 percent of good time, approximately 84 projects have used the SEAC computer, and about half of these remained in process as of May 1, 1953. In this group the Loran tables were the largest single project, comprising 10 major subdivisions. The magnitude of these problems and the considerable variation in types may be inferred from the following list of six projects which are considered typical:

1. Computation of Loran tables, for the Hydrographic Office.
2. Calculations of missile trajectories.
3. Strength of wing components, for the NACA.
4. Tables of power points in analysis-of-variance tests.
5. Differential equations for nerve fibre reactions.
6. Wave functions for lithium.

The flexibility in scheduling mathematical work is of special interest. During a typical "long" day of nearly 24 hours available for computation, some 2 to 6 runs of 2 to 8 hours each are made. In addition, as many as 12 mathematical code-checking runs are made, some as short as 5 or 10 minutes. Another way of expressing this feature is to state that the original experimental model of SEAC has demonstrated that it can divide its time efficiently among at least 15 mathematical projects from totally unrelated fields of science; i.e., each project can get two or more sizeable runs plus code checking during the week.

Operating SEAC on such widely diversified projects requires a staff of 30 to 40 "digital mathematicians," exclusive of the physicists, engineers, or others who originally formulate the problem and digest the data. This number includes those who translate the mathematical formulation into numerical analysis, program the work for machine solution, and code the analysis into the detailed instructions for the computer.

In addition to the NBS staff, scientists from other Government agencies, as well as from private laboratories and universities, have taken an active part in programming and coding problems that were of special interest to them. This has been necessary both for reasons of security and

[1] Total hours were taken from the SEAC log as of May 1, 1953.

efficiency because members of the NBS staff cannot obtain all the information needed to solve effectively some scientific problems.

2. SEAC TIME SCHEDULE AND OPERATING EFFICIENCY

A typical weekly schedule for SEAC is so arranged that the engineering periods of 4 to 8 hours each are interspersed in the problem solution schedule throughout the day, evening, and early morning periods. A half-hour code-checking period is reserved between 8:30 and 9:00 A.M. 4 days a week. Different projects are scheduled for periods ranging from one-half hour to 8 hours each.

Approximately 25 hours a week are scheduled for the research and development groups to study new computer circuitry, devices, and auxiliary equipment associated with the computer and, consequently, to modify it by installing additional equipment. The following list includes typical modifications and additions to the machine since SEAC has been operating on a regular productive schedule:

a. Williams electrostatic storage system.
b. Three-address circuitry (either three- or four-address operation is optional to the coder).
c. Automonitor system.
d. External selector unit.
e. Magnetic tape handling units.
f. Magnetic wire handling units.
g. Magnetic tape and wire compression.
h. Memory parity check for the acoustic memory.
i. Internal clock phase monitor.
j. Air-cooling unit.
k. Stabilized power supplies.

From the total time available each week for experimental operation and engineering, an 8-hour period is reserved for training engineering personnel in the operation, adjustment, and repair of the machine; for making special studies of parts of the circuitry for possible improvement of reliability; for improving the versatility of the machine or providing features to make the machine easier to operate; for installing certain engineering innovations for ease of adjustment or to simplify fault analysis; for making special studies of components already in the machine or substitute components from the laboratory; and for installing and testing completely redesigned functional parts of the machine. This time is sometimes used to locate an elusive intermittent trouble that is known to exist but is not serious enough to take the machine out of operation during scheduled problem solution time.

An additional 8 hours each week are regularly scheduled for component inspection and adjustment of circuitry in SEAC. The first 4 hours of the preventive maintenance period are used for measuring the characteristics of components from the machine for compliance with operating specifications. The remainder of the time is used for circuit adjustment, calibration, and voltage tolerance checking with diagnostic test routines.

Table 1 contains the distribution of SEAC time for the period from October 1950 through March 1953 and the operating efficiency during the period. Operating efficiency is defined as the sum of

TABLE 1

Year	Quarter	Time scheduled for computation						Time scheduled for engineering	
		Total hours	Problem solution	Code checking	Down time	Idle in order	Operating efficiency	Total hours	Total machine operation
			%	%	%	%	%		%
1950-----	Oct.-Dec.-------	966	49.6	16.3	32.1	2.07	68.0	1,242	56.3
1951-----	Jan.-Mar.-------	1,072	34.1	24.3	41.6	2.42	60.6	1,088	50.3
1951-----	April-June------	1,114	45.5	19.5	29.1	6.01	71.0	1,070	49.0
1951-----	July-Sept.------	1,129	39.4	28.5	29.5	3.11	70.7	1,079	48.8
1951-----	Oct.-Dec.-------	1,594	55.4	25.7	17.9	1.00	82.0	614	27.8
1952-----	Jan.-Mar.-------	1,704	61.9	14.7	22.8	0.59	77.1	480	22.0
1952-----	April-June------	1,722	49.7	14.8	35.2	.35	64.7	462	21.1
1952-----	July-Sept.------	1,627	64.8	9.59	25.6	.06	74.5	581	26.3
1952-----	Oct.-Dec.-------	1,590	72.0	5.47	22.3	.06	77.5	618	28.0
1953-----	Jan.-Mar.-------	1,597	64.3	6.60	29.0	.00	71.0	563	26.1

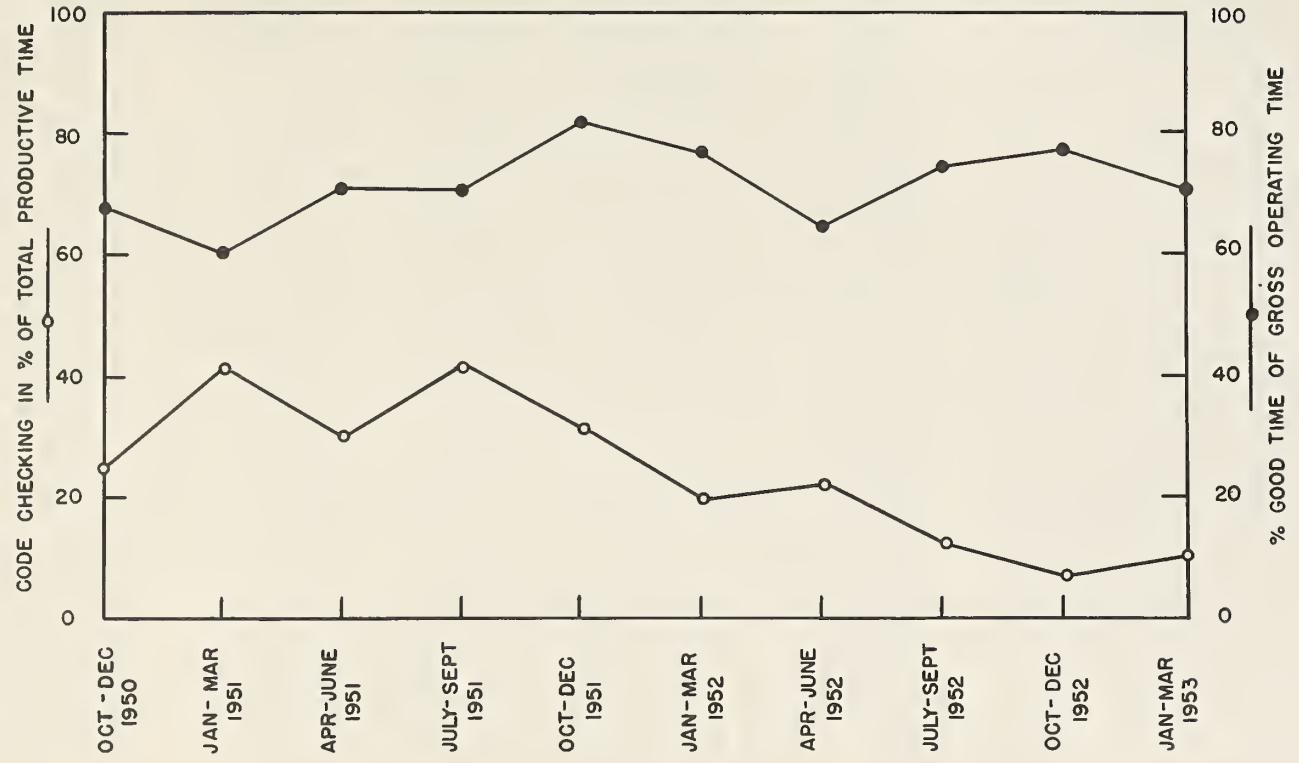

FIGURE 7.1. *Graph showing operating efficiency of SEAC over a 30-month period.*

problem-solution time, code-checking time, and idle-in-order time divided by the total time assigned for computation. Figure 7.1 shows graphically the over-all machine operating efficiency versus time, as well as a plot of time utilized for code checking versus total productive time. The graph shows that operating efficiency has varied as much as 20 percent between 3-month periods. The variations, as well as the fact that over-all efficiency has not increased appreciably since the completion of the original installation, are understandable since SEAC has been a gradually expanding computer and has grown to approximately three times its original size.

The graph also shows an increase in code-checking time during the first months of the operating period. This was at a time when more complex problems were being prepared for the machine. During June 1951, the Automonitor, which enables each instruction (or just certain ones selected by the mathematician) and its result to be automatically printed out, was installed. Initiation of its regular use for the automatic monitoring of programs aided greatly in proving out problem programs. Since then, the addition of the magnetic wire output units, which permit the operator to print automonitor output onto magnetic wire for later printing on an auxiliary high-speed page printer, has materially reduced the time required for code checking from approximately 25 percent to 6 percent of the total machine time assigned for problem solution. Much of the credit for reducing time required for code checking should be given to the NBS Applied Mathematics Division for developing of new programming and coding techniques.

"Down-time" is defined as that portion of scheduled time in which productive time was lost as a result of machine malfunctions during attempted problem solution, diagnosis and correction of a malfunctioning, rerun time required for problems not completed because of machine difficulties, and idle-out-of-order. The average operating efficiency for the entire period reported was 72 percent. The efficiency for the best quarter was 82 percent. Possibly the best week was that of October 27, 1952, with an efficiency of 93.5 percent of 124 hours total assigned time.

Operating efficiency has been reduced by three external factors which were not anticipated when the machine was originally designed. The first is that experimental engineering and design groups made use of periods of time that were interspersed with problem solution time. Although every effort was made to get the machine back in operation on schedule, trouble frequently followed the manipulations of the engineering period, and a portion of the computation period was required to correct the difficulties resulting from experimental work on the machine. This time was charged against the operating efficiency.

Second, SEAC operated for 2 1/2 years on a poor power line, and for many months on a temporary three-phase line which was continuously subject to slow 10-percent line voltage variations and much larger variations as transients. This condition might not have been serious with stabilized power supplies. However, the completely reliable and simple 12-phase power supplies for the SEAC were intended for a line with ±5-percent tolerance, except during brief catastrophes such as electric storms, and were not stabilized.

A third difficulty resulted from periods of operation with the building air-conditioning system inoperative. The system for circulating air throughout the machine was designed to operate with normal room ambient temperatures. During the period that the building was supplied by a temporary power feeder, the building-air-conditioning system could not be operated simultaneously with SEAC.

3. INSPECTION AND CALIBRATION

The 8-hour preventive maintenance period each week is divided between inspection and adjustment of the machine. A typical inspection and adjustment includes several tests, each of which will be discussed briefly. These tests evolved during the early operating life of SEAC, basically because the machine had been very rapidly designed and built, and was in fact an ensemble of first experimental chassis. It is quite probable that a regular engineering design would require less attention.

1. *Vacuum Tubes.* There are 1,424 vacuum tubes in SEAC. Each tube is removed from the machine and tested approximately every 3 months. To accomplish this task, about 120 tubes are tested weekly during each component inspection period.

2. *Germanium Diodes.* The germanium diodes in SEAC are contained in plug-in octal tube bases. Each base contains 4 to 8 diodes connected in 1 of 32 configurations. There are 2,518 diode plug-in units containing 15,159 diodes in the machine. Each plug-in unit is removed from the machine and the forward and back current characteristics measured for each diode on an average of once every 3-month period. Approximately 200 clusters containing 1,000 germanium diodes are removed for test during the 4-hour component checking period each week.

3. *Timing Generator.* The timing system is based on a crystal-controlled sinusoidal oscillator operating at a frequency of 1 Mc. After being split into phases, the output of the oscillator, more commonly known as the clock, is distributed throughout the machine to about 1,000 destinations. Slight changes in timing caused by aging of components and the inherent delay in the distribution system are compensated for by adjustment of series-resonant phase-correcting circuits at the input of each rack in the machine. The outputs of the three-phase amplifiers are checked for correct phase relationship, and the outputs of phase compensators at individual racks are corrected to within 0.02 μsec during each scheduled inspection period. The amplitude of the clock pulse is also checked. The actual need for these checks is not great and would be very slight in a second model of the machine.

4. *Acoustic Memory.* A memory test routine is executed by the machine, and marginal checking techniques are used to locate memory cells whose recirculation amplifiers need adjustment. This test and the necessary adjustments are made once a week.

5. *Input–Output Equipment.* Regular preventive maintenance procedures have been established for the input-output mechanisms. These include routine cleaning, lubrication, mechanical tolerance checking, adjustment, and replacement of worn parts. This work is performed while other machine components are being checked and does not require additional machine down-time.

4. DIAGNOSTIC TEST ROUTINES AND MARGINAL CHECKING

It was early demonstrated in the SEAC that the inherent program—controlled operation provided great flexibility in diagnosis of the operating condition of the machine. Indeed, the control portions of the machine were built prior to the arithmetic and memory units for just this purpose. More than 100 test routines have been written and used since SEAC first started operating over 3 years ago. At the present time only five test routines are used regularly for maintenance and these are stored on magnetic wire cartridges. For convenience, all routines have been adjusted to have the same digit sum, and a standard memory summing routine is provided to check the reading in of each routine. The longest routine may be read into SEAC in less than 10 seconds. Copies are available on teletype tape in case of wire input trouble.

Two of the test routines are for the mercury memory; one for adjusting the gain of the recirculation amplifiers and the other to print out the physical location of any memory errors. There are also an arithmetic test, for which the instructions are maintained without modifications, and a tape test, which has four subroutines for making tests on the magnetic wire and tape units. The fifth is an over-all test, similar to Wheeler's (University of Illinois) Leapfrog Test, which performs every type of operation in every memory address. These and most of the other test routines were designed and coded by the engineers responsible for maintaining SEAC. In addition, there has been a great deal of development of programmed test techniques for the Williams memory, which is not part of the routine service of SEAC.

Experience has shown that it is unnecessary to run test routines at frequent regular intervals in order to determine the operating condition of SEAC. This is due both to the serial nature of the machine and to its almost continuous use by mathematicians. Test routines are run only after engineering work has been done on SEAC or when a mathematician reports trouble. However, once a week, after the regularly scheduled preventive maintenance period, the arithmetic and memory test routines are run while marginal variations are made on the computer voltages. If the tolerances are not satisfactory, the machine is worked on until the trouble is located and corrected.

One of the design parameters included in SEAC circuitry was a 10-percent voltage tolerance. A routine operational check includes varying the supply voltages associated with the computer circuits while the machine is executing a specially coded test problem. The voltage at which the machine fails and the type of failure are noted. If the failure occurs at voltages within the established tolerances, corrective measures are taken to regain normal voltage tolerance.

Although provisions have been made for varying all eight computer circuitry supply voltages, experience and theory show that it is usually sufficient to make tests varying only the −10- and +4-v supplies. The secondary winding of each pulse transformer is returned to −10 v for stages with positive output pulses and to +4 v for stages whose outputs are negative. The positive and negative pulses can effectively be made weaker by varying these voltages, and the weaker stages can then be isolated. Over-all voltage tolerances for the machine may be measured, or individual sections may be tested, while holding constant voltage on the remainder of the machine. No automatic switching has been provided, since such switching, although fairly complex, would not appreciably increase the facilities for marginal checking.

The present method employed for checking recirculation amplifiers in the mercury memory makes use of marginal checking. The machine performs a special memory test routine which alternately loads and unloads the memory, compares the contents of each memory cell with a standard, and prints out the cell number and its contents if there is disagreement. Marginal recirculation amplifiers are located by varying the −10 supply voltage within standardized limits. Changing the −10-v level effectively varies the output pulse level on all vacuum tube stages. Corrections are then made to marginal recirculation amplifiers to regain the established tolerance.

5. VACUUM TUBE EXPERIENCE IN SEAC

Of the 1,424 tubes operating in SEAC and its associated auxiliary equipment, 1,050 are 6AN5's, 248 are 6AK5's (mostly used as preamplifiers in the acoustic and Williams memory systems), and the remaining 126 are a miscellaneous group composed of 32 different types used as auxiliary amplifiers, voltage regulators, sine and square wave generators, and power rectifiers. A further breakdown of these miscellaneous tubes is shown in table 2 in which types occurring in numbers greater than five are listed separately.

TABLE 2. SEAC tube complement

Tube type	Number used	Location
6AN5	1,050	General purpose switching tube.
6AK5	248	Williams and acoustic memories.
2051	10	Auxiliary equipment.
6AG7	8	Williams memory.
6AS7	18	Power supplies.
616	5	Do.
12AU7	8	Auxiliary equipment.
12AX7	9	Do.
12AY7	6	Power supplies and auxiliary equipment.
807	8	Williams memory.
All others	44	----------

Since a standard pulse-repeater stage using a 6AN5 is the basic building block of the SEAC, it was not only possible but very desirable to study these tubes in some detail. The use of a single type of amplifier stage to perform extremely varied logical functions was a new concept, and the usefulness of the concept depended upon how reliably the basic components—tubes and germanium diodes—would operate in actual use. In addition, development of the 6AN5 was partially supported for use in computer applications; therefore information was desired to determine how reliable the tube would be as a computer component over an extended period of operation.

For this purpose, it was decided in December 1950 that regular maintenance procedures would be supplemented by recording data on all tubes used in the computer. Accordingly, every tube used in SEAC from that time on has been assigned a serial number, and readings of its characteristics have been recorded at intervals of about 2 to 3 months. The following information is recorded for each tube:

1. Number of hours service at the time each check was made.
2. Plate and screen current with 6.3 v on the heaters, 0 v on the grid, and 62 v on both plate and screen grids.

3. Plate and screen current with 5.7 v on the heaters, 0 v on the grid, and 62 v on both plate and screen grids.
4. Plate and screen current with 6.3 v on the heaters, −5.7 v on the grid, and 62 v on both plate and screen grids.
5. Plate and screen current with 5.7 v on the heaters, −5.7 v on the grid, and 62 v on both plate and screen grids.
6. The position of the tube in the computers.
7. The reason for tube rejection.

The data-taking process was set up more as an operational procedure than as a research investigation to determine any specific information. Tubes were removed whenever they approached the tolerance limits of machine operation. Hence, in all cases, operation took precedence over the study of tube characteristics. Readings were taken to 2-percent accuracy, but systematic errors in the equipment used indicate that readings may have been as much 10 percent in error at times.

During the 3 years SEAC has been operating, approximately 2,500 6AN5's have been used in the machine, 1,300 having been rejected for various reasons. Rejections are made almost exclusively during the preventive maintenance periods. Operational failures of 6AN5's in SEAC have been very few except during an early period of excessive heater voltages. During the 15-month period from February 1952 to April 1953, for example, it was necessary to replace only 18 tubes during machine operation.

An idea of over-all tube experience can be gained from figure 7.2, which shows a tube survival curve for 1,775 6AN5's used up to March 1953. This group does not include the approximately 700 tubes associated with the Williams memory and short experimental developments. The curve has been plotted by considering batches of tubes installed within 500 hours of the indicated average as single entities and weighting the points on a survival curve for such a group of tubes according to the number contained in each batch. Thus this curve represents a weighted average of survival curves for 16 different groups of tubes, i.e., the percentage of tubes one would expect to survive after a given number of hours.

Figure 7.3 shows a survival curve for 346 tubes installed in the arithmetic and control circuitry of the computer about December 1950. All of these tubes passed the initial SEAC acceptance tests and were used in essentially the same type of circuitry, the only difference in usage being that some stages were operated with plate voltage of 200 v, whereas others used 120 v. (This was done so that essentially the same type of computer stage could be used to drive more gating loads.) The curve shows that the median life of this population is 12,000 hours, which is considerably more than the median life of 8,700 hours for all 6AN5's used in the computer (fig. 7.2). It is assumed that this is due to inclusion in figure 7.2 of data of 6AN5's used for miscellaneous purposes. In addition, early failures in the acoustic memory resulting from stages being operated at excessive heater voltages bring down the average.

The SEAC specifications for the 6AN5 have been varied somewhat during the life of the computer. Originally, the JAN specifications for the tube were the basis for the tube choice and subsequent procurement, although the physical environmental specifications were not needed. Actual requirements were extremely simple, a single plate current measurement generally being sufficient.

Detailed specification of cut-off was completely unnecessary. Originally the screen current was required to be under 8 ma at zero grid volts to limit screen dissipation under some operating conditions. At about 4,000 hours of machine life, since tubes having high screen currents invariably had high plate currents also, it was decided that screen current could be ignored as a specification, although data continued to be recorded. Likewise the maximum plate current at −5.7-v grid voltage was originally specified to be 8 ma, but this specification was also discarded as unnecessary.

The basic specification requires that the plate current at zero grid bias and +62 v on both plate and screen must lie between 25 and 55 ma. These limits were set in the early design phase of the SEAC high-speed circuits and have been adhered to ever since. They represent limits set by the design of the SEAC standard stage with about a 20-percent safety factor having been included in the specification. When SEAC first began operation, heater voltages varied seriously in different portions of the computer. Accordingly, plate currents were measured with heater voltages at 5.7 as well as 6.3 v to make sure that variations in heater voltage did not affect computer operation. If

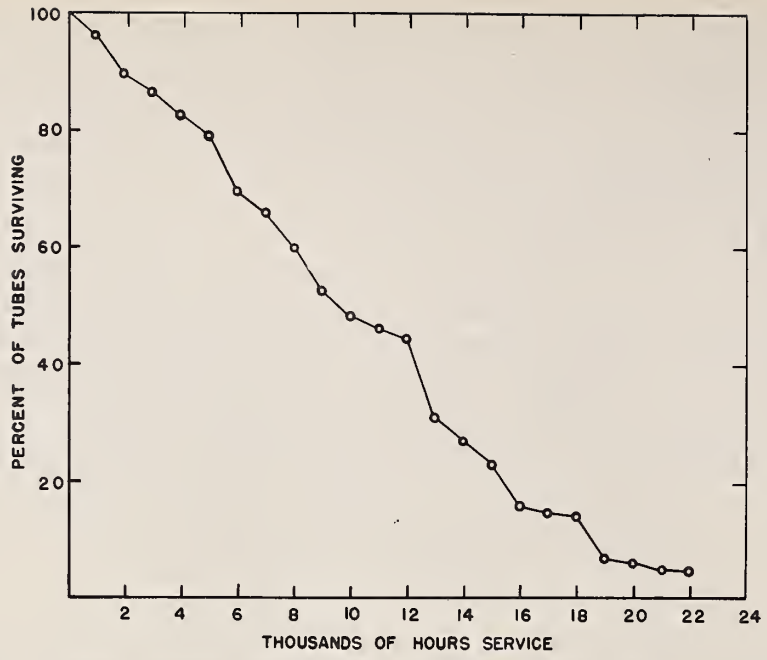

FIGURE 7.2. *Overall tube survival versus time in service.*

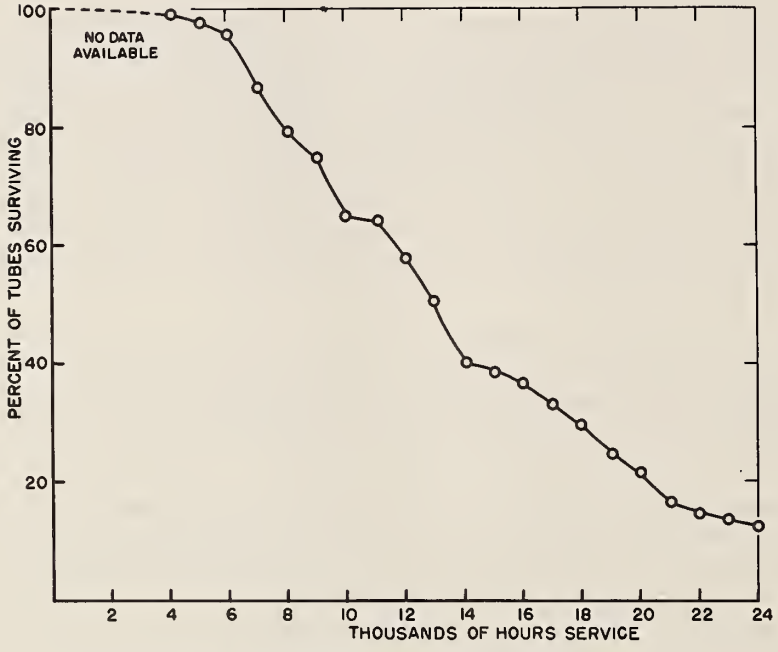

FIGURE 7.3. *Tube survival versus time for 346 tubes.*

there was a drastic change in plate current when heater voltage was decreased, the tubes were discarded as "heater sensitive."

In addition to preventing weak tubes from being installed in stages having low heater voltage, heater sensitivity might provide an indication that the cathode of a tube would soon be rejected for low plate current. Because the maintenance procedure called for tubes to be checked every 3 months, it was felt that such an indication would be useful in rejecting tubes before they failed from low emission. Thus, in September 1951 heater sensitivity was formalized in a specification that called for rejection of all tubes that showed a reduction in plate current of 25 percent or more when heater voltage was changed from 6.3 to 5.7 v. Approximately 55 percent of all tube rejects in SEAC have been made because of this specification.

About 15 percent of all replacements have resulted from other factors. Some were damaged mechanically in handling, some were replaced without defining the failure, and the remainder included grid-cathode shorts and opens, and a few tubes sufficiently microphonic to affect the standard large-signal circuits. The latter were presumably due to momentary contact of the grid and the cathode or loosened particles of the cathode, since the normal spacing is very small.

Figure 7.4 shows cumulative loss curves of 796 tubes from SEAC. These are broken down into the three categories of low emission, heater sensitivity, and other causes. Although some of these tubes were installed before the heater sensitivity test was initiated, the curves show that after 8,000 hours heater sensitivity has been the main cause for replacement.

As the abnormal heater voltages were corrected long ago to be within 3 percent of 6.3 v everywhere in the SEAC, the value of heater sensitivity measurements in eliminating weak tubes that might fade seriously between regular inspections might be questioned. The high percentage of replacements indicated in figure 7.4, for instance, might mean only that the 25-percent sensitivity limit is much more stringent than the 25-ma limit. Unfortunately, the tube program could not be controlled in a fashion to obtain clear-out experimental results. As heater sensitivity came into standard usage as an independent basis for rejection only after the first 10,000 hours of operation, it was not generally possible to study tube behavior as the tubes deteriorated toward and below the 25-ma limit. However, figure 7.5 shows the results of a study made on heater sensitivity up to this 25-ma limit.

For this study, a population of 50 tubes was selected under the following controls: All were installed in the very early period of the machine, at very nearly the same time, and all were rejected after a service period of 10,000 to 12,000 hours. During most of that time, heater sensitivity was not used as an independent basis for rejection. Plate-current history is shown by the solid lines and heater sensitivity by the dotted ones (see fig. 7.5). For each group of curves the middle curve represents the median of the observations, and the upper and lower curves were drawn at the 10-percent and 90-percent points in the ordered data for each particular time interval. These are an aid in considering how characteristic the trends are in the population as a whole. Two features of these curves seem noteworthy. First, the median of the heater sensitivities tends to exceed 25 percent at about two inspection time intervals before the mean of the plate currents might sag to 25 ma. Second, the heater sensitivity varies quite widely; in fact, over a range greater than 10:1.

Another type of presentation has been used for a group of 42 tubes rejected after various lengths of service during the same early period when heater sensitivity was not a standard basis for rejection. In figure 7.6 the data for these tubes are arranged in descending order of their plate currents at time of installation. The corresponding heater sensitivity for each tube is plotted at the same abscissa as the plate current. At installation, the heater sensitivities were small and show negligible correlation with plate currents, as can be seen more directly by a scatter plot of sensitivity versus initial plate current, shown in figure 7.7. Figure 7.8 shows similar data for the same tubes taken at the times they were rejected. The plate currents are again shown in descending order of magnitude. It is apparent that sensitivity alone would be a poor criterion because it would pass 11 of the 32 low-current tubes and reject 5 of the 10 tubes above 25 ma.

It is apparent that heater sensitivity increases with tube age and is cause for some alarm if heater voltages fluctuate. It is not apparent that such data provide a special warning service shortly before serious slumps in plate current. Accordingly, the heater sensitivity test has been temporarily abandoned.

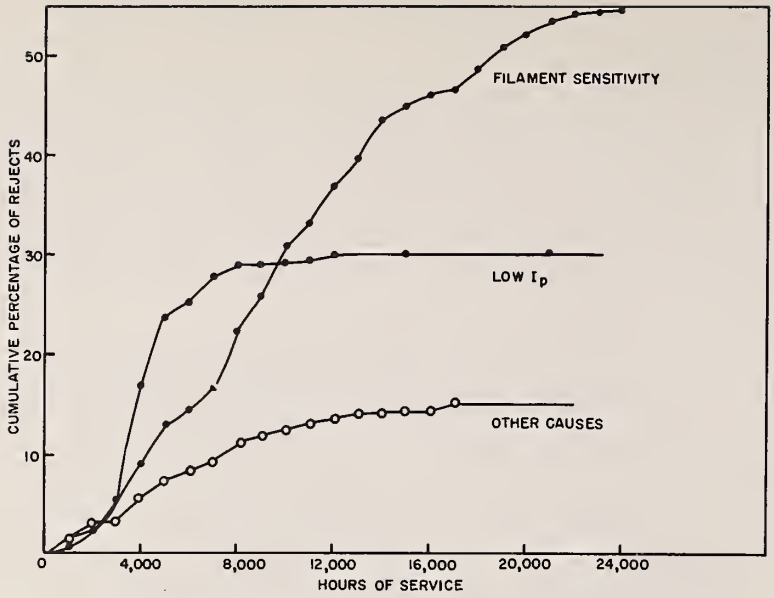

FIGURE 7.4. *Cumulative loss curves for 796 tubes.*

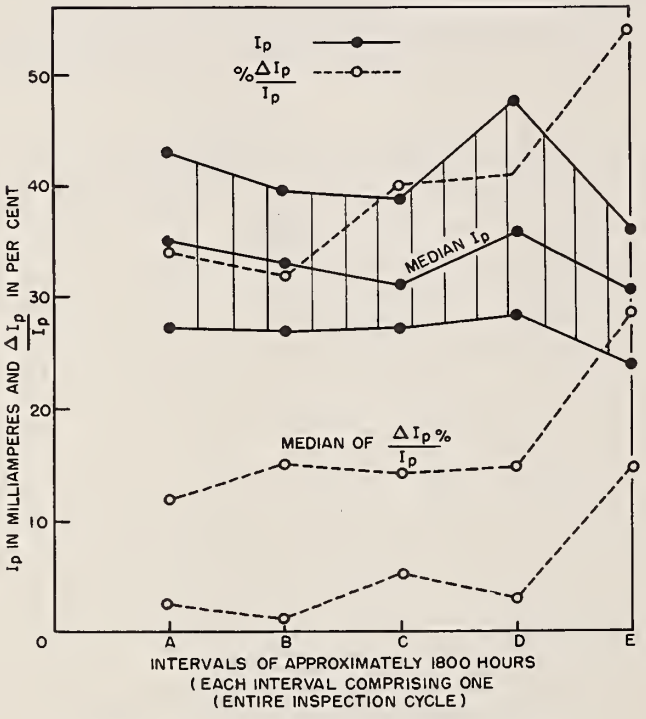

FIGURE 7.5. *Heater sensitivity data for 50 tubes.*

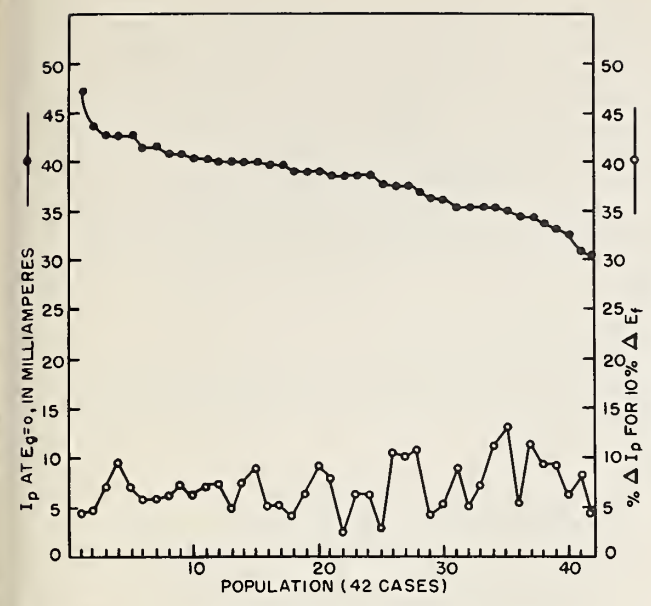

FIGURE 7.6. *Heater sensitivity data on 42 tubes at time of installation.*

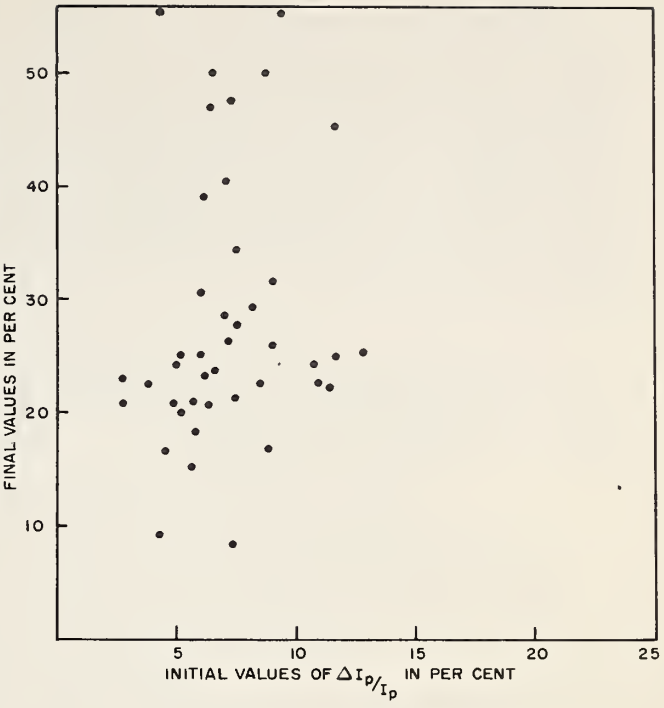

FIGURE 7.7. *Scatter plot of 42 tubes: heater sensitivity versus initial plate current.*

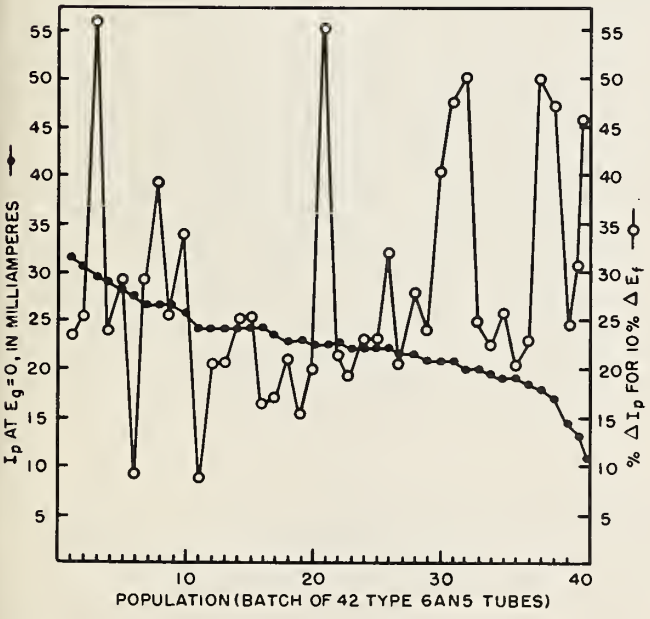

FIGURE 7.8. *Heater sensitivity data on 42 tubes at time of rejection.*

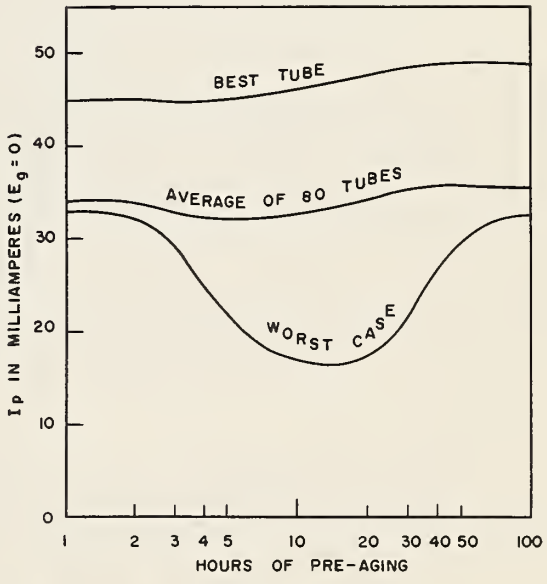

FIGURE 7.9. *Plate current curves of worst, average and best tubes in a lot of 80 during their first 50 hours.*

In the past few years much concern has been expressed over the incidence of "sleeping sickness," or cathode interface, in computer tubes, especially among these tubes which may operate for a large percentage of time at little or no plate current. Under such conditions the impurities commonly present in the nickel supporting base, notably silicon, cause the formation of a semiconducting layer between the base and the active material of the cathode. This may have a resistance of several dozen ohms and result in considerable loss in transconductance. There is also an associated capacitance across the interface of such a value as to make the associated RC time constant 0.1 to 0.3 μsec in common cases. While this phenomenon has never been a problem in the 6AN5's in SEAC (partly because the overshoot of pulses resulting from interface does not hinder the operation of SEAC gating circuits), some experiments on interface have been made. These experiments indicate that the percentage of overshoot due to interface is not noticeably greater for old tubes rejected from SEAC than for new ones.

Table 3 shows the results of these experiments. The percentages shown are percentage overshoot for a 1-v square-wave signal (25 kc) applied to the grid of a tube biased at 3v. Measurements were made by using a high-speed oscilloscope, which required 8-percent correction for the overshoot inherent in the scope amplifier itself.

TABLE 3. Cathode interface measurements on batches of 6AN5 tubes

The voltages listed, 6.3 and 5.0, refer to conditions at time of observation. During regular operation the heater voltage is 6.3.

	Low-duty cycle[a]		High duty cycle[b]		Preaged only		New, unaged	
	6.3 v	5.0 v	6.3 v	5.0 v	6.3 v	5.0 v	6.3 v	5.0 v
Total observed---	20	20	25	25	80	80	80	80
Worst case—%----	2	2	4	21	3	4	2	4
Cases over 2%----	None	None	3	4	3	5	0	5
Cases over 10%---	None	None	None	One	None	None	None	None

[a] 1-percent duty cycle, old tubes replaced in SEAC.

[b] 50-percent duty cycle, old tubes replaced in SEAC.

Early experience with SEAC tubes indicated that some 6AN5's failed at less than 50 hours of service. In order to investigate such early failure, sample groups of tubes were placed in a test rack and readings of their plate current observed every hour. The results of an early study are shown in figure 7.9. The curves show that there is a tendency for the plate current of some tubes to decrease seriously during the first few hours and then to increase for the next 50 to 75 hours. No detailed explanation of this phenomenon can be given here. It seems to be associated with difficulty in activating tubes which have passive nickel for a cathode base. In order to prevent computer malfunction, all tubes installed in SEAC since August 13, 1951, have been aged for 100 hours before installation in the computer. A survey of records kept on tube aging indicates that very few that met specifications before preaging were rejected afterward, and a few that were originally below plate current requirements became usable. The procedure is not intended to salvage tubes but to insure that tubes installed in the computer will not cause computer faults due to this short-term phenomenon.

A few other facts concerning use of the 6AN5 deserve mention. One is that, at least for one scattered sampling of 455 tubes, it seemed that tubes having the higher plate currents at installation tended to have shorter lives. This is probably because tubes having high plate currents have very high screen dissipation which eventually results in poisoning of the cathode by particles of the screen coating. No provision was made in the SEAC for gradually heating the heaters to eliminate damage from thermal shock. The heaters are turned on by a simple switch and turned off the same way. The experience seems to justify the procedure, since a negligible number of tubes have exhibited heater failures and none at all during the year of operation from May 1952 to May 1953.

6. GERMANIUM DIODE EXPERIENCE IN SEAC

The specifications for germanium diodes used in SEAC are listed in table 4 and are comprised entirely of simple d-c measurements. They were set up early in the history of the computer and are based both upon the circuit design used in NBS computers and the results of early experience with various types of diodes. Back currents are measured with 40 v across the diode because this is the greatest back voltage applied to diodes in the computer. Correspondingly, 20 ma is the highest current flowing in the forward direction anywhere in the machine and is thus used as a standard for measuring forward voltage drop. Back current of 750 μa and forward voltage of 2.3 v are used as in-service specifications as these are values that are safe limits for "worse case" conditions in the actual circuitry.

TABLE 4. SEAC germanium diode specifications

	Maximum back current at −40 v		Maximum forward voltage
	Normal	Drifter	
	μa	μa	v
Procurement specification	150 at 25° C 250 at 50° C	100 at 25° C 150 at 50° C	2.0
Installation specification (after shelf-life and soldering).	300 at 25° C	200 at 25° C	2.0
In service	500 at 25°C 750 at 50° C	300 at 25° C 500 at 50° C	2.3

The acceptance and installation specifications were set up to allow for about a 2-to-1 deterioration of the back current and much less deterioration of the more stable forward characteristics in line with early experience. More stringent requirements were placed on diodes whose characteristics varied while under test (hereafter referred to as "drifters") because the back current of such diodes varies with time much more than diodes that do not show this effect. Also, diodes that drifted more than 50 μa in the half-minute inspection period were rejected.

Specifications are given at both 25° C (room temperature) and 50° C for convenience in checking. Temperatures in the computer vary from 25° to 50° C, and it is known that back current values vary considerably with temperature. Hence the procedure now established is to measure all diodes at 25° C and to remeasure at 50° C only those diodes that fail to pass the 25° C specification. In addition, in-service checks are made at 50° C on all diodes used in the mercury memory as the temperature there is higher than in the rest of the computer.

All diodes are checked individually upon delivery and once again after being soldered in plug-in tube bases for installation. Individual records are kept of the forward and reverse characteristics of all diodes, readings being taken on each diode about once every 3 months.

The basic measure of reliability of diodes in the computer is the rate at which diode failures cause machine malfunctioning. Table 5 provides such data for a 2-year period through December 1952, covering 15,819 hours of operation under d-c and signal voltages. The total failures amount to 0.3 percent of the population under study, or 0.02 percent per 1,000 hours. Summaries are split according to diode manufacturer and class of defect. Entries marked "short" simply mean reverse currents exceeding 5,000 μa at 40 v. These data do not include diodes in the Williams Memory, which has not been in regular operation.

The failures of table 5 are few indeed and are offset by the preventive maintenance replacements listed in table 6. These replacements did not interfere with the mathematical assignments of the machine because they were made during regular maintenance periods. Parts (a) and (b) are for two successive periods of approximately 6 months each (approximately 4,000 service hours), each interval being chosen to cover exactly two complete cycles of inspection of the population listed. The

TABLE 5. Operational failures of germanium diodes in SEAC during the period December 10, 1950, to December 30, 1952 (elapsed time: 3,693 to 19,512 service hours)

Manufacturer	High E_f	High I_b	Drift	"Short"	"Open"	Total failures	Total population
X	---	3	3	5	2	13	2,544
Y	---	2	4	3	1	10	7,135
Z	---	---	1	1	1	3	3,030
Unspecified	---	---	---	---	---	13	---
Totals	---	5	8	9	4	39	12,709

TABLE 6. Preventive maintenance replacements of germanium diodes in the SEAC computer

Manufacturer	Cases of high e_f	High I_b	Drift	"Short"	"Open"	Total rejects	Total population
(a) Dec. 1951 to July 1952 (elapsed time: 10,830 to 15,000 hr)							
X	2	8	65	---	---	75	2,544
Y	12	149	98	8	8	275	7,135
Z	23	38	48	3	5	117	3,030
Totals	37	195	211	11	13	467	12,709
(b) July 1952 to Dec. 1952 (elapsed time: 15,001 to 18,905 hr)							
X	1	8	55	10	4	78	2,544
Y	11	97	72	42	19	241	7,135
Z	2	7	44	5	4	62	3,030
Totals	14	112	171	57	27	381	12,709
(c) March 1952 to December 1952 (elapsed time: 13,209 to 18,953 hr) for the mercury memory only exclusive of data in (a) and (b)							
X	3	28	235	3	6	275	1,406
Y	4	15	83	8	3	113	1,001
Z	1	11	22	---	3	37	560
Totals	8	54	340	11	12	425	2,967

over-all replacement rates for the two periods are notably similar, as are the replacement rates by source of diode supply. The diodes from the several manufacturers differ in their susceptibilities to type of defect. Thus the diodes from X are consistently replaced for drift rather than for excessive back current, while the diodes from Y are replaced for excessive back current rather than drift. It should be noted that tables 5 and 6 do not represent a stable population since during this period diodes from X, Y, and Z were used to replace diodes from V, which had shown a marked tendency to drift.

It can be seen from part (c) of table 6 that the diodes in the Mercury Memory suffered a much higher replacement rate than elsewhere in the computer. The memory data have been isolated in the tables because the conditions of inspection there were more rigorous and the conditions of operation involved higher operating temperatures than elsewhere in the machine. Inspections were made almost twice as frequently in the memory as elsewhere in the machine, thus increasing the rejection rate, and as mentioned previously tests were made at 50° C on all memory diodes. It is worthy of note that diodes from X and Y necessitated replacement much more than diodes from Z, whereas for the main portion of the computer the rejection rates for the three types have been nearly identical. Accelerated life experiments have shown types X and Y to be more rapidly damaged under high humidity and temperature than type Z, both back current and drift being affected.

The maintenance records of table 6 do not include 276 replacements made in all parts of the machine, including the Williams memory, during three short periods of poor operation during the summer 1952. During those periods the air-conditioning equipment was inoperative during weather of unusually high humidity and temperature, operating conditions for which the machine was not designed. Ambient temperatures for the diodes ranged from 45° to 55° C. During this period it was also necessary to replace an unusually large number of "spare" diodes, i.e., diodes used for replacements in the computer, probably because of the hot humid weather conditions. No large-scale experiments have been conducted on shelf life of diodes of the several manufacturers, but the general experience is that diodes do not drift outside of the specifications of table 5 even though large changes in back currents have been noted over periods of several months.

The weakest features of performance of the diodes are their tendency towards high back current drift. Actually, SEAC circuitry is extremely tolerant of back current; currents five times greater than specifications are allowable in many places. Furthermore, many of the diodes in the machine are well within the standard specification. Figures 7.10, 7.11, and 7.12 show the distribution of back currents (at 40 v) among large samples of diodes from the three sources of present procurement. An effort has been made to indicate progressive changes in this distribution with elapsed time in service up to 12,000 hours.

Caution must be exercised in interpreting these data because the conditions of computer operation prevented the investigation from being conducted as a controlled experiment. In the first place, a small percentage (see tables 5 and 6) of the diodes were removed after reaching 500 μa and no longer appear in the distribution. Second, at any time of service, data were available for only a portion of the basic population. Finally, the service hours indicated do not correspond to exactly the same period of the computer history for various diodes but are measured from the particular time of installation of each diode. However, the data do represent approximately the first half of the SEAC history (in-service hours), i.e., the period up to June 1952.

These curves show that for types X, Y, and Z the great majority of diodes remaining in service (95, 66, and 82%, respectively) have less than 200-μa reverse current at any time up to 12,000 hours. This is quite encouraging, despite the fact that present-day computers can fail from a single bad component. It is apparent that diodes of type Y tended toward much higher currents than the other types, both in the initial distribution and as a function of time in service. At 12,000 hours, less than 24 percent of the cases are under 100 μa as compared with 48 percent for type Z. It is shown in table 6 that type Y diodes were replaced chiefly for excessive reverse current, and these curves show the same general trend.

In the original design of the computer, 1 $\mu\mu$f of capacity was allowed for each germanium whisker diode used. Response times of gating circuits were thus estimated to 0.01 μsec. Investigations made during 1951 showed that vastly larger effects existed even in quite conservative diode use.[1] When a typical SEAC diode is subjected to infrequent half-microsecond pulses of 20-ma forward current, the initial forward voltage will be much higher than the usual steady state value. This transient is markedly reduced when the duty cycle is raised to 50 percent, i.e., to a 1-Mc square wave. In a typical case the ratio between the forward voltage at 0.03 μsec and that at 2 μsec is nearly 2:1, and is in the range of 3:1 in an appreciable number of cases. For junction diodes the ratio is much larger, about 10:1, with a time constant of about 3 μsec for a commercially available unit.

The reverse current transient is more alarming. When the reverse voltage is varied, the effect is that which one would expect of a 1 or 2-$\mu\mu$f capacitor. However, in the customary use of the diode for switching or clamping, rapid transitions in polarity occur and are the basic conditions of operation. Under these conditions the reverse current is very large immediately after the transition from the forward state, even though the change in reverse voltage is no greater than when the reverse voltage is merely varied.

Figures 7.13 and 7.14 provide a statistical treatment for step-function response measurements made on batches of 175 type Z and 150 type Y diodes that had been in use in SEAC. The readings were corrected for the effects of wiring capacitances, the correction amounting to 500 to 800 μa at

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[1] J. H. Wright, Transient response limitations of various semiconductor diodes (Pennsylvania State University, June 8-19, 1953).

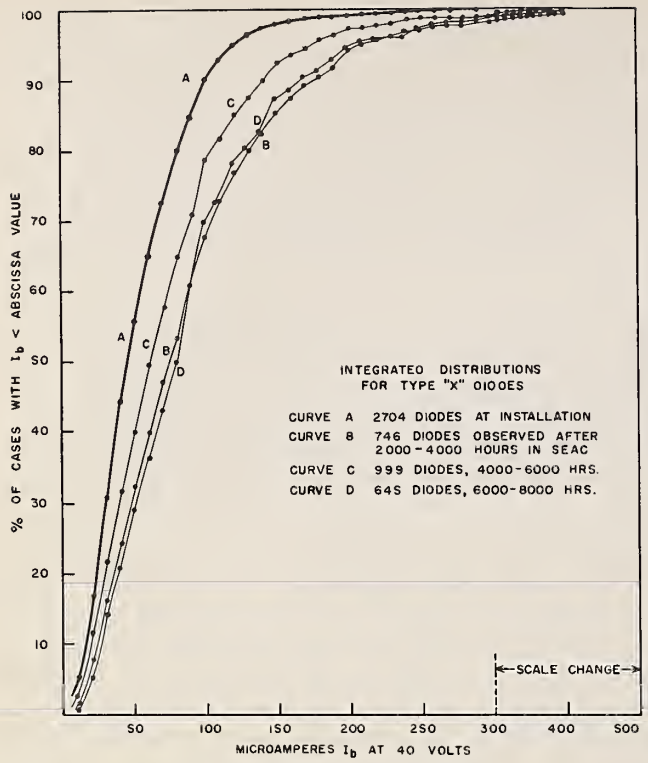

FIGURE 7.10. *Integrated distribution of back currents at 40 volts for diodes of manufacturer "X."*

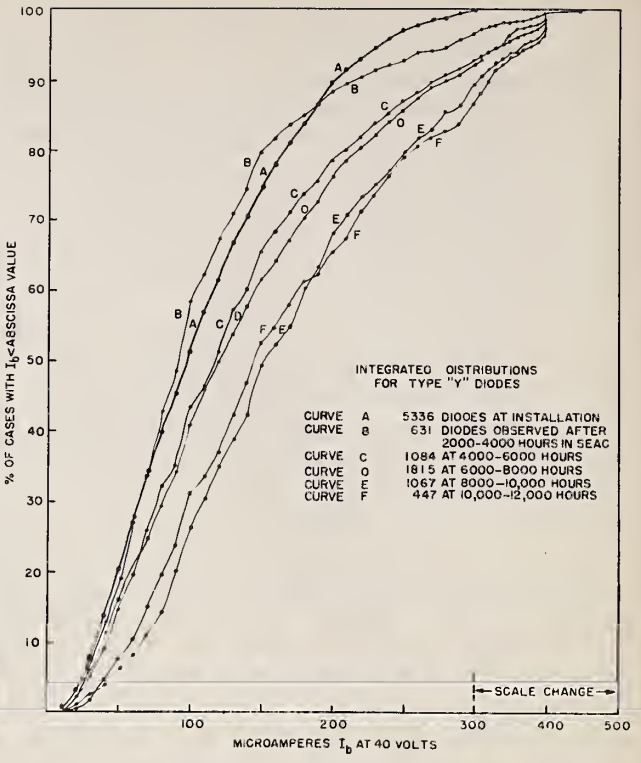

FIGURE 7.11. *Integrated distribution of back currents at 40 volts for diodes of manufacturer "Y."*

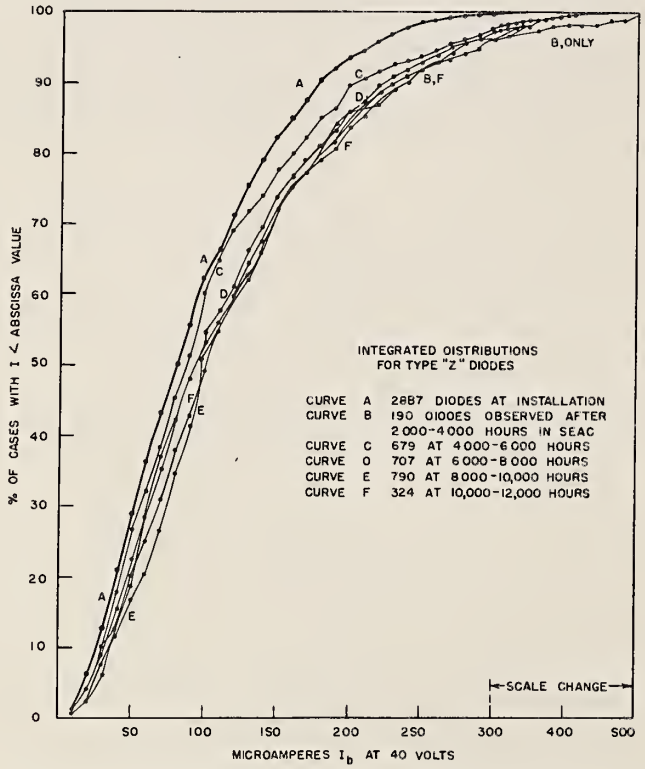

FIGURE 7.12. *Integrated distribution of back currents at 40 volts for diodes of manufacturer "Z."*

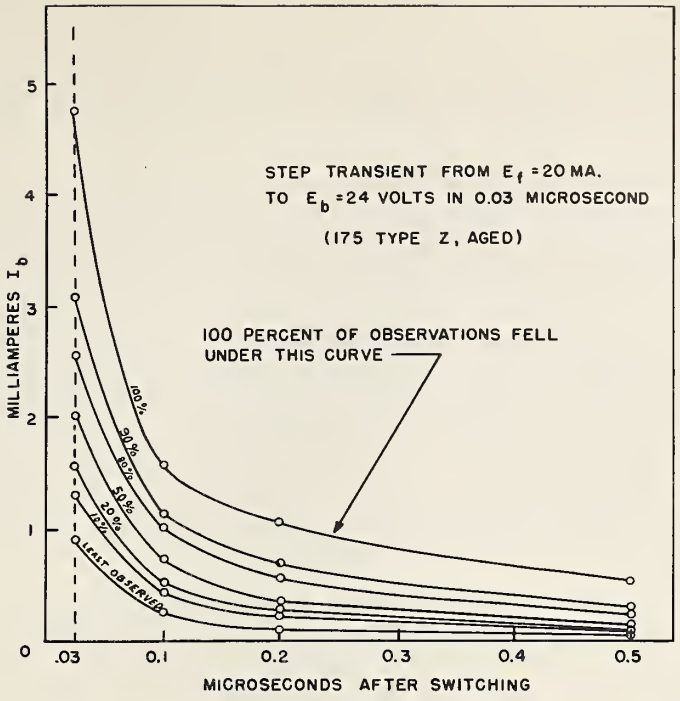

FIGURE 7.13. *Curves of step function response measurements on 175 diodes (type Z).*

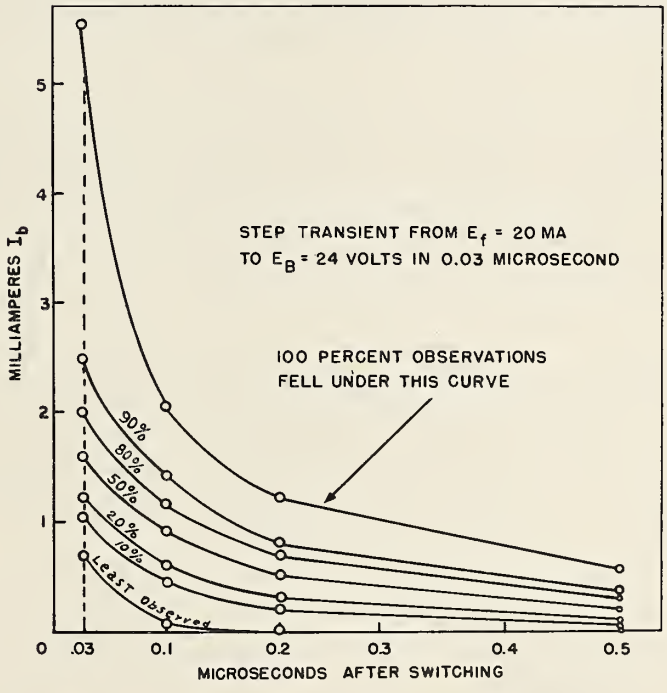

FIGURE 7.14. *Curves of step function response measurements on 150 diodes (type Y).*

the 0.03-μsec points only. The observations were not made at the same time, nor was the service life the same for all the units, being generally in the range of 5,000 to 10,000 hours. The fact that the weekly periods available for removal of SEAC components were short made closer control impossible. As can be seen, the phenomenon is similar for both type Y and type Z diodes. Similar curves for various other types of germanium whisker diodes have shown about the same effects.

Diode experience at the NBS Electronic Computers Laboratory indicates that improvements in diode sealing are desirable for SEAC and are quite necessary for intermittent service or mobile field applications. For those applications a tentative specification involving 240 hours of aging at 65° Centigrade and 98-percent relative humidity has been set. Also, a tentative mechanical specification has been set calling for tests at 30-g peak acceleration with vibrations transverse to the whisker axis.

Experience also indicates that a low-frequency (about 60 cycles) scan test of diodes would be more satisfactory than the present d-c test. Such a test automatically plots the forward and reverse characteristic curves of a diode on the face of an oscilloscope and thus allows for a quick (although less accurate) visual inspection of diode characteristics. Observations by this technique have already been made on 1,400 service-reject diodes. Equipment is currently being built to replace the present d-c tests on SEAC with tests of this type, and tentative specifications have been set up taking account of the shape of the characteristic curve and the trace separation due to hysteresis as well as the previously mentioned d-c specifications.

A 100-ma diode can possibly be used to replace diodes presently used in parallel for disconnects and "bumping" at the transformer output of the typical 6AN5 repeater stage. For these applications much higher reverse currents, both transient and steady state, are permissible. The disadvantage of such a procedure is that two distinct types of diodes requiring different specifications would thus become computer components.

7. EXPERIENCE WITH MISCELLANEOUS COMPONENTS IN SEAC

In addition to tubes and diodes, four other types of components are used extensively in SEAC, namely, resistors, electromagnetic delay lines, capacitors, and pulse transformers. Of these, only resistors, delay lines, and pulse transformers form a part of the actual computer circuitry, capacitors being used solely to bypass places where excessive noise pickup would cause the generation of spurious signals.

Resistors in SEAC circuitry are required to be within 10 percent of their design value. A set of measurements has been initiated to determine how far, in the 3 years of operation, resistors have varied from their initial rated value. The information obtained so far indicates that about 5 percent of the resistors in the computer have exceeded the rated tolerance. These are being replaced as they are discovered. No records have been kept on the number of shorted or open resistors occurring during the 3 years. About 2 or 3 resistors that are suspected of causing trouble are replaced each month.

Troubles with delay lines have been of three types. The most commonly occurring trouble is that the line opens because of corrosion of the solder joint connecting the fine wire of the line to its termination. Other troubles occurring less frequently are shorting between a line and its grounding shield and occasional crosstalk between sections of a long, coiled delay line, supposedly due to deterioration of either the line itself or the associated components. About a dozen instances of troubles of the first kind have been reported in the life of the computer. Troubles of the second and third types occur less frequently. Capacitors have caused very little trouble during the life of the computer and consequently no records have been kept on them.

Pulse transformers have caused very little trouble in SEAC until quite recently. Shorted and open transformers have been extremely rare. The more usual trouble is that the inductance of the transformer decreases as a result of spreading of the laminations in the iron core, the output pulse of the transformer "droops." This has been the cause for replacement of about 20 to 30 transformers during the first 3 years of SEAC operation.

In spite of the intended use of SEAC as an "interim" computer, its record of problem solving stands as concrete evidence of its reliability. A considerable amount of the information compiled in 3 years of combined service and incidental experimental engineering has had its obvious effect on the component design of the DYSEAC. It is believed that operation of the DYSEAC will reflect the improvements that have thus resulted.

8. SEAC—Review of Three Years of Operation

P. D. Shupe, Jr., and R. A. Kirsch

1. PURPOSE FOR CONSTRUCTION OF SEAC

Since September of 1950 the National Bureau of Standards has had SEAC, a digital automatic computer, in almost continuous daily usage. It was originally conceived as an interim computing facility for the use of the Government until a more complete computing system could replace it. Consequently, in constructing the machine, it was intended to put into productive operation as soon as possible a minimal machine that could produce computed results. However, the machine proved quite reliable, and the experiments involved in its design were sufficiently successful that SEAC was expanded and kept in operation as a permanent tool at the National Bureau of Standards. It is the purpose of this paper to present some of the operating experience that has been obtained from the use of this computer and to indicate the ways in which component reliability and maintenance procedures have affected the amount of useful computation that has been obtained from SEAC.

When SEAC was first put into productive operation, the demand for its use was so great that it became necessary to schedule it for operation on a 24-hour-a-day 7-day-a-week basis. As it was apparent that the computer would have to be expanded, at first this time was divided nearly equally between the engineering groups modifying the computer and experimenting with it and the mathematicians who were producing computed results for the various Government agencies. After a year of operation, the engineering time was reduced to about one-quarter of the total available time.

By the use of flexible scheduling, and largely because of the very convenient input-output facilities of SEAC, a great number of concurrent mathematical projects were able to use the computer. This kept a staff of from 30 to 40 mathematicians busy formulating and coding problems. It has at all times been possible to allow both short and long runs on the computer because the time that is involved in switching over from one problem to another can be less than 2 minutes. This has resulted in SEAC being used for over 85 different projects of varying length and of diverse natures.

Interspersed with the productive computation have been periods during which research and development have been conducted on SEAC. These engineering periods are, typically, 8 hours in length. During this time, investigations have been conducted into new computer circuitry and accessory devices. As a result of this engineering work, many new features were added to the computer.

Because SEAC has been used for both computation and development, there has been some decrease in the reliability of the system from what it would have been on a SEAC that was solely a computing device. Examination of the operating record shows that since the initial period of experimentation, this loss of reliability has been small. After engineering periods, the attempt is made to restore the machine to the condition it was in prior to the period. Obviously, this is not always possible. In general, however, the engineering periods on the machine do have the effect of hastening failures that may be intermittent or marginal. Removing components, turning power on and off frequently, and physically dislocating sections of the circuitry for the duration of temporary experimental changes accelerate the failure of components that would perform satisfactorily for a longer time in ordinary operation. An analysis of machine failures, which will be given later, will show the extent to which experimentation has caused failures in machine operation.

2. OPERATING AND MAINTENANCE PROCEDURES ON SEAC

Until recently, when the 168-hour-a-week schedule was relaxed, there were 4 periods per week of approximately 8 hours in length, during which SEAC was used for engineering or during which maintenance work was performed. At all other times, the computer was operated by mathematicians. These mathematicians are responsible for the mathematical formulation of the problem, for the preparation of the code, and for operating the console during the running of the problem on the computer. In

general, they are not expected to be familiar with the logical structure of the computer except insofar as it is manifest in the structure of the operation code.

When a problem is scheduled for solution on SEAC, the mathematician who has prepared it puts the problem into the computer and follows its operation during the time that it is on the machine. As there is no automatic checking provision in SEAC, with the exception of the memory parity check, it is usual for the mathematician to provide program checks or to have printouts on the Teletype at sufficiently frequent intervals to enable him to monitor the operation and to detect any machine errors. It is also usual when the mathematician suspects a failure in machine operation, for him to call a maintenance technician, The information that the mathematician can provide is usually sparse and sometimes misleading. Occasionally, the mathematician gives a report simply that the machine has "hung up." The technician must then determine whether the machine has indeed made an error or whether the error is in the code. Not being familiar with the code, he often first tries to rerun the section that is claimed to have produced the error. If inconsistent results are obtained, it is fairly certain that the machine has made at least one intermittent error.

The maintenance staff of SEAC for three-shift operation consists of three engineers and five technicians. One technician is occupied full time in the construction and repair of replacement parts. At all times when the computer is in operation, there is a technician present and an engineer available for consulting purposes.

In the event of a machine error, it is desirable for the maintenance technician to be able to reproduce the machine conditions under which the error occurred. Unfortunately, the technician is generally not qualified to analyze the code that was running and to detect the immediate nature of the error. In such circumstances, it would be highly desirable if the person who operates the computer were familiar not only with the code but also with the logical organization of the computer. For a machine like SEAC, where the electronic structures are highly iterated, it is necessary only to have a machine operator who can analyze troubles from the logical standpoint and a technician familiar with the electronic nature of the circuitry in order to maintain the machine. The luxury of a standby engineering staff present for consultation in emergencies is a fortunate aspect in maintaining an experimental machine. For computer installations of a nonexperimental nature, this auxiliary staff is not available.

In the event of a failure, the computer is not always removed from problem solution. When the failure is highly intermittent, it is usually more economical of time to allow computation to proceed until such a time as either computation becomes impossible, the error occurs frequently enough to make it possible to locate it, or a scheduled maintenance period occurs.

In the diagnosis of an error, several systematic procedures are used. The most frequently used technique is the diagnostic test routine. There is a library of such routines available to the person doing the "debugging." In general, the test routines are predicated on the assumption that the operator has assured himself that control functions in the computer are operating properly. These routines then perform any one of a number of computations involving special parts of the computer with a diagnostic printout if an error is produced. One routine, for example, loads the acoustic memory with different word patterns and then checks the memory for the storage of these patterns. If an error is detected, the routine prints on the Teletype information that indicates to the technician operating the routine where the failure has occurred in the memory. Obviously, this indication can only be approximate, but for errors that involve such commonplace failures as those due to improper gain adjustments in the recirculation amplifiers, a test routine that will save diagnosis time for technicians is highly valuable.

There is a compensating disadvantage in unqualified use of diagnostic test routines like this memory test. When technicians and semiskilled maintenance personnel use these routines, they have a tendency to rely too greatly on the indications provided by the test routine. When subtle troubles occur for which the test routines were not designed, there is often a significant loss of time involved in trying to find failures where they do not exist. Despite the occasional lapses into indiscriminate use of these test routines, the amount of effort saved by allowing the computer to do its own testing is great.

Among the various diagnostic tests available for use with SEAC are those that check specific portions of the machine: the memory, either acoustic or electrostatic; the arithmetic unit; the magnetic tape auxiliary memory; and the magnetic wire input-output. Other routines cause the computer to perform operations that result in the highly repetitive production of special patterns of standard pulses at test points. These routines are used in conjunction with an oscilloscope for observing the patterns produced. Failure is then detected visually.

Another type of test routines frequently used is written as the trouble is observed. It is usually less complicated than the diagnostic routine and is written to test for a very specific trouble. It is also more effective than the diagnostic routine for troubles that involve the control section of the computer and other troubles of a serious nature that cause radically incorrect behavior of the machine. This type of routine is also of use in the detection of highly intermittent errors where the lower duty cycle of testing of some diagnostic routines might make the detection of the error less probable.

Another systematic procedure for the detection of computer errors which has always been in use on SEAC involves marginal checking. In SEAC, most of the signal outputs of tubes are coupled to the rest of the circuitry by the use of pulse transformers. By varying the d-c voltage to which these transformer secondaries are returned, it is possible to vary the effective output voltage of all tube and transformer stages in the computer. Only two such voltages need to be varied to affect almost all stages in the computer in the same manner. These two voltages can be used to provide an over-all marginal test of the computer or of individual chassis. It is often possible to set these voltages at such a point that only the single weakest stage in the computer will be effectively inoperative. It is also sometimes possible to increase the frequency of intermittent failures by this technique. The marginal check is incorporated as a part of the preventive maintenance schedule.

With one single area of the computer failing under marginal voltage variations, the trouble is traced to the individual component that is to blame. Note that all during this period the operation of the system would be error-free under normal voltages. This forcing of the system to fail allows trouble shooting to be performed on the computer during "cheap" time, that is, during a maintenance period rather than during time that would otherwise be scheduled for computation. For components that are approaching the failure condition gradually, as in the case of vacuum tubes whose transconductance may gradually decrease, it is possible to anticipate failures during maintenance by marginal checking. The marginal check gives a nondestructive quantitative measure of the operating tolerances under which the machine is working. Another reason for the marginal check is to allow computer troubles to be debugged one at a time. If the failures are allowed to accumulate between maintenance periods, the situation will arise where there are two or more faults present in the computer simultaneously. The difficulty in locating the source of malfunctioning under such conditions is vastly greater than the effort that would be needed to isolate them individually. The computer represents a very powerful tool for use in debugging many parts of its own internal structure. However, to allow the computer to lapse into the degree of disrepair in which more than a single trouble is present at a time is to make it generally very difficult to use this powerful debugging tool.

For over 2 years of operation, SEAC had no automatic checking facilities. All checks that were performed were programmed. For example, one checking procedure that was devised enables the computer operator to minimize the amount of time that is lost in the event of the detection of an error. Once every half-hour or hour during long runs the entire contents of the high-speed internal memory are recorded on a magnetic wire unit. Under the control of the program, this recording is then read by the computer and a check sum of the recording is compared with the corresponding check sum of the contents of the memory. If the sums agree, it indicates that the recording has been made accurately, and the machine automatically resumes computation at the point in the main routine where it left off. The memory-recording routine requires only eight memory cells and is completed within less than 2 minutes when transferring the contents of the 1,024-word memory. If the operator makes use of this routine, he can insure that in the event an error is detected the time lost will be no more than the time since the last memory recording was made. To resume computation at the point of the last memory recording, he simply reads the recording back into the memory. In a matter of a few seconds, the computer is recalculating in the part of the routine that occurred after the last recording.

Not only is this routine useful for minimizing lost time due to errors, but it enables short periods of machine time to be used effectively in the solution of long problems.

At the beginning of 1953 it was decided to incorporate some degree of automatic checking in one section of the computer that gave less reliable operation than other parts of the electronic circuitry. It was found that transient errors involving the change of a single binary digit would occur in the acoustic memory. Often, these errors could not be attributed to the failure of any single component. On the other hand, such errors were relatively rare in the main body of the computer which used more conventional circuitry. This was a case in which checking circuitry could be built that would have a margin of reliability considerably greater than that of the circuits being checked. The parity checker that was built incorporated standard SEAC-type tube and transformer stages with diode gating. After its initial experimental stage, this checking circuitry was able to detect the great majority of errors in the acoustic memory. Because of the experience and success gained with this addition to the computer, investigations of the possibility of incorporating automatic checking for the input-output and electrostatic memory circuits are now under way.

3. ANALYSIS OF THE SEAC LOG

Whenever there is a failure in the operation of SEAC an entry is made in the Operations Log. These entries may be made either by the operator or by a technician or engineer. A record is also kept of all modifications to the computer. Because of the transient nature of some errors that the computer makes, it is not always possible to identify the cause with certainty. Therefore, it is often the case that an entry will simply record the loss of computing time with no explanation of the cause. At the end of each week, figures are obtained for the operating efficiency of the computer. Operating efficiency is defined as the ratio of productive computation during assigned time to total assigned time. The remainder of assigned time after productive computation constitutes machine errors, overrun of engineering time into scheduled operating time, and downtime due to debugging.

A graph of the operating efficiency of SEAC for 3 years of operation is shown in figure 8.1. The average efficiency for that time was 74 percent. The ratio of code-checking time to productive computation time is also shown. Only a small portion of operating time is needed for code checking because of such features as the Automatic Monitor and the high-speed wire output, which enable each operation to be monitored as it is performed and to be recorded rapidly on an output unit for later transcription to printed copy with auxiliary equipment.

In order to understand the manner in which various failures have contributed to downtime on SEAC, the operation log may be analyzed. Naturally, some of the failures that are of a transient nature cannot readily be analyzed. However, a recent period of a month has been selected during which a large percentage of the failures that occurred during scheduled operation were capable of analysis. Of a total of 477 hours scheduled for computation during that month all but 112 hours produced error-free calculation. The operating efficiency of this period was therefore 77 percent. Only about 12 hours of lost time could not be attributed to specific faults. The data from this analysis of the operation log are shown in table 1.

In the first column is the cause of the failure. The second column gives the number of individual cases during which computation was delayed due to a component failure. The numbers in this column are considerably greater than the total number of times that debugging was necessary because in many cases the machine errors were of a trivial nature that were easily detected or corrected by the operator. The third column gives the amount of downtime that was caused by these machine errors. The fourth column of the table gives an indication of the most common length of computation time lost as a result of the failure. The last column gives the number of individual components the failures of which caused the number of computer failures shown in the second column.

The table shows that during this time there were three diode failures. These were bad diodes that were not found during the preventive maintenance diode check. There were eight individual times during which these three diodes caused machine failures. All other failures among over 15,000 diodes were dectected during the preventive check before they could cause machine failures.

TABLE 1. Nature of failures on SEAC for 1 month

Cause of failure	Number of machine failures	Total downtime		Most common length of downtime		Number of components that failed
		hr	*min*	*hr*	*min*	
Diodes	8	6	05	0	30	3
Vacuum tubes:						
6AN5	3	2	30	0	45	2
6AK5	3	2	35	0	45	2
Input-output and magnetic tape	29	14	20	0	30	----------
Pulse transformers	14	17	30	1	00	3
Experimentation:						
Parity checker	26	11	40	0	25	----------
Other	10	9	05	0	55	----------
Electrical connections	4	6	50	1	30	4
Switches	2	3	30	1	45	2
Adjustments:						
Acoustic memory	7	2	10	0	20	----------
Magnetic input-output units	9	5	25	0	30	----------
Mechanical equipment	13	4	45	0	20	----------
Auxiliary equipment	18	5	20	0	15	----------
Miscellaneous	5	6	40	---------		----------
Undiagnosed	20	13	30	---------		----------

During this period of a month there were four tube failures that caused six failures in machine operation. The two 6AN5 tubes came from standard SEAC pulse repeater stages. They were rejected for low emission. The two 6AK5 tubes were removed from the acoustic memory.

The most frequently occurring fault in SEAC operation involved the input-output equipment. In general, no component was at fault. Rather, mechanical variations that are difficult to control in such equipment were at fault. Because there is no automatic checking for the input-output, incorrect data input often is not even detected after the computation has progressed to the point where programmed checks occur, although for ordinary reading of program information, a checking routine is common. This minimizes the lost time from such input. The most costly input-output failures occur when the final computed results are incorrectly transferred to the output medium.

The failure rate shown for transformers is not typical in SEAC operation. It does, however, serve to indicate the extent to which certain components cause loss of computing time all out of proportion to their frequency of occurrence. The transformers that failed during this time were all of the standard type used in the SEAC pulse repeater stage. For over 2 years of operation, transformer failures were so rare as to make it unnecessary to do any checking of them. Furthermore, it was correctly anticipated that the most common type of failure that would occur was catastrophic in nature, and it is not easy to anticipate such failures by testing the suspected transformers. As a result, when these three transformers developed intermittent openings or shorts in their windings, they caused a great deal of trouble before they were located.

It has already been mentioned that some failures in SEAC could be attributed to its use as an experimental machine. Shortly before the month in consideration, it was decided to install a parity checker for the acoustic memory. The new circuitry was debugged and installed in the computer. It began to detect many "errors," some spurious and others of such a nature that they would not cause computer malfunctioning. Eventually an error was found in the construction of the new unit, but not before it had caused a great deal of lost time on the computer. Now that this circuitry has been thoroughly debugged, it is performing with the reliability that was anticipated and has succeeded in locating most of the transient errors in the acoustic memory. The remainder of the downtime attributed to engineering was caused by overruns of engineering time into scheduled computation and by changes that were made during engineering that were mistakenly not restored until after the engineering period had ended.

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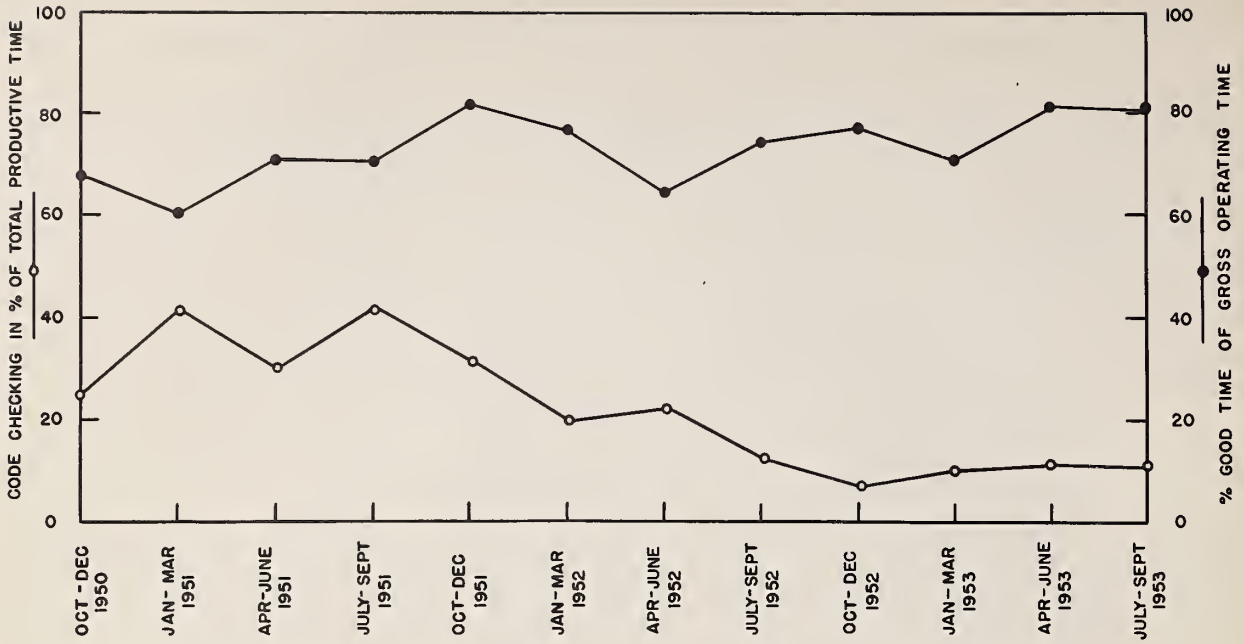

FIGURE 8.1. *Graph of operating efficiency of SEAC from October 1950 to March 1953.*

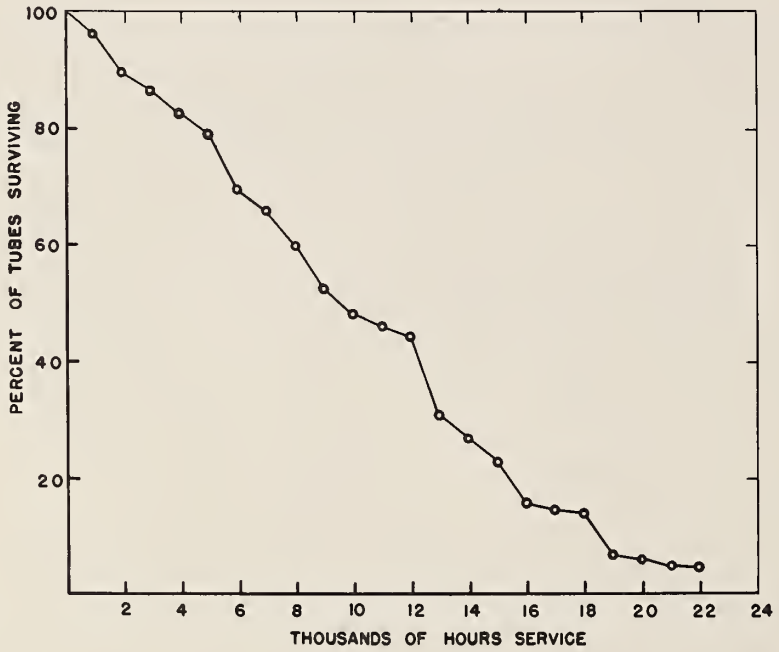

FIGURE 8.2. *Overall tube survival versus time in service for 1,775 type 6AN5 tubes.*

SEAC went into operation with a number of joints unsoldered. At first, there were few malfunctionings due to these poor connections, largely because the wires involved were uncorroded. As the wires became corroded, they caused malfunctionings and were consequently located. It is safe to estimate that there are still a few of these unsoldered or rosined connections in the computer, although they are probably in uncritical areas. Most of the current troubles with connections arise from those that have become loose because of the extensive removal of components. When plug-in components are removed, there is motion of the wiring on the plugs. In addition, for many of the voltage busses, there was inadequate provision to leave slack or stress loops in the wiring so that these connections have been rather prone to coming loose. During the month under consideration, there were four bad connections discovered, a fairly typical number.

In two cases during the month faulty switches caused machine malfunctioning. In terms of lost time, these were rather costly failures because the connections involved were intermittent. Most of the switches in SEAC are rotary type and cause little failure. The push-button and toggle switches have been less reliable but only because they are used more frequently and with more enthusiasm.

Although the next three adjustments shown in the table are performed during the maintenance periods, it has also been necessary to perform them between maintenance periods. The failures indicated generally occurred in groups in short periods before it was recognized that an adjustment was necessary, so that only about two of each type of adjustment were necessary during the month.

A coincidental situation accounts for the large number of failures due to auxiliary equipment during this period. Magnetic recordings of codes and input data are generally made at times other than when the operator is scheduled to operate the computer. In this case many such recordings had been made but were not used on the computer until some time later. When the faults in the auxiliary equipment were discovered, it was too late to rerecord the data and lost time resulted. As a result of this experience, it was suggested to the operators that they use another auxiliary device, the outscriber, to check all inscriptions on wire by punching paper tapes on the outscriber and comparing the output tape with the originally punched tape. This is recommended where there are no programmed means provided for checking the input from magnetic wire.

During this period of a month there were also five miscellaneous failures and 20 cases of machine failure that were not diagnosed.

4. COMPONENT RELIABILITY IN SEAC

Vacuum Tubes. There are a total of 1,424 vacuum tubes in SEAC and its associated auxiliary equipment, comprising 32 different types. However, because the type 6AN5 vacuum tube occurs more frequently than other types, discussion will be confined to this tube. A total of 1,050 6AN5 tube locations currently exist in SEAC. During the first 3 years of SEAC operation, approximately 2,500 6AN5's were used in the machine. Of these, 1,300 tubes were rejected for various reasons. Rejections were made almost exclusively during the preventive maintenance periods. Operational failures of 6AN5's in SEAC have been very few. During a 15-month period from February 1952 to April 1953, for example, it was necessary to replace only 18 tubes during computation time.

Figure 8.2 shows graphically vacuum-tube survival for 1,775 6AN5's used up to March 1953. This group does not include the approximately 700 tubes associated with the Williams memory and short experimental developments. The curve has been plotted by considering batches of tubes installed within 500 hours of the indicated average as single entities and weighting the points on a survival curve for such a group of tubes according to the number contained in each batch. This curve shows the percentage of tubes one would expect to survive after a given number of hours.

When SEAC was first placed in operation there existed considerable variation in heater voltage in various parts of the machine. Accordingly, plate currents were measured with heater voltages at 5.7 as well as 6.3 v to allow for abnormal heater voltage during use in the computer. If there was a drastic change in plate current when the heater voltage was decreased, the tube was discarded as "heater sensitive." In addition to preventing weak tubes from being installed in stages having low heater voltage, it was thought that heater sensitivity might provide an indication that the tube would soon be rejected for low emission. Thus, in September 1951, heater sensitivity was formalized in a specification that called for rejection of all tubes that showed a reduction of plate current

of 25 percent or more when the heater voltage was changed from 6.3 to 5.7 v. This part of the specification was adopted even though at that time abnormal heater voltages had been corrected on all chassis. Approximately 55 percent of all tube rejects in SEAC until June 1953 were made for heater sensitivity. An analysis of tube data showed that after 8,000 hours of service heater sensitivity was the main cause for replacement. (More detailed information on tubes and diodes used in SEAC is included in paper 7 of this Circular.)

During June 1953 an analysis of our 6AN5 vacuum-tube experience showed that heater sensitivity increases with tube age and is some cause for alarm if heater voltages fluctuate. It is not apparent, however, that heater sensitivity provides a definite indication before a serious slump in plate current. The analysis also indicated that the median life expectancy for tubes rejected for all reasons except heater sensitivity was 10,000 to 12,000 hours, whereas if heater sensitivity was also included as a reject criterion, the median life appeared to be 8,700 hours. Since June 1953, the heater sensitivity test has not been included in the vacuum-tube test for the computer. Experience does not yet show that this increase in tube life expectancy as a result of relaxing the heater sensitivity requirement coincides with any material increases in the incidence of tube failures during scheduled machine operation.

Germanium Diodes. The basic measure of diode reliability in SEAC is the rate at which diodes cause machine failures. As there are over 15,000 diodes in the computer, any substantial failure rate would be intolerable. During the 3 years that SEAC has been in operation, however, this failure rate has been kept so low that diodes have been a minor consideration in the production of machine failures. Over the 3-year period, diodes have had an in-operation failure rate of less than two per month. Table 2 shows the type of diode failures that occurred during a 2-year period of regular machine operation. Those diodes with high forward voltage had a voltage drop of greater than 2 v when a current of 20 ma was passed through them. High back current was indicated by more than 500 μa when 40 v was applied in the reverse direction. Drift was indicated by a change of more than 300 μa in reverse current while the diodes were under test.

The failures of table 2 are few indeed and are offset by the preventive rejects shown in table 3. The figures for the computer exclusive of acoustic memory are representative of a period that is roughly half the period covered by table 2. The diodes came from sections of the computer (other than the acoustic memory) where environmental conditions were less harsh. The figures for the acoustic memory alone show the preventive replacements for a slightly shorter period than that of the computer alone.

TABLE 2. Operational failures of germanium diodes in SEAC, December 1950 to December 1952 (total diode population: 15,676; elapsed time: 3,693 to 19,512 service hours)

Nature of failure	Number of diodes
High E_f	4
High I_b	14
Drift	8
Unspecified	13
Total	39

TABLE 3. Preventive maintenance replacements of germanium diodes in SEAC December 1951 to December 1952 (elapsed time: 10,830 to 18,905 service hours)

	Replaced for—			Total replacements	total population
	High E_f	High I_b	Drift		
Computer exclusive of acoustic memory.	91	375	382	848	12,709
Acoustic memory	20	65	340	425	2,967

It can be seen from table 3 that the diodes in the mercury memory suffered a much higher replacement rate than elsewhere in the computer. The memory data have been isolated in the tables because the conditions of inspection there were more rigorous and the conditions of operation involved higher operating temperatures than elsewhere in the machine. Inspections were made almost twice as frequently in the memory as elsewhere in the machine, thus slightly increasing the rejection rate.

The maintenance records of table 3 do not include 276 replacements made in all parts of the machine during three short periods of poor operation during the summer of 1952. During those periods the airconditioning equipment was inoperative during weather of unusually high humidity and temperature, operating conditions for which the machine was not designed. Ambient temperatures for the diodes ranged from 45° to 55° C. During this period it was also necessary to discard an unusually large number of "spare" diodes, i.e., diodes used for replacements in the computer, probably because of the hot, humid weather conditions.

The weakest features of performance of the diodes are their tendency towards high back current and back current drift. Actually, SEAC circuitry is extremely tolerant of back current; currents five times greater than specifications are allowable in most places.

It has been estimated that if diode specifications had been chosen to cover specific applications in the SEAC circuitry and grouped into three or even two types, the preventive maintenance replacements shown in table 3 would have been materially reduced, perhaps as much as 10 to 1. Instead, at the time SEAC was designed it was decided in the interest of simplicity to use diodes to one specification—therefore all diodes were tested to the same specification as the ones used in the most critical part of the SEAC gating structure because the mounted configurations were not identified with circuit application. This tends to make diodes appear less reliable than they might actually be if typed according to application. This consideration becomes less important if preventive checking is not practiced and diodes are sought out and replaced only when failing.

Miscellaneous Components. In addition to tubes and diodes, four other types of components are used extensively in SEAC, namely, resistors, electromagnetic delay lines, capacitors, and pulse transformers. Of these, only resistors, delay lines, and pulse transformers form a part of the actual computer circuitry, capacitors being used solely to bypass places where excessive noise pickup would cause the generation of spurious signals.

Resistors in SEAC circuitry are required to be within 10 percent of their design value. A set of measurements has been initiated to determine how far in the three years of operation, resistors have varied from their initial rated value. The information obtained so far indicates that about 5 percent of the resistors in the computer have exceeded the rated tolerance. These are being replaced as they are discovered. No records have been kept on the number of shorted or open resistors occurring during the 3 years. About 2 or 3 resistors are replaced each month during preventive maintenance.

Infrequent troubles with delay lines have been due to corrosion of the solder joint connecting the fine wire of the line to its termination. About a dozen instances of this kind have been reported during the life of the computer.

Pulse transformers have caused very little trouble in SEAC until quite recently when shorted and open primary windings increased the incidence of failure. Another type of failure was caused by decrease of transformer inductance which results from spreading of the gap after failure of the clamping band. Mechanical design of the transformers has been changed to correct these troubles.

5. CONCLUSION

The extent to which SEAC has served as an experimental machine during more than 3 years of operation is indicated by the increase in the number of vacuum tubes from about 750 to about 1,450. During a good part of this time SEAC was the only large-scale automatic digital computer available to the Government. Its record of productive computation coupled with its expansion and increasing power and efficiency of operation have proved that it is possible to operate a computer for experimental purposes while obtaining useful computation from it.

The most recent of the major modifications to the computer has been the addition of automatic checking circuitry. The principle followed in the addition of this feature was that the reliability of the system should be balanced. As the standard SEAC pulse repeater stage has proved very reliable for continuous operation, it was the basis of the construction of the checking circuitry.

Maintenance procedures have had considerable effect on the reliability of the system. The large-scale removal of diodes and tubes has resulted in trouble from these sources being reduced to the point where they are among the least troublesome of the components in the computer. This has been accomplished at the expense of discarding some components that could have functioned in the computer for a longer time. If diode specifications were established on the basis of the circuit function for which use was intended, the number of rejects could probably be reduced by an order of magnitude without any loss in computer reliability. For vacuum tubes, the filament-sensitivity test has proved to be too stringent, and by the elimination of this test, the number of tubes rejected can be decreased considerably.

Input-output has proved to be the least reliable of the functions that the system performs. However, the recognition of this fact has enabled the difficulty from this trouble to be greatly reduced by the incorporation of programmed checks into routines that involve large amounts of input-output.

New constructional techniques that have resulted from the experience with SEAC have been incorporated into DYSEAC. It is believed that the use of printed-circuit techniques will materially reduce the troubles that have resulted from the wiring methods that have been used in SEAC. In addition, the need for more rugged construction of removable components which has been indicated by SEAC experience has been incorporated into the DYSEAC design.

The 3 years of SEAC operation have contributed to making it a far more reliable machine than when it was first put into operation. Weak elements in the system have been eliminated, and the addition of new features has enabled it to increase its power of operation.

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