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SHF IMPULSE GENERATOR

James R. Andrews
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Electromagnetic Technology Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Boulder, Colorado 80303

June 1978

Final report prepared for:

Department of the Air Force
Air Force Avionics Laboratory
Wright-Patterson Air Force Base, Ohio 45433
Contract MIPR #FY117577N1864

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U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, Secretary

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FOREWORD

This generator was designed and built under contract MIPR-FY117577N1864 for the Air Force Avionics Laboratory at Wright-Patterson Air Force Base, Ohio. It was designed specifically to be used with an existing Air Force μ - ϵ measurement system. This generator increases the frequency range of measurements to 18 GHz. The Air Force contract monitor was Mr. Larry Carter.



Figure 1. NBS SHF Impulse Generator.

* Note: The inclusion of manufacturer's names in this report is not intended as an endorsement. Other manufacturers' products might perform equally as well or better.

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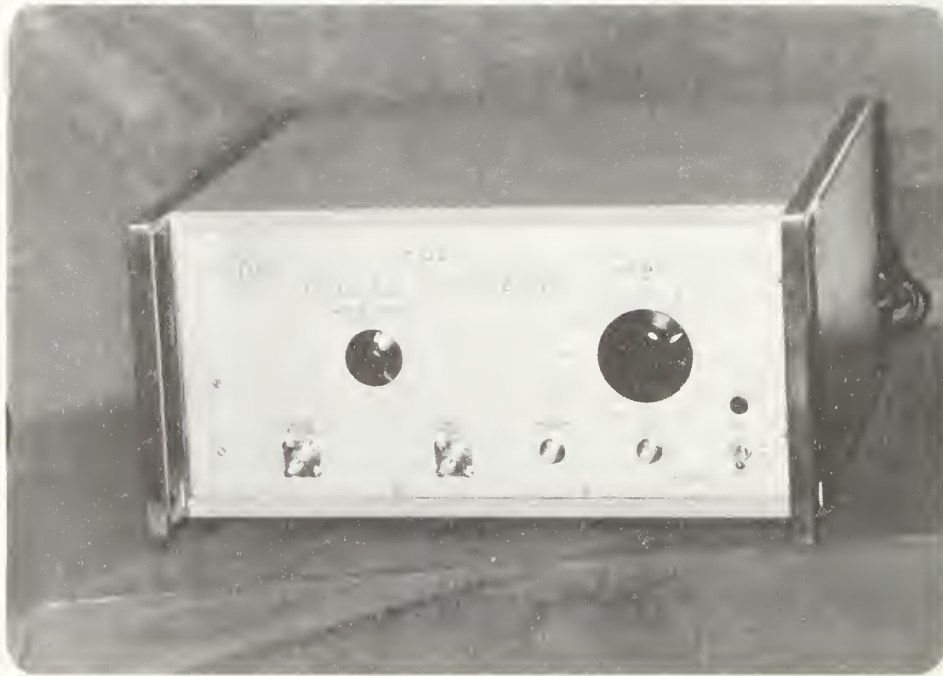


Figure 1. NBS SHF Impulse Generator.

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SHF IMPULSE GENERATOR

James R. Andrews and Eugene E. Baldwin

A super-high-frequency (SHF) impulse generator designed and built by the National Bureau of Standards is described in detail. The generator produces three different waveforms. The first is a simple impulse of 1 volt amplitude (3 V option) and 60 ps duration with a useful spectrum (15 dB down) extending from low frequencies out to 9 GHz. The second waveform is a single cycle 5 GHz sine wave (doublet) of 0.8 volts peak-to-peak amplitude (1.6 V option). Its useful spectrum extends from 0.5 GHz to 11.7 GHz. The third waveform is an exponentially damped rf pulse. It has a center frequency of 12.5 GHz and a damping time constant of 1/4 ns. The peak-to-peak amplitude is 0.8 volts. The useful spectrum extends from 6 GHz to 18 GHz.

1. INTRODUCTION

This report describes in detail a super-high-frequency (SHF) impulse generator (IG) (fig. 1) designed and built by the National Bureau of Standards (NBS) for the Air Force Avionics Laboratory (AFAL). It produces a useful spectrum extending up to 18 GHz.

This SHF impulse generator was designed specifically to be used with an existing Air Force μ - ϵ measurement system. The system uses time domain measurement techniques and the Fourier transform to determine the complex μ and ϵ of various materials as a function of frequency. The μ - ϵ measurement system is described in references [1-7]. The original AFAL system was designed by an outside contractor and covered the frequency range 0.1 GHz to 10 GHz. The same contractor then built an additional rf pulse generator to provide coverage from 9 GHz to 16 GHz [4].

The Air Force encountered problems in obtaining repeatable measurements in the 9 GHz to 10 GHz region where the two systems overlapped. This was in part due to the fact that the spectrum amplitudes, $S(f)$, from their low frequency (0.1 GHz to 10 GHz) and from their high frequency (9 GHz to 10 GHz) generators were both rolling off quite rapidly in the 9 GHz to 10 GHz region [5]. Another

major source of potential error is higher order moding in the 14 mm coaxial lines used in the measurement setup. NBS contracted to build a new generator that would eliminate the spectrum roll-off problem in the 9 GHz to 10 GHz region. The new generator was to cover both the low and high frequency regions and extend the frequency coverage to 18 GHz. To solve the moding problem, we recommend that a new measurement setup be built using precision 7 mm air lines. The 14 mm lines are only recommended for use up to 8.5 GHz. The 7 mm lines are useful up to 18 GHz. For still higher frequencies, 3.5 mm lines should be used.

The SHF IG is designed to provide two test waveforms for use with the Air Force μ - ϵ system. A simple, 1 volt, 60 ps impulse is used for measurements up to 9 GHz. The other signal is an exponentially damped rf pulse. It has a nominal center frequency of 12.5 GHz and a 1/4 ns damping time constant. The peak-to-peak amplitude is 0.8 volts, and the useful spectrum extends from 6 GHz to 18 GHz. The type of waveform delivered to the main pulse output is determined simply by setting the waveform switch to either the IMPULSE or RF PULSE position.

The SHF IG also provides a separate reference pulse output. The reference pulse is derived from the main pulse. In the Air Force μ - ϵ measurement system, the reference pulse is used solely for the purpose of a timing reference in a 3-point scanning technique that reduces the effects of horizontal timing drifts during data acquisition [8]. For other applications, the reference pulse may also be found useful as a test signal. With the generator in the impulse mode, the reference pulse is a single cycle, 5 GHz, sine wave of 0.8 volts peak-to-peak amplitude. The useful spectrum extends from 0.5 GHz to 11.7 GHz.

This report gives the complete details on the SHF IG. The specifications, operation, and typical waveforms and spectra are found in sections 2-4. The circuit description, circuit diagrams, and alignment procedures are in sections 5-7. The parts list, mechanical drawings, and p.c. board art work are found in sections 8-9.

2. SPECIFICATIONS

MAIN PULSE OUTPUT

Waveform: Impulse or damped rf pulse as selected by front panel control

Impulse Specs.

Amplitude: 1.0 volt, $\pm 10\%$, into 50 ohms (3 volt option).
Polarity: Positive.
Baseline: 0 volts.
Duration(50%): 60 ps, $\pm 10\%$.
Source Impedance: 50 ohms, ± 1 ohm at DC. $\pm 0.02 \rho$ maximum as measured with 30 ps TDR.
Spectrum Amplitude: 44 dB μ V/MHz nominal, ± 3 dB ripple from 0.2 GHz to 4 GHz, down 15 dB at 9 GHz. *
Spurious Pulses: 12 ns after the impulse, low level (>20 dB down) internal reflections appear at the output.

RF Pulse Specs.

Amplitude: 0.8 volts peak-to-peak, $\pm 20\%$, into 50 ohms.
Baseline: 0 volts.
Center Frequency: 12.5 GHz, nominal.
Duration(1/e): 1/4 ns, nominal.
Source Impedance: 50 ohms for 12.8 ns with $\pm 0.02 \rho$ maximum as measured with a 30 ps TDR, open circuit after 12.8 ns.
Spectrum Amplitude: 32 dB μ V/MHz nominal, ± 7.5 dB ripple, from 6 to 18 GHz. *
Spurious Pulses: 12 ns after the rf pulse, low level (>20 dB down) internal reflections appear at the output.

*Note: Spectrum amplitude, $S(f)$, is defined in terms of the magnitude of the Fourier transform, $V(f)$, of a time-domain signal function, $v(t)$.

$$S(f) = 2 |V(f)| \quad \text{where } V(f) = \int_{-\infty}^{\infty} v(t) e^{-j2\pi ft} dt .$$

The unit in common usage is microvolts per megahertz (μ V/MHz). Values are usually expressed in decibel microvolts per megahertz (dB μ V/MHz) above 1 μ V/MHz.

$$S(\text{dB}) = 20 \log_{10} \left[\frac{S(\mu\text{V}/\text{MHz})}{1\mu\text{V}/\text{MHz}} \right] .$$

REFERENCE PULSE OUTPUT

Waveform: Doublet impulse. Reference pulse is derived from the main pulse. Waveform depends upon whether impulse or rf pulse is selected.

Amplitude: 0.8 volts (impulse) or 0.6 volts peak-to-peak (rf pulse), $\pm 20\%$, into 50 ohms (1.6 V or 1.2 V option).

Baseline: 0 volts.

Duration (baseline): 0.2 ns (impulse) or 0.5 ns (rf pulse), nominal.

Source Impedance: 50 ohms for 10 ns with $\pm 0.02 \rho$ maximum as measured with a 30 ps TDR, 83 ohms nominal, after 10 ns.

Spectrum Amplitude: >30 dB μ V/MHz nominal, from 1 GHz to 10 GHz (impulse) and 0.7 GHz to 7 GHz (rf pulse). *

Spurious Pulses: 10 ns after the reference pulse, low level (>18 dB down) internal reflections appear at the output.

Relative Timing: The reference pulse lags the main pulse by 5.7 ns.

REPETITION RATE, TRIGGER, AND TIMING

Internal Rep. Rate: 50 Hz to 100 kHz in a 1,2,5 sequence, quartz crystal controlled ($\pm 0.001\%$).

Ext. Sync. Input

Frequency: DC to 100 KHz maximum, repetition rates in excess of 100 kHz are internally limited to 100 kHz maximum.

Pulse Required: Standard TTL pulse
0V < "0" < 0.8 V
2V < "1" < 5 V.

Polarity: Triggering occurs on positive going transition.

Input Loading: 430 ohm, AC coupled.

Delay: Nominal 20 ns lag at trigger output port referred to the external input port.

Trigger Output Pulse

Source Impedance: 50 ohms.
Amplitude: 1.4 volts, $\pm 25\%$, into 50 ohms.
Polarity: Positive.
Baseline: 0 volts.
Transition Duration
(10-90%): 0.4 ns, $\pm 25\%$.
Duration (50%): 30 ns, $\pm 25\%$.
Timing: Leading edge of trigger pulse is 85 ns, ± 5 ns,
in advance of impulse output.
Jitter: < 10 ps jitter in the delay between the trigger output
and the main pulse output.

GENERAL

Supply Voltage: 117 volts, $\pm 10\%$, 60 Hz.
Power Consumption: 40 watts, nominal.
Size: 21.5 cm x 43.5 cm x 44.5 cm.
Weight: 14.3 kg, less accessories.

ACCESSORIES FURNISHED

1. Power cord, 2.4 m.
2. 2 APC-7/N male adapters.
3. 180 cm, RG-55/U coaxial cable.
4. Mounting hardware for standard 48 cm relay rack.
5. Operating and service manual.
6. Calibration certificate.

3. OPERATION

The operation of the NBS SHF IG is quite straightforward. There are only three controls (fig. 1); namely, the power switch, the repetition rate switch, and the waveform selector switch. Three outputs are provided: (1) main pulse; (2) reference pulse; and (3) trigger pulse. An external sync input is also provided.

For operation with the Air Force μ - ϵ measurement system, the remote sampling head is connected carefully to the main and reference pulse outputs using the furnished APC-7/N male adapters. The generator trigger output is connected to the sampling oscilloscope trigger input using the furnished 180 cm, RG-55/U cable. Depending upon the actual triggering delay in the particular sampling oscilloscope used, it may be necessary to adjust the length of the trigger cable to position the output pulses in the proper location on the CRT. Once these connections are made, the power switch is turned on, the repetition rate switch is set to the desired frequency, and the waveform selector switch is set to the desired waveform (impulse or rf pulse). The impulse waveform is used for measurements up to 10 GHz while the rf pulse is used for measurements from 6 GHz to 18 GHz. If it is desired to operate the generator at a frequency other than those supplied internally, then an external clock pulse may be applied to the external sync input.

4. TYPICAL OUTPUT WAVEFORMS AND SPECTRA

This section shows typical output waveforms and spectra for an NBS SHF IG. The examples included herein are typical results and are not to be considered as the exact performance to be obtained with a particular instrument. For his individual instrument, the operator is referred to its calibration report, which is separate from this instruction manual.

The waveforms shown here were all measured on the NBS Automatic Pulse Measurement System (APMS), model III. Earlier versions of the APMS are described in references [10-11]. The APMS consists of an NBS modified sampling oscilloscope interfaced with and controlled by a dedicated minicomputer (fig. 2). The APMS sampler has a 20 ps transition duration (10-90%) and a dc-18 GHz bandwidth. The input impedance is 50 ohms. The waveforms shown here are computer-generated graphics. The spectra of the various waveforms were computed by the minicomputer using the fast Fourier transform (FFT) [12,13].

When the generator is operated in the impulse mode, the main pulse output is the impulsive waveform shown in figure 3. The impulse consists of (1) a small, slow, precursor pulse, (2) the main, narrow impulse, and (3) some low level damped ringing that lasts approximately 2 ns after the main impulse. There are no other signals emanating from the main pulse output earlier or later in time than those shown, with the exception of a low level doublet 20 dB below the main impulse occurring 15 ns after the main impulse. The impulse amplitude is 1 volt, and its 50% level duration is 61 ps. It should be noted that a 10 dB attenuator is used inside the generator. Thus, the internal impulse is actually 3.2 volts in amplitude. The spectrum amplitude, $S(f)$, of the impulse is shown in figure 4. $S(f)$ is seen to be relatively flat out to 4 GHz. At 1 GHz, $S(f)$ is 44 dB μ V/MHz. A minor dip occurs at 5 GHz. The spectrum then rolls off smoothly above 6 GHz. At 10 GHz it is \approx 15 dB down from its 1 GHz value.

When the generator is operated in the rf pulse mode, the main pulse output is the damped rf pulse waveform shown in figure 5. The peak-to-peak amplitude is 0.8 volts. The nominal center frequency appears to be 12.5 GHz. The damping time constant appears to be of the order of 1/4 ns. As with the impulse, the only other signal emanating from the main pulse output is a low level rf burst 20 dB below the main rf pulse and occurring 13.5 ns later. The spectrum amplitude of the rf pulse is shown in figure 6. The spectrum peaks at 9.7 GHz with 40 dB μ V/MHz. From 12 GHz to 18 GHz, $S(f)$ remains fairly level at 27 dB μ V/MHz with \pm 3 dB ripple. From a level of 20 dB μ V/MHz at 1.5 GHz up to the peak at 9.7 GHz, $S(f)$ is characterized by a smooth gradual increase with frequency.

In the impulse mode of operation, the reference pulse is a doublet (fig. 7). The pulse consists of a small, slow, precursor pulse, the doublet, and then some low level, damped ringing that lasts for 2 ns. The peak-to-peak amplitude of the doublet is 0.8 volts. A 6 dB attenuator is used within the generator; thus, the internal reference pulse is 1.6 volts in amplitude. The baseline duration of the doublet is 200 ps; thus, the doublet appears as a single cycle of a 5 GHz sine wave. A low level pulse (18 dB down) appears in the output 14 ns after the doublet. The spectrum amplitude, $S(f)$, of this doublet is shown in figure 8. As expected from the waveform, the spectrum is seen to peak at 5 GHz with a level of 37 dB μ V/MHz. The spectrum rolls off smoothly on either side of 5 GHz. It is 15 dB down at 0.5 GHz and 11.7 GHz.

In the rf pulse mode of operation, the reference pulse is a distorted doublet (fig. 9). The pulse consists of (1) a small, slow, precursor pulse, (2) a fast positive impulse followed by a broader, undershoot impulse and (3) some

damping ringing that lasts for 1.5 ns. The peak-to-peak amplitude of this doublet is 0.7 volts. The baseline duration of the doublet is of the order of 0.5 ns. As before, a low level (18 dB down) pulse follows this reference pulse by 14 ns. The spectrum amplitude of this reference pulse is shown in figure 10. The spectrum peaks at 2.5 GHz with a level of 36 dB μ V/MHz. The spectrum rolls off smoothly on either side and is 15 dB down at 0.35 GHz and 9 GHz.

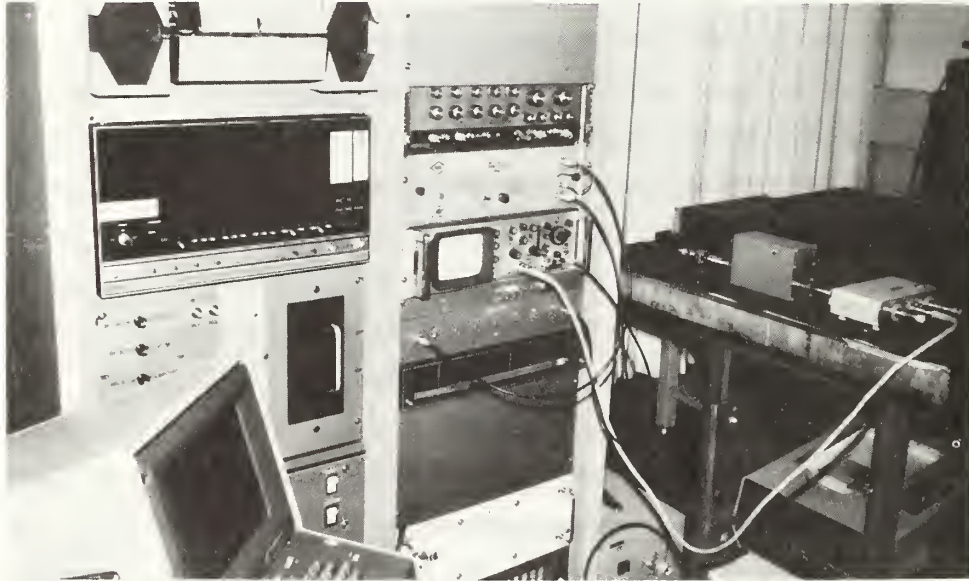


Figure 2. NBS Automatic Pulse Measurement System (APMS).

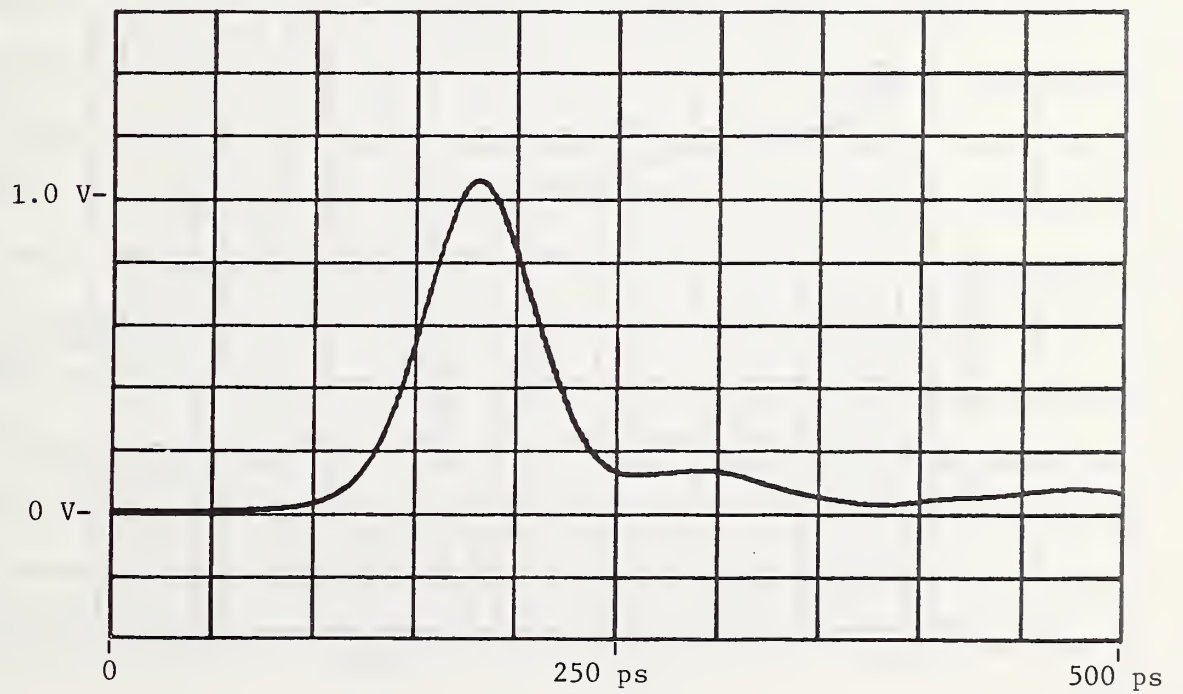
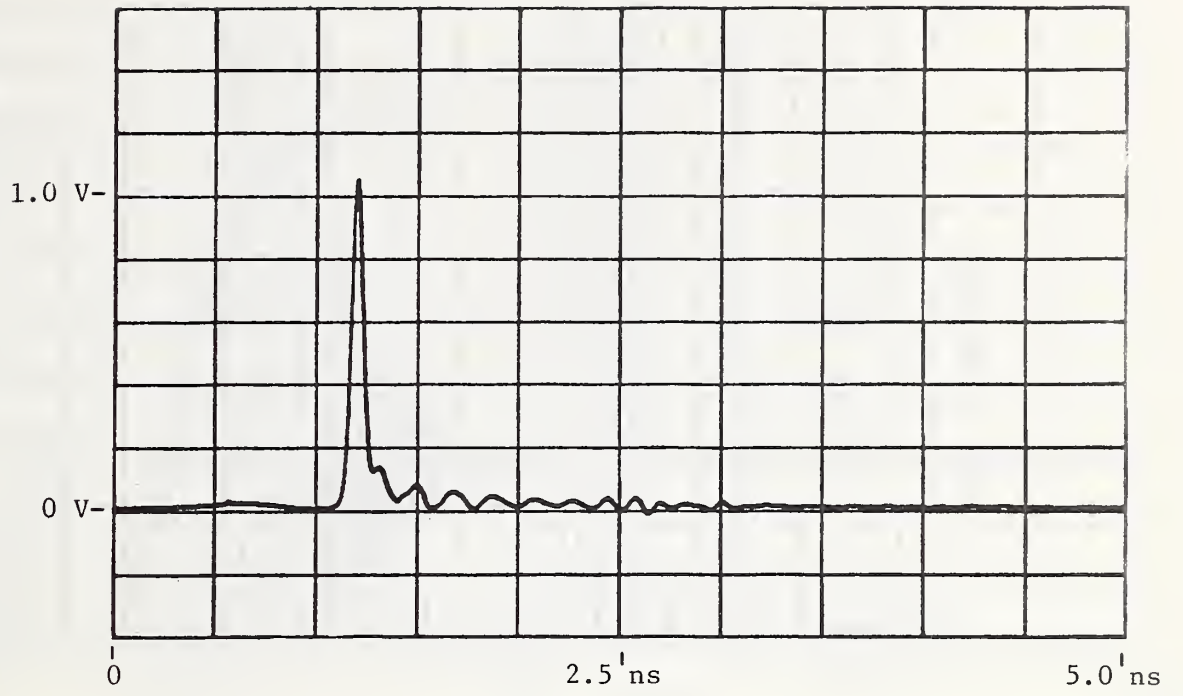


Figure 3. Typical main pulse output waveform, impulse mode.

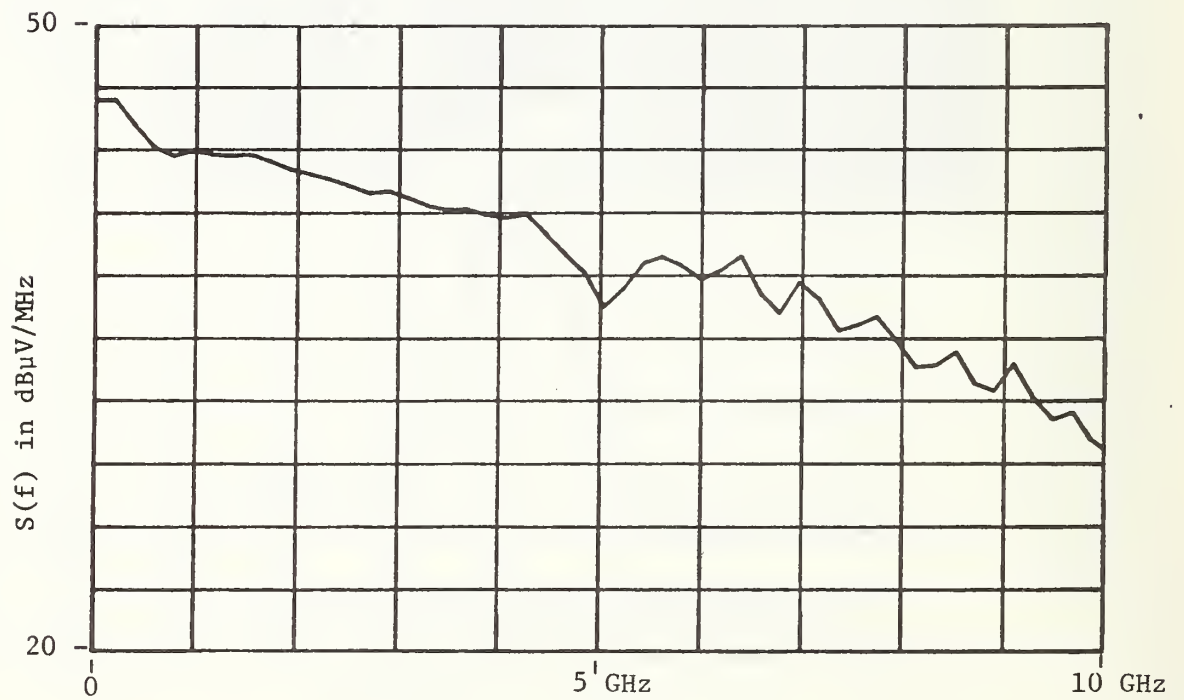
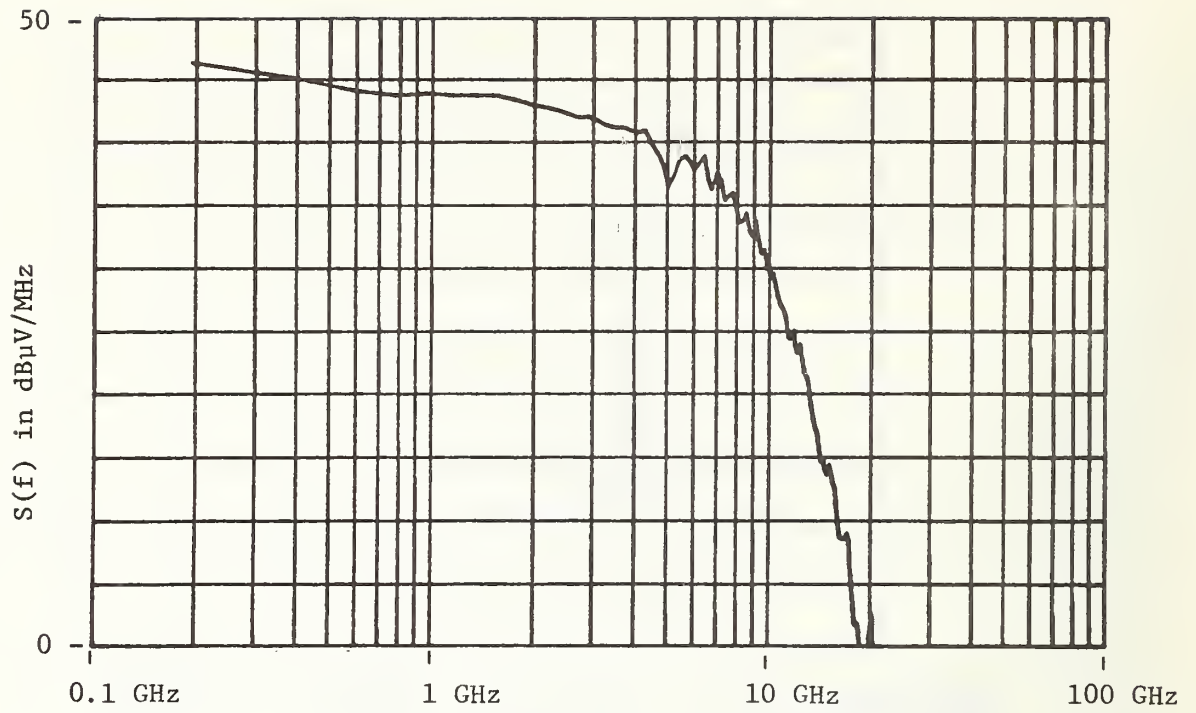


Figure 4. Typical main pulse output spectrum, impulse mode.

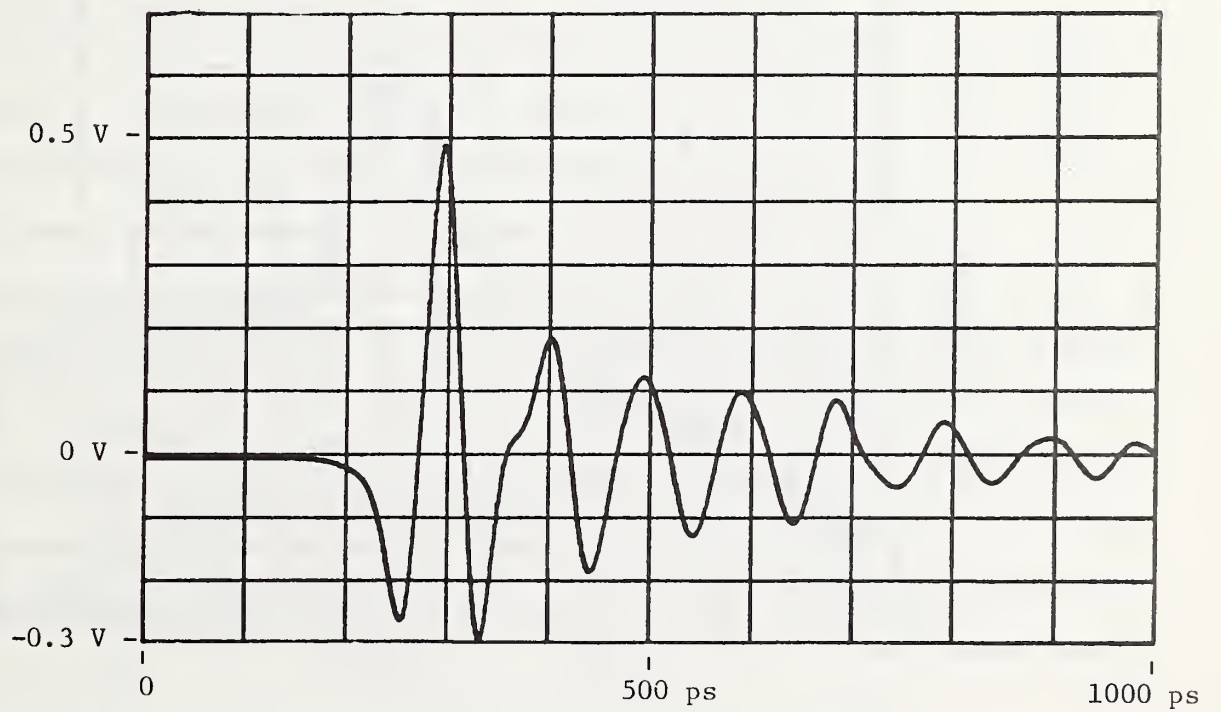
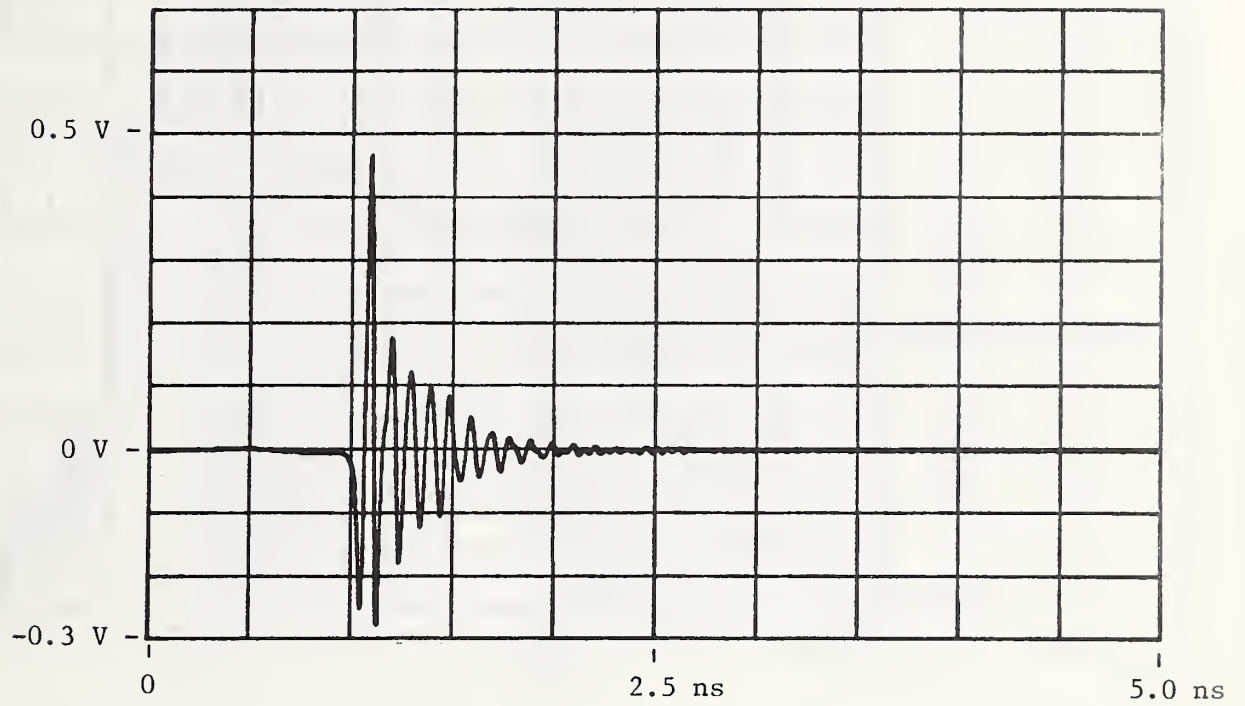


Figure 5. Typical main pulse output waveform, rf pulse mode.

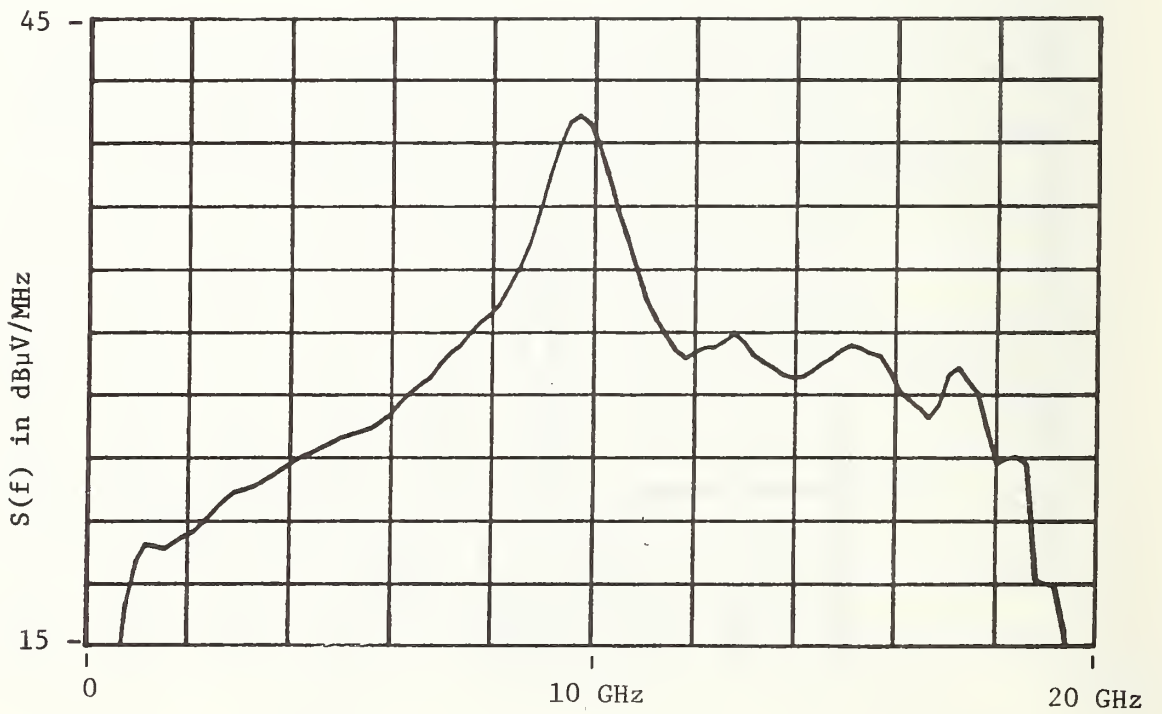
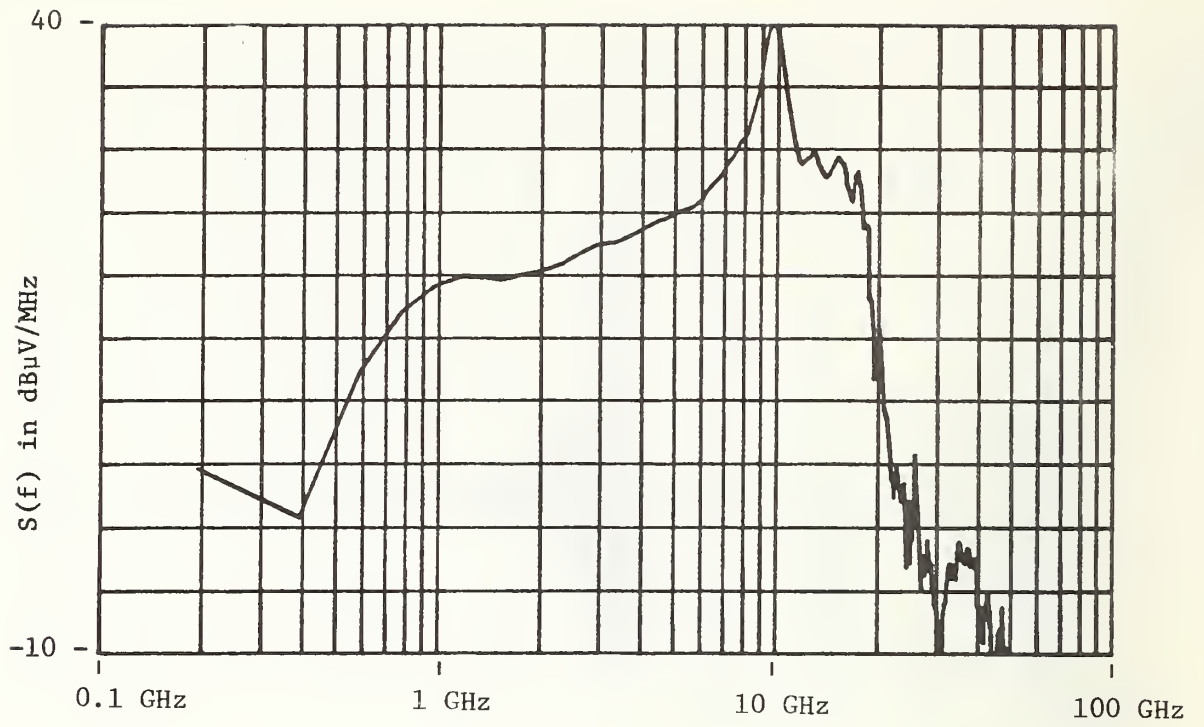


Figure 6. Typical main pulse output spectrum, rf pulse mode.

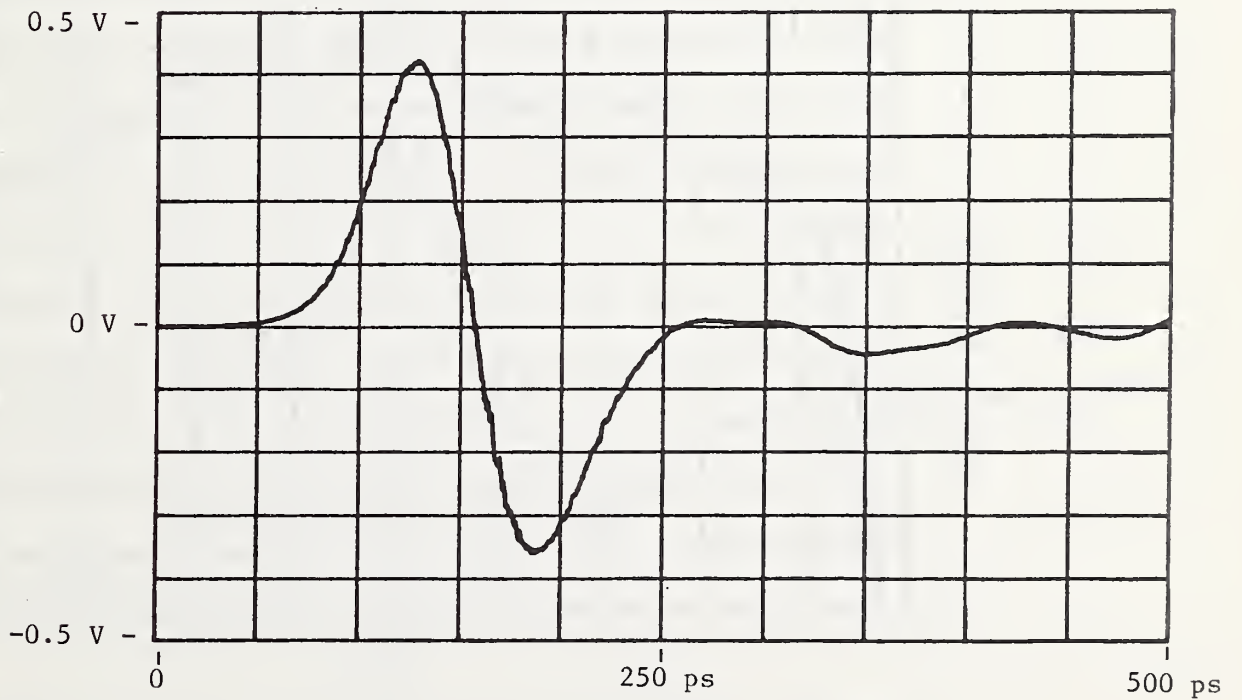
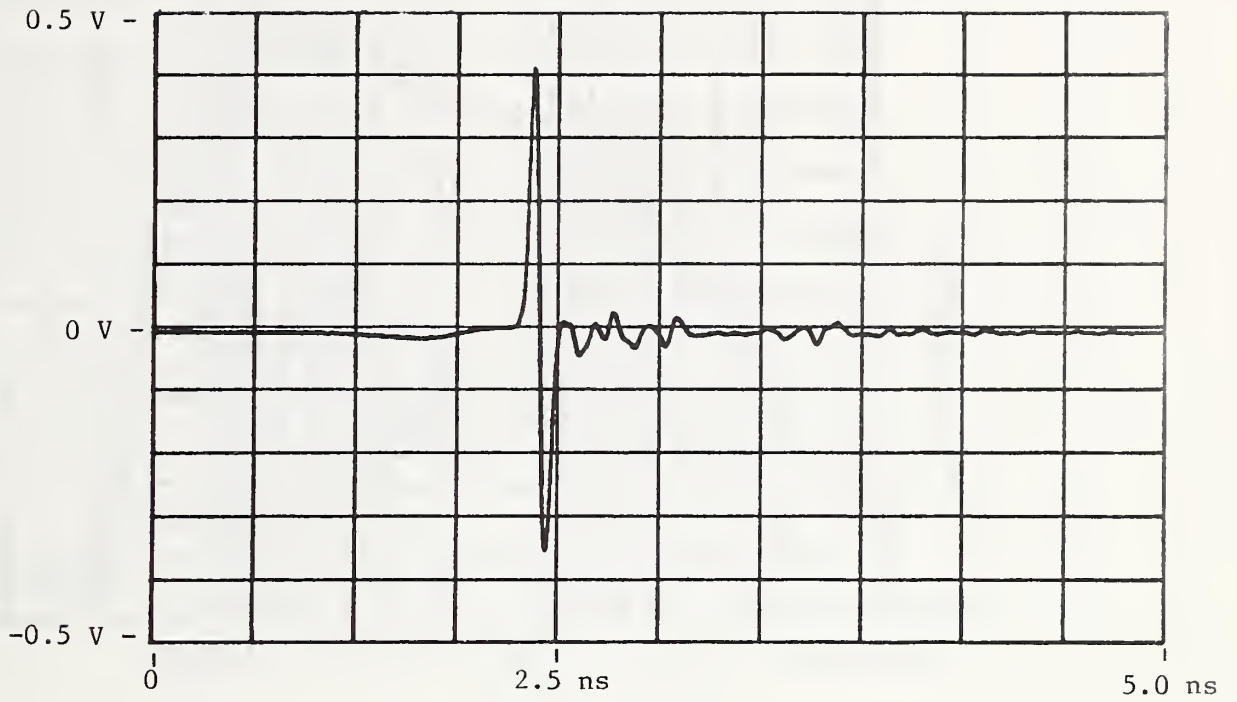


Figure 7. Typical reference pulse output waveform, impulse mode.

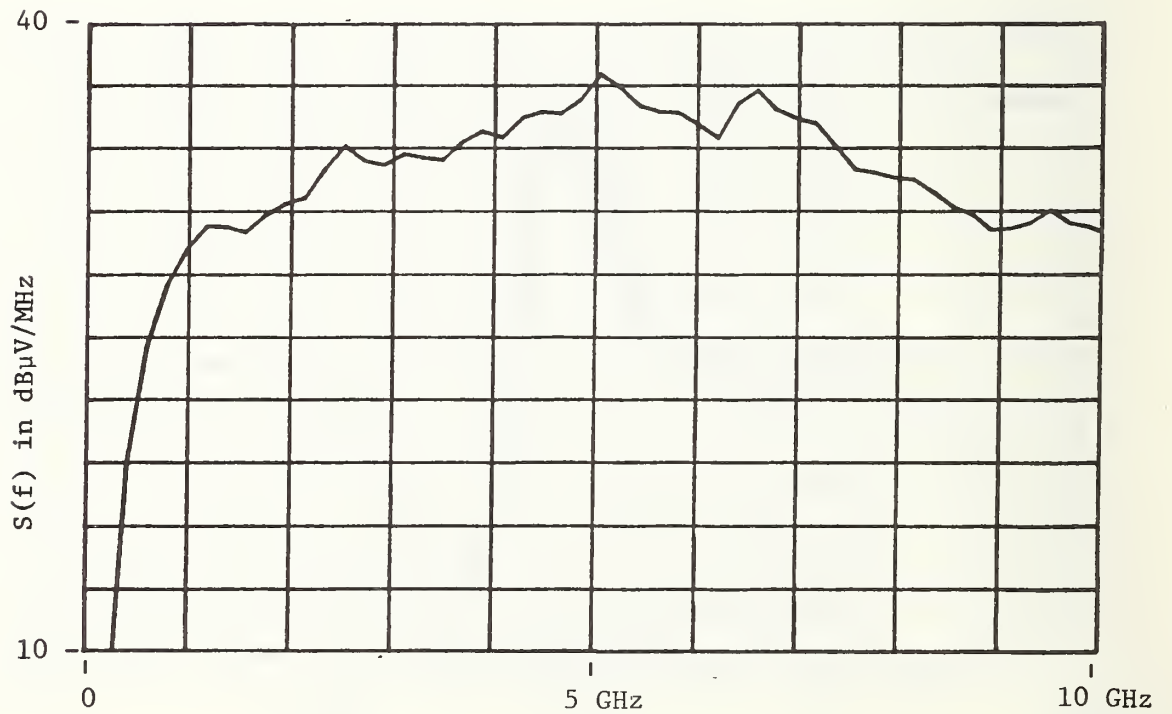
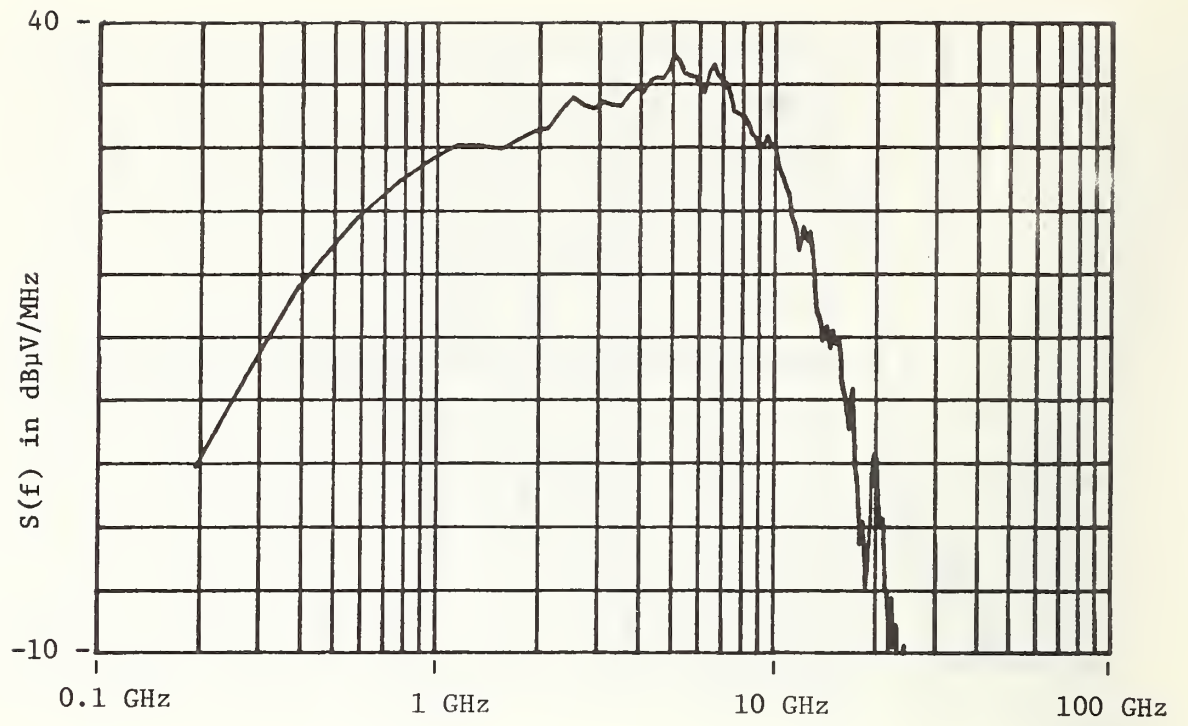


Figure 8. Typical reference pulse output spectrum, impulse mode.

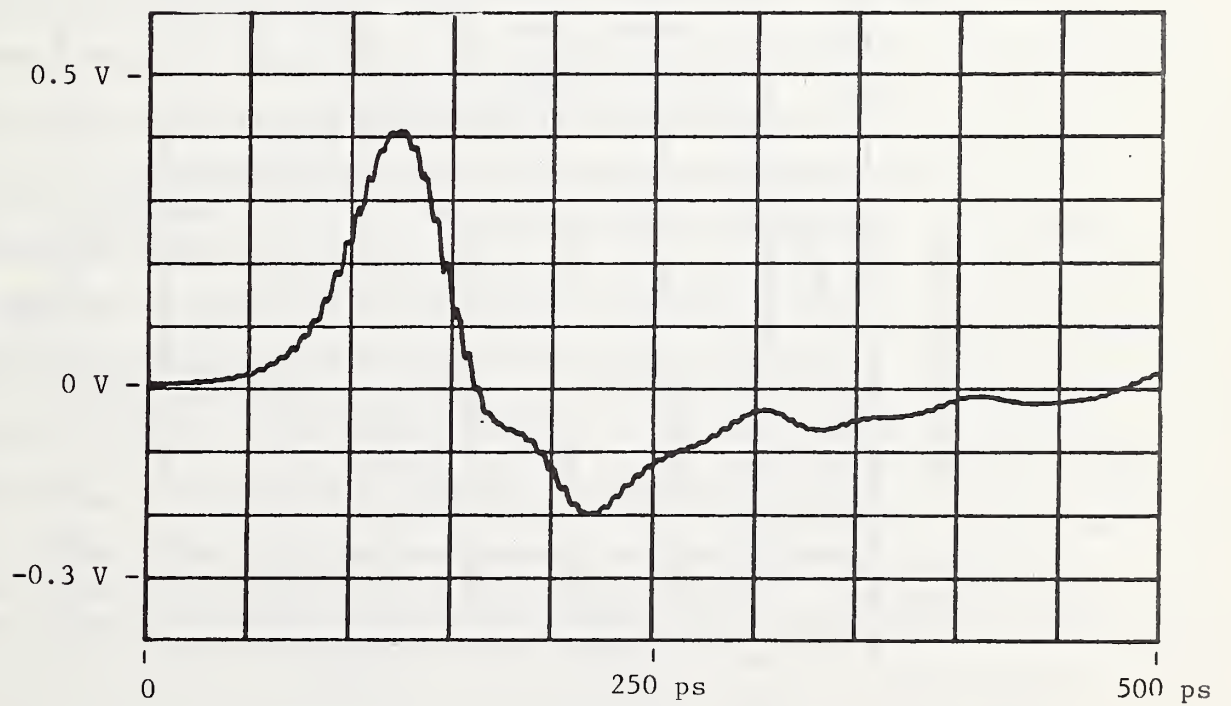
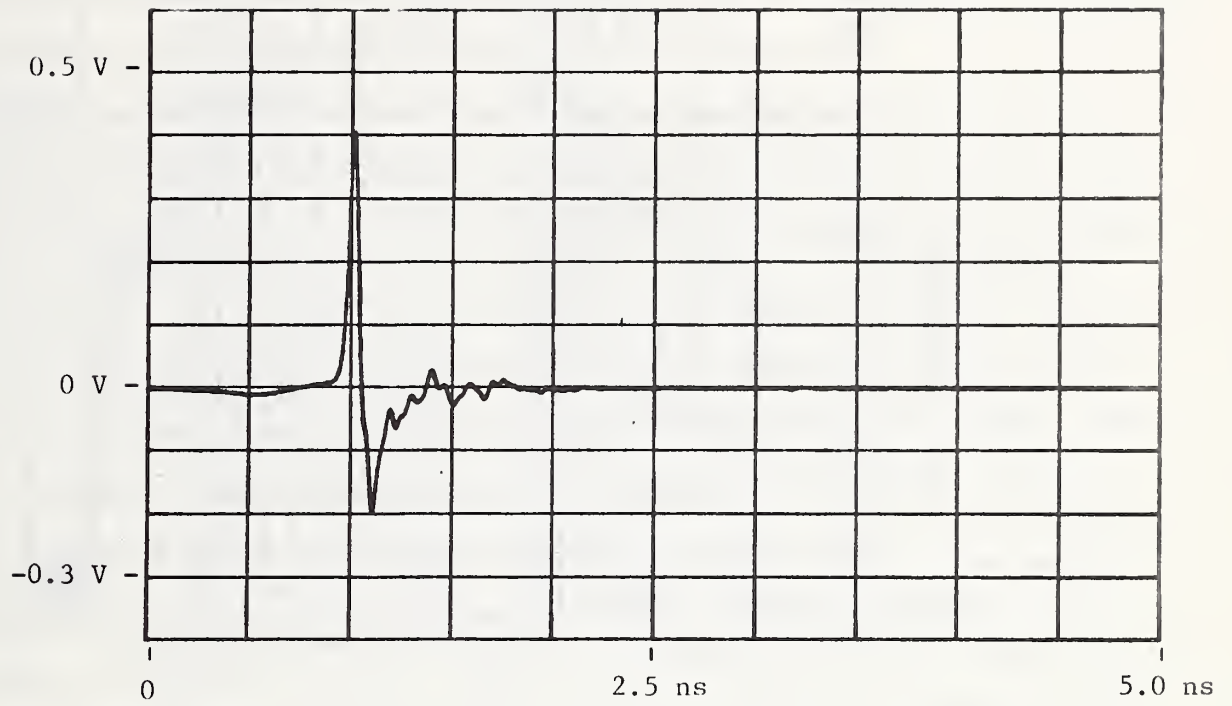


Figure 9. Typical reference pulse output waveform, rf pulse mode.

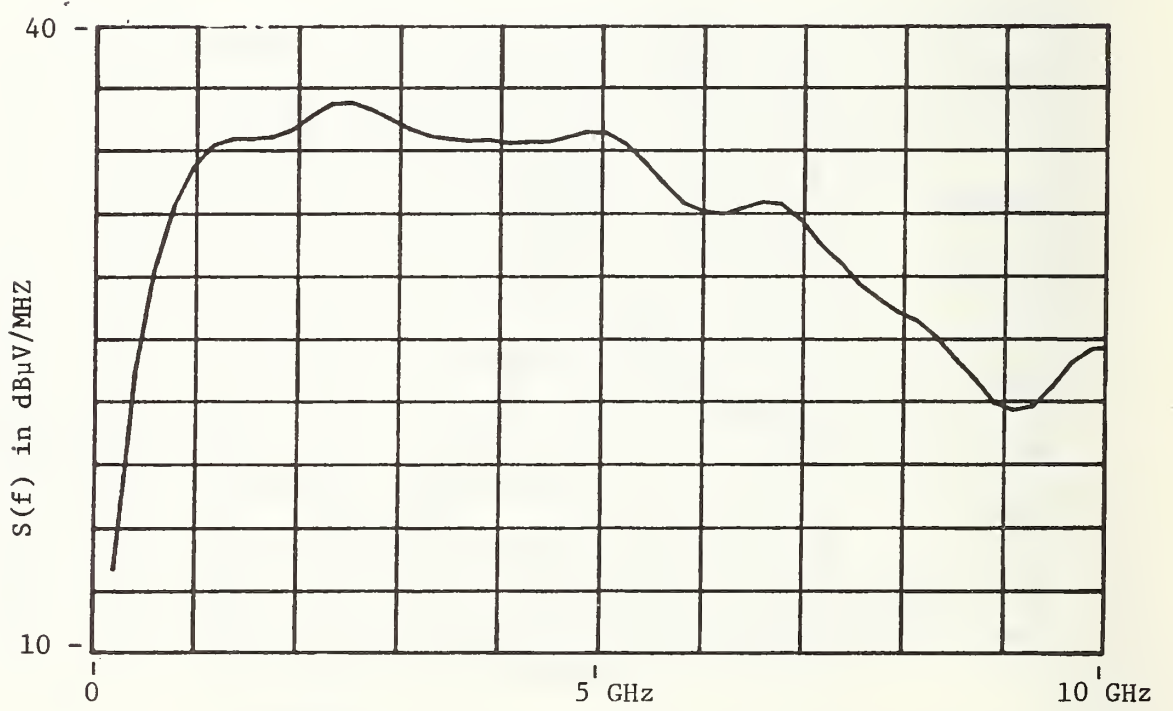
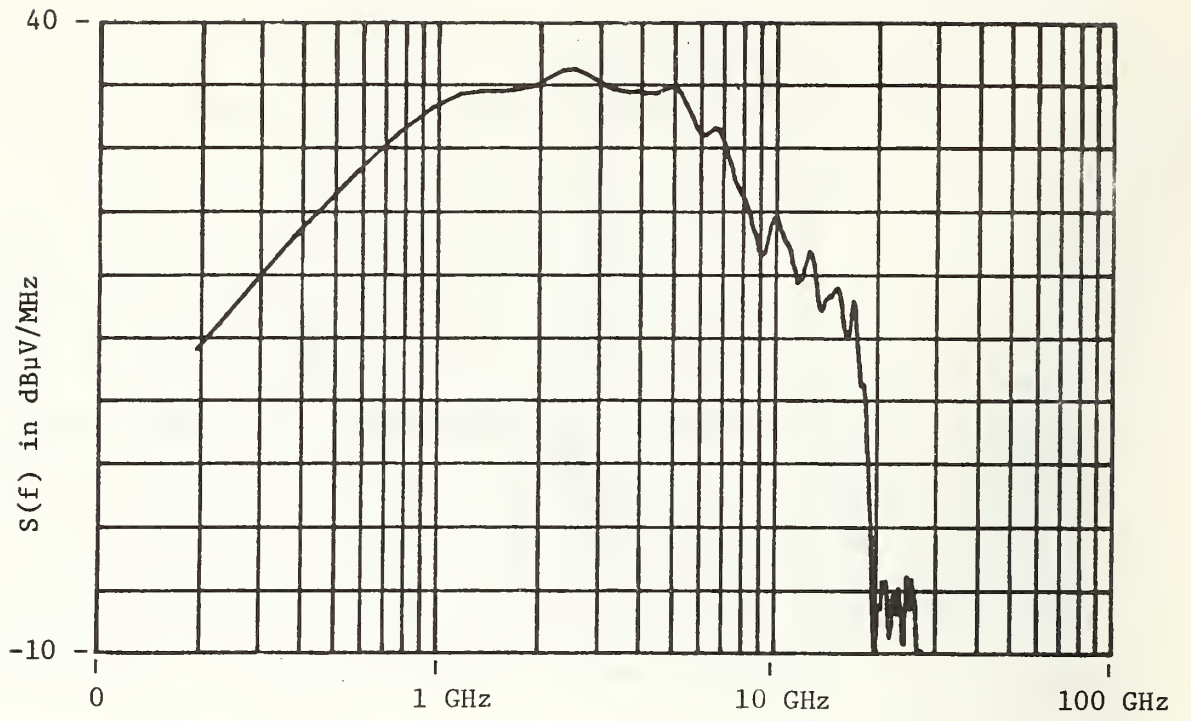


Figure 10. Typical reference pulse output spectrum, rf pulse mode.

5. CIRCUIT DESCRIPTION

Figure 11 is the basic block diagram of the NBS SHF IG. The basic pulse generating techniques are similar to other NBS impulse generators [14,15]. The internal repetition rate is derived from a 10 MHz crystal controlled oscillator. The 10 MHz frequency is divided into lower frequencies from 100 kHz down to 50 Hz using TTL, $\div 2$, $\div 5$, and $\div 10$ dividers. The internal or external repetition rate source is used to trigger the avalanche transistor driving pulse generator. This generator produces a 50 volt driving pulse into 50 ohms. The 10% to 90% first transition duration is 0.4 ns. The pulse duration (50%) is 20 ns. A portion of this driving pulse is tapped off and supplied to the front panel as a trigger pulse. The driving pulse is connected to an 82 ns coaxial delay line (DL1,7,&8). At the output of the delay line is an extremely fast step recovery diode, SRD1, which sharpens the leading edge of the driving pulse to a transition duration of 60 ps. Bias current for the SRD is supplied at the input to the delay line. This sharpened pulse is then differentiated by passing it through a 12 GHz to 18 GHz, 3 dB directional coupler, DC2, thus producing the desired output impulse (fig. 3). The purpose of the directional coupler is twofold. In addition to providing the necessary differentiation of the fast step from the SRD, it also provides an excellent 50 ohm generator source impedance. To insure that only a single impulse is obtained, the driving pulse duration is made longer than the measurement time window. The Air Force μ - ϵ system uses a 10 ns time window. The second transition duration (90% to 10%) of the driving pulse is intentionally made slower (~ 15 ns) to reduce the level of the secondary spurious pulses that come out of the generator. When the SRD snaps off to its nonconducting state, it sends a transient towards the main pulse output connector and also back down the delay line towards the driving pulse generator. This reverse wave SRD pulse passes through a 7 ns delay line (DL7&8) and then through a 12 GHz to 18 GHz, 3 dB directional coupler, DC1. The coupler differentiates the SRD pulse into an impulse similar to the main output pulse. This impulse is again differentiated by the 0.9 pF blocking capacitor, C1, to form a doublet. This doublet is used as the reference pulse output (fig. 7). Delay lines 4, 8, and 9 are used to provide the necessary 12 ns reflection-free measurement time window and the required 5.7 ns timing lag between the reference pulse and the main pulse. Broadband coaxial attenuators, R4 and R5, are used to limit the level of the output pulses to below the ± 1 volt limit allowed by the sampling oscilloscope used in the Air Force μ - ϵ measurement

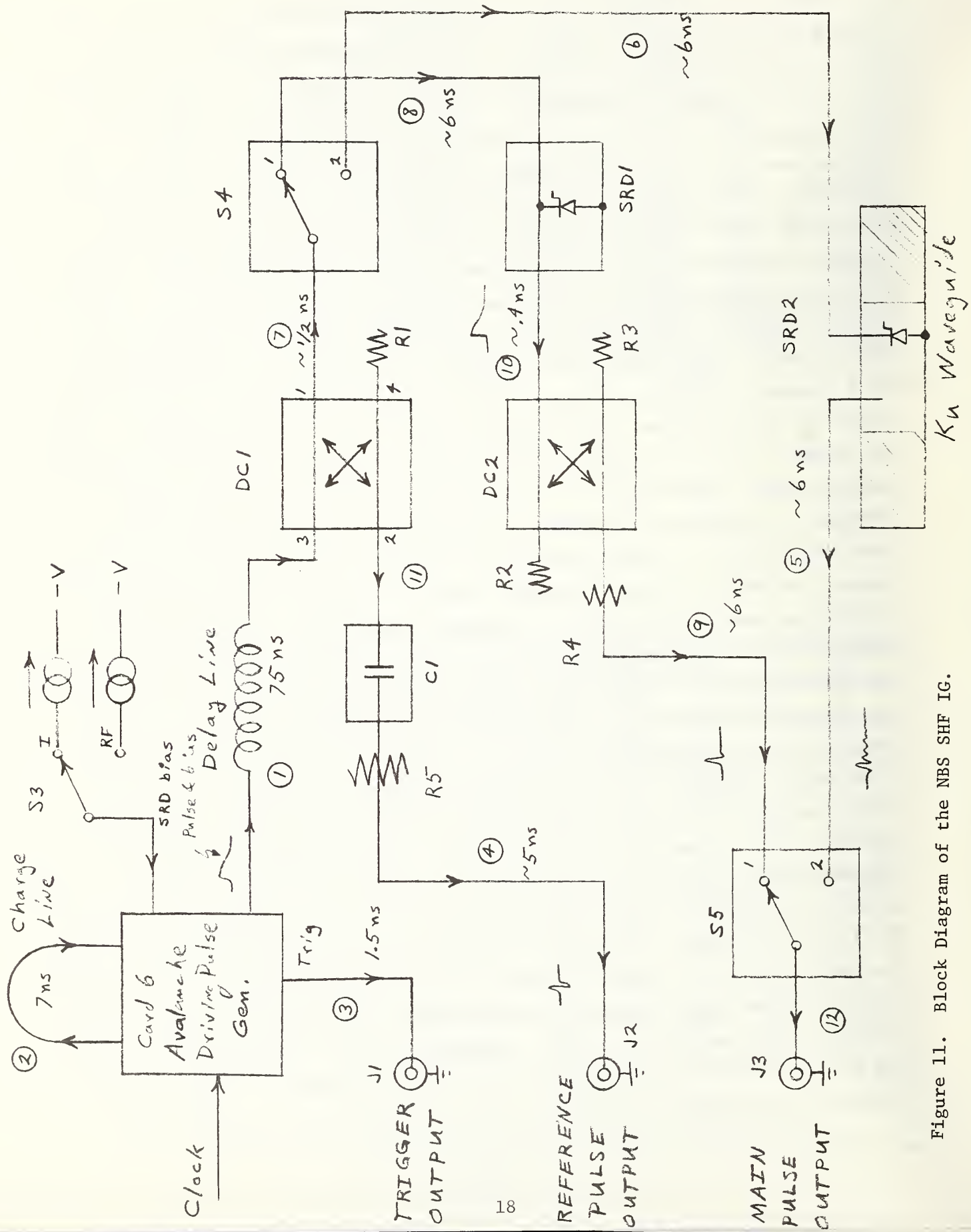


Figure 11. Block Diagram of the NBS SHF IG.

system. For other applications that require larger signals, these attenuators can be removed.

The above described the generator operation with the waveform selector switch in the IMPULSE position. When the RF PULSE mode is selected, the two coaxial switches are placed in position 2. In this position a different SRD circuit is selected. In the impulse mode, an SRD is mounted in shunt across a 50 ohm, 3 mm coaxial line. In the rf pulse mode, an SRD is mounted inside a piece of WR-62, K_j band, waveguide. The waveguide acts as a high pass filter for the 60 ps transient generated when the SRD snaps off. An E-field probe is positioned close to the SRD. The probe is close enough so that sufficient capacity coupling exists to provide a slow, low-frequency roll-off. If the probe-SRD spacing were much greater, the waveguide would then provide an extremely sharp low-frequency cut-off at 9.486 GHz. The waveguide is terminated on each end with tapered plugs of lossy foam. This is done to eliminate multiple reflections from the ends of the waveguide section. These reflections would appear later in time and distort the desired output signal if they were allowed to exist. The resultant main pulse output is a rapidly damped rf pulse (fig. 5). The reference pulse is generated in the same manner as before. It is again a doublet (fig. 9) although it is not as clean a waveform as obtained in the impulse mode.

The remainder of this section will discuss in more detail the circuits found on each printed circuit card. All schematic diagrams are found in section 6. Figure 12 is the chassis wiring diagram.

Card 1 - Low Voltage

Printed circuit card number 1 contains the low voltage power supplies. Figure 13 is the schematic diagram. +15 V, +5 V, -15 V, and -18 V are supplied by this card. Most components are mounted directly on the card with the exception of the power transformer, the -15 V regulator, and the +5 V pass transistor. The circuits are conventional and need no detailed explanation. Integrated circuit voltage regulators are used throughout with the exception of the -18 V, which is obtained using a zener diode.

Card 2 - High Voltage

Figure 14 is the schematic for the high voltage power supply. The high voltage transformer is mounted on the chassis. The circuit is quite conven-

tional. With the resistor combination of R1 and R2, the output voltage is nominally 170 V at normal line voltage.

Card 3 - High Voltage Regulator and SRD Bias Current Regulator

Printed circuit board 3 (fig. 15) contains two separate circuit functions; namely, the high voltage regulator and the SRD bias current regulator. The driving pulse generator requires well-regulated +100 V and +135 V for its avalanche transistor circuits. The +170 V raw dc from the high voltage card is dropped to +135 V by the series pass transistor Q2. R4, R7, and R8 provide a sample of the +135 V output to the (+) input of the operational amplifier IC1. A fixed +6.8 V reference voltage is supplied to the (-) input by the zener diode, CR2. IC1, Q4, and Q3 form the feedback error amplifier to drive the series pass transistor Q2. R3 and Q5 are used to provide current limiting protection. The +100 V is obtained from the +135 V by the zener diode, CR8, and the emitter follower Q6.

The remaining components of board 3 are the SRD bias current regulator. The collector of Q8 acts as a high impedance current source for the SRD. Operational amplifier, IC2, and Q7 function as the feedback error amplifier for Q8 to regulate the SRD bias current. The emitter current of Q8, which is approximately the same as its collector current, is regulated by IC2 by comparing the voltage drop across R12 with the adjustable reference voltage set by R13 or R20 and zener diode CR3. By connecting Q7 in a Darlington configuration with Q8, a super-high beta transistor results so that the SRD bias current is essentially identical to the emitter current of Q8, which is regulated by IC2. The diodes CR4-7 are included to provide an alternate path for the SRD bias current in the event that the SRD is not connected. They also provide overvoltage limiting protection for the SRD. R19 supplies a small offset current to insure that the diode current(s) do not climb during the switching interval. R18-C6 acts to filter out small noise signals.

Card 4 - 10 MHz Clock

Printed circuit card 4 (fig. 16) contains the 10 MHz crystal controlled oscillator and the ÷1, ÷2, ÷5 frequency divider for the internal repetition rate

source. Q1 is the oscillator. Q2 is a high input impedance FET buffer amplifier, while Q3 is an overdriven squaring amplifier to provide a TTL logic level, 10 MHz square wave to the TTL frequency dividers. The 7400 quad, dual input NAND gate is included to allow digital selection of either the internal source or an external clock. This feature was designed for some previous NBS pulse generators, but is not used with this generator. For this generator the INT line, pin 25, is permanently connected to the +5 V while the EXT line, pin 5, is grounded. The 7490 is connected to function as independent $\div 2$ and $\div 5$ frequency dividers driven by a common 10 MHz clock. Thus, from the 7490 three frequencies, namely 10 MHz, 5 MHz, and 2 MHz, are available. The 7454 functions as a digitally controlled switch to select one of these frequencies. "Cold" switching is used; i.e., only dc control voltages are selected by the repetition rate switch (fig. 17) with the actual signal switching being performed on the circuit board. +5 V is required to activate the desired switch.

Card 5 - Frequency Divider

Printed circuit card 5 (fig. 18) contains a chain of TTL frequency dividers. IC1-5 are 7490, $\div 10$ dividers connected in series to reduce the frequency from the clock card in steps of 10. The 7454 and 7451 are used for "cold" switch selection of the desired frequency in the same manner as on the clock card. The 7402 is used as an OR gate to combine the outputs of the 7454 and 7451.

Card 6 - Driving Pulse Generator

The driving pulse generator circuit is found on card 6 (fig. 19). The clock pulse, either internal or external, from the rep. rate switch is applied to two 74H00 NAND gates to sharpen up the positive going transition. The positive going pulse from the output of the second 74H00 gate is differentiated by C7 and is then used to trigger the first avalanche transistor, Q1. When Q1 avalanches, it very rapidly discharges C8 through pulse transformer T1. The large (~ 100 V) pulse from the discharge of C8 is coupled through the transformer to the second avalanche transistor, Q2. The secondary of the transformer is floating with respect to circuit ground. Thus, terminals 4 and 6 produce, respectively, a positive and negative going pulse, which is coupled to the base-emitter junction of Q2 through the 1 k Ω resistors, R8 and R9. This differential

drive pulse produces a large turn-on base current for Q2, and yet it is well balanced with respect to ground such that it produces a negligible signal on the output line. C9 is used as a trimmer to improve the differential balance and null out the Q1 pulse on the output. R8 and R9 are chosen to be large compared with 50 ohms to produce negligible loading of the Q2 output pulse. When Q2 avalanches, it very rapidly discharges the charge line, DL2, into the 50 ohm output circuit. DL2 was previously charged up to the B+ voltage (typically +135 V) through the charging resistor, R20. Q2 produces a 50 V pulse into 50 ohms with a 0.4 ns, 10% to 90% first transition time. R18-C12 and C11 are used to provide some peaking on the leading edge to compensate for the delay line distortion. The pulse duration of 14 ns is determined by twice the electrical length of DL2. The 90% to 10% second transition time of 15 ns is intentionally made slower by the RC network, R19-C13, at the far end of DL2. The 50 V pulse from Q2 is too large for the SRD's used, which typically have 25 V reverse breakdown voltages. Thus, a simple pi network 6dB, attenuator is used to reduce the Q2 pulse to an amplitude just slightly less than the SRD's breakdown voltage. RFC3&4 and C10 are used as a bias insertion network to supply dc, forward bias current to the SRD's. R15-R16&17 are used as a 20:1 voltage divider to provide a sample of the driving pulse for use as a trigger output pulse. R16 and 17 in parallel sets the output impedance of the trigger pulse at 50 ohms.

The 74H00 gates, IC-1, and the 96S02 monostables, IC-2, are used as a maximum repetition rate limiter. The circuit limits the maximum repetition rate to 125 kHz to prevent damage to the avalanche transistors Q1 and Q2 due to excessive power dissipation. The positive going transition of the input clock pulse, pin 53, is differentiated by R1 and C1. This positive spike is inverted twice and sharpened by gates IC-1d and IC-1c and is used to trigger Q1. The output of the first gate, IC-1a, is also used to trigger the first monostable, IC-2a. IC-2a produces a 4.1 μ s pulse which is added together with its triggering pulse in gate IC-1b to produce a 4.1 μ s pulse to insure triggering of Q2. The trailing edge of the IC-2a, 4.1 μ s pulse is used to trigger the second monostable, IC-2b. IC-2b produces a 3.8 μ s pulse. The 4.1 μ s and 3.8 μ s pulses are added together in gate IC-1b to produce a 7.9 μ s pulse. R4 and C4 are a delay network to compensate for the propagation delay through IC-2b. IC-1a inverts the 7.9 μ s pulse and applies it to the second input of the gate, IC-1d. This disables IC-1d so that it will not accept any additional input clock pulses for 7.9 μ s, thus preventing any further triggering of Q1 and Q2 until the end of the 7.9 μ s holdoff period.

drive pulse produces a large turn-on base current for Q2, and yet it is well balanced with respect to ground such that it produces a negligible signal on the output line. C9 is used as a trimmer to improve the differential balance and null out the Q1 pulse on the output. R8 and R9 are chosen to be large compared with 50 ohms to produce negligible loading of the Q2 output pulse. When Q2 avalanches, it very rapidly discharges the charge line, DL2, into the 50 ohm output circuit. DL2 was previously charged up to the B+ voltage (typically +135 V) through the charging resistor, R20. Q2 produces a 50 V pulse into 50 ohms with a 0.4 ns, 10% to 90% first transition time. R18-C12 and C11 are used to provide some peaking on the leading edge to compensate for the delay line distortion. The pulse duration of 14 ns is determined by twice the electrical length of DL2. The 90% to 10% second transition time of 15 ns is intentionally made slower by the RC network, R19-C13, at the far end of DL2. The 50 V pulse from Q2 is too large for the SRD's used, which typically have 25 V reverse breakdown voltages. Thus, a simple pi network 6dB, attenuator is used to reduce the Q2 pulse to an amplitude just slightly less than the SRD's breakdown voltage. RFC3&4 and C10 are used as a bias insertion network to supply dc, forward bias current to the SRD's. R15-R16&17 are used as a 20:1 voltage divider to provide a sample of the driving pulse for use as a trigger output pulse. R16 and 17 in parallel sets the output impedance of the trigger pulse at 50 ohms.

The 74H00 gates, IC-1, and the 96S02 monostables, IC-2, are used as a maximum repetition rate limiter. The circuit limits the maximum repetition rate to 125 kHz to prevent damage to the avalanche transistors Q1 and Q2 due to excessive power dissipation. The positive going transition of the input clock pulse, pin 53, is differentiated by R1 and C1. This positive spike is inverted twice and sharpened by gates IC-1d and IC-1c and is used to trigger Q1. The output of the first gate, IC-1a, is also used to trigger the first monostable, IC-2a. IC-2a produces a 4.1 μ s pulse which is added together with its triggering pulse in gate IC-1b to produce a 4.1 μ s pulse to insure triggering of Q2. The trailing edge of the IC-2a, 4.1 μ s pulse is used to trigger the second monostable, IC-2b. IC-2b produces a 3.8 μ s pulse. The 4.1 μ s and 3.8 μ s pulses are added together in gate IC-1b to produce a 7.9 μ s pulse. R4 and C4 are a delay network to compensate for the propagation delay through IC-2b. IC-1a inverts the 7.9 μ s pulse and applies it to the second input of the gate, IC-1d. This disables IC-1d so that it will not accept any additional input clock pulses for 7.9 μ s, thus preventing any further triggering of Q1 and Q2 until the end of the 7.9 μ s holdoff period.

Figures 21, 22, and 23 in the section on troubleshooting show typical waveforms for card 6.

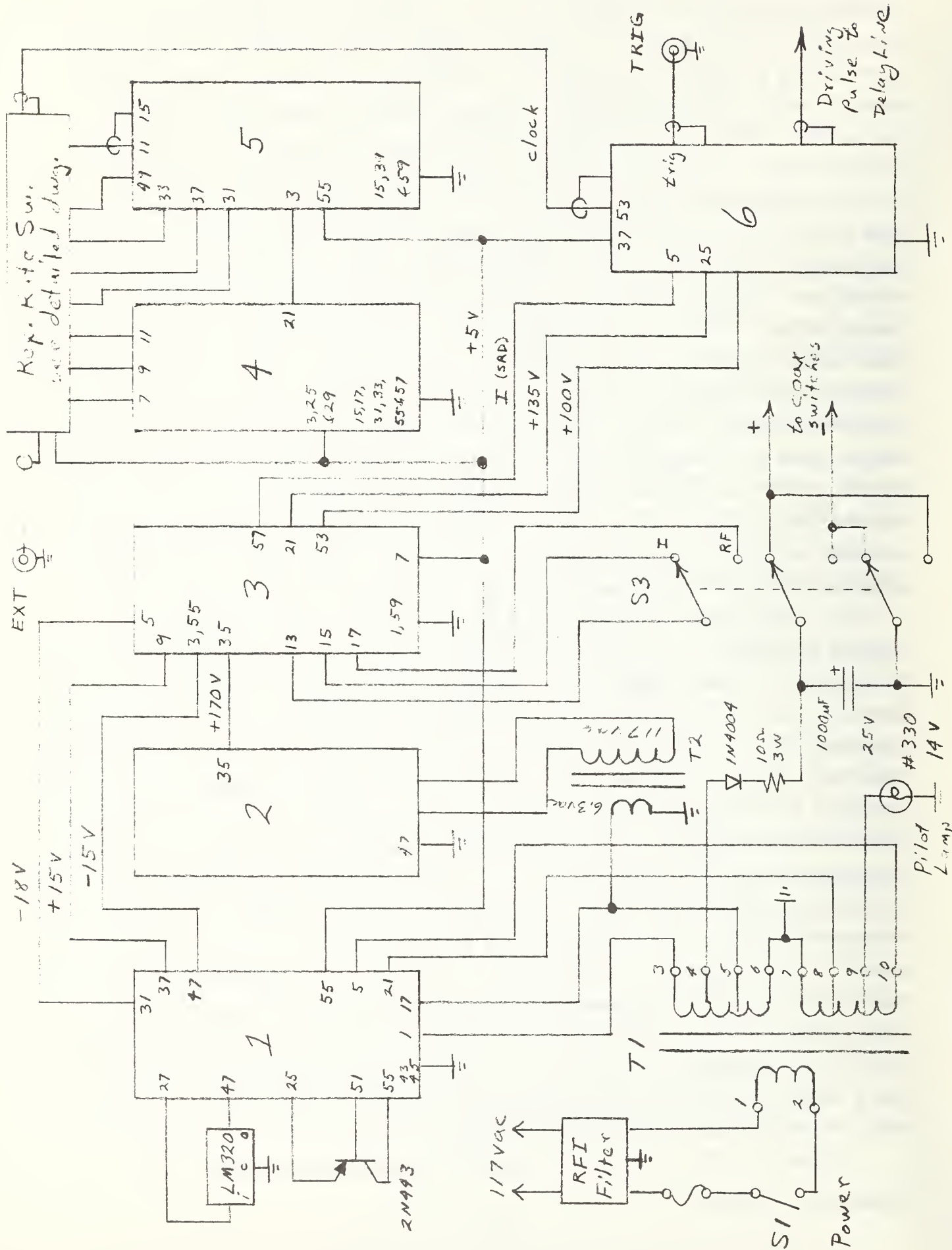


Figure 12. Chassis Wiring Diagram.

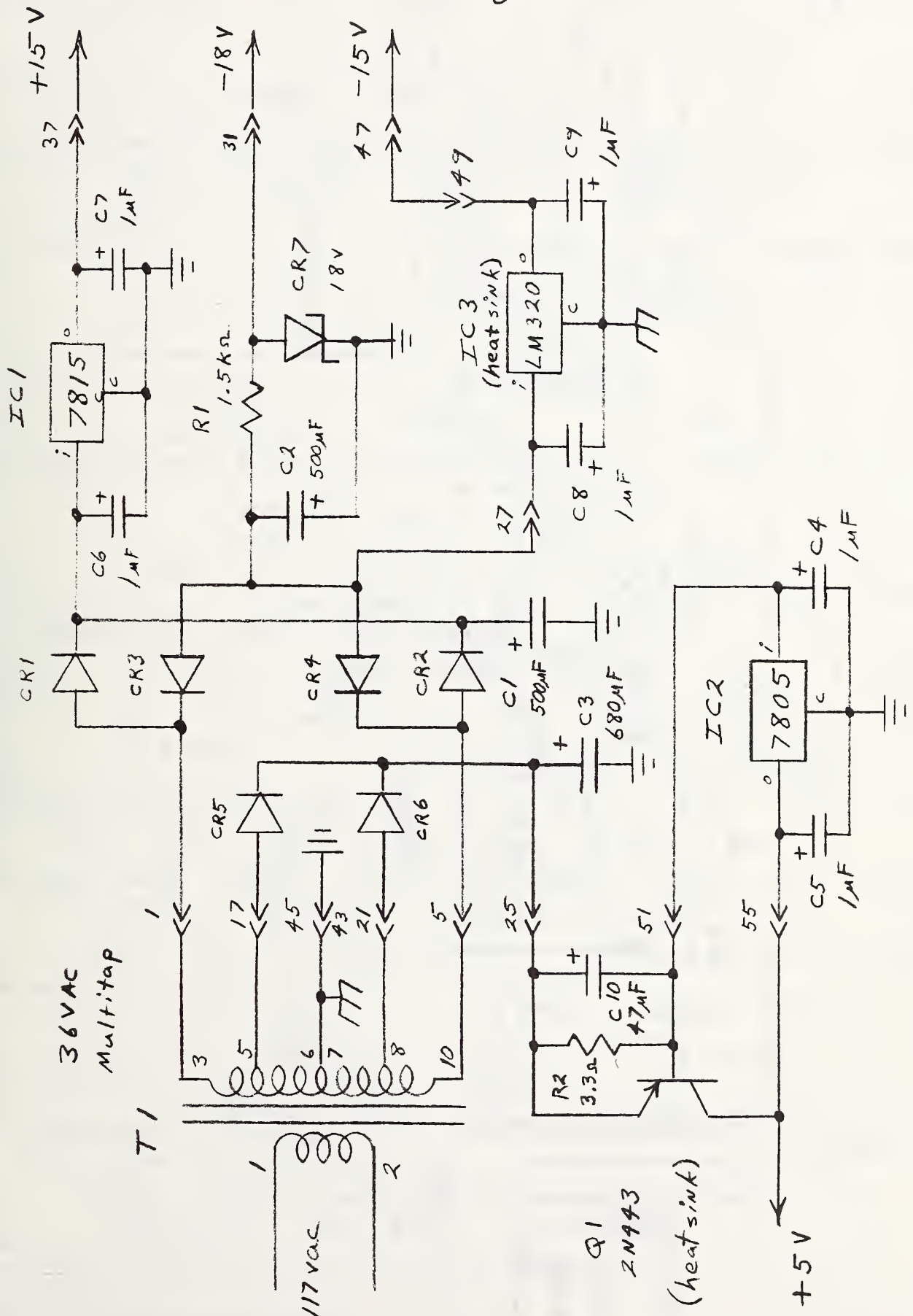


Figure 13. Schematic Diagram.

BY EEB DATE Oct 77
CHKD. BY JRA DATE Jan 78
Fig. 14

SUBJECT Card 2
High Voltage Power
Supply

SHEET NO. _____ OF _____
JOB NO. 2764373

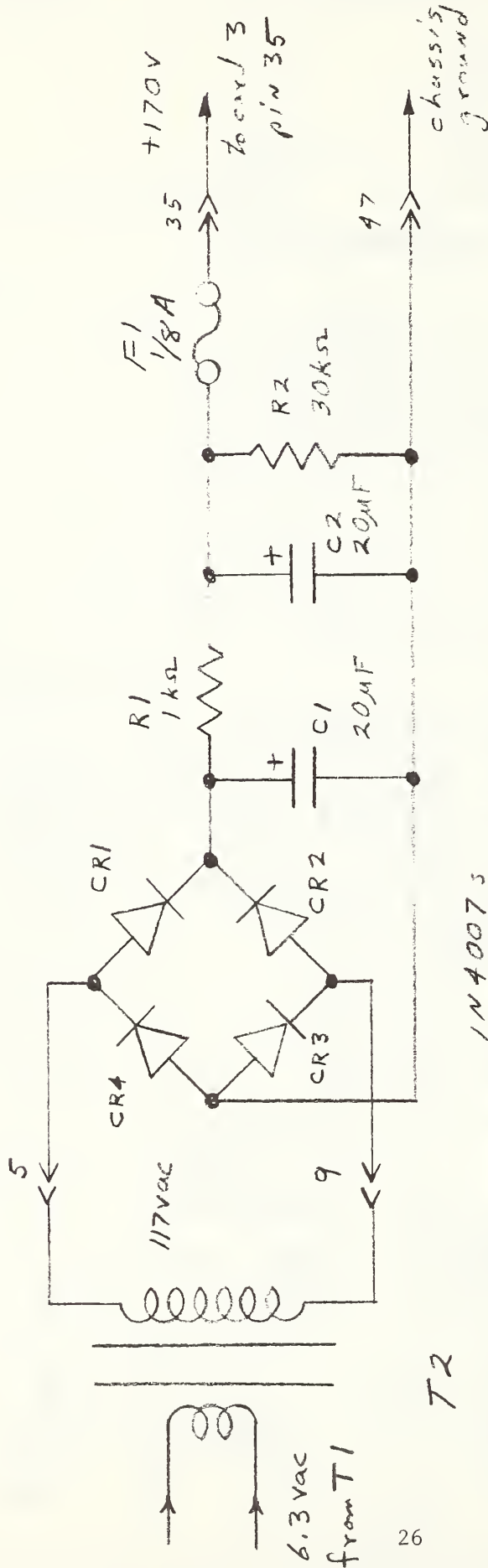


Figure 14. Schematic for the High Voltage Power Supply.

J. R. Andrews 14 July 75

BY _____ DATE _____

CHKD. BY _____ DATE _____

Revised Oct 77

SUBJECT **Card 3 - HV
Regulator & SRD Bias**

SHEET NO. _____ OF _____

JOB NO. _____

Fig. 15

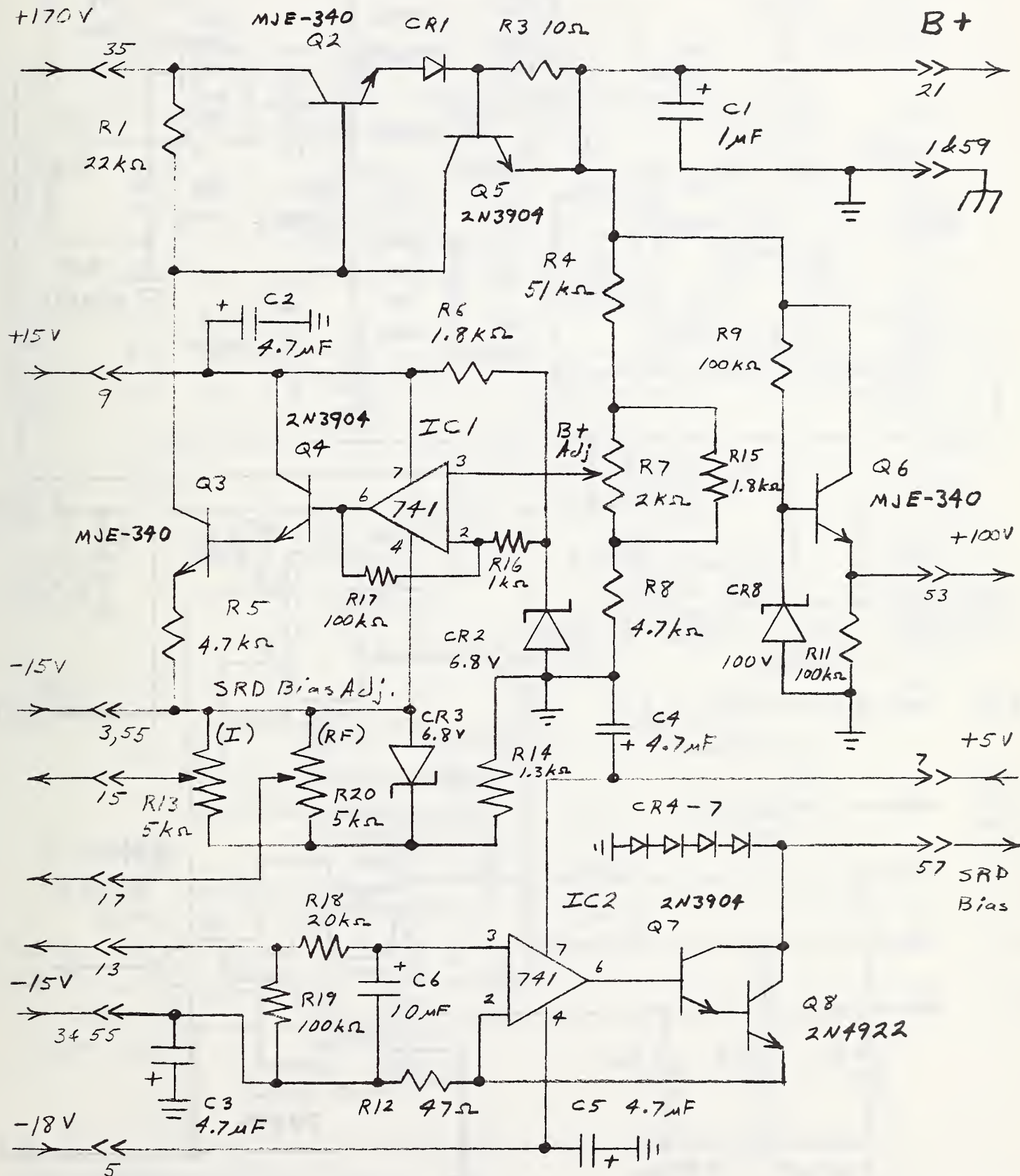


Figure 15. Regulator and SRD Bias.

Fig. 16

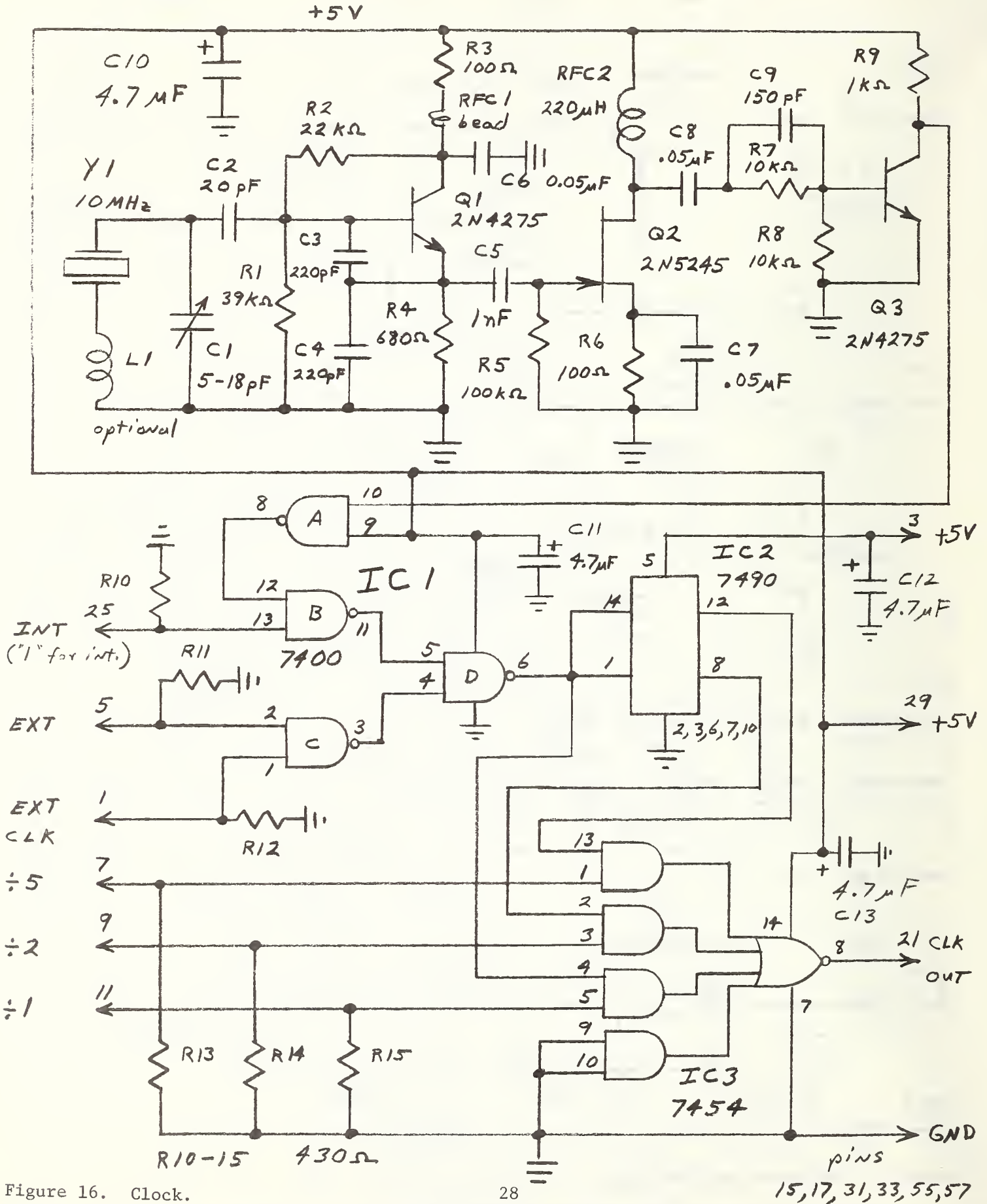


Figure 16. Clock.

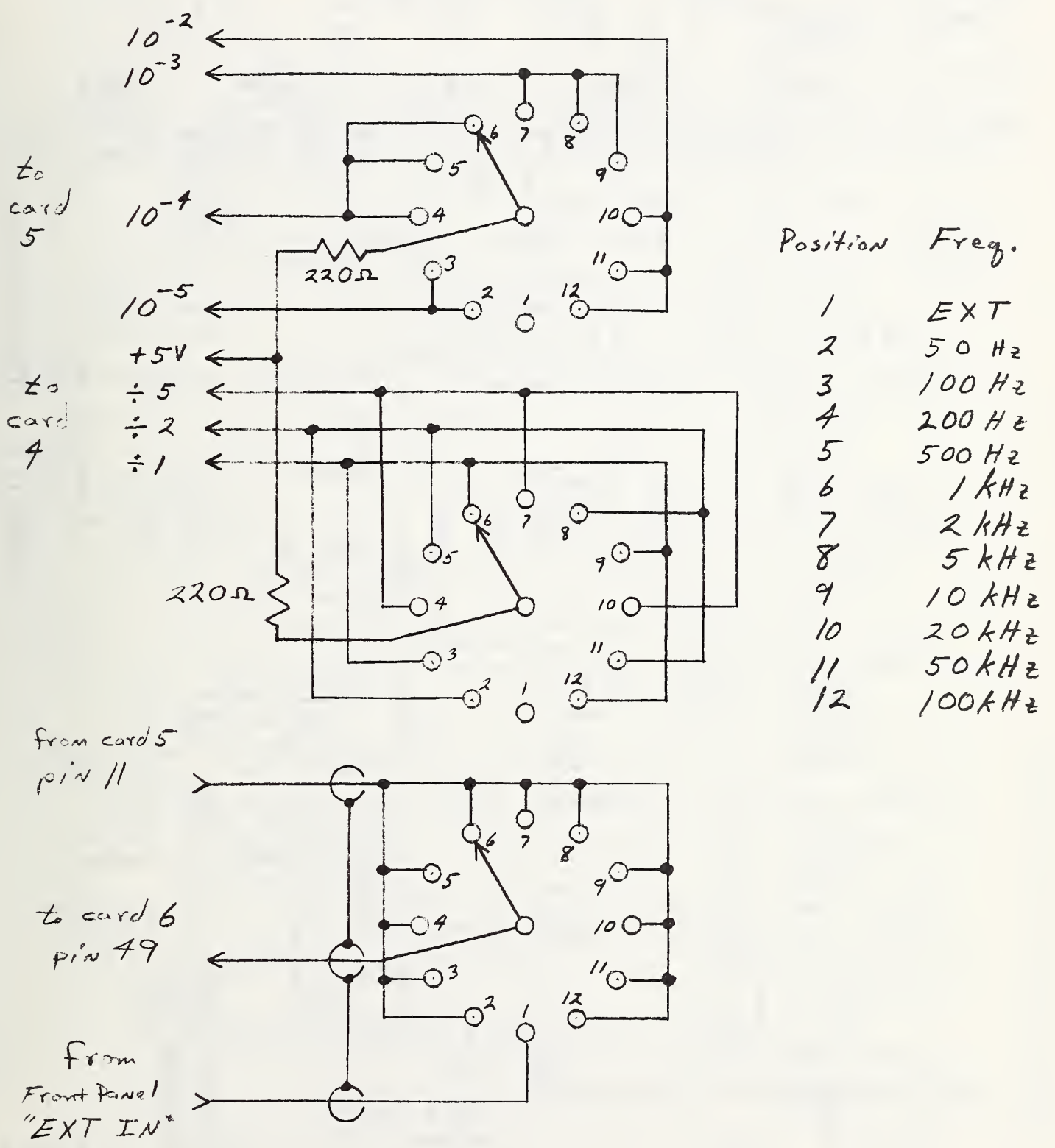


Figure 17. Repetition Rate Switch. 29

Fig. 18

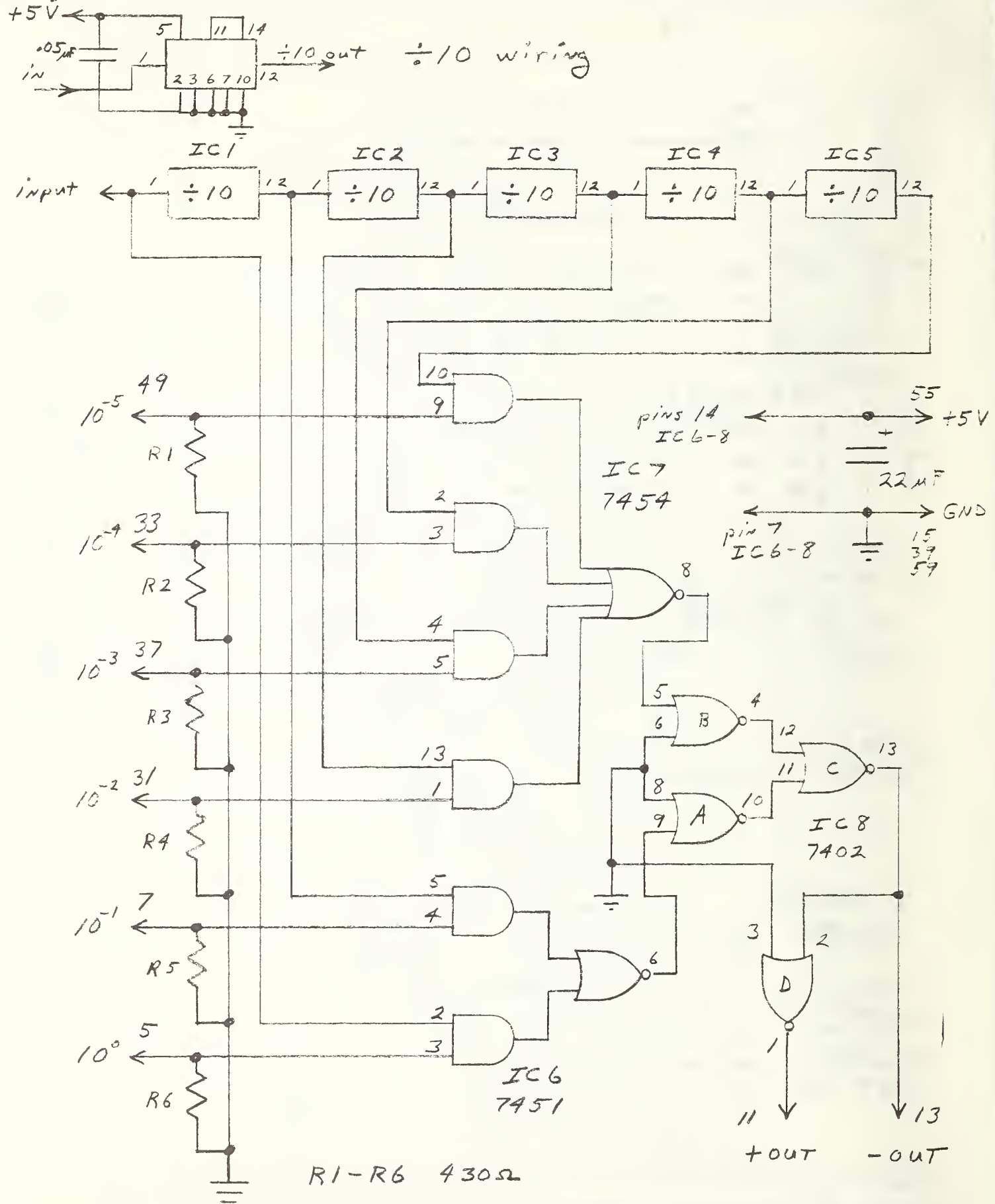


Figure 18. Divider.

Fig. 19

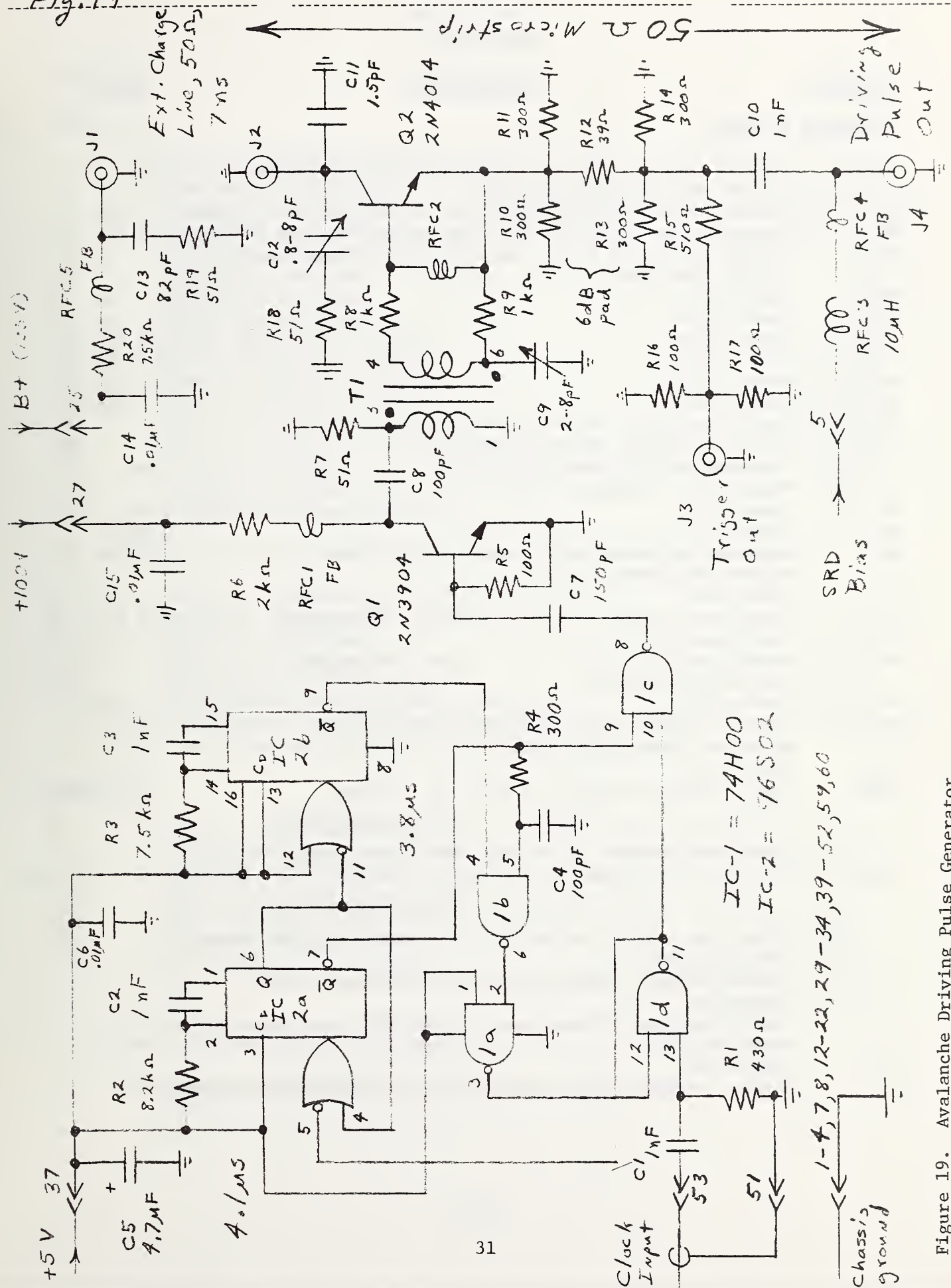


Figure 19. Avalanche Driving Pulse Generator.

PARTS LIST

<u>Part No.</u>	<u>Description</u>	<u>Value</u>
<u>Microwave Hardware</u>		
DL1	Coaxial cable, 50 ohm, 3 mm, semirigid, Phelps-Dodge 141-50, SMA plugs on each end	75 ns
DL2	Coaxial cable, RG-58/U, SMA right angle plugs on each end	7 ns
DL3	Coaxial cable, RG-55/U, SMA right angle plug and BNC plug	1.5ns
DL4	Coaxial cable, 50 ohm, 3 mm, semirigid, Phelps-Dodge 141-50, SMA plugs	5 ns
DL5	Same as DL4	6 ns
DL6	Same as DL4	6 ns
DL7	Same as DL4	0.5ns
DL8	Same as DL4	6 ns
DL9	Same as DL4	5.2ns
DL10	Same as DL4	.46ns
DL11	Coaxial adapter, SMA male/SMA male	
DL12	Coaxial adapter, SMA male/SMA male	
R1	Termination, SMA male, dc-18 GHz Midwest Microwave model 2055	50 Ω
R2	Same as R1	50 Ω
R3	Same as R1	50 Ω
R4	Attenuator, SMA male/SMA female, dc-18 GHz, Midwest Microwave model 333	10 dB
R5	Same as R4	6 dB
C1	Capacitor, coaxial, series blocking, NBS design, see figure 32	0.9 pF
DC1	Hybrid coupler, 90°, 12.4 - 18 GHz, SMA female, Anaren model 10019-3	3 dB
DC2	Same as DC1	3 dB
S4	Coaxial switch, dc-18 GHz, SMA female, 12 V, HP model 8761A option 555	SPDT
S5	Same as S4	SPDT
SRD1	Step recovery diode; $V_B > 15$ V, $T_T < 80$ ps, $\tau \sim 10$ ns, $.25$ pF $< C_j(6$ V) $< .5$ pF, Alpha model DVB-6100A; mounted in NBS SRD mount, see figures 32 & 33	24 V, 60 ps
SRD2	Step recovery diode; $V_b > 15$ V, $T_T < 80$ ps, $\tau \sim 10$ ns, $.25$ eF $< C_j(6$ V) $< .5$ pF, Alpha model DVB-6100A; mounted in NBS, K _j band waveguide, SRD mount, see figure 34	24 V, 60 ps
J1	Coaxial adapter, BNC jack/BNC jack, bulkhead mount, UG-492A/U	
J2	Coaxial adapter, flange mount N jack/SMA jack, omni-Spectra model OS-21011	
J3	Same as J2	
J4	Coaxial adapter, BNC jack/BNC jack, bulkhead mount, UG-492A/U	

PARTS LIST
(continued)

<u>Part No.</u>	<u>Description</u>	<u>Value</u>
<u>Card 1</u>		
R1	Resistor, composition, 1/2 W, 5%	1.5 k Ω
C1	Capacitor, electrolytic	500 μ F, 50 V
C2	Capacitor, electrolytic	500 μ F, 50 V
C3	Capacitor, electrolytic	680 μ F, 25 V
C4	Capacitor, tantalum	1 μ F, 25 V
C5	Capacitor, tantalum	1 μ F, 25 V
C6	Capacitor, tantalum	1 μ F, 25 V
C7	Capacitor, tantalum	1 μ F, 25 V
CR1	Diode, rectifier, silicon	1N4004
CR2	Diode, rectifier, silicon	1N4004
CR3	Diode, rectifier, silicon	1N4004
CR4	Diode, rectifier, silicon	1N4004
CR5	Diode, rectifier, silicon	1N4004
CR6	Diode, rectifier, silicon	1N4004
CR7	Diode, 18 V zener	1N5248
IC1	Integrated voltage regulator, 15 V	7815
IC2	Integrated voltage regulator, 5 V	7805

The following are part of card 1 electronics but are mounted on the main chassis.

R2	Resistor, composition, 1/2 W, 5%	3.3 Ω
C8	Capacitor, tantalum	1 μ F, 25 V
C9	Capacitor, tantalum	1 μ F, 25 V
C10	Capacitor, tantalum	47 μ F, 20 V
Q1	Transistor, Ge, PNP, power	2N443
IC3	Integrated voltage regulator, -15 V	LM320
TI	Transformer, 115 V primary, 36 V multitap secondary, Transformer Electronics Corp., Boulder, Colorado	TEC#0801000

Card 2

R1	Resistor, wire wound 3 W, 5%	1k Ω
R2	Resistor, wire wound, 5 W, 5%	30 k Ω
C1	Capacitor, electrolytic, 250 V	20 μ F
C2	Capacitor, electrolytic, 250 V	20 μ F
CR1	Diode, rectifier, silicon	1N4007
CR2	Diode, rectifier, silicon	1N4007
CR3	Diode, rectifier, silicon	1N4007
CR4	Diode, rectifier, silicon	1N4007
F1	Fuse	1/16 A

Transformer T2 is mounted on the chassis.

T2	Transformer, Stancor, P6134, 1.2 A	117:6.3 VAC
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PARTS LIST
(continued)

<u>Part No.</u>	<u>Description</u>	<u>Value</u>
<u>Card 3</u>		
R1	Resistor, composition, 1/2 W, 5%	22 k Ω
R2	Deleted	
R3	Resistor, composition, 1/2 W, 5%	10 Ω
R4	Resistor, metal film, 1/2 W, 5%	51 k Ω
R5	Resistor, composition, 1/4, 5%	4.7 k Ω
R6	Resistor, composition, 1/4 W, 5%	1.8 k Ω
R7	Resistor, 10 turn trimmer	2.0 k Ω
R8	Resistor, composition 1/4 W, 5%	4.7 k Ω
R9	Resistor, composition, 1/4 W, 5%	100 k Ω
R10	Deleted	
R11	Resistor, composition, 1/4 W, 5%	100 k Ω
R12	Resistor, wire wound, 3 W, 5%	47 Ω
R13	Resistor, 10 turn trimmer	5 k Ω
R14	Resistor, composition, 1/4 W, 5%	1.3 k Ω
R15	Resistor, composition, 1/4 W, 5%	1.8 k Ω
R16	Resistor, composition, 1/4 W, 5%	1.0 k Ω
R17	Resistor, composition, 1/4 W, 5%	100 k Ω
R18	Resistor, composition, 1/4 W, 5%	20 k Ω
R19	Resistor, composition, 1/4 W, 5%	100 k Ω
R20	Resistor, 10 turn trimmer	5 k Ω
C1	Capacitor, electrolytic, low leakage	1 μ F, 250 V
C2	Capacitor, tantalum	4.7 μ F, 25 V
C3	Capacitor, tantalum	4.7 μ F, 25 V
C4	Capacitor, tantalum	4.7 μ F, 25 V
C5	Capacitor, tantalum	4.7 μ F, 25 V
C6	Capacitor, tantalum	10 μ F, 25 V
CR1	Diode, rectifier, silicon	1N4007
CR2	Diode, 6.8 V zener	1N5235
CR3	Diode, 6.8 V zener	1N5235
CR4	Diode, signal, silicon	1N4153
CR5	Diode, signal silicon	1N4153
CR6	Diode, signal, silicon	1N4153
CR7	Diode, signal, silicon	1N4153
CR8	Diode, 100 V zener	1N5271
IC1	Integrated operational amplifier	741
IC2	Integrated operational amplifier	741
Q1	Transistor, high voltage, silicon, NPN	Motorola MJE-340
Q2	Deleted	
Q3	Transistor, high voltage, silicon, NPN	Motorola MJE-340
Q4	Transistor, silicon, NPN	2N3904
Q5	Transistor, silicon, NPN	2N3904
Q6	Transistor, high voltage, silicon, NPN	Motorola MJE-340
Q7	Transistor, silicon, NPN	2N3904
Q8	Transistor, medium power, silicon, NPN	2N4922

PARTS LIST
(continued)

<u>Part No.</u>	<u>Description</u>	<u>Value</u>
<u>Card 4</u>		
R1	Resistor, composition, 1/4 W, 5%	39 k Ω
R2	Resistor, composition, 1/4 W, 5%	22 k Ω
R3	Resistor, composition, 1/4 W, 5%	100 Ω
R4	Resistor, composition, 1/4 W, 5%	680 Ω
R5	Resistor, composition, 1/4 W, 5%	100 k Ω
R6	Resistor, composition, 1/4 W, 5%	100 k Ω
R7	Resistor, composition, 1/4 W, 5%	10 k Ω
R8	Resistor, composition, 1/4 W, 5%	10 k Ω
R9	Resistor, composition, 1/4 W, 5%	1 k Ω
R10	Resistor, composition, 1/4 W, 5%	430 Ω
R11	Resistor, composition, 1/4 W, 5%	430 Ω
R12	Resistor, composition, 1/4 W, 5%	430 Ω
R13	Resistor, composition, 1/4 W, 5%	430 Ω
R14	Resistor, composition, 1/4 W, 5%	430 Ω
R15	Resistor, composition, 1/4 W, 5%	430 Ω
C1	Capacitor, ceramic trimmer	5-18 pF
C2	Capacitor, silver mica	20 pF
C3	Capacitor, silver mica	220 pF
C4	Capacitor, silver mica	220 pF
C5	Capacitor, ceramic	1 nF
C6	Capacitor, ceramic	0.05 μ F, 12 V
C7	Capacitor, ceramic	0.05 μ F, 12 V
C8	Capacitor, ceramic	0.05 μ F, 12 V
C9	Capacitor, silver mica	100 pF
C10	Capacitor, tantalum	4.7 μ F, 25 V
C11	Capacitor, tantalum	4.7 μ F, 25 V
C12	Capacitor, tantalum	4.7 μ F, 25 V
C13	Capacitor, tantalum	4.7 μ F, 25 V
L2	Wire jumper--use if needed for freq. adjust	
RFC1	Ferrite bead on R3 lead	
RFC2	R.F. Choke, miniature	220 μ H
Y1	Crystal, quartz, type CS-1 parallel resonance, 32 pF load	10.000 MHz
Q1	Transistor, silicon, NPN	2N4275
Q2	Transistor, field effect	2N5245
Q3	Transistor, silicon, NPN	2N4275
IC1	Integrated circuit, TTL	7400
IC2	Integrated circuit, TTL	7490
IC3	Integrated circuit, TTL	7454

Card 5

R1	Resistor, composition, 1/4 W, 5%	430 Ω
R2	Resistor, composition, 1/4 W, 5%	430 Ω
R3	Resistor, composition, 1/4 W, 5%	430 Ω
R4	Resistor, composition, 1/4 W, 5%	430 Ω
R5	Resistor, composition, 1/4 W, 5%	430 Ω
R6	Resistor, composition, 1/4 W, 5%	430 Ω

PARTS LIST
(continued)

<u>Part No.</u>	<u>Description</u>	<u>Value</u>
<u>Card 5 (cont.)</u>		
C1	Capacitor, disc ceramic	0.05 μ F, 12 V
C2	Capacitor, disc ceramic	0.05 μ F, 12 V
C3	Capacitor, disc ceramic	0.05 μ F, 12 V
C4	Capacitor, disc ceramic	0.05 μ F, 12 V
C5	Capacitor, disc ceramic	0.05 μ F, 12 V
C6	Capacitor, disc ceramic	0.05 μ F, 12 V
IC1	Integrated circuit, TTL	7490
IC2	Integrated circuit, TTL	7490
IC3	Integrated circuit, TTL	7490
IC4	Integrated circuit, TTL	7490
IC5	Integrated circuit, TTL	7490
IC6	Integrated circuit, TTL	7451
IC7	Integrated circuit, TTL	7454
IC8	Integrated circuit, TTL	7402
<u>Card 6</u>		
R1	Resistor, composition, 1/4 W, 5%	430 Ω
R2	Resistor, composition, 1/4 W, 5%	8.2 k Ω
R3	Resistor, composition, 1/4 W, 5%	7.5 k Ω
R4	Resistor, composition, 1/4 W, 5%	300 Ω
R5	Resistor, composition, 1/4 W, 5%	100 Ω
R6	Resistor, composition, 1/4 W, 5%	2.0 k Ω
R7	Resistor, composition, 1/4 W, 5%	51 Ω
R8	Resistor, composition, 1/8 W, 5%	1.0 k Ω
R9	Resistor, composition, 1/8 W, 5%	1.0 k Ω
R10	Resistor, composition, 1/8 W, 5%	300 Ω
R11	Resistor, composition, 1/8 W, 5%	300 Ω
R12	Resistor, composition, 1/8 W, 5%	39 Ω
R13	Resistor, composition, 1/8 W, 5%	300 Ω
R14	Resistor, composition, 1/8 W, 5%	300 Ω
R15	Resistor, composition, 1/8 W, 5%	510 Ω
R16	Resistor, composition, 1/8 W, 5%	100 Ω
R17	Resistor, composition, 1/8 W, 5%	100 Ω
R18	Resistor, composition, 1/8 W, 5%	51 Ω
R19	Resistor, composition, 1/8 W, 5%	51 Ω
R20	Resistor, composition, 1/8 W, 5%	7.5 k Ω
C1	Capacitor, ceramic	1 nF
C2	Capacitor, silver mica, 5%	1 nF
C3	Capacitor, silver mica, 5%	1 nF
C4	Capacitor, silver mica, 10%	100 pF
C5	Capacitor, tantalum, 25 V	4.7 μ F
C6	Capacitor, ceramic	0.01 μ F
C7	Capacitor, silver mica, 10%	150 pF
C8	Capacitor, silver mica, 10%	100 pF

PARTS LIST
(continued)

<u>Part No.</u>	<u>Description</u>	<u>Value</u>
<u>Card 6 (cont.)</u>		
C9	Capacitor, ceramic trimmer, Erie model 2-8A	2-8 pF
C10	Capacitor, ceramic chip, 25 V, Johanson MDI-1415	1 nF
C11	Capacitor, silver mica, 10%	1.5 pF
C12	Capacitor, glass trimmer, sub-min., Johanson gigatrim model 7291	0.8-8 pF
C13	Capacitor, silver mica 10%	82 pF
C14	Capacitor, ceramic, 200 V	0.01 μ F
C15	Capacitor, ceramic, 200 V	0.01 μ F
IC1	Integrated circuit, TTL, quad NAND	74H00
IC2	Integrated circuit, TTL, dual monostable	96S02
Q1	Transistor, Si, NPN, selected for $BV_{CER} \geq 110$ V, Motorola	2N3904
Q2	Transistor, Si, NPN, selected for $BV_{CER} \geq 140$ V, Motorola	2N4014
T1	Pulse transformer, sub-min., Mini Circuits Lab, MCL T1-1	1:1, 50 Ω
RFC1	Ferrite bead on R6 lead	0.4 μ H
RFC2	3 turns of #28 insulated wire through ferrite bead	4.7 μ H
RFC3	RF Choke, min., 10%, 455 mA	10 μ H
RFC4	Ferrite bead on RFC3 lead	0.4 μ H
RFC5	Ferrite bead on R20 lead	0.4 μ H
J1	SMA PC board mount jack, E. F. Johnson model JCM-142-0298-001	
J2	SMA PC board mount jack, E. F. Johnson model JCM-142-0298-001	
J3	SMA PC board mount jack, E. F. Johnson model JCM-142-0298-001	
J4	SMA PC board mount jack, E. F. Johnson model JCM-142-0298-001	

7. PERFORMANCE CHECK, MAINTENANCE, AND ADJUSTMENTS

NOTICE: The calibration of the NBS SHF Impulse Generator is void if the instrument has been opened or evidence exists that it has been previously opened with the NBS seal broken.

7.1. Performance Check

To determine if the NBS SHF IG is functioning properly, a simple observation of the output waveforms on a sampling oscilloscope is sufficient. The trigger output of the IG is connected to the external trigger input of the sampling oscilloscope with a short (<2m) coaxial cable. The main pulse and/or reference pulse output is connected to the signal input of the oscilloscope. The sampling oscilloscope should have a 10% to 90% transition time of less than 35 ps and an input impedance of 50 ohms. The observed waveforms should resemble Figures 3, 5, 7, and 9, section 4, if the instrument is functioning properly.

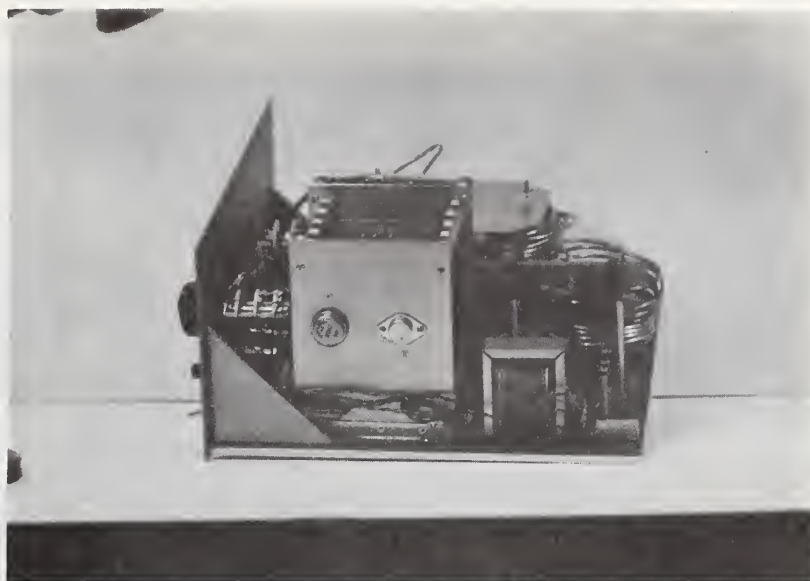
7.2. Periodic Maintenance

Periodic checks of the impulse output waveform are recommended. However, it is not recommended that the instrument be opened for periodic internal cleaning, checking of internal voltages and waveforms, or adjustment of internal controls. Any adjustment of internal controls or movement of components will change the impulse wave shape, hence its spectrum, and will invalidate the calibration.

7.3. Troubleshooting

If, after checking the impulse output waveform, it is apparent that the generator is not functioning properly, then the instrument may be opened for maintenance (calibration is voided). Figure 20 is a set of photographs of the interior. Table 7-1 lists some potential problems and their cures. Figures 21, 22, and 23 show the typical waveforms on card 6.

(a)



(b)

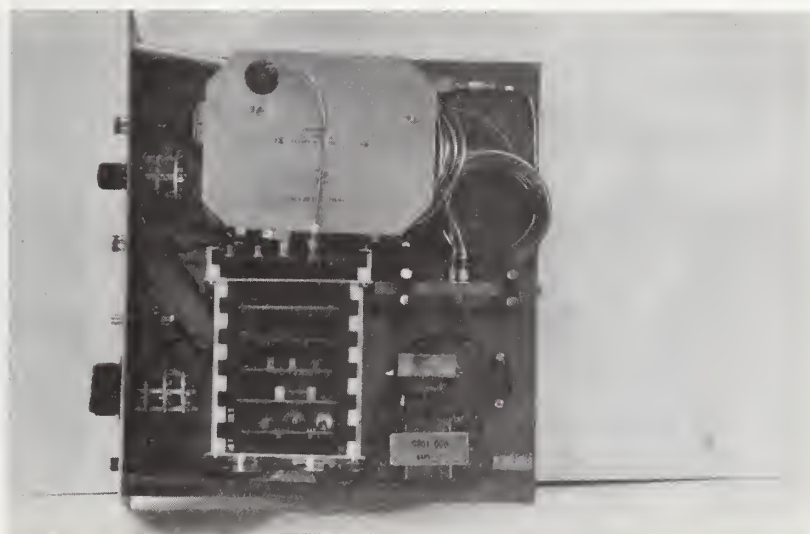
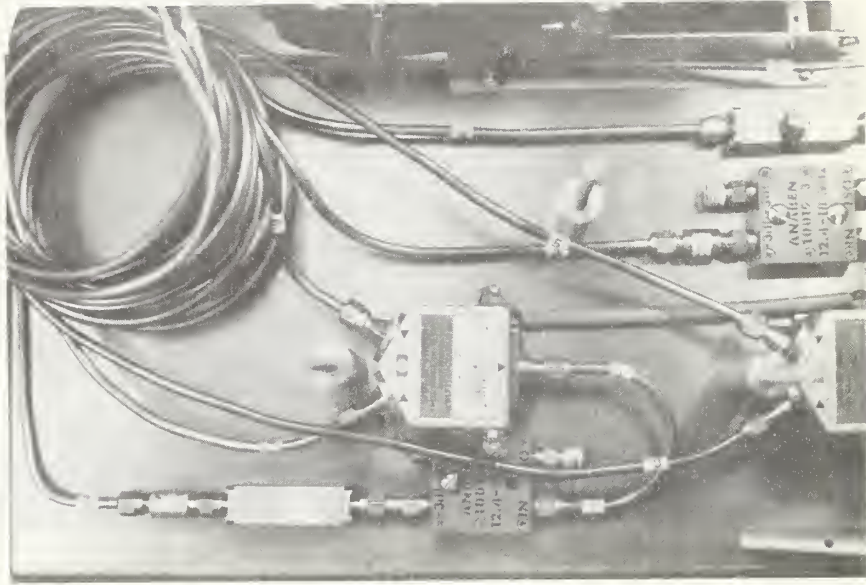


Figure 20. Photographs of the interior of the generator: (a) side view; (b) top view; (c) microwave components on the base plate with the delay line removed; (d) delay line in place.

(c)



(d)

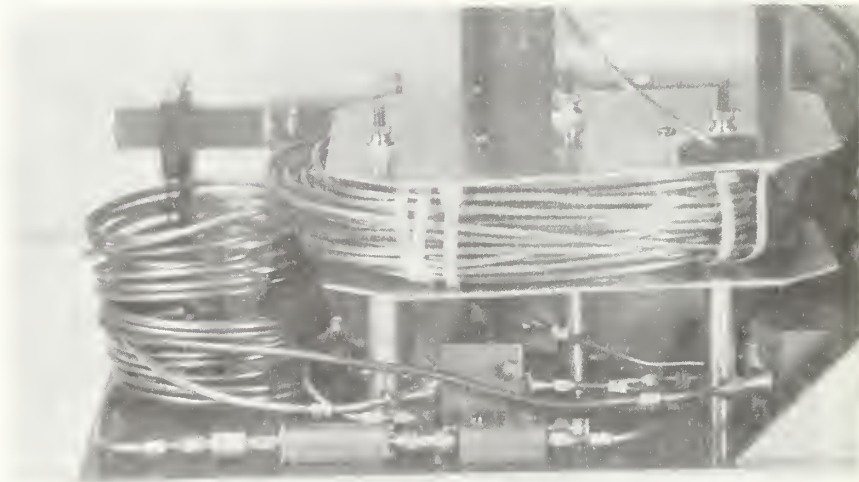


Table 7-1. Troubleshooting

Problem	Possible Cause	Cure
1. No trigger pulse output.	Q1 or Q2 defective.	Replace with selected transistor.
2. No impulse output. RF pulse and trigger pulse O.K.	SRD 1 loose in mount.	Tighten holding screw.
	SRD 1 defective.	Replace SRD 1.
	No bias current.	Check SRD bias regulator, board 3.
	Defective coaxial switches.	Repair or replace.
3. No rf pulse output. Impulse and trigger pulse O.K.	Same as #2 only with SRD 2.	See #2 above.
4. Generator free runs and can't be synchronized by ext. input pulse.	Q2, card 6 defective.	Replace Q2.
	B+ voltage set too high.	Adjust B+ to lower voltage for stable operation.
5. Generator functions properly at low rep. rates but is erratic at high rep. rates.	IC-2, card 6 defective.	Replace IC-2.
6. Excessive jitter.	B+ ripple or oscillations.	Troubleshoot HV regulator, card 3.
	Ripple or oscillations on SRD bias current.	Check current regulator on card 3.
	Malfunction in max. rep. rate circuit, card 6.	Replace IC-2.

While removal is not recommended, if the delay line (Cable 1), figure 20, needs to be removed for some reason, the following procedure should be followed:

1. Remove A.C. line from rear of cabinet.
2. Remove 4 knurled head 10-32 screws and nylon washers to remove main assembly.
3. Pull main assembly forward and disconnect internal A.C. line cord.
4. Locate the SMA connectors on Cable 1 and loosen them.
5. Gently lift and rock the complete delay line package while guiding the lower end of cable around obstructions to prevent excessive bending.
6. Place the delay line package in a safe place to prevent deforming of cable bends.
7. Reassembly is in reverse order, with special attention on not bending the cable ends excessively. Once SMA connectors are aligned and started, tighten gently and do not over-stress.
8. Standing the cabinet on its back for final assembly will eliminate any problem due to the A.C. cord inside the cabinet being pinched.
9. Do not lift on delay lines or waveguide.
10. The various delay lines have a specific order of (dis)assembly. For removal, such as when troubleshooting, Cable 1 must be removed first, following above directions. Next is Cable 5, then 6, 9, 8, 4, 3, 7, and finally 10.
11. The charge line (Cable 2) may be removed or not as required. Cable 3 will usually reach the TRIG. connector with Card 6 in an extender socket.

The following test procedure should be followed for checking out the various circuit boards:

1. With the power switch on, if the pilot lamp is out, check the main fuse.
2. Remove all the printed circuit cards. Be sure the power switch is off before removing the cards.

3. Insert card no. 1 and turn the power on. Check that the following voltages referenced to the chassis are present on card socket no. 1:

<u>Terminal</u>	<u>Voltage</u>
37	+15 V \pm 1 V
55	+ 5 V \pm 0.5 V
49	-15 V \pm 1 V
31	-18 V \pm 1.5 V

Turn the power off.

4. Insert card no. 2 and turn the power on. Check that +170 V (\pm 20V) referenced to the chassis is present at card socket no. 2, terminal 35. Turn the power off. If +170 V is not present, check the fuse on card no. 2.
5. Insert card no. 3 and turn the power on. Measure the B+ voltage present at terminal 21 of card socket no. 3. The actual value of this voltage is dependent upon the breakdown characteristics of the particular 2N4014 avalanche transistor used for Q2 on the avalanche driver board, card 6. The B+ voltage should be within \pm 2 V of the value noted on the chassis within the instrument. Record the measured B+ voltage. Typically, it will be +135 V, but depending upon the 2N4014 used, it may vary anywhere from +115 V to 150 V. Adjust R7 over its full range and check that the B+ voltage is adjustable from 100 V to 150 V. Reset the voltage to the value recorded above. Turn the power off.
6. Check that +100 V (\pm 5 V) referenced to the chassis is present at terminal 53 of card socket no. 3.
7. Connect a milliampmeter (100 mA full scale) between the chassis and terminal 57 of card socket no. 3. Set the waveform switch to Impulse. Record the dc current measured. Typically, it will be 15 mA to 20 mA but depending upon the SRD used it may be anywhere from 5 mA to 100 mA. The actual values of SRD bias used at the time of construction are noted on the chassis. Adjust R13, "set SRD Bias," on card no. 3 over its full range and check that the current is adjustable from 5 mA to 100 mA. Reset to the current noted above. Set the waveform switch to RF Pulse and repeat the above procedure with R20.
8. Insert card no. 4 and turn the power on. Connect an oscilloscope or digital frequency counter to terminal 21 of card socket no. 4. As the rep. rate switch is rotated a TTL level pulse train of various frequencies as listed in the following table should be observed.

Table 7-2. Clock board frequencies.

Rep. Rate Switch	Frequency in MHz
100	10
50	5
20	2
10	10
5	5
2	2
1	10
0.5	5
0.2	2
0.1	10
0.05	5
EXT	0

9. With the rep. rate switch set to 100, the frequency should be 10.0000 MHz ($\pm 0.001\%$). If it is out of specification, C1 on card no. 4 may be adjusted as necessary. Turn the power off.
10. Insert card no. 5 and turn the power on. Connect the oscilloscope or digital frequency counter to terminal 11 of card socket no. 5. As the rep. rate switch is rotated, a TTL level pulse train of frequencies corresponding to the switch setting should be observed. Turn the power off.
11. Insert card no. 6 and reconnect the charge line, trigger line, and delay line to the card. Turn the power on. With a 10 M Ω probe and a wide band (>200 MHz) oscilloscope, the pulse waveforms at various points in the circuit should be checked and compared with the typical waveforms shown in Figures 21 and 22. The oscilloscope should always be triggered by the positive going transition of the input TTL pulse at terminal 53 of card 6. Turn the power off.
12. If everything checks O.K. up to this point, then the problem is probably in one of the SRD modules (figs. 33 or 35). Then the suspected SRD module should be removed but not disassembled. Ohmmeter checks should be made of the SRD module. The maximum open circuit voltage of the ohmmeter should not exceed 3 V and the short circuit current should not exceed 100 mA. At the input terminal between the center conductor and the case, a finite resistance should be observed with the center pin voltage negative with respect to the case and an open circuit for the opposite polarity. If these conditions are not met, then either the SRD has

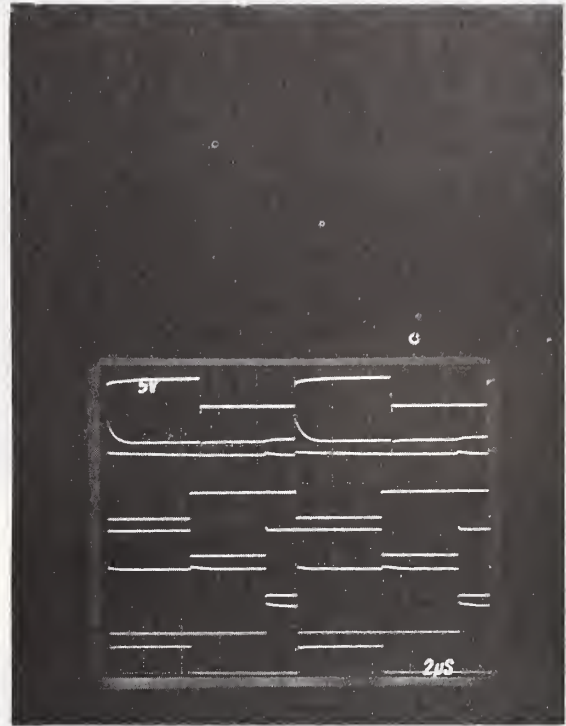
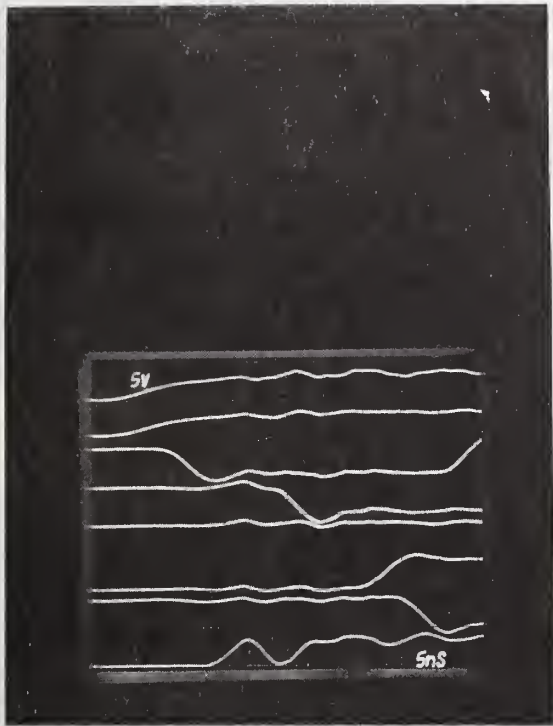


Figure 21. Typical waveforms found in the trigger lockout circuit on card 6. Vertical scale is 5 v/div. Horizontal scale is 5 ns/div. (left) and 2 μ s/div. (right). Test points are from top to bottom as follows: 1. clock input (@100 kHz); 2. IC1d pin 13; 3. IC1d pin 11; 4. IC2a pin 7; 5. IC2b pin 9; 6. IC1b pin 6; 7. IC1a pin 3; 8. IC1c pin 8. Waveforms measured with a 10 M Ω probe and a 225 MHz bandwidth oscilloscope.

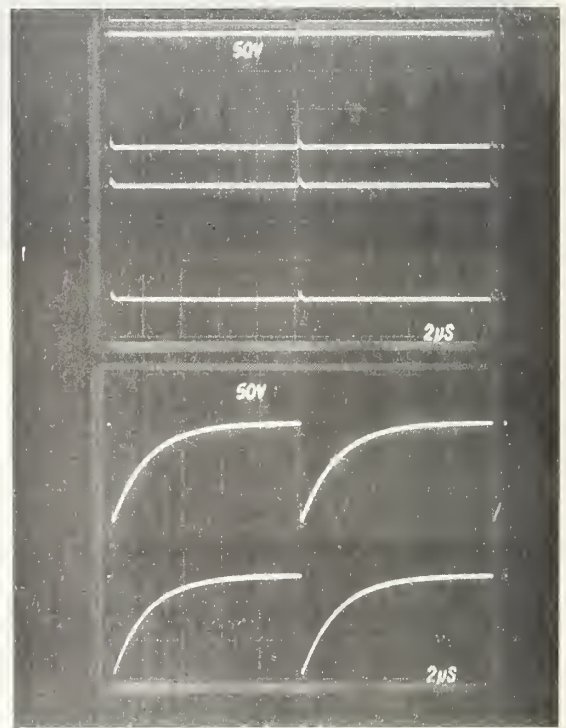
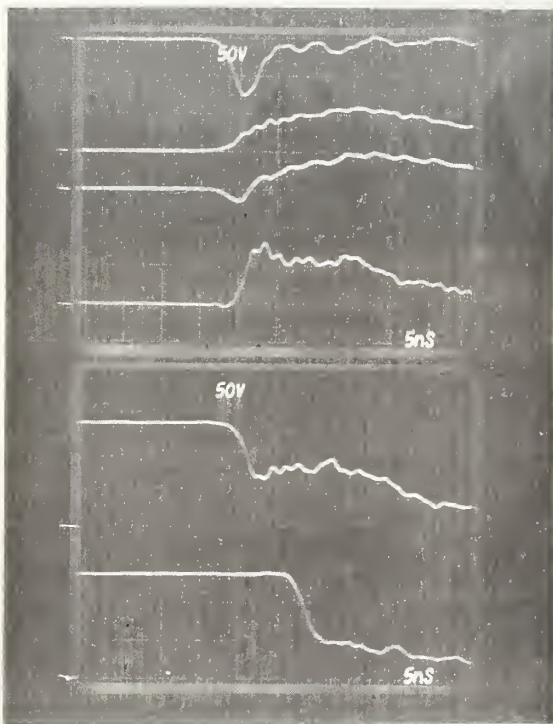
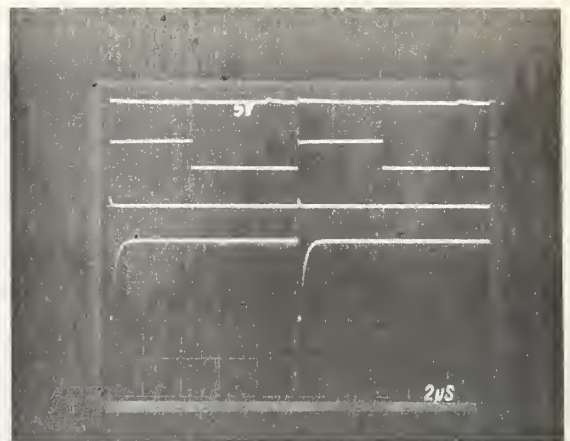
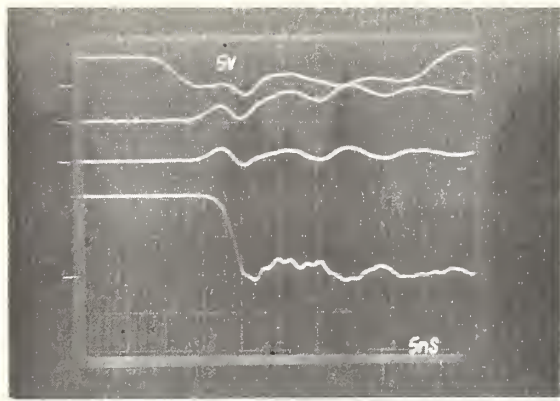


Figure 22. Typical waveforms found in the avalanche transistor circuits on card 6. Vertical scale is 5 V/div. (top 3 traces) and 50 V/div. (remaining traces). Horizontal scale is 5 ns/div. (left) and 2 μ s/div. (right). Test points are from top to bottom as follows: 1. IC1d pin 11; 2. IC1c pin 8; 3. Q1 base; 4. Q1 collector; 5. T1 primary; 6. T1 pin 4; 7. T1 pin 6; 8. Q2 emitter; 9. Q2 collector; 10. J1. Waveforms measured with a 10 M Ω probe and a 225 MHz bandwidth oscilloscope.

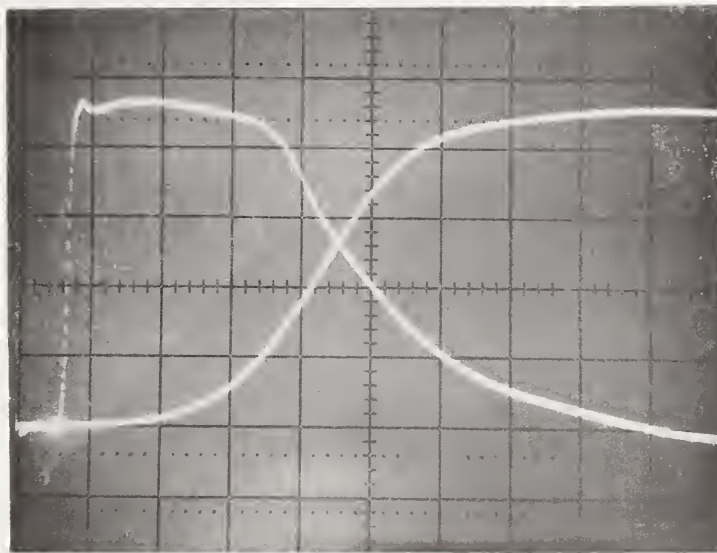
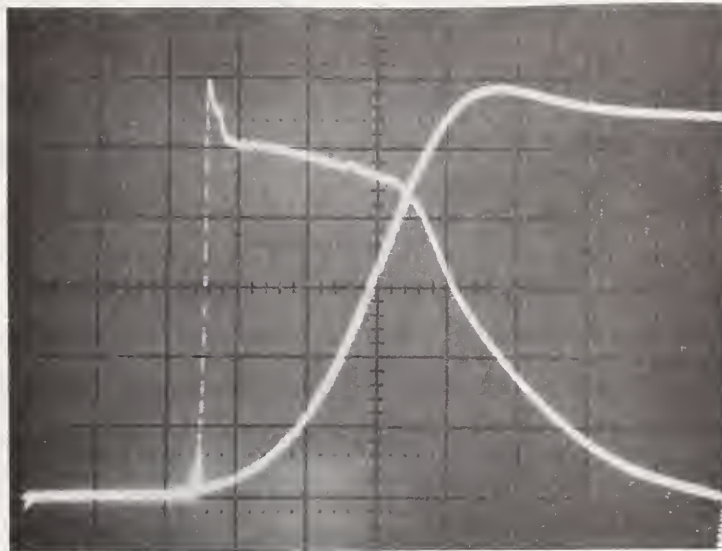


Figure 23. Driving pulse output from card 6 before installation of pi attenuator (R10-R14). Vertical scale is 10 V/div. Horizontal scales are 5 ns/div. for the pulse and 200 ps/div. for the leading edge. (a) Driving pulse directly from card 6. (b) Driving pulse after transmission through 75 ns delay line. Waveforms measured with a 40 dB pad and an 18 GHz bandwidth sampling oscilloscope.

failed or it is not making contact in the module. If it is not making good contact, this can be corrected by adjusting the SRD mounting screw.

13. It is not recommended that repairs be attempted on the SRD module. The entire instrument should be returned to NBS for repair and recalibration.

7.4. Adjustments

The NBS SHF IG was designed to have an absolute minimum number of internal adjustments. Where necessary, precision components were used instead. This improved the reproducibility of the design and the interchangeability of circuit cards. The most critical adjustments are the SRD bias as they drastically affect the impulse or rf pulse amplitude and waveshape and hence their spectra. The following table lists the possible adjustments and their effects.

Table 7-3. Adjustments.

Adjustment	Location	Nominal Setting	Effects
1. "Freq"	Card 4, C1	10.0 MHz ($\pm 0.001\%$)	Rep. rate accuracy
2. "B+"	Card 3 top, R7	+135 V (± 1 V) (see chassis notes)	Varies B+ for avalanche transistors Q2-Q3. Changes driving pulse amplitude.
3. "SRD Bias (I)"	Card 3 top, R13 (Waveform switch set to Impulse)	15-20 mA (5-100 mA range) (see chassis notes)	Varies SRD bias current. The impulse output amplitude and waveform are very dependent upon this adjustment.
4. "SRD Bias (RF)"	Card 3 top, R20 (waveform switch set to RF Pulse)	15-20 mA (5-100 mA range) (See chassis notes)	Varies SRD bias current. The rf pulse amplitude and waveform are very dependent upon this adjustment.
5. "Impulse Precursor"	Card 6, C9	min. C	Changes impulse (or rf pulse) output precursor baseline waveform and spectrum amplitude below 1GHz.
6. "Impulse Ringing"	Card 6, C12	max. C	Changes baseline ringing after impulse (or rf pulse).

8. MECHANICAL CONSTRUCTION

This section describes in detail the mechanical construction of the impulse generator. It deals with the printed circuit cards, the special SRD mounts, and the chassis construction.

Printed Circuit Boards

The first five printed circuit (P.C.) boards are conventional boards in most ways, with minor hardwired modifications in places to improve operation or make a minor change. The sixth card is much more critical and will be described in more detail later. All cards are designed to fit a standard 60 contact socket such as Amphenol 261-10030-2 or equivalent. While our cards are only 8.8 cm wide and 11 cm high, it would be simple to leave larger borders and size them to fit other guides or card file hardware. Several of these basic cards have been used before and only slight changes were required for this project, helping reduce costs.

Card 1 (fig. 24) is a low-voltage supply with only low dissipation items on the card. A 2N443 pass transistor Q1 is mounted on the mainframe, as is the -15 volt regulator LM320, IC3.

Card 2 (fig. 25) is the H.V. rectifier with the fuse mounted near the top of the card for ease of removal and as a test point.

Card 3 (fig. 26) regulates the H.V. and supplies regulated currents for SRD1 and SRD2. A second trimmer resistor was added to obtain two levels of current allowing each diode to be set up for optimum results.

Card 4 (fig. 27), the clock, contains a trimmer for frequency adjustment if needed and a different crystal could be used as long as the max. rep. rate is not exceeded.

Card 5 (fig. 28), the frequency divider, in connection with the clock uses "cold switching" on board and like all cards uses sockets to ease replacement of I.C.'s should this be needed.

The heart of the cards is no. 6 (figs. 29 and 30). Card 6 must be reproduced almost identically as high speed pulses are present and even lead dress becomes important. Several extra holes are provided on this double sided board, and wires are pushed through these and soldered on both sides as well as all components to both sides where possible. The OSM connectors should be the first items mounted as more heat is required to solder them to the

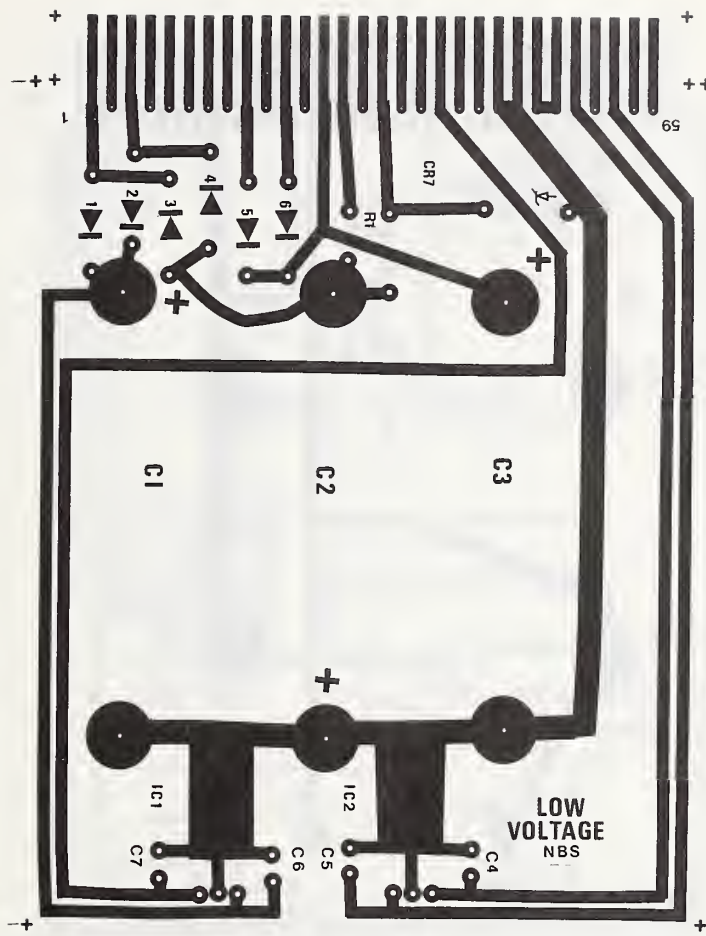


Figure 24. Low voltage, card 1, artwork.

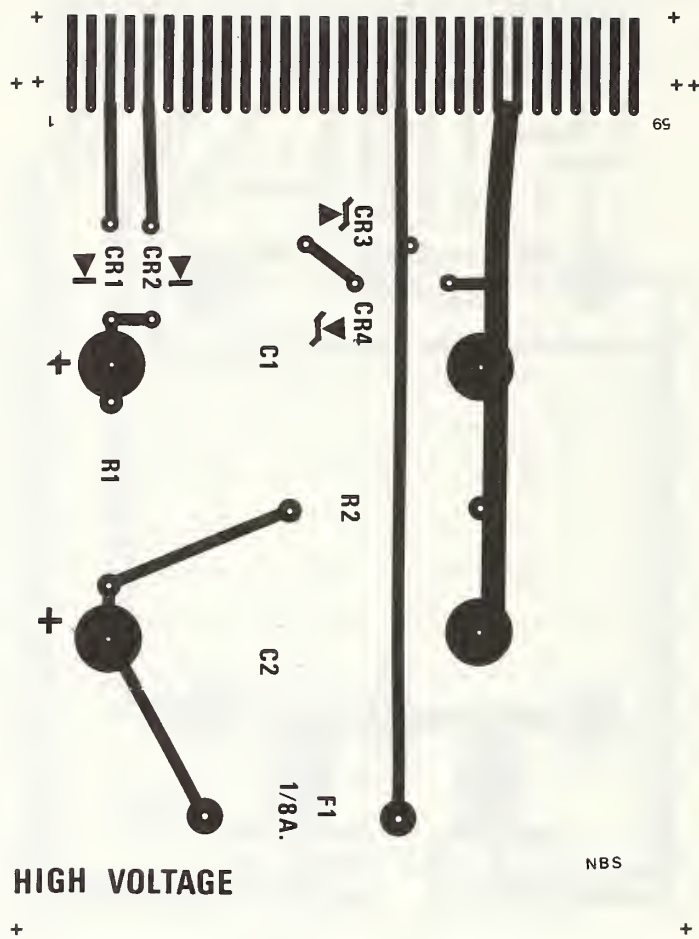


Figure 25. High voltage, card 2, artwork.

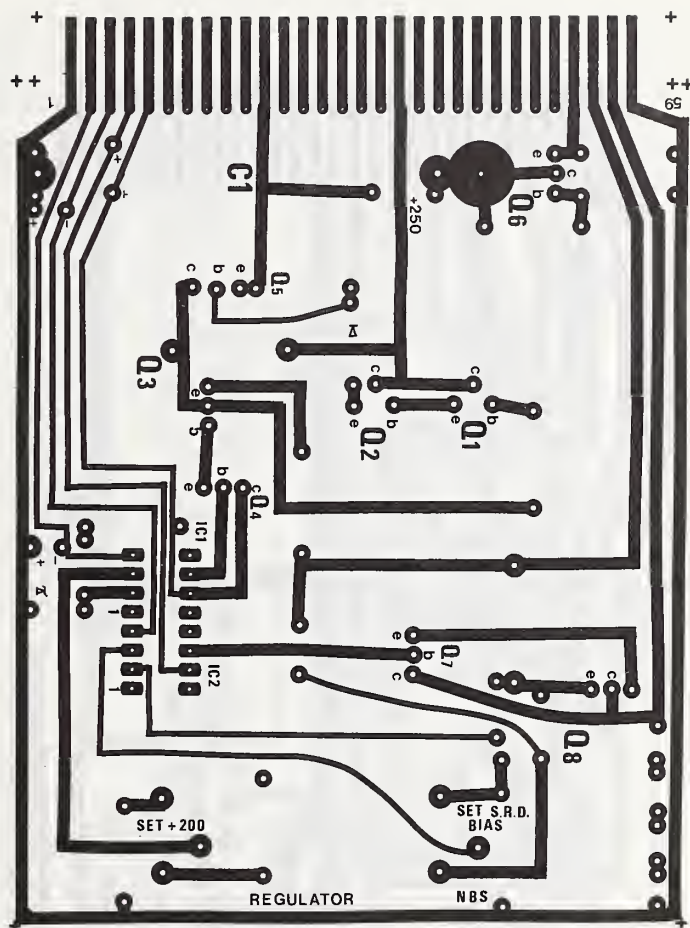


Figure 26. Regulator, card 3, artwork.

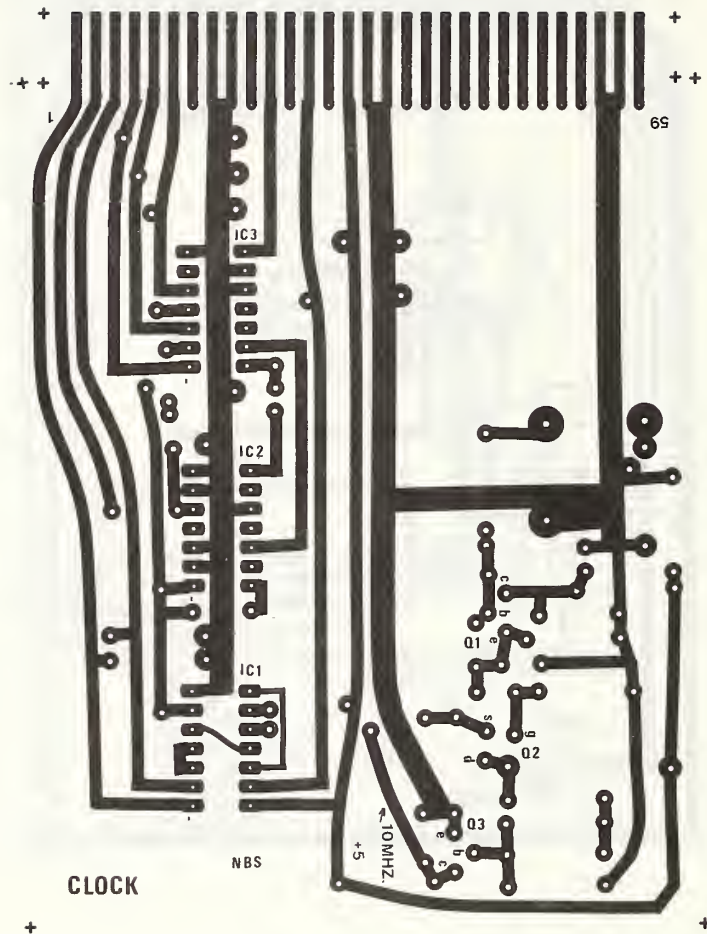


Figure 27. Clock, card 4, artwork.

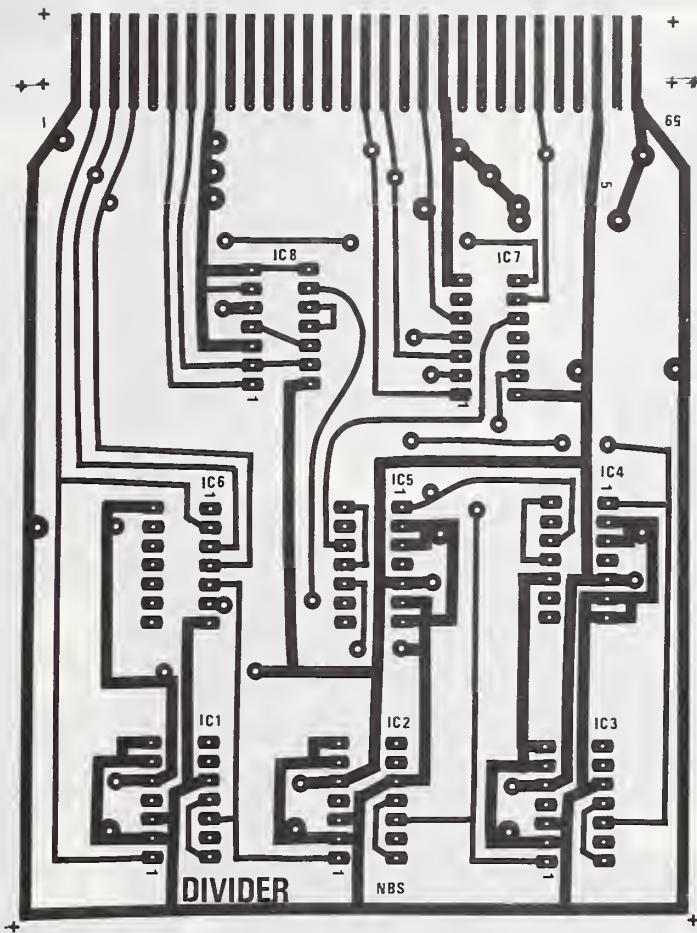


Figure 28. Divider, card 5, artwork.

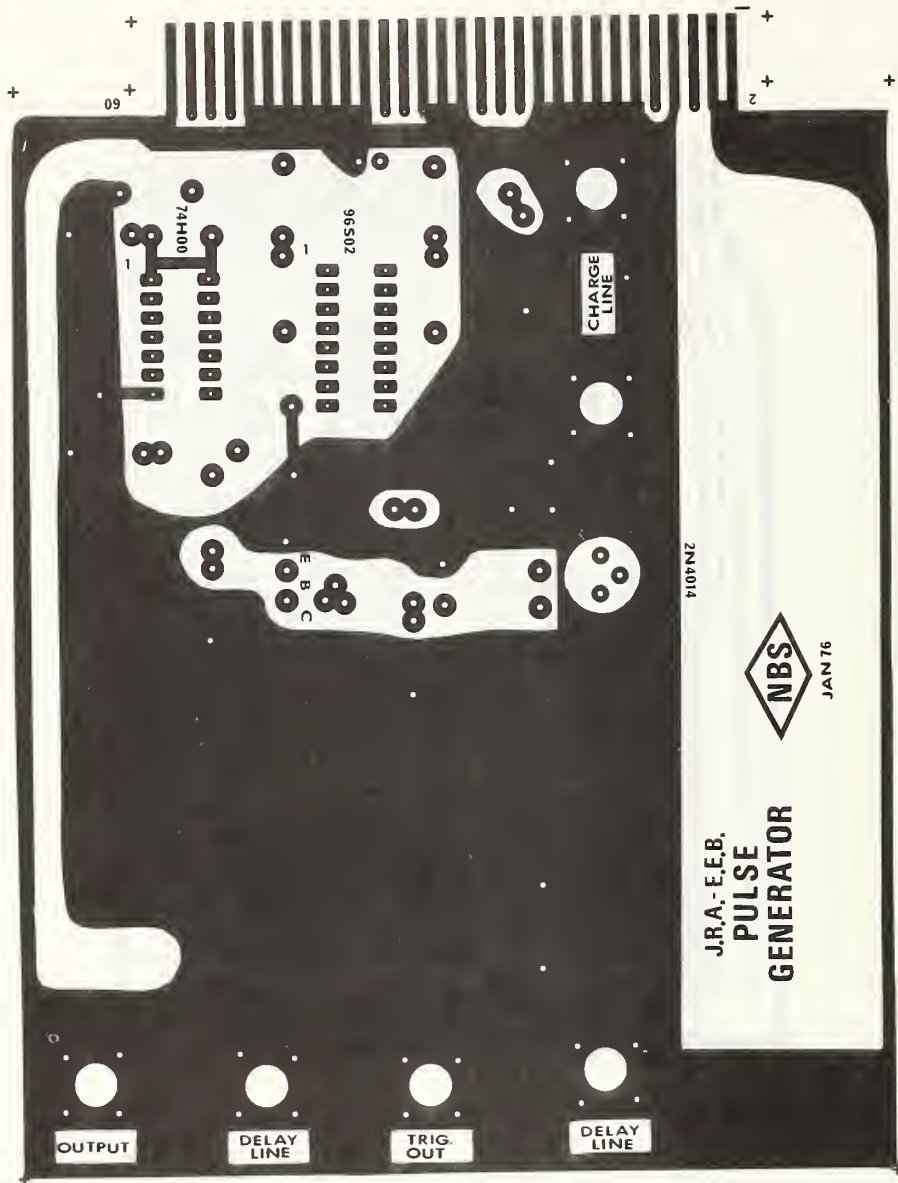


Figure 29. Top of pulse generator board 6.

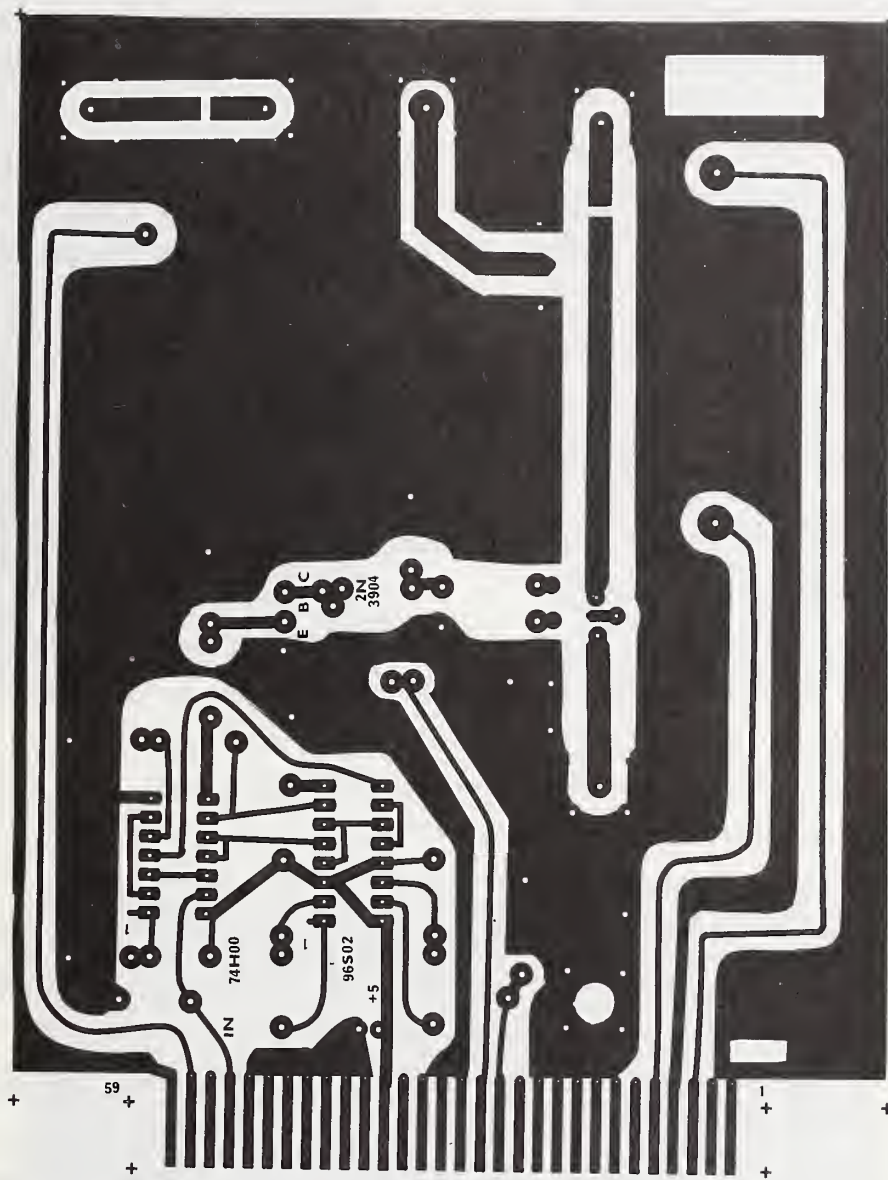


Figure 30. Bottom of pulse generator board 6.

board; and, after cooling, flux remover may be used to clean around them before other parts are mounted. Figure 31a shows the main items on the component side of the board and figure 31b shows the reverse side of the completed card. Trimmer capacitor C9 mounts near the board center at an angle of about 45°. Leads on this, as well as most of the parts on this card, have been kept as short as possible.

Using the artwork shown, two circuit traces must be cut. Using a modeler's knife or something similar, cut out 3 or 4 mm of the lead from pin 53 on the connector to IC1d, pin 13. This gap is bridged with a one nanofarad capacitor, C1.

Next, cut a 4 mm section from the stripline approximately as shown in figure 31b. 1/8 watt resistors are used at this point to form a "pi" attenuator as shown in figure 31c and described in section 5-8. Small holes should be drilled through the board here, and the final resistors chosen should be soldered on both sides. This method is also followed for the trigger divider resistors, R15-16-17 as shown in Figure 31d.

Chip capacitor C10 (fig. 31d) may be installed by lightly tinning the stripline first, then reheating just enough to flow the solder while holding C10 in place with tweezers. Excessive heat should be avoided.

Miniature socket pins are installed at the 2N4014 (Q2) location to facilitate selection and installation of an optimum device. Care should be taken to prevent filling the sockets with excessive solder due to "wicking."

Ferrite beads are used on R20, R6, and RFC3. After sliding the bead over the device's lead, bend the lead at 90° for a short distance, then back in the original direction. Keep lead lengths short.

RFC2 is made by passing a short length of #28 insulated wire through the hole in the bead so that three turns pass through the hole. Then, clean and tin the leads very close to the bead. This forms a compact choke of about 4.7 μ Hy., yet physically small as may be seen in figure 31e. This choke mounts between base and emitter as seen in figure 31f.

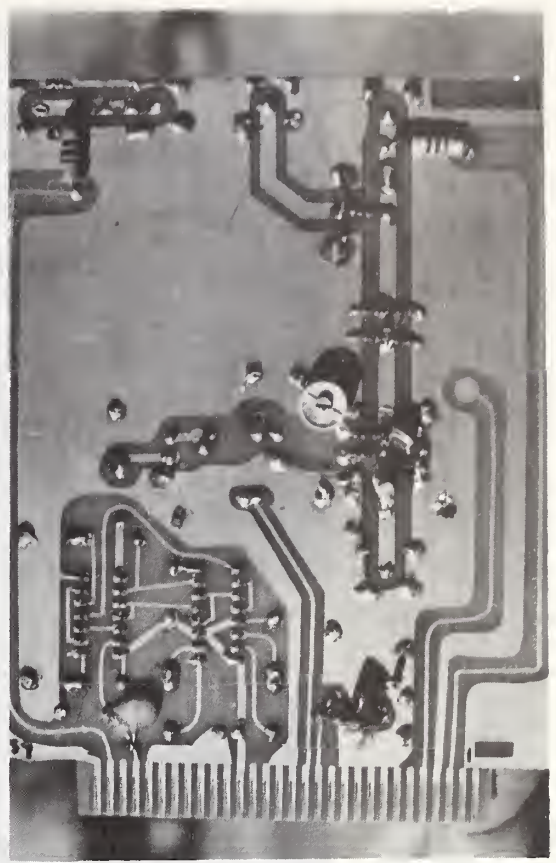
The glass trimmer C12 is soldered to the socket and charge line junction as in figure 31g, with R18 and C11 soldered to C12 and all leads kept to a minimum.

Details of the charge line termination at J1 are shown in figure 31h.

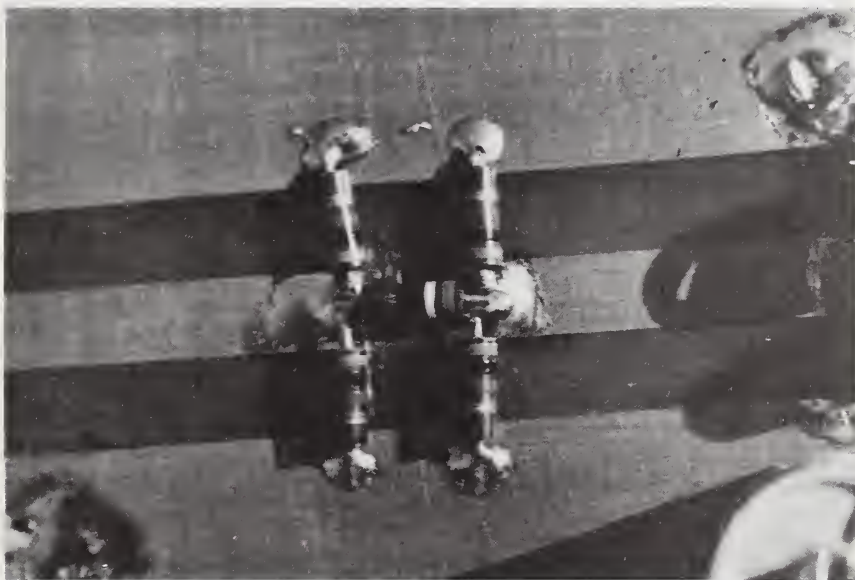
As the high speed connections to card 6 are all on board, it may be operated with a card extender as may all the other cards. This greatly assists in tuneup or troubleshooting.



(a)

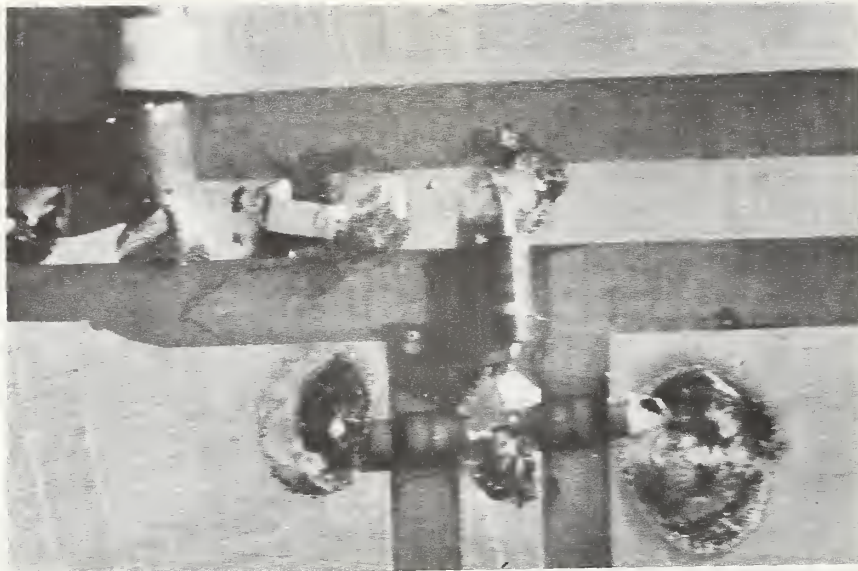


(b)



(c)

Figure 31. Component layout on card 6. (a) Top view. (b) Bottom view. (c) Pi attenuator. (d) Trigger pickoff and SRD bias insertion. (e) RFC2. (f) R18, C11, and C12 detail. (g) C12 detail. (h) Charge line termination.



(d)

Figure 31.
(continued)



(e)



(f)



(g)



(h)

Figure 31. (continued)

Capacitor C-1--SRD-1 Mount

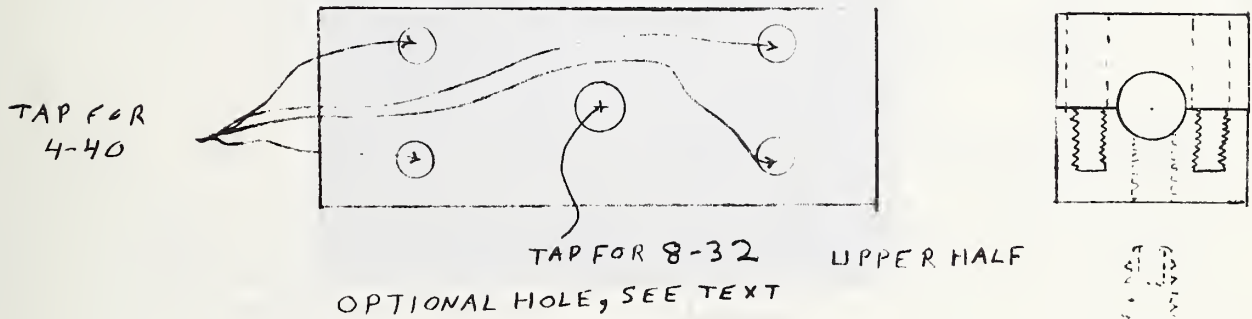
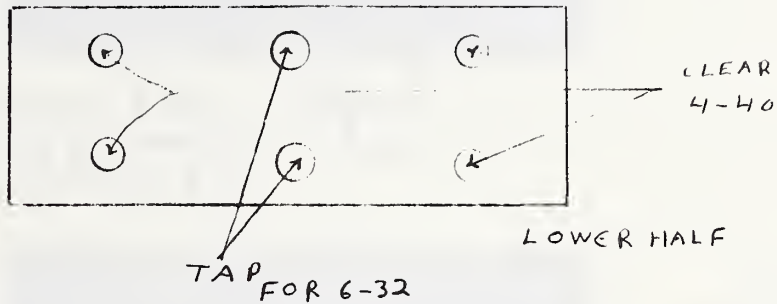
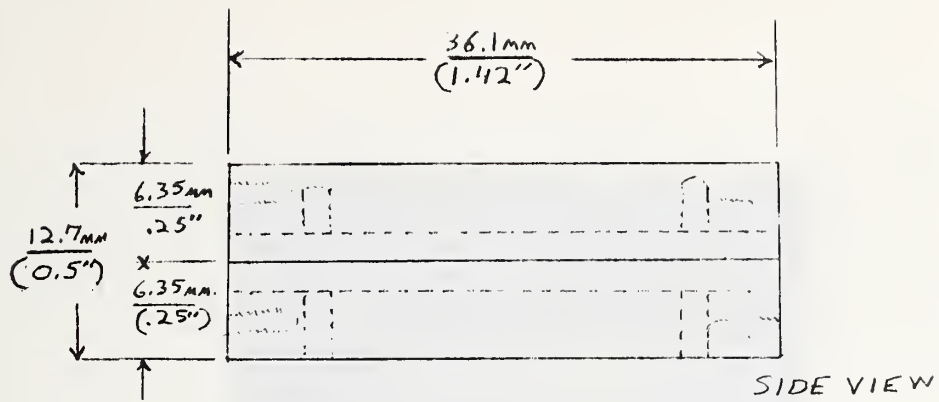
The SRD is mounted in a coaxial brass holder (figs. 32 and 33) made of two strips of 36.1 mm by 12.7 mm by 6.35 mm (1.42"x1/2"x1/4") brass flats. Two of these may be drilled and tapped allowing them to be held together rigidly while the axial bore is made. The bore size is such as to allow insertions of an OSM 204CC connector, and the length allows the ends of the center conductor almost to touch.

Two versions of the holder are used. In the first, an 8-32 threaded hole is provided in the center of the upper half to allow inserting a modified 8-32x1/2" brass set screw, which places a modified SRD in contact with the center conductor; while in the second version, the hole is omitted, and a tiny piece of 1 MIL Teflon tape closes the gap in the center conductor forming capacitor, C1. In the SRD holder, this gap is closed by carefully soldering the ends together and dressing the diameter down to maintain the 50 ohm impedance.

In both versions, the airspace remaining must be filled with small portions of Teflon with only a small hole to allow space for the SRD. The OSM 204CC connector has a captive center pin, which makes the assembly easier. One extra connector will furnish enough material to fill airspaces in the two holders.

J Band SRD Mount

The J band generator, SRD2, mount is formed of a 15 cm section of WR-62 waveguide. As shown on the drawing (fig. 34), two OSM-244-2 connectors are mounted on the waveguide section, one each 0.5 cm from the center of the waveguide. Only a large enough hole for the insulation is used, and a counter-sink or similar tool allows the flared portion of the connector to be recessed slightly to obtain a snug fit. The screws used for mounting the connectors may require dressing down as they must not extend into the waveguide and preferably should be flush. The nut shown may be soldered to the guide by turning it onto a fairly long screw or threaded stock whose threads are brushed lightly with graphite. With the guide in a clamp or vise, and with the side to be soldered up, drop the screw through both the desired hole and the connector hole. The weight of the screw will hold the nut in place long



USING #49 DRILL,
CENTER + DRILL
HOLE 3 MM. DEEP
IN TIP OF SCREW

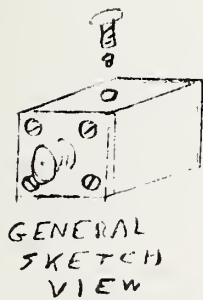
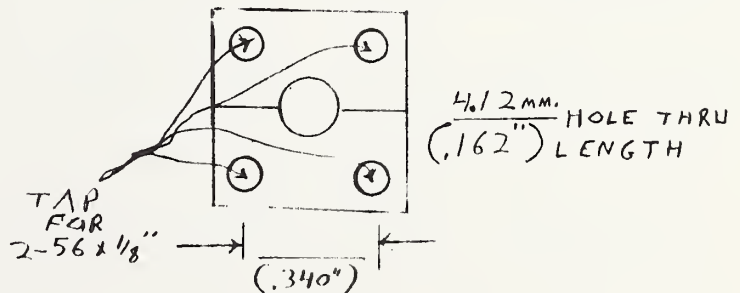
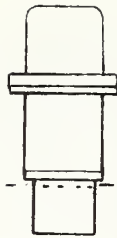
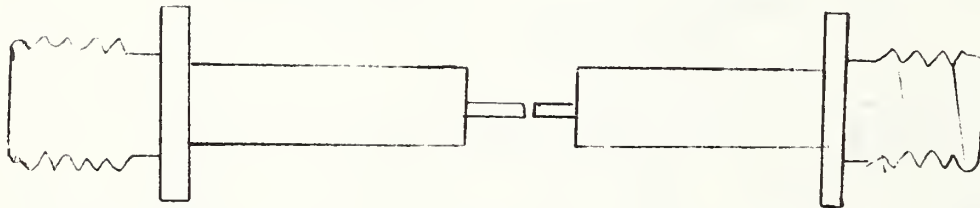


Figure 32. Capacitor C2--SRD1 mount.



DVB-6800
STEP RECOVERY DIODE

CUT HERE WITH
JEWELERS SAW. DO NOT USE
EXCESSIVE FORCE

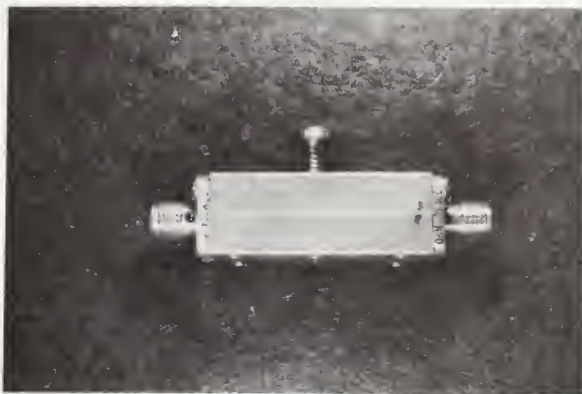


OSM 204 CC



NOTE HOLE FOR S.R.D.
IN ONE SECTION

Figure 32. (continued)

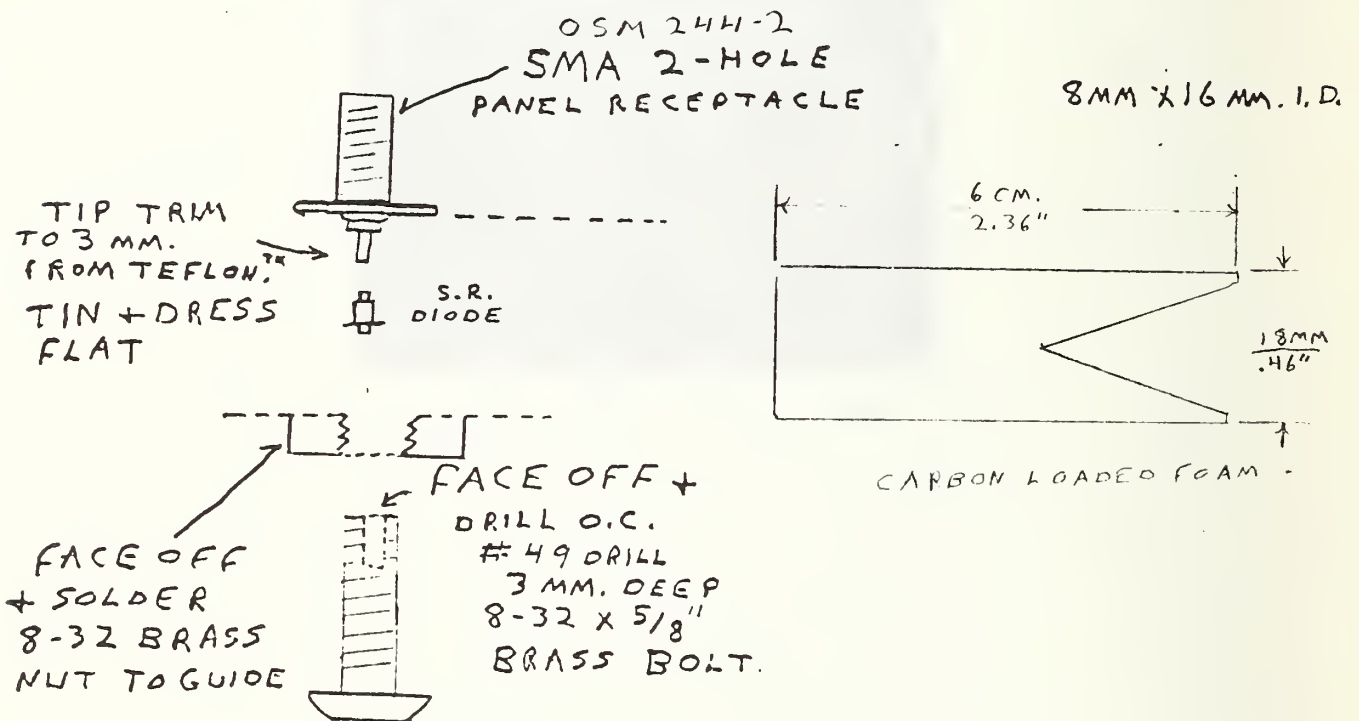
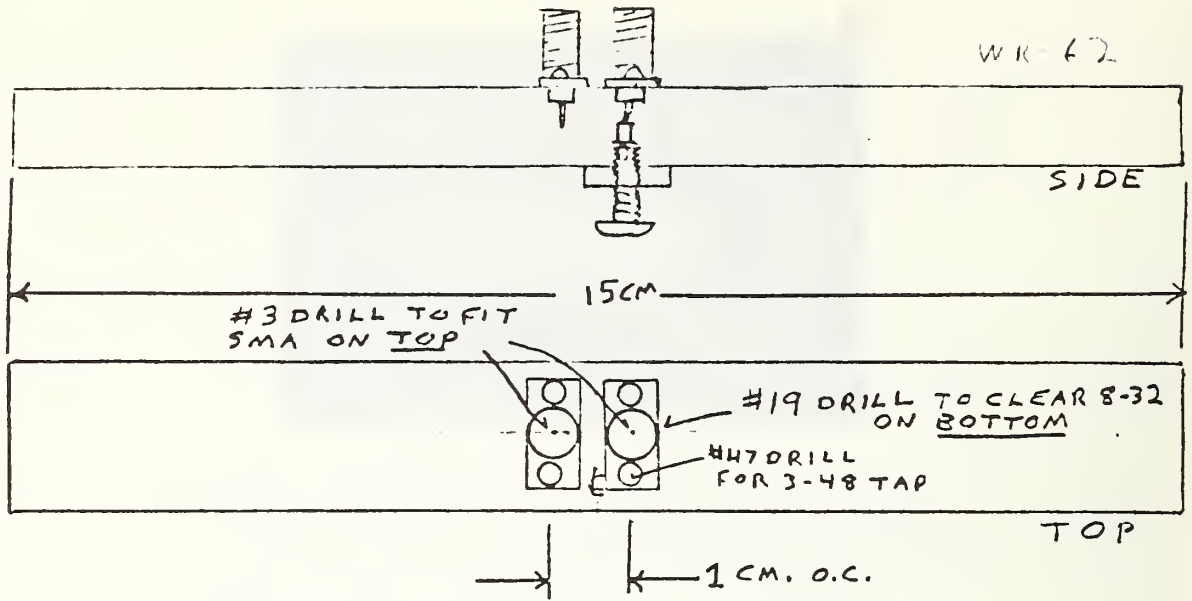


(a)



(b)

Figure 33. SRD1 coaxial mount (a) and modified SRD and set screw (b).



DRESS TIPS OF 3-48 X 1/8" BOLTS TO BE FLUSH WITH INNER WALL OF GUIDE. DE-BURR + CLEAN GUIDE WELL.

Figure 34. J band waveguide mount for SRD2.

enough to solder, and the graphite will prevent seizure of the threads. After the solder has cooled, remove the screw and carefully clean the area. It must be noted that any foreign matter inside the guide may shift the spectrum of the output signal, and great care is required to keep dirt, flux, metal filings, etc., out of this area.

Next, take one of the OSM-244-2 connectors and trim the center conductor to within 3 mm of the dielectric, tin, and dress smooth with a jeweler's file. This provides a contact area for SRD-2 when installed. The second connector may be tinned and smoothed to an even profile. This connector acts as a pickup probe and should extend to the center of the waveguide.

The SRD is mounted in a 3 mm deep hole in the end of an 8-32x5/8" brass screw, and the screw and diode may be easily threaded into place by holding the guide with the nut on the bottom and keeping the diode mounting screw vertical. Do not overtighten.

Electrical contact can be verified by an ohmmeter or curve tracer connected to the SMA connector. A photo of the assembly is shown in figure 35.

Diode Modification

Care must be taken when modifying the diode as these are easily damaged by static electricity or mechanical stress. The method used here was to hold the diode by the metal just above the flange with only enough pressure to ensure not losing it. A fine tooth jeweler's saw, size 1/0, was used to remove the excess lead length. Then a very fine file was used to dress the end smooth, as this is the point of contact with the coax center conductor in the SRD-1 mount, and also contacts the SMA center pin in the SRD-2 mount.

The last item involved in the J band mount is to make two resistive loads described in 5-4, which are fitted in the ends of the 15 cm waveguide. These were made by cutting a strip of carbon loaded foam of nominal 6.35 mm (.25") thickness to a width of 18 mm (.46") and 6 cm (2.36") length. These are then notched at one end starting at the corners and cutting toward the center about 2.54 cm (1"). These fit snugly within the guide and, after final adjustment, may be fastened in place by a drop of rubber cement.

Mechanical Chassis Construction

The basic hardware attaches to a 6.35 mm (.25") aluminium plate 38.1 cm (15") wide by 34.2 cm (13.5") deep, which is screwed to the 40 cm (15.75") by 17.8 cm (7") panel, and the two are reinforced by two triangular plates made by cutting a 10.16 cm (4") square plate of 6.35 mm (.25") aluminium on the diagonal.

The card guides as well as most other hardware are generally held to this plate by drilling and tapping the plate where required. The balance of items such as SRD mounts, couplers, etc., are bolted on through counter-bored holes on the plate's bottom side so that no screw heads protrude to block easy removal of the "chassis" from the cabinet for service or tune-up.

In the same respect, the cabinet has removeable covers allowing access to the inside while still connected into a system.

An RFI filter connects the 117 VAC line while serving the dual roles of keeping outside line noise from the electronics and at the same time reducing radiation of pulsed energy from within the cabinet.

Power transistor Q1 (2N443) and regulator IC3 (LM320) are mounted on the metal end of the card rack, which serves as a heat sink.

Photographs in figure 20 show details of the hardware layout. None of this is critical with the exception of the length of each of the coaxial lines. These are tagged at each end for easy identification and should be installed in the order mentioned in 7-2.

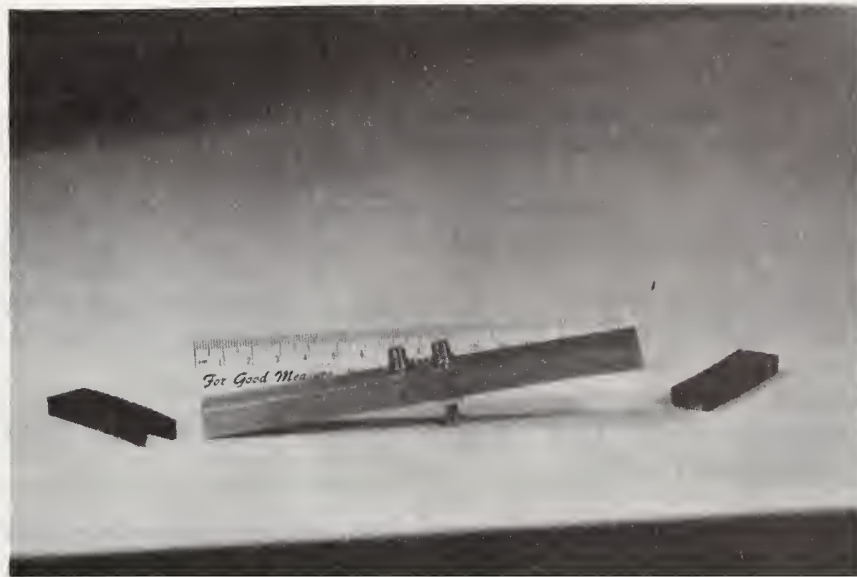


Figure 35. J band waveguide mount for SRD2 with carbon loaded foam terminations.

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<p>16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)</p> <p>A super-high-frequency (SHF) impulse generator designed and built by the National Bureau of Standards is described in detail. The generator produces three different waveforms. The first is a simple impulse of 1 volt amplitude (3 V option) and 60 ps duration with a useful spectrum (15 dB down) extending from low frequencies out to 9 GHz. The second waveform is a single cycle 5 GHz sine wave (doublet) of 0.8 volts peak-to-peak amplitude (1.6 V option). Its useful spectrum extends from 0.5 GHz to 11.7 GHz. The third waveform is an exponentially damped rf pulse. It has a center frequency of 12.5 GHz and a damping time constant of 1/4 ns. The peak-to-peak amplitude is 0.8 volts. The useful spectrum extends from 6 GHz to 18 GHz.</p>			
<p>17. KEY WORDS (six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons) Avalanche transistor; impulse generator; J band; microwave; picosecond; spectrum amplitude; step recovery diode; time domain.</p>			
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