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Evaluation of a CMOS/SOS Process Using Process Validation Wafers

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
National Engineering Laboratory
Center for Electronics and Electrical Engineering
Semiconductor Devices and Circuits Division
Washington, DC 20234

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J. S. Suehle, L. W. Linholm, and G. M. Marshall

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

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Abstract

The objective of this work was to determine baseline electrical parameters that could be used to evaluate a fabrication process. Two lots of wafers containing NBS-16 test chips were fabricated at a commercial vendor in a radiation-hard, CMOS/SOS process. These wafers were then returned to NBS for testing and evaluation. Testing was performed using an automated computer-controlled integrated circuit test system. Test results were evaluated using analysis techniques which provided a statistical estimate of selected parameters and identified spatial correlations between data sets. Further analysis was then performed in order to identify process irregularities. A complete description of the test results and analysis procedure can be found in the appendices.

Key words: integrated circuits; microelectronics; process control; process validation wafer; silicon on sapphire; test chip; test pattern; test structure; yield.

I. Introduction

This report is an extension of earlier work [1] involving the development of process assessment methods using microelectronic test structures to evaluate integrated circuit manufacturing. The primary objectives of this project were to determine if test results from a Process Validation Wafer (PVW) [2,3] accompanying a product lot of integrated circuits are representative of results on other PVW wafers within the lot and to examine electrical test results useful in evaluating and characterizing the fabrication process.

A previously developed test chip, NBS-16 [1], was fabricated by a Defense Nuclear Agency (DNA) commercial contractor and subsequently tested and evaluated at NBS. Photomasks were made from a pattern generator tape supplied by NBS. Two process lots of wafers patterned only with NBS-16 test chips were delivered to and evaluated at NBS.

An automatic computer-controlled integrated circuit test system was used to determine baseline dc electrical parameters of selected test structures. Portions of each NBS-16 test chip on a wafer were tested and electrical results recorded on a line printer and floppy disc. Statistical analysis techniques were used to evaluate the test results.

II. Experimental Details

II.A Test Chip NBS-16 Description

NBS-16 is a square test chip, 250 mils (6.35 mm) on a side. It is divided into seven basic areas as shown in figure 1. Four areas of interest have a specific function as listed in table 1. A computer-generated plot of NBS-16 is shown in figure 2. Only test structures found in the process parameter pattern of Area 1 were used in this project. This pattern is a square approximately 100 mil (2.54 mm) on a side and contains 28 test structures laid out in 2 by N [4] probe pad arrays. For this pattern, N varies between 10 and 14 depending on the column being measured. A detailed description of the design rules, test methods used, and chip layout can be found elsewhere [1].

II.B Wafer Fabrication

The integrated circuit process used to fabricate NBS-16 was a radiation-hard, phosphorus-doped silicon gate, CMOS/SOS process. An eight-level mask set is used in the fabrication process. Two lots of NBS-16 test chips were fabricated. The first lot contained nine 3-in. (76.2-mm) diameter wafers; the second lot contained seventeen 3-in. (76.2-mm) diameter wafers. Eighty-two sites on the wafer are occupied by identical NBS-16 test chips, and five sites are used for test chips designed by the DNA contractor.

II.C Electrical Measurements and Testing System Description

Electrical testing of each wafer was performed on 11 selected test structures included in the Process Parameter Area in each of the 82 NBS-16 test chip sites. A total of 20 electrical parameters, listed in table 2, were measured.

The system used to measure each of the wafers consists of a minicomputer-controlled electrical test system. This system is similar to commercial testing systems currently available. A block diagram of the measurement system is shown in figure 3. The minicomputer is configured with 352 kilobytes of memory, two 10 megabyte disc drives, two floppy disc drives, a 9-track dual density magnetic tape drive, a system console, several CRTs and hard-copy terminals, a line printer, a digital plotter, and a multiuser operating system. The test equipment consists of an automatic wafer prober which can be programmed in English or metric units; a current supply with 1-μA resolution and compliance voltage programmable up to 100 V; two voltage supplies with 1-mV resolution and 550-mA current capability; a digital voltmeter with 1-μV resolution and operating modes which provide either high precision or high speed readings; a digital picoammeter with 1-pA resolution; 16 single-pole, single-throw dry reed relays; and eight 20-channel scanners, all digitally programmable and operating under computer control.

The software to control these instruments consists of a set of assembly language subprograms, one to control each instrument; several assembly language subroutines for mathematical operations; and a driver within the operating system. The instruments may also be controlled in an interactive mode from a terminal.

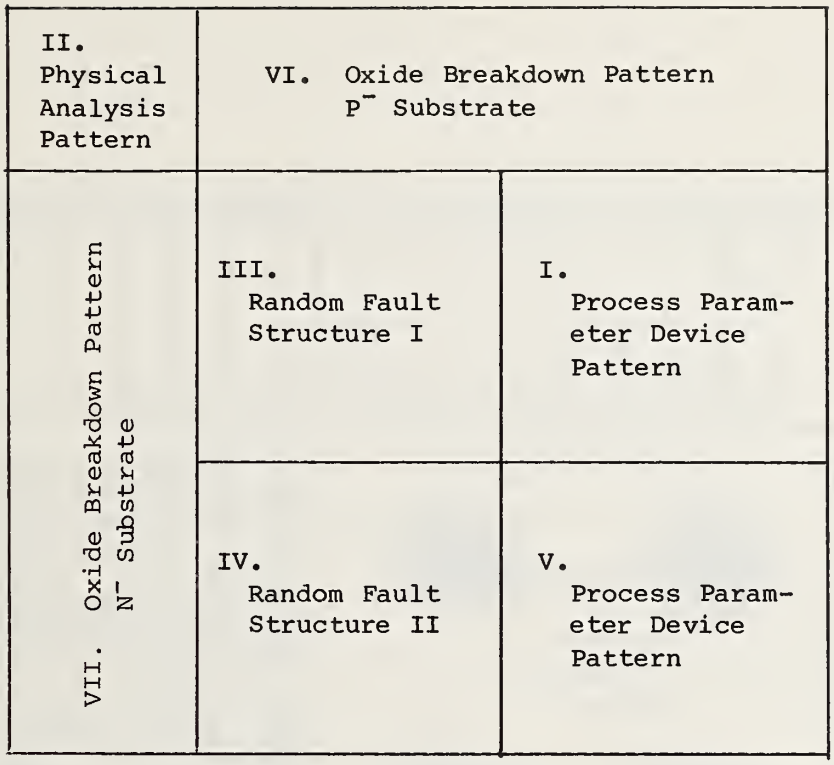

Figure 1. Seven basic areas on NBS-16 test chip.

Table 1. Functions of Four Different Areas on NBS-16.

	Area	Function
I.	Process Parameter Pattern	Allows the measurement of baseline electrical parameters.
II.	Physical Analysis Pattern	Provides physical, visual, or beam analysis. No electrical testing is performed.
III.	Random Fault Structure I	Allows the determination of the random fault density of a MOSFET array and the location and nature of any faults detected.
IV.	Random Fault Structure II	Allows the determination of the fault density of gate oxide dielectric breakdown, primarily at the epi island edge.

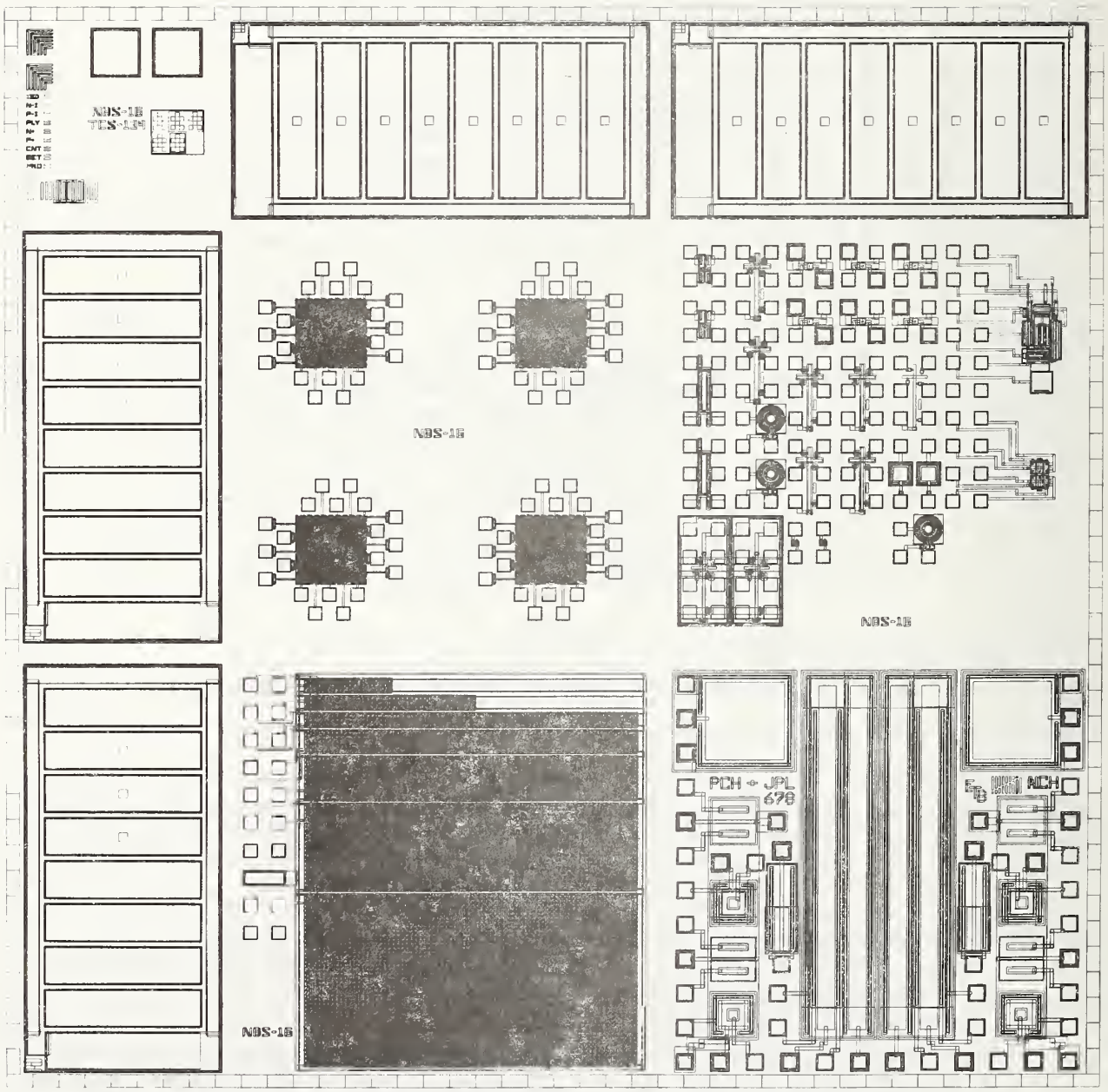

Figure 2. Computer-generated plot of test chip NBS-16.

Table 2. Structures Tested and Parameters Measured on NBS-16.

Structure	Parameter Measured on Each Structure
n-channel four-terminal MOSFET p-channel four-terminal MOSFET	Threshold voltage Source-to-drain breakdown voltage Source-to-drain leakage current
p^+ cross-bridge sheet resistor n^+ cross-bridge sheet resistor p^+ doped poly cross-bridge sheet resistor n^+ doped poly cross-bridge sheet resistor Metal cross-bridge sheet resistor	Sheet resistance Linewidth of conducting layer
Metal-to-p^+ contact resistor Metal-to-n^+ contact resistor Metal-to-p^+ doped poly contact resistor Metal-to-n^+ doped poly contact resistor	Contact resistance

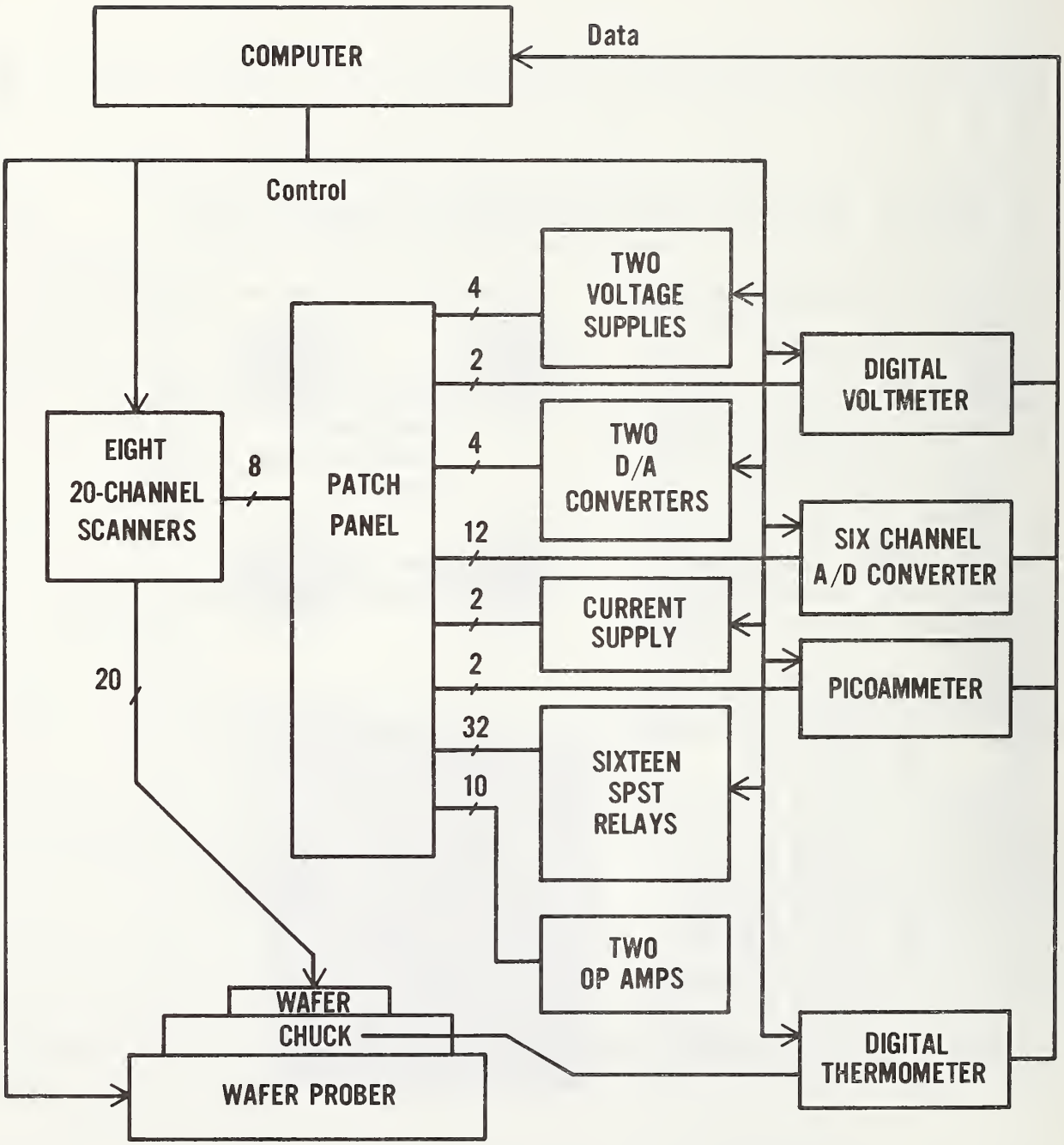

Figure 3. Block diagram of computer-controlled electrical test system.

In a typical measurement, data are acquired from selected structures at each test site on a wafer, and the test results are logged to the line printer and recorded on a floppy disc. The testing time is determined by the data acquisition rate and the total number of sites tested.

III. Techniques Used for Analysis of Test Results

Test results were statistically examined using the statistical analysis program STAT2 [5]. This program is an interactive program which can analyze one parameter by:

1. calculation of mean, median, and standard deviation of data within the set,

2. identification and deletion of test results from structures suspected of containing defects,

3. entry of a reduced data set sample into a data base for use in calculating sample correlation coefficients of other data sets, and

4. production of a wafer map illustrating parameter variations across a wafer and from wafer to wafer.

In order to characterize a process lot, it is necessary to determine important process parameters which predict or determine the degree of process control and to establish the value and range of these parameters. To accurately determine these parameters, it is necessary to identify test results from defective structures or defective measurements which do not accurately represent the parameter being measured.

Data can be eliminated for the following conditions:

1. the data were known to be bad based on previous knowledge (for example, a test structure which has been physically damaged due to handling, etc.),

2. the test instrument indicates an open or short circuit compliance limit, or

3. the test results are beyond a known limit determined by experience or results from a circuit simulation model.

For this experiment, only the first two conditions were used because no previous experience existed, and accurate circuit simulation results are not available.

In order to improve the effectiveness with which data from suspected defective test sites can be identified, a statistical analysis program, STAT2, was used which provides a means for identification and subsequent elimination of these test results. First, all points in the main data set that meet conditions 1 and 2 are eliminated and a mean, μ, and standard deviation, σ, are determined for the remaining data set. A parameter, Y_i, is rejected as an

outlier if the magnitude of the difference between the datum and the mean is greater than K times the standard deviation or:

$$|Y_i - \mu| > K\sigma \ , \tag{1}$$

where K is a value to be calculated. K is determined by specifying p, the probability of rejecting Y_i when it, in fact, is not an outlying observation. The value of K satisfies the equation [6]:

$$\int_{-\infty}^{K} \frac{e^{\frac{-x^2}{2}}\, dx}{\sqrt{2\pi}} = \frac{1 + (1 - p)^{1/N}}{2} \ . \tag{2}$$

After K is determined, outliers are excluded using eq (1). This procedure is repeated until a data set N' is determined from which no new outliers have been detected. For this work, p = 0.2 was determined to be a reasonable value based on previous experience. The remaining data set, N', can now be characterized by the statistics μ and σ.

In evaluating a process, it is important to evaluate the spatial variation of the parameter over a wafer and to determine if similarities exist between parameter variations of interest. In order to do this, a correlation technique was used to identify similarities between data sets. A sample correlation coefficient, r, was calculated between data sets where:

$$r = \frac{\sum_{i=1}^{n} (x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\left[\sum_{i=1}^{n} (x_i - \bar{x})^2\right]\left[\sum_{i=1}^{n} (y_i - \bar{y})^2\right]}} \ ,$$

where $\bar{x}$ and $\bar{y}$ are the sample means of x and y, respectively, over the n points [7]. The parameter r must take on values in the range (-1,1). This coefficient serves as a screen or indicator of possible correlations; the closer the coefficient is to one, the greater the degree of correlation.

Many parameter variations may be examined and compared quickly with correlation coefficients given for every data set pair. Analyzing particular correlation or lack of correlation provides a further insight into determining process-related problems. Sample correlation coefficients were determined from reduced data sets in order to minimize data storage and handling. A reduced sampling plan containing fourteen samples located at sites illustrated in figure 4 was used.

Once correlation between data sets is determined, it can be presented in the form of wafer maps. The wafer map is an eight-scale, gray-tone illustration of the spatial parameter variations over the wafer. Examples of wafer maps can be found in the appendices. The "x" symbols on the maps represent the

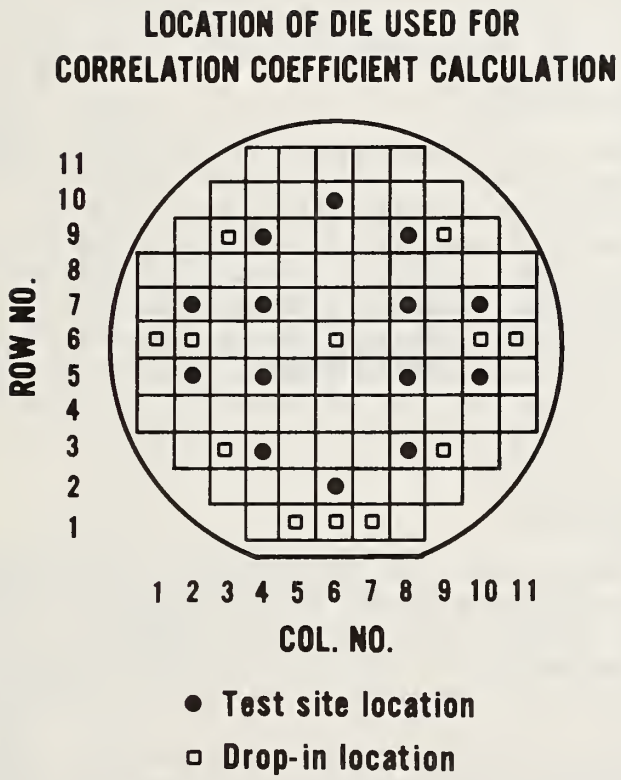

Figure 4. Location of test sites used for determining correlation coefficient for the 14-point sample and location of sites which contained patterns other than NBS-16.

locations of nondefective test sites. These sites provided the test results used to calculate mean, median, and standard deviation for each parameter. A further description of the statistical analysis techniques used in this work can be found in Appendix A.

IV. Evaluation of Test Results

IV.A First Lot Evaluation

The first lot delivered by the DNA contractor contained nine wafers. The wafers were tested and evaluated using the equipment and analysis techniques previously described.

IV.A.1 Wafer-to-Wafer Evaluation

Test results from these measurements can be evaluated on a wafer-to-wafer basis or on an intrawafer basis. Figure 5 shows the wafer-to-wafer variation of p- and n-channel threshold voltage within the first lot. Each point represents the average value of approximately 82 measurements across one wafer. The bars represent the sample standard deviation of the data set on that wafer. As can be seen, the threshold voltages appear to be very uniform within the lot. In general, all of the parameters measured showed a high degree of uniformity with less than a 5-percent wafer-to-wafer variation. Other test results indicate that the measurement repeatability on a given wafer is within 1 to 2 percent.

IV.A.2 Intrawafer Evaluation

Sample correlation coefficients between measured parameters were determined for each wafer in the lot in order to identify possible parameter correlations within a wafer. Table 3 shows a table of sample correlation coefficients for selected parameters for wafer C1. This table is representative of similar tables that were generated for other wafers within the lot.

The table shows correlation between parameters where correlation is expected. For instance, a high degree of correlation is expected between the sheet resistance of the polycrystalline silicon used to mask the p^+ implant and the sheet resistance of the poly used to mask the n^+ implant during device fabrication. Since both poly resistors are heavily n^+ doped from previous process steps and little compensation is expected in the first sheet resistor, a high degree of correlation is expected between the two parameters. As can be seen from table 3, a sample correlation coefficient of 0.89 was calculated. Electrical linewidth measurements from test structures in adjacent areas are also expected to show a high degree of correlation since optical lithography techniques were used to define the structures. Intrawafer linewidth variation showed a flat profile which is indicative of a good etch control.

Average values for all measured parameters are summarized in table 4. Wafer maps illustrating selected process parameter variations across a representative wafer in the lot are given in Appendix B. Test results from the first process lot suggest a reasonable degree of process control as evidenced by a uniform distribution (less than 5 percent) in critical process parameters within a wafer and from wafer to wafer.

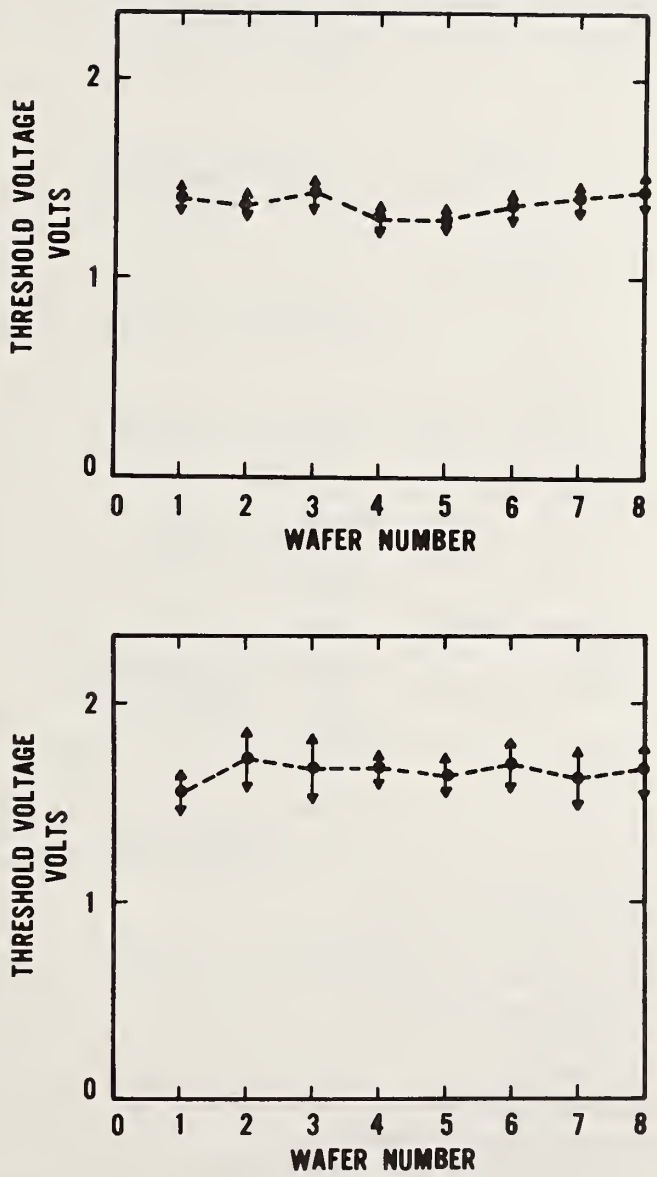

Figure 5. Average p-channel threshold voltage (top) and average n-channel threshold voltage versus wafer number for the first lot.

Table 3. Sample Correlation Coefficients Based on a 14-Site Sampling Plan for One Wafer in the First Lot Tested.

	1	2	3	4	5	6	7	8	9	10
1	1.00									
2	-0.12	1.00								
3	-0.41	0.17	1.00							
4	0.31	0.33	0.08	1.00						
5	-0.32	-0.19	0.12	-0.31	1.00					
6	-0.30	-0.29	0.13	-0.31	0.99	1.00				
7	-0.67	0.48	0.25	-0.03	0.24	0.22	1.00			
8	0.18	-0.06	-0.59	-0.37	0.21	0.15	0.14	1.00		
9	-0.76	0.56	0.50	0.12	0.15	0.12	0.89	-0.22	1.00	
10	-0.11	0.35	-0.36	-0.15	-0.10	-0.22	0.12	0.55	0.13	1.00

1 p-channel MOSFET threshold voltage
2 p-channel MOSFET breakdown voltage
3 n-channel MOSFET threshold voltage
4 n-channel MOSFET breakdown voltage
5 p^+ cross-bridge linewidth
6 n^+ cross-bridge linewidth
7 p^+ doped poly cross-bridge sheet resistance
8 p^+ doped poly cross-bridge linewidth
9 n^+ doped poly cross-bridge sheet resistance
10 n^+ doped poly cross-bridge linewidth

Table 4. Summary of Test Results for the First Process Lot Tested (2193-1).

Structure Number	Structure	Parameter	Typical Manufacturer's Value	Average Measured Parameter Value	Average Std Deviation
1	p-channel MOSFET	threshold voltage	-1.5 V	-1.42 V	0.06
		source-to-drain breakdown voltage	-24 V	-22.71 V	0.30
2	n-channel MOSFET	threshold voltage	1.7 V	1.67 V	0.13
		source-to-drain breakdown voltage	20 V	22.86 V	0.37
9	p^+ cross-bridge sheet resistor	p^+ sheet resistance	110-130 Ω/□	111.1 Ω/□	1.4
		electrical linewidth	-	12.13 μm	0.26
10	n^+ cross-bridge sheet resistor	n^+ sheet resistance	15-40 Ω/□	67.33 Ω/□	2.12
		electrical linewidth	-	11.87 μm	0.26
11	p^+ doped poly cross-bridge sheet resistor	p^+ doped poly sheet resistance	-	43.29 Ω/□	6.14
		electrical linewidth	-	11.53 μm	0.27
12	n^+ doped poly cross-bridge sheet resistor	n^+ doped poly sheet resistance	-	29.11 Ω/□	1.78
		electrical linewidth	-	11.49 μm	0.25
13	metal cross-bridge sheet resistor	metallization sheet resistance	-	0.03 Ω/□	0.00
		electrical linewidth	-	9.33 μm	0.33
18	metal-to-p^+ contact resistor	metal-to-p^+ contact resistance	-	5.54 Ω	0.69
19	metal-to-n^+ contact resistor	metal-to-n^+ contact resistance	-	13.73 Ω	3.56
20	metal-to-p^+ doped poly contact resistor	metal-to-p^+ doped poly contact resistance	-	1.07 Ω	0.23
21	metal-to-n^+ doped poly contact resistor	metal-to-n^+ doped poly contact resistance	-	0.98 Ω	0.11

IV.B Second Lot Evaluation

The second lot contained 17 wafers. These wafers were fabricated using a process similar to that used in the first lot.

Electrical testing of 20 device parameters was completed on four wafers from the lot. Selected parameters were tested on four additional wafers. All data were statistically evaluated using STAT2 and wafer maps were produced for each measured parameter.

IV.B.1 Wafer-to-Wafer Evaluation

The average value and sample standard deviation for each measured parameter were calculated and plotted for each wafer tested across the lot. Generally, the parameters showed a high wafer-to-wafer uniformity as in the first lot. However, analysis of test results from the metal-to-n^+ contact resistor structure revealed an unusually high contact resistance.

The contact resistor is a four-terminal Kelvin type structure with current taps separated from voltage taps, thus eliminating the effects of probe-to-probe-pad contact resistance and the series load resistance of the epi layer and of the metal layer connecting the probe pads to the voltage taps. Further description of this structure can be found elsewhere [8].

Figure 6 shows a plot of the average metal-to-n^+ contact resistance for each tested wafer in the second lot. Each point represents the mean of approximately 82 measured sites. The vertical bars represent the standard deviations which can be seen to be quite large. The average metal-to-n^+ contact resistance per wafer is also much higher than typical values of 10 to 20 Ω found from the first lot. These results suggest a problem with the processing associated with metal-to-n^+ contact resistance. Nothing unusual was seen in the data of the other measured parameters.

IV.B.2 Intrawafer Evaluation

Parameter correlation was examined for all parameters measured for each wafer tested. A listing of sample correlation coefficients for selected parameters within one wafer is seen in table 5. This table shows a high correlation between metal-to-n^+ contact resistance and metal-to-p^+ contact resistance. Similar comparisons for other wafers within the lot were also examined and showed correlation between contact resistor test structures. These correlations indicate that a processing step common to all of these structures may be responsible for the unusually high contact resistance of the metal-to-n^+ contact resistors. Such a process step is the contact window lithography step.

Additional testing was performed on a manual probe station and transistor curve tracer. Contact resistors with a large contact resistance exhibited a current *versus* voltage curve that was nonlinear about the origin and exhibited a diode-like junction characteristic.

Several metal-to-n^+ contact resistors which had a high nonlinear contact resistance were visually inspected using an optical microscope. Based on

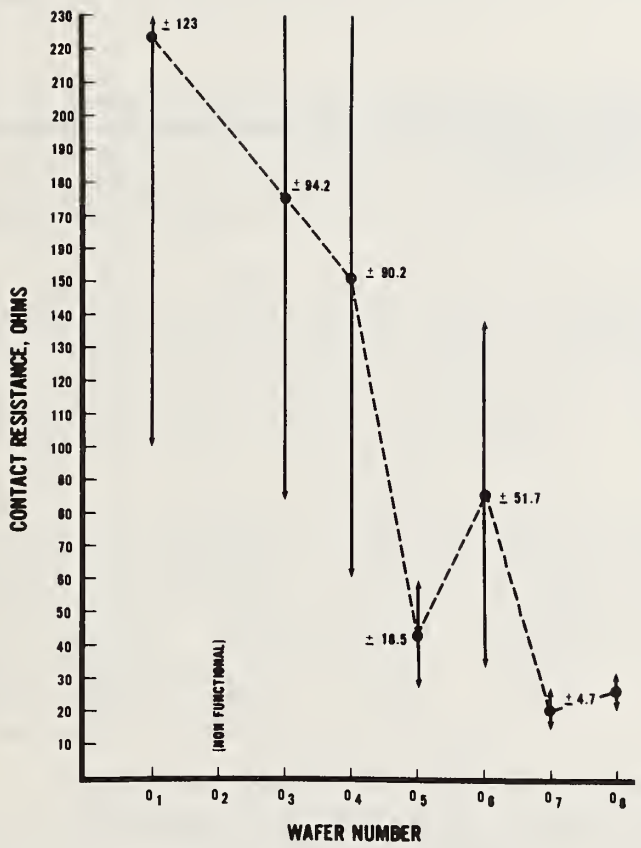

Figure 6. Average metal-to-n^+ contact resistance for each tested wafer in the second lot.

Table 5. Sample Correlation Coefficients Based on a 14-Site Sampling Plan for One Wafer in the Second Lot Tested.

	1	2	3	4	5	6
1	1.00					
2	0.95	1.00				
3	-0.02	0.09	1.00			
4	0.78	0.87	0.19	1.00		
5	0.17	0.27	0.71	0.34	1.00	
6	0.72	0.82	0.02	0.95	0.14	1.00

1 - p^+ doped poly cross-bridge sheet resistance
2 - n^+ doped poly cross-bridge sheet resistance
3 - metal-to-p^+ contact resistance
4 - metal-to-p^+ doped poly contact resistance
5 - metal-to-n^+ contact resistance
6 - metal-to-n^+ doped poly contact resistance

this inspection, it was determined that the contact window lithography step had been performed; however, several devices had either partially etched or nonexistent windows. It was concluded that process irregularities associated with the contact window lithography process resulted in contact windows which were not properly etched and resulted in a very high and widely varying contact resistance measurement.

Average values for all measured parameters are shown in table 6. Wafer maps illustrating selected process parameter variations across a representative wafer in the second lot can be found in Appendix B.

V. Summary

In order to be able to characterize the performance of integrated circuits, it is necessary to determine the baseline electrical parameters of the lot. Test results from two process lots were analyzed using the statistical techniques described in this report.

Test results from the first process lot indicate a reasonable degree of intrawafer and wafer-to-wafer uniformity in critical process parameters, e.g., threshold voltage. Test results from the second process lot uncovered a serious processing problem associated with the contact lithography step used in fabricating the metal-to-n^+ contact resistors. This problem exists in six out of the eight wafers tested in the second lot.

This work suggests that testing one PVW can provide a good statistical estimate of critical process parameters. The PVW also provided information which was used to establish the spatial variation of these parameters over the wafer. Spatial correlations based on a 14-site sampling plan were calculated between each data set pair. If a processing irregularity exists, examining spatial correlation between data sets can be a useful tool in identifying the nature and cause of the problem.

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Table 6. Summary of Test Results for the Second Process Lot Tested (2193-2).

Structure Number	Structure	Parameter	Typical Manufacturer's Value	Average Measured Parameter Value	Average Std Deviation
1	p-channel MOSFET	threshold voltage	-1.5 V	-1.35 V	0.05
		source-to-drain breakdown voltage	-24 V	-24.88 V	0.21
2	n-channel MOSFET	threshold voltage	1.7 V	1.15 V	0.04
		source-to-drain breakdown voltage	20 V	24.64	0.54
9	p^+ cross-bridge sheet resistor	p^+ sheet resistance	110-130 Ω/□	105.08 Ω/□	0.96
		electrical linewidth	-	12.55 μm	0.40
10	n^+ cross-bridge sheet resistor	n^+ sheet resistance	-	76.29 Ω/□	1.21
		electrical linewidth	-	12.11 μm	0.28
11	p^+ doped poly cross-bridge sheet resistor	p^+ doped poly sheet resistance	-	91.91 Ω/□	14.05
		electrical linewidth	-	11.05 μm	0.42
12	n^+ doped poly cross-bridge sheet resistor	n^+ doped poly sheet resistance	-	47.06 Ω/□	3.59
		electrical linewidth	-	11.18 μm	0.39
13	metal cross-bridge sheet resistor	metallization sheet resistance	-	0.03 Ω/□	0.00
		electrical linewidth	-	10.18 μm	0.13
18	metal-to-p^+ contact resistor	metal-to-p^+ contact resistance	-	5.84 Ω	1.71
19	metal-to-n^+ contact resistor	metal-to-n^+ contact resistance	-	103.60 Ω	764.80
20	metal-to-p^+ doped poly contact resistor	metal-to-p^+ doped poly contact resistance	-	0.84 Ω	0.27
21	metal-to-n^+ doped poly contact resistor	metal-to-n^+ doped poly contact resistance	-	0.80 Ω	0.16

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APPENDIX A

Originally published in *Semiconductor Silicon/1981*, H. R. Huff, R. J. Kriegler, and Y. Takeishi, Eds., pp. 906-920 (Electrochemical Society, Pennington, N.J., May 1981).

CHARACTERIZING AND ANALYZING CRITICAL INTEGRATED CIRCUIT PROCESS PARAMETERS*

by

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ABSTRACT

Microelectronic test structures are frequently used to measure the degree of process control in developmental integrated circuit processes. Test results from these structures must be obtained and interpreted in a timely fashion in order to be used for correcting or improving the process. This paper describes techniques for determining and displaying critical process parameters in forms convenient for characterizing the intrawafer variation of these parameters.

INTRODUCTION

With the increasing complexity of integrated circuits, it is becoming more difficult for both the manufacturer and user to fully characterize circuit performance. Functional testing alone is an impractical approach for evaluating complex circuits. As a result, greater utilization is being made of microelectronic test structures which provide clear and unambiguous test results for characterizing the integrated circuit fabrication process (1).

In a developmental integrated circuit process, test structures are used to identify which parameters accurately predict or determine the degree of process control; to establish the value and range of these parameters for a given process lot; and to determine how these parameters vary across an integrated circuit die, across a wafer, from wafer to wafer, and from lot to lot (2-5). Test results must be ob-

*This work was conducted as a part of the NBS program on Semiconductor Measurement Technology. Portions of this work were supported by the Air Force Wright Aeronautical Laboratory and by the Defense Nuclear Agency.

tained and interpreted in a timely fashion in order to be used for correcting or improving the process.

This paper describes analytical techniques for identifing test results from nondefective structures, estimating parameter correlations, and presenting results graphically. These techniques can provide the user with a relatively fast analysis capability for characterizing an integrated circuit process through the determination of the magnitudes of baseline parameters and their variation over the wafer for "properly" fabricated devices. It is assumed that the process being characterized is in sufficient control to produce a high percentage of "properly" fabricated test structures and that defective structures which are encountered are mainly the result of gross defects introduced by handling, by lithography voids, or by similar process irregularities.

A laboratory-based minicomputer-controlled test system is used both to measure selected structures found on a process validation wafer (PVW) and to analyze the resulting data. After identifying and excluding test results from test structures considered to be defective, the mean, median, and standard deviation are calculated for the remaining data set. Further analysis is done to identify possible correlations between critical process parameter data sets. These sets are then displayed as wafer maps to provide graphical illustrations of parameter variation over the wafer.

In the next section the data analysis techniques will be described. An example will then be presented where the techniques are used to analyze a serious process problem.

DATA ANALYSIS TECHNIQUES

The characterization and analysis of a given parameter is performed with a computer program named STAT2. STAT2 is an interactive program, written primarily in FORTRAN, which can analyze a set of data for one parameter. The analysis includes (1) calculation of mean, median, and standard deviation of all data within the set; (2) identification and removal from the data set of test results from structures suspected of containing defects; (3) entry of a 13-point sample of the data set into a data base for use in determining correlations with other data sets; and (4) production of a wafer map in which the parameter variations are displayed as a gray-tone illustration.

To characterize baseline electrical parameters, it is necessary to identify test results from defective structures or defective measurements which did not accurately represent the parameter being measured. The inclusion of data from these structures would result in an incorrect determination and analysis of baseline electrical parameters. Data are initially excluded from the main data set if they

could easily be identified as coming from a defective test structure, e.g., a structure with an open or short between test points. Identification of defective structures in the remaining data base is very difficult without either additional electrical or visual information which requires additional time to obtain or precise fault simulation models which provide an accurate description of the interactions between fault occurrence and measured test results.

After excluding data from the main set for reasons previously described, the remaining measurement data (y_1, y_2, ... y_N) are assumed to be normally distributed with a relatively high occurrence of outliers (up to 20 percent). The outliers are occasionally of a large magnitude and are not necessarily distributed symmetrically about the mean. A datum y_i is rejected as an outlier if:

$$| y_i - \tilde{\mu} | > K \tilde{\sigma}, \tag{1}$$

where $\tilde{\mu}$ and $\tilde{\sigma}$ are the mean and standard deviation calculated from measurements at the included sites (those sites which have not already been identified as outliers), and K is a value to be determined. In order to determine K, the experimenter must specify p, the probability with which he is willing to reject at least one "good" value from N included sites. The value of K satisfies the equation

$$\int_{-\infty}^{K} \frac{e^{-\frac{x^2}{2}}}{\sqrt{2\pi}} dx = \frac{1 + (1 - p)^{1/N}}{2}, \tag{2}$$

involving the standard normal distribution (6). The value of K is numerically computed using an algorithm for the percent point function of the standard normal distribution (7). Knowing K, outliers are identified using eq (1) and excluded. If any points are excluded, new values of $\tilde{\mu}$ and $\tilde{\sigma}$ are calculated based on the new population, N', of included sites. A new value of K is calculated for N' (p is held constant). The procedure is repeated until no new outliers are identified. The number of iterations required depends on the selected value of p. In this work, p = 0.2 was determined to be a reasonable value based on experience using realistic data. Further techniques for robust outlier detection can be found elsewhere (8,9).

The data sets are then analyzed to identify possible spatial correlations between sets. When the paired observations (x_1, y_1), (x_2, y_2), ..., (x_n, y_n) are taken on two quantitites, if a large value of x implies a large value of y, then the quantities are said to be positively correlated. If a large value of x implies a small value of y, then the quantities are said to be negatively correlated. If a large value of x implies nothing about y, then x and y

are said to be uncorrelated. The measure of correlation is the correlation coefficient, ρ, which is estimated by the statistic r:

$$r = \frac{\sum_{i=1}^{n} (x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\left[\sum_{i=1}^{n} (x_i - \bar{x})^2\right]\left[\sum_{i=1}^{n} (y_i - \bar{y})^2\right]}}, \tag{3}$$

where $\bar{x}$ and $\bar{y}$ are the sample means of x and y, respectively, over the n points (8). Note that r must take on values in the range [-1,1].

The statistic, r, is calculated from a 13-point data sample from paired sets to serve as a screen or indicator of possible correlation between parameters measured on the same wafer or on different wafers. The data contained in the 13-point sample are from the selected test sites shown in figure 1. A set of 13 was determined to be a reasonable compromise between keeping sufficient information to characterize the spatial parameter variation and minimizing data storage requirements.

Often it is of interest to know whether the computed value of r is significantly different from zero (or some other number). If the (x,y) pairs are from a bivariate normal population, then a confidence interval can be computed using the Fisher z-transformation [10]. Consider the variance-stabilizing transformation function

$$f(r) = \frac{1}{2}\ln\left(\frac{1 + r}{1 - r}\right) \tag{4}$$

and its inverse

$$g(z) = \frac{e^{2z} - 1}{e^{2z} + 1}. \tag{5}$$

The value $z = f(r)$ is approximately normally distributed with variance $1/(n - 3)$, thus a $100(1 - \alpha)$ percent confidence interval for z can be constructed of the form

$$(z_l, z_u) = \left(z - \frac{k}{\sqrt{(n - 3)}}, z + \frac{k}{\sqrt{(n - 3)}}\right), \tag{6}$$

where subscripts l and u represent the lower and upper bounds of the confidence interval, and k is the $(1 - \alpha/2)$ critical point of the standard normal distribution. For example, for the case of a confidence interval of 99 percent, 99 percent of the points in a normal distribution lie within 2.58 standard deviations of the mean; therefore, k in this example would be 2.58. Using the inverse transforma-

tion g, the $100(1 - \alpha)$ percent confidence interval for ρ can be constructed as

$$(r_l, r_u) = [g(z_l), g(z_u)] \quad . \tag{7}$$

For example, for a calculation based on 13-point pairs which yields r equal to 0.70, the 99-percent confidence interval for ρ would be [0.051, 0.933]. It may be concluded that the correlation is statistically significant because the interval does not include zero.

Data from sets containing possible correlation are displayed as wafer maps. The wafer map provides a graphic illustration of the spatial parameter variations over the wafer. A map, shown in figure 2, uses an eight-level gray scale to represent parameter values. The height and width of the display as well as the maximum and minimum values to be plotted can be selected. The map is made on a line printer, each data point being represented by a 5 by 7 dot symbol. In between data point locations, other symbols are placed with the shade of gray determined by interpolation, thus producing a continuous wafer map. Each actual data point location is represented on the map by an "x," if the parameter value is greater than the maximum plotted value by a "+", and if the parameter value is less than the minimum plotted value by a "-".

By using these techniques, it is possible to quickly examine large quantities of test data. Analysis of selected data sets can lead to the identification of previously unknown process problems or a hypothesis as to the cause of known problems. The analysis can also serve as a guide for the selection of other measurement techniques requiring more time or specialized analysis equipment. In some cases the identity and physical nature of process problems can be determined.

AN EXAMPLE

This technique was used to analyze data obtained on test pattern NBS-16 (11). This pattern, shown in figure 3, was designed to evaluate a developmental CMOS/SOS silicon gate process. It was implemented into a commercial manufacturing facility as a process validation wafer (PVW) (12,13), a wafer consisting only of identical test patterns. Ninety-five NBS-16 test patterns were fabricated on each 3-in. (76.2-mm) diameter silicon-on-sapphire PVW. One PVW accompanied each production run and was subsequently tested in order to determine the value and range of critical process parameters.

The measurement system used to test the PVWs consists of a laboratory-based minicomputer and associated electrical test instruments. The minicomputer is configured with 544 kilobytes of memory, two 10-megabyte disc drives, two floppy disc drives, a nine-track dual

density magnetic tape drive, a system console, several CRT and hard-copy terminals, a line printer, a digital plotter, and a multiuser operating system. The test instruments consist of (1) an automatic wafer prober, (2) a bipolar current supply with 1-μA resolution, (3) two bipolar voltage supplies with 1-mV resolution, (4) an autoranging five-digit digital voltmeter with 1-μV resolution, (5) an autoranging three-digit picoammeter with 1-pA resolution, (6) eight 20-channel scanners, (7) a six-channel autoranging analog-to-digital converter, (8) two digital-to-analog converters, (9) 16 single-pole, single-throw relays, and (10) a digital thermometer with 0.1-K resolution (for reading wafer chuck temperature). All these instruments are digitally programmable. The configuration of the test system is shown in figure 4.

After testing is completed, test results are analyzed using the techniques previously described. Table 1 is a list of the sample correlation coefficients for the 13-point samples from selected parameters on one PVW. From this information, an unexpected correlation is observed between metal-to-n^+ contact resistance and n^+ sheet resistance. These parameters were determined from data taken on a four-terminal contact resistor (14) and a cross-bridge resistor (15), respectively, that were located in adjacent areas of test pattern NBS-16. The magnitude of the sample correlation coefficient, r = 0.76, suggests that the high metal-to-n^+ contact resistance is a function of n^+ sheet resistance or phosphorus concentration.

Sample correlation coefficients between these parameters and other selected parameters were also examined. Because both metal-to-n^+ and metal-to-p^+ contact resistors are adjacent devices, and because the contact window is defined in the same photolithographic process for both structures, variations or problems with contact window photolithography, etching, and subsequent thermal processing are likely to result in similar parameter variations for these structures. Since no apparent correlation was determined, r = 0.01, it was concluded that these processing steps were properly performed. Also, since the contact resistor test structure is a four-terminal kelvin-type structure with current taps separated from voltage taps, the effects of probe-to-probe-pad contact resistance or the series resistance of the epi layer or metal layers connecting the probe pads to the voltage taps do not affect the measurement.

Wafer maps for metal-to-n^+ contact resistance and n^+ sheet resistance were produced and are shown in figure 5. A wafer map of metal-to-p^+ contact resistance is shown in figure 2. Based on the correlation between metal-to-n^+ contact resistance and n^+ sheet resistance and lack of correlation between metal-to-n^+ contact resistance and other parameters, the variation in phosphorus concentration was considered to be the likely cause of metal-to-n^+ contact resistance variation.

The phosphorus concentration of the measured structures was controlled by a two-stage phosphorus implant. The first implant was intended to dope the majority of the epi island region. The second was intended to increase the dopant concentration at the island surface in order to decrease contact resistance in source and drain regions. Both implants were made through a gate oxide which covered the epi island.

It was concluded that due to variations in the gate oxide thickness which were unaccounted for in the process design, the peak of the phosphorus implant varied between the silicon and silicon dioxide depending upon the oxide thickness. This caused significant variations in the amount of phosphorus reaching the silicon surface during the implant and caused the observed variation in metal-to-n^+ contact resistance.

To further support this conclusion, subsequent capacitance measurements on a p-type MOS capacitor were made with a manual test system. The results of these measurements indicated that the gate oxide thickness was greatest in the areas of lowest phosphorus concentration.

Based on the calculated correlation coefficient and associated wafer maps, of test results from a single wafer, specific parameters were identified and further analysis was performed which led to the identification of a serious process problem. The identification and analysis of this processing problem was possible only because both parameter magnitude and test site location were recorded and analyzed in a manner that allowed the rapid spatial correlation of these parameters. Such correlations require enough data to obtain statistically significant results; they cannot be reliably obtained from measurements at only two or three test structures per wafer, as is often done at "drop-in" sites.

SUMMARY

In order to be able to characterize the performance of an integrated circuit process, it is necessary to determine the baseline electrical parameters of the process. The example presented shows that significant variations in these parameters can occur across a wafer.

Statistical correlation techniques and graphical parameter mapping are important tools for analyzing critical parameter variations and identifying process problems in a timely manner from measurements on a single PVW.

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Table 1. Sample Correlation Coefficients for Selected Process Parameters

Wafer: NBS-16, A10

Original Sample Size: 13

	A	B	C	D	E	F	G
A	1						
B	-0.80	1					
C	-0.13	0.11	1				
D	-0.01	-0.12	0.01	1			
E	-0.65	0.57	-0.03	-0.13	1		
F	0.28	-0.30	-0.10	0.76	-0.41	1	
G	-0.13	0.12	-0.68	-0.61	0.16	-0.50	1
H	-0.29	0.01	0.60	-0.07	-0.13	-0.23	-0.27

Parameter

A	p-channel threshold voltage
B	n-channel threshold voltage
C	metal-to-p^+ contact resistance
D	metal-to-n^+ contact resistance
E	p^+ sheet resistance
F	n^+ sheet resistance
G	metallization linewidth
H	polysilicon sheet resistance

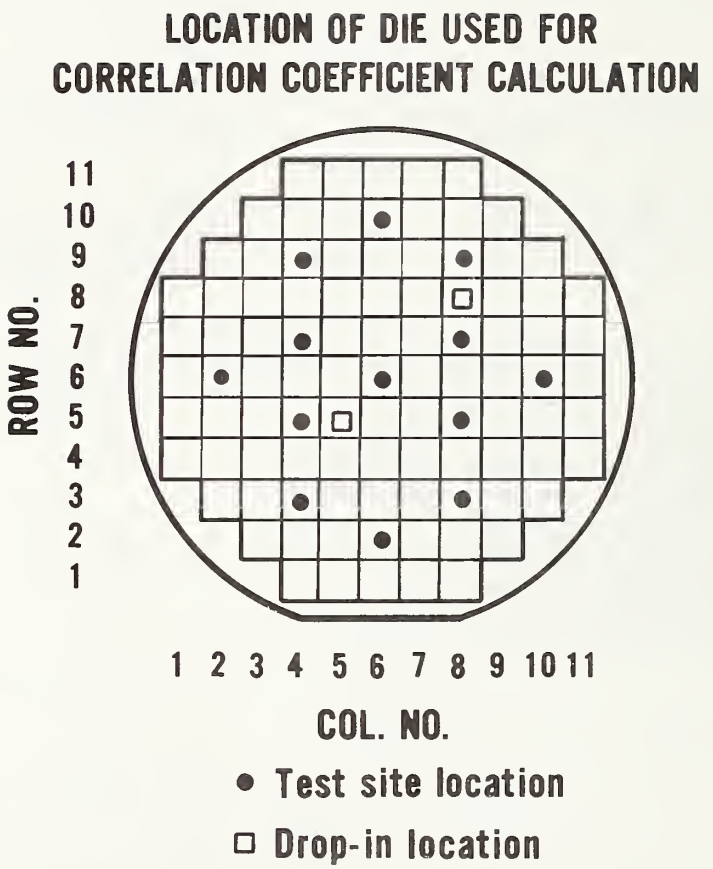


Figure 1. Location of test sites used for determining correlation coefficient for the 13-point sample and location of the "drop-in" sites which contained test patterns other than NBS-16.

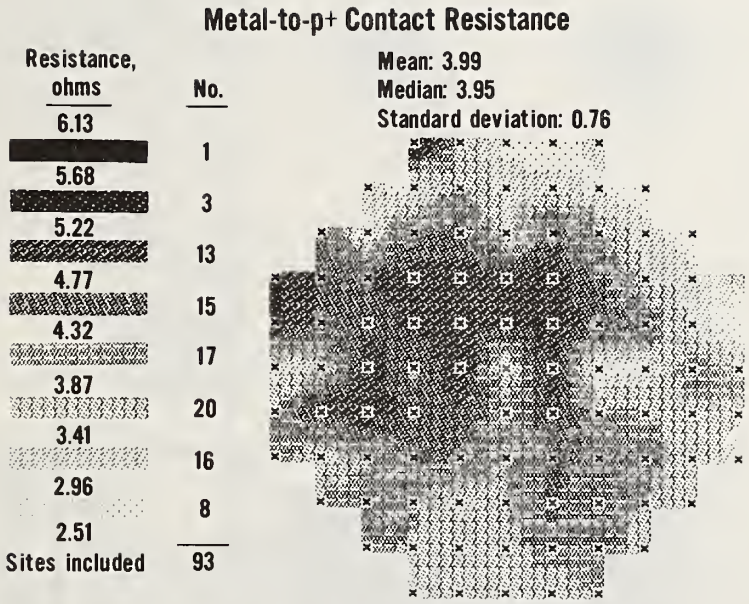


Figure 2. Metal-to-p^+ contact resistance computer-generated (eight-level) gray scale wafer map showing test site location and intrawafer parameter variation.

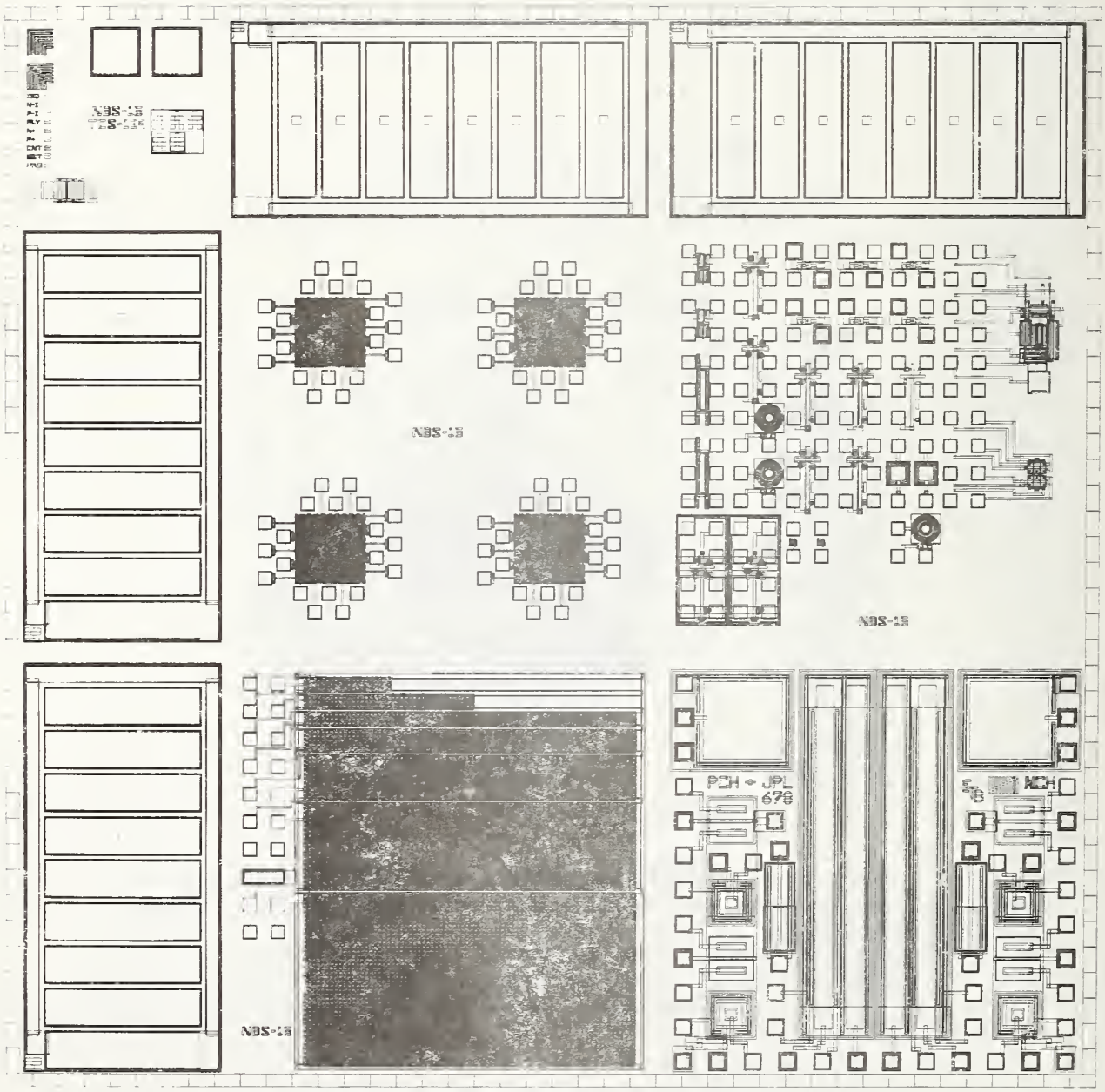


Figure 3. Computer-generated plot of test pattern NBS-16.

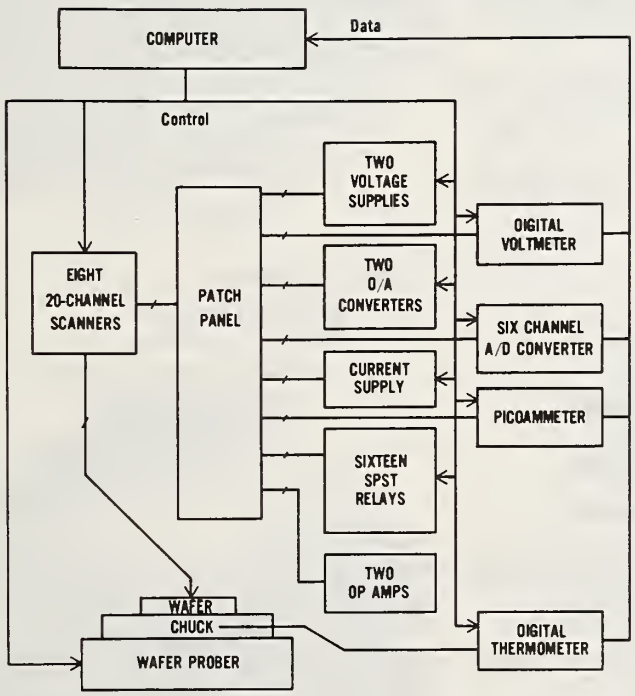


Figure 4. Block diagram of computer-controlled electrical test system.

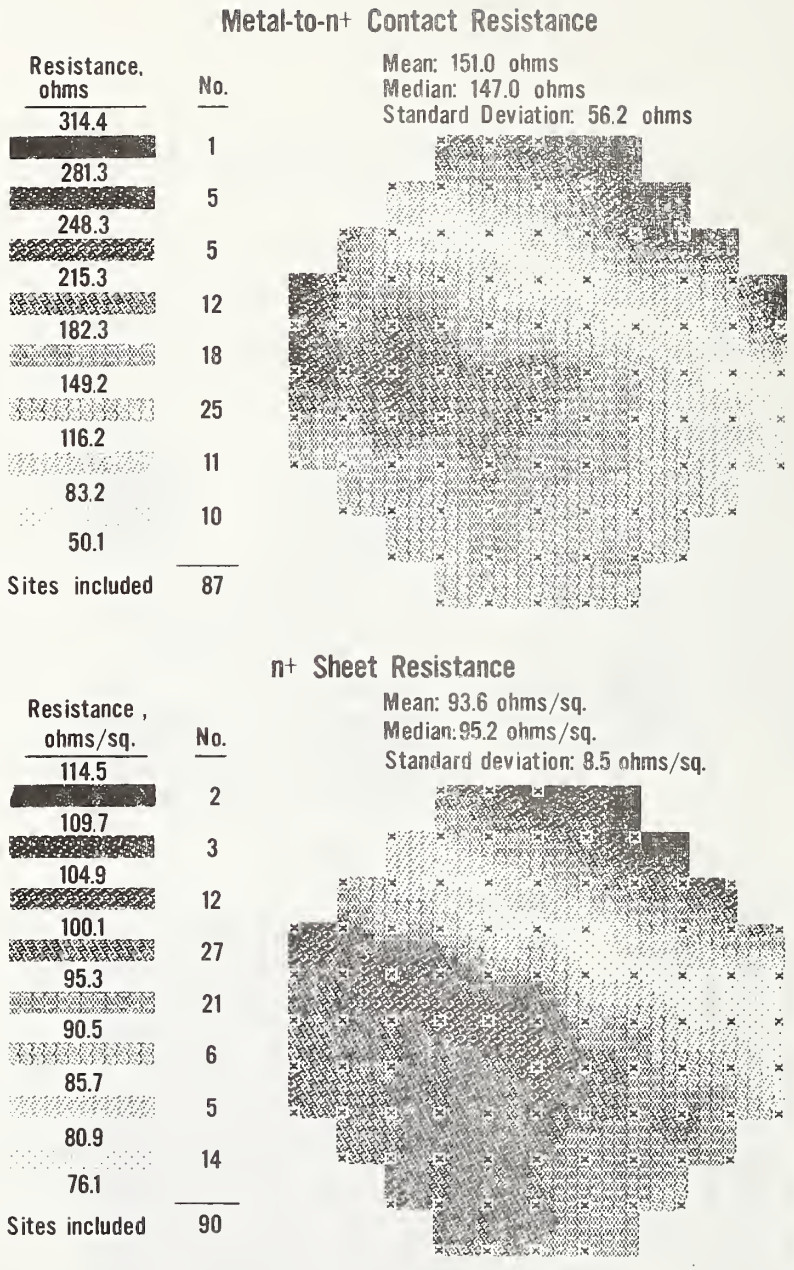
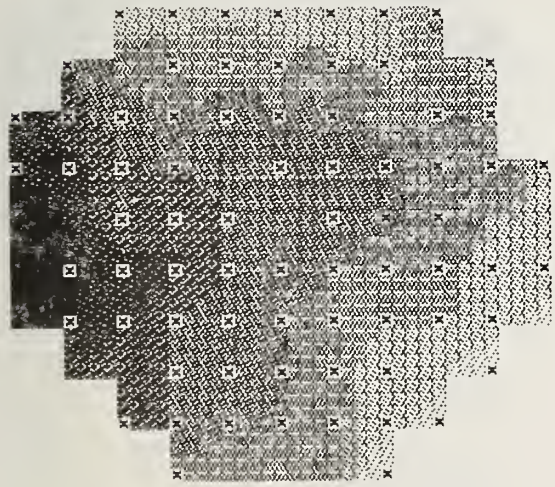


Figure 5. Wafer maps of metal-to-n^+ contact resistance (top) at 87 test sites and n^+ sheet resistance (bottom) at 90 test sites for an NBS-16 process validation wafer containing 95 test sites. In both maps, the scale or gray tone boundaries were selected such that the upper bound of the darkest gray tone was the largest resistance value, and the lower bound of the lightest gray tone was the smallest resistance value. The "x" symbols on the maps represent the locations of nondefective test sites. Test results from these sites were used to calculate mean, median, and standard deviation and also to produce the wafer map.

Appendix B - Wafer Maps of Selected Process Parameter Variations

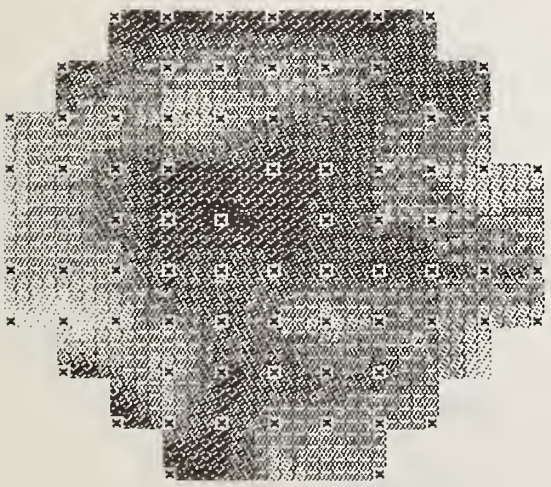
P-CHANNEL MOSFET THRESHOLD VOLTAGE C1



SAMPLE MEAN −1.40 V
SAMPLE STD. DEV. −0.058 V
SAMPLE MEDIAN −1.40 V

PARAMETER VALUE (V)			# SITES
−1.52	TO	−1.57	1
−1.48	TO	−1.52	6
−1.44	TO	−1.48	7
−1.40	TO	−1.44	24
−1.35	TO	−1.40	18
−1.31	TO	−1.35	14
−1.27	TO	−1.31	2
−1.22	TO	−1.27	1
SITES INCLUDED			73

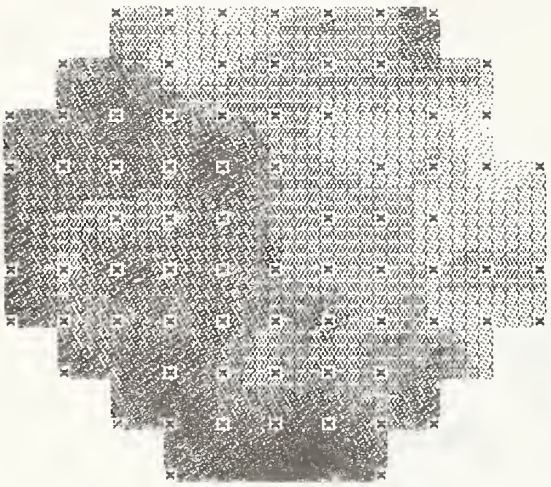
P-CHANNEL MOSFET BREAKDOWN VOLTAGE C1



SAMPLE MEAN −22.85 V
SAMPLE STD. DEV. −0.18 V
SAMPLE MEDIAN −22.84 V

PARAMETER VALUE (V)			# SITES
−23.24	TO	−23.37	0
−23.11	TO	−23.24	5
−22.98	TO	−23.11	12
−22.84	TO	−22.98	20
−22.71	TO	−22.84	24
−22.58	TO	−22.71	11
−22.45	TO	−22.58	2
−22.32	TO	−22.45	1
SITES INCLUDED			75

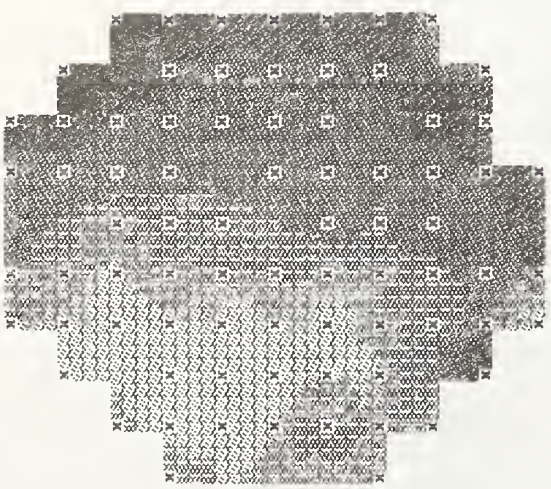
P-CHANNEL MOSFET LEAKAGE CURRENT C1



SAMPLE MEAN	0.98 nA
SAMPLE STD. DEV.	0.12 nA
SAMPLE MEDIAN	0.97 nA

PARAMETER VALUE (nA)			# SITES
1.26	TO	1.35	3
1.17	TO	1.26	4
1.07	TO	1.17	8
0.98	TO	1.07	19
0.89	TO	0.98	25
0.80	TO	0.89	14
0.70	TO	0.80	2
0.61	TO	0.70	1
SITES INCLUDED			76

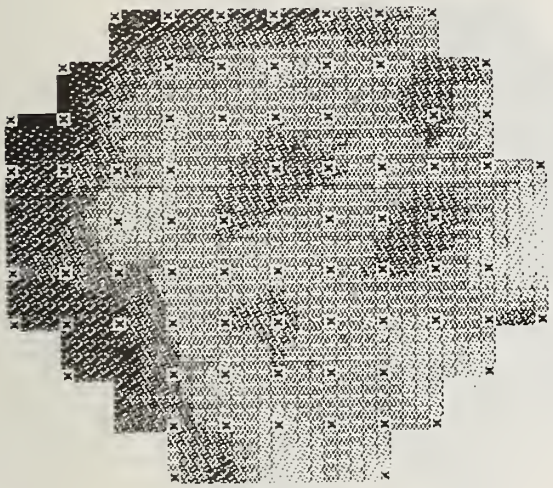
N-CHANNEL MOSFET THRESHOLD VOLTAGE C1



SAMPLE MEAN	1.57 V
SAMPLE STD. DEV.	0.12 V
SAMPLE MEDIAN	1.57 V

PARAMETER VALUE (V)			# SITES
1.83	TO	1.93	4
1.74	TO	1.83	3
1.65	TO	1.74	9
1.56	TO	1.65	24
1.46	TO	1.56	21
1.37	TO	1.46	14
1.28	TO	1.37	2
1.192	TO	1.28	0
SITES INCLUDED			77

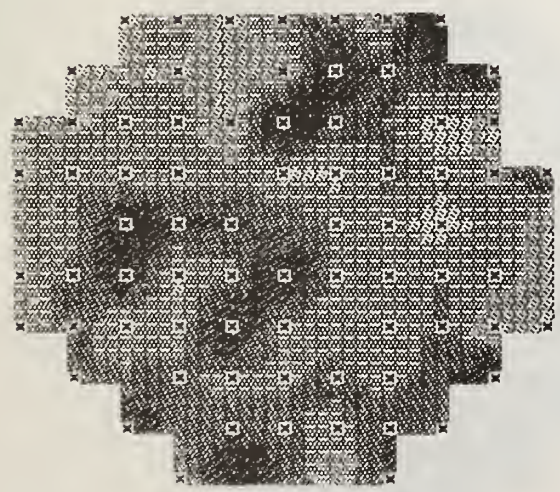
N-CHANNEL MOSFET BREAKDOWN VOLTAGE C1



SAMPLE MEAN	22.61 V
SAMPLE STD. DEV.	0.31 V
SAMPLE MEDIAN	22.56 V

PARAMETER VALUE (V)			# SITES
23.31	TO	23.54	2
23.07	TO	23.31	6
22.84	TO	23.07	5
22.61	TO	22.84	20
22.37	TO	22.61	27
22.14	TO	22.37	11
21.91	TO	22.14	3
21.67	TO	21.91	1
SITES INCLUDED			75

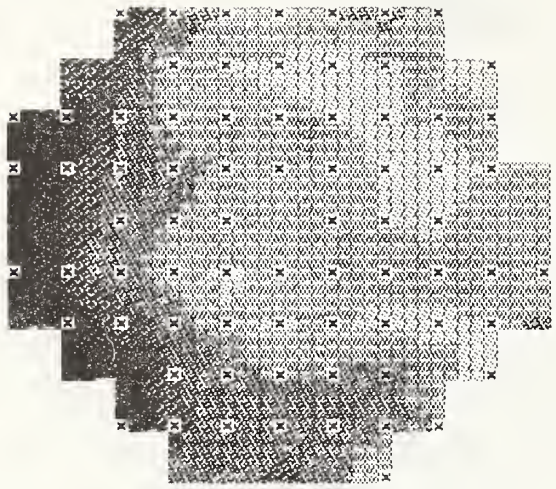
N-CHANNEL MOSFET LEAKAGE CURRENT C1



SAMPLE MEAN	1.76 nA
SAMPLE STD. DEV.	0.63 nA
SAMPLE MEDIAN	1.55 nA

PARAMETER VALUE (nA)			# SITES
3.17	TO	3.64	5
2.70	TO	3.17	3
2.23	TO	2.70	7
1.76	TO	2.23	14
1.29	TO	1.76	26
0.82	TO	1.29	17
0.35	TO	0.82	1
0.118	TO	0.35	0
SITES INCLUDED			73

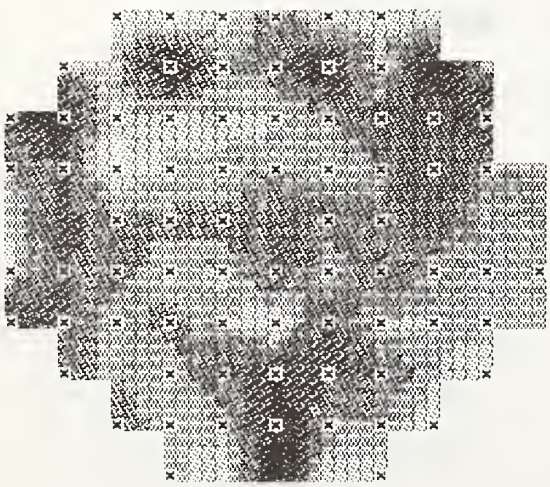
N+ CROSS-BRIDGE SHEET RESISTANCE C1



SAMPLE MEAN	66.09 Ω/□
SAMPLE STD. DEV.	1.45 Ω/□
SAMPLE MEDIAN	65.65 Ω/□

PARAMETER VALUE (Ω/□)			# SITES
69.29	TO	70.37	5
68.22	TO	69.29	3
67.14	TO	68.22	5
66.07	TO	67.14	13
65.00	TO	66.07	31
63.92	TO	65.00	16
62.85	TO	63.92	0
61.78		62.85	0
SITES INCLUDED			73

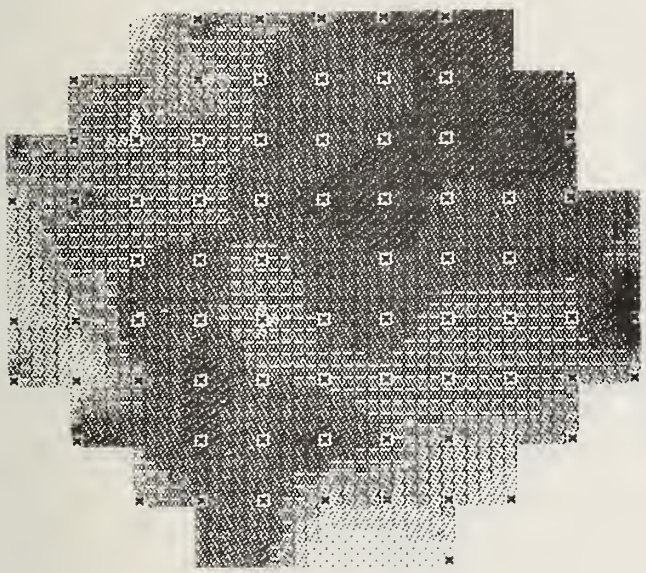
METAL TO N+ CONTACT RESISTANCE C1



SAMPLE MEAN	10.42 Ω
SAMPLE STD. DEV.	1.86 Ω
SAMPLE MEDIAN	10.18 Ω

PARAMETER VALUE (Ω)			# SITES
14.56	TO	15.95	2
13.18	TO	14.56	6
11.80	TO	13.18	9
10.42	TO	11.80	14
9.04	TO	10.42	24
7.65	TO	9.04	17
6.27	TO	7.65	2
4.89	TO	6.27	0
SITES INCLUDED			74

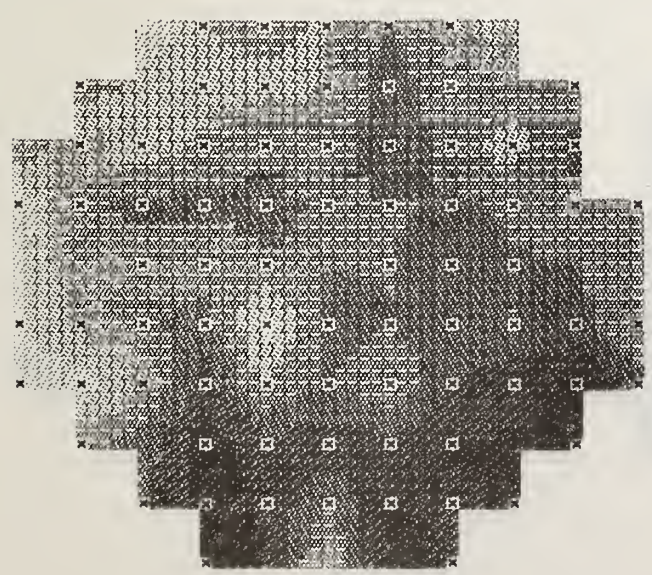
P-CHANNEL MOSFET THRESHOLD VOLTAGE D3



SAMPLE MEAN −1.46 V
SAMPLE STD. DEV. −0.04 V
SAMPLE MEDIAN −1.46 V

PARAMETER VALUE (V)			# SITES
−1.55	TO	−1.58	1
−1.52	TO	−1.55	2
−1.49	TO	−1.52	11
−1.46	TO	−1.49	24
−1.43	TO	−1.46	19
−1.40	TO	−1.43	10
−1.37	TO	−1.40	4
−1.34	TO	−1.37	2
SITES INCLUDED			73

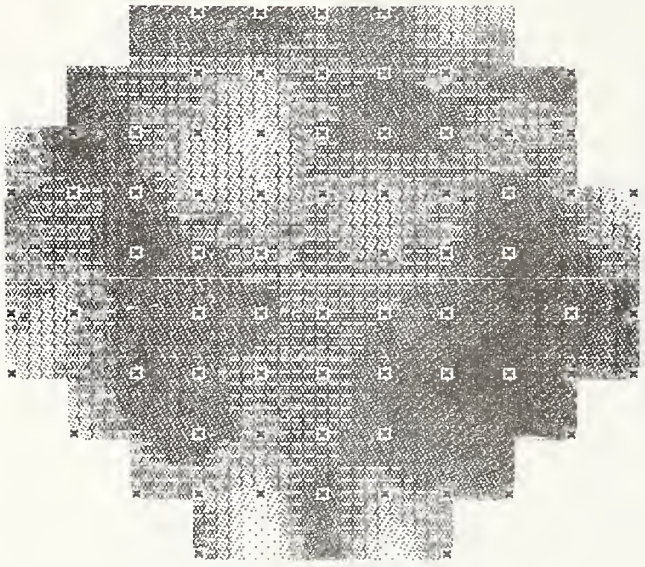
P-CHANNEL MOSFET BREAKDOWN VOLTAGE D3



SAMPLE MEAN −24.43 V
SAMPLE STD. DEV. −0.22 V
SAMPLE MEDIAN −24.41 V

PARAMETER VALUE (V)			# SITES
−24.93	TO	−25.10	1
−24.77	TO	−24.93	7
−24.60	TO	−24.77	8
−24.43	TO	−24.60	20
−24.26	TO	−24.43	25
−24.09	TO	−24.26	9
−23.92	TO	−24.09	6
−23.75	TO	−23.92	0
SITES INCLUDED			76

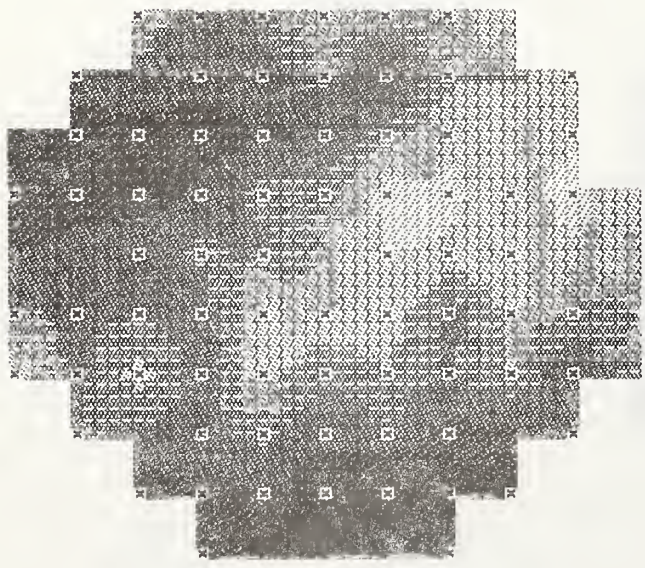
P-CHANNEL MOSFET LEAKAGE CURRENT D3



SAMPLE MEAN	0.55 nA
SAMPLE STD. DEV.	0.03 nA
SAMPLE MEDIAN	0.55 nA

PARAMETER VALUE (nA)			# SITES
0.63	TO	0.66	0
0.60	TO	0.63	6
0.58	TO	0.60	8
0.55	TO	0.58	20
0.52	TO	0.55	22
0.50	TO	0.52	11
0.47	TO	0.50	2
0.44	TO	0.47	1
SITES INCLUDED			70

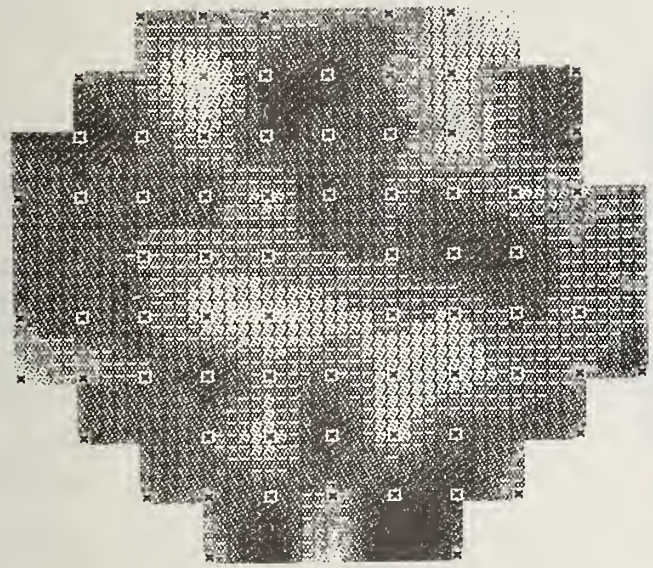
N-CHANNEL MOSFET THRESHOLD VOLTAGE D3



SAMPLE MEAN	1.20 V
SAMPLE STD. DEV.	0.03 V
SAMPLE MEDIAN	1.21 V

PARAMETER VALUE (V)			# SITES
1.28	TO	1.31	1
1.26	TO	1.28	3
1.23	TO	1.26	15
1.20	TO	1.23	20
1.18	TO	1.20	14
1.15	TO	1.18	17
1.13	TO	1.15	3
1.10	TO	1.13	0
SITES INCLUDED			73

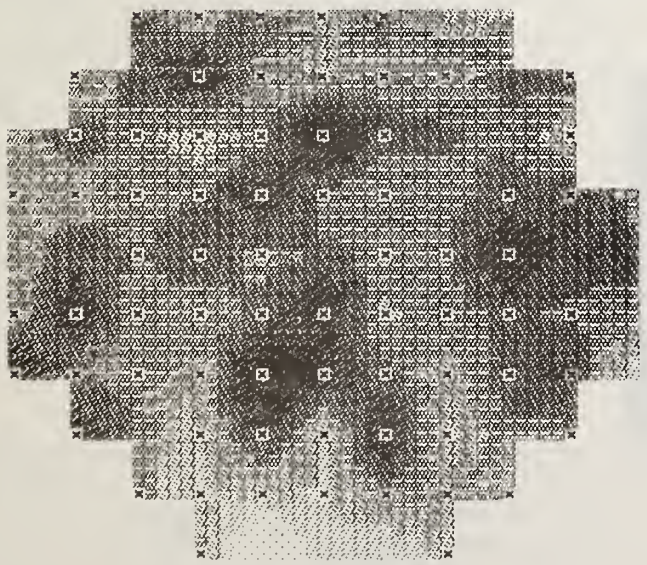
N-CHANNEL MOSFET BREAKDOWN VOLTAGE D3



PARAMETER VALUE (V)			# SITES
25.21	TO	25.50	0
24.91	TO	25.21	4
24.62	TO	24.91	15
24.32	TO	24.62	21
24.03	TO	24.32	15
23.73	TO	24.03	12
23.44	TO	23.73	4
23.15	TO	23.44	1
SITES INCLUDED			72

SAMPLE MEAN	24.32 V
SAMPLE STD. DEV.	0.39 V
SAMPLE MEDIAN	24.37 V

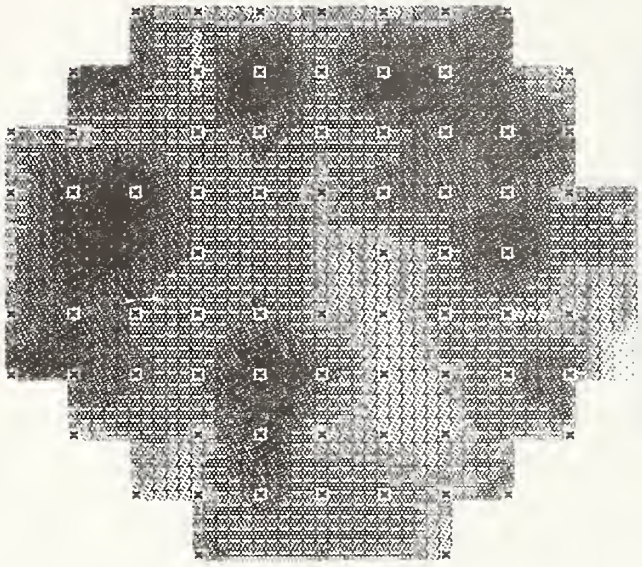
N-CHANNEL MOSFET LEAKAGE CURRENT D3



PARAMETER VALUE (nA)			# SITES
4.85	TO	5.76	2
3.94	TO	4.85	7
3.03	TO	3.94	6
2.12	TO	3.03	11
1.21	TO	2.12	29
0.30	TO	1.21	13
0.0	TO	0.30	2
SITES INCLUDED			70

SAMPLE MEAN	2.12 nA
SAMPLE STD. DEV.	1.23 nA
SAMPLE MEDIAN	1.86 nA

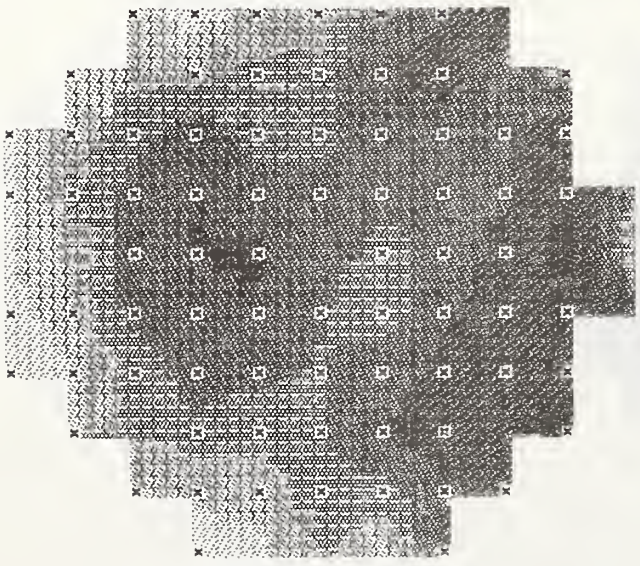
METAL TO N+ CONNTACT RESISTANCE D3



SAMPLE MEAN	176.68 Ω
SAMPLE STD. DEV.	94.35 Ω
SAMPLE MEDIAN	139.72 Ω

PARAMETER VALUE (Ω)			# SITES
386.32	TO	456.20	2
316.44	TO	386.32	5
246.56	TO	316.44	9
176.68	TO	246.56	15
106.79	TO	176.68	24
36.91	TO	106.79	17
32.96	TO	36.91	1
2.84	TO	32.96	0
SITES INCLUDED			73

N+ CROSS-BRIDGE SHEET RESISTANCE D3



SAMPLE MEAN	81.60 Ω/□
SAMPLE STD. DEV.	1.15 Ω/□
SAMPLE MEDIAN	81.75 Ω/□

PARAMETER VALUE (Ω/□)			# SITES
84.18	TO	85.04	0
83.32	TO	84.18	2
82.46	TO	83.32	14
81.60	TO	82.46	25
80.74	TO	81.60	17
79.88	TO	80.74	9
79.02	TO	79.88	6
78.16	TO	79.02	2
SITES INCLUDED			75

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5. AUTHOR(S)

John S. Suehle, Loren W. Linholm, and Gina M. Marshall

6. PERFORMING ORGANIZATION (If joint or other than NBS, see instructions)

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10. SUPPLEMENTARY NOTES

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

The objective of this work was to determine baseline electrical parameters that could be used to evaluate a fabrication process. Two lots of wafers containing NBS-16 test chips were fabricated at a commercial vendor in a radiation-hard, CMOS/SOS process. These wafers were then returned to NBS for testing and evaluation. Testing was performed using an automated computer-controlled integrated circuit test system. Test results were evaluated using analysis techniques which provided a statistical estimate of selected parameters and identified spatial correlations between data sets. Further analysis was then performed in order to identify process irregularities. A complete description of the test results and analysis procedure can be found in the appendices.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

Integrated circuits; microelectronics; process control; process validation wafer; silicon on sapphire; test chip; test pattern; test structure; yield.

13. AVAILABILITY

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