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Semiconductor Measurement Technology:

Silicon-on-Insulator: A Categorized Bibliography Including Abstracts

A. Bagdadi and E. J. Walters, Editors

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Semiconductor Measurement Technology:

Silicon-on-Insulator: A Categorized Bibliography Including Abstracts

A. Baghdadi and E. J. Walters, Editors

Semiconductor Electronics Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
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1. INTRODUCTION

This bibliography was compiled mainly from a literature search of three data bases, INSPEC, Engineering Index, and Chemical Abstracts. We attempted to include all the papers in the databases which dealt with silicon-on-insulator materials or devices. However, we do not claim that all relevant papers on silicon-on-insulator technology have been included in this bibliography. Moreover, since the literature search itself was conducted in February 1987, only a few papers published late in 1986 or later have been included. The results of the literature search were edited to remove redundancies and nonrelevant papers, and to correct any obvious errors. We decided to include the abstracts, as well as the titles of the papers, in the bibliography. The resulting manuscript was then re-written using the mathematical typesetting system "TEX"*† in order to produce a clear and easily readable bibliography.

Written permission has been received from the three databases to download and publish selected records. The source database is noted in the right margin at the end of the abstract (CA – Chemical Abstracts, EI – Engineering Index, IN – INSPEC). Those abstracts not so identified were added by the authors.

The basic approach used in organizing this bibliography was to place papers which covered the same (or similar) subjects together, so that the reader could readily compare one paper to another. The papers were originally stored in the databases in reverse chronological order. For this bibliography, the papers were classified according to the technique covered (e.g., silicon-on-sapphire or SIMOX), and then subclassified according to the type of work (e.g., characterization, materials, or devices) and treatment (general, experimental, or theoretical). For many techniques, the resulting sub-subsections or subsections only contained a few papers. In that case, the files were recombined so that most subsections now contain a fair number of papers.

This bibliography can either be used to obtain a quick evaluation of the "state of the art" in a particular field, to compare the progress achieved by fundamentally different approaches to producing SOI substrates, or to find articles on a specific subject or written by leading scientists in this field.

The first section of the bibliography itself (section 3 in this report) covers silicon-on-insulator generally. These papers either deal with silicon-on-insulator generically, or cover several different SOI techniques, so that they could not be placed in any one specific section. Two other sections cover more than one technique: section 4 covers "device transfer" and "bonding and etchback" under the title "Novel Techniques". Section 8 covers heteroepitaxial growth on crystalline substrates other than sapphire. Each of the remaining sections covers one particular technique for producing SOI materials. Section 10, on recrystallization techniques, was so large that it was further subdivided according to the heat source used for the recrystallization.

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* The TEX logo is a trademark of The American Mathematical Society.

† Certain commercial materials are identified in this paper. Such identification does not imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the materials identified are necessary the best available for the purpose.

The following proceedings of symposia or conferences contain many excellent papers on silicon-on-insulator technology:

Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium
26-28 Feb. 1984, Albuquerque, NM
North-Holland, Amsterdam

Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
14-17 Nov. 1983, Boston, MA, Mater. Res. Soc.
North-Holland, New York, Volume 23

Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar
on 'Solid Phase Epitaxy and Interface Kinetics,' 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984
Symposium 1985, 26-30 Nov. 1984, Boston, MA
Mater. Res. Soc., Pittsburgh, PA, Volume 35

Chiang, A.; Geis, M.W.; Pfeiffer, L. (Editors)
Semiconductor on Insulator and Thin Film Transistor Technology,
3-6 Dec. 1985, Boston, MA, Volume 53

Thompson, M.O.; Picraux, S.T.; Williams, J.S. (Editors)
Beam-Solid Interactions and Transient Processes
1-4 Dec. 1986, Boston, MA
Mater. Res. Soc., Pittsburgh, PA, Volume 74

Disclaimer

Although the records have been edited, the authors are not responsible for any errors which may have been introduced by the abstracting services.

Acknowledgment

The editors are pleased to thank Dr. Peter Roitman of NBS and Dr. John Schott of RADC for reviewing this bibliography.

2. DISCUSSION

The purpose of this section is to provide an overall view of each of the sections of the bibliography, and to recommend certain leading articles, where this was appropriate. The numbers in parentheses refer to the reference numbers in this bibliography. These articles are pointed out in the main body of the bibliography by a "bullet" in the left margin. This section concludes with lists of papers which use particular materials characterization techniques.

Section 3 contains review or "perspective" articles which can be most useful to obtain a quick education on the rationale for SOI and the progress of SOI research. We recommend the articles by Partridge (6), Schott (9), Murphy (19), Tsaur (47), Colinge (50), Maby (57), Baerg (63), and Yamaguchi (82). We were not able to obtain the article by Gibbon (43), but it appears to be a very interesting evaluation of radiation hardness of VLSI technology.

Section 4 covers two novel techniques which have not yet been reported widely. We recommend the papers by Frye (83) and Lasky (88) on the Bonding and Etch-Back technique.

Section 5 covers epitaxial overgrowth. This technique appears to be limited to very small areas, as discussed in the article by Jastrzebski (96).

Section 6 covers the fabrication of SOI structures by using porous oxidized silicon. This still developing technique is covered by Baumgart (125), Benjamin (126), Imai (129,130), and Takai (134).

Section 7 covers silicon layer growth by molecular beam epitaxy (see the article by Bean, 135).

Section 8 covers the growth of silicon layers on non-silicon, non-sapphire crystalline substrates (see the paper by Hokari, 145).

Section 9 covers SOI structures in which a layer of devices are fabricated in a top polysilicon layer, which was grown over an insulating substrate. Since the devices are built into a polycrystalline silicon layer, they are suitable only for very limited applications.

Section 10 covers the production of SOI structures by recrystallizing a polycrystalline silicon layer grown on top of an insulator. Since this was a very popular subject, it was further subdivided into four sections: one generic, and one each covering recrystallization using electron beams, laser beams and zone heaters, respectively. The latter technique is often called the zone-melting or strip-heater technique. The laser- and electron-beam-based techniques, although they may be useful tools for investigating the recrystallization process, are not as likely to be adaptable for large-scale semiconductor fabrication as the zone heater techniques. In the generic subsection, we recommend the papers by Pinizzotto (166), Sedgwick (170), McGinn (178), and Vu (182). In the electron beam subsection, we recommend the papers by Ohmura (199), Hayafuji (209), and Knapp (228). In the laser subsection, we recommend the papers by Biegelsen (230), Celler (232), Kamins (239), Egami (249), Lee (253), Lu (255), Nakashima (260), and Kim (289). In the zone heater subsection, we recommend the papers by Chen (352,353), Cline (354), Higuchi (366), Kubota (390), Bensahel (393), Biegelsen (394), Chen (396), Dutartre (398), Fan (399), and Tsaur (420,421). We should not conclude from the size of the research effort devoted

to the development of SOI structures by recrystallization techniques that it is the most advanced technique at this time. It does show considerable promise in the long run, and appears to be a very popular research topic at this time (especially for university reseachers).

Section 11 covers the production of SOI structures by SIMOX. This appears to be the most advanced technique, both in terms of devices and circuits built on SIMOX substrates (see Chen, 505, Colinge, 509, Davis, 512, and Kajiyama, 519) and in terms of the industrial interest in the technique. We also recommend papers by Celler (428,429), Davis (442), Kamins (447), Barklie (460), Chang (462), Cristoloveaunu(465), Fathy (468), Foster (469), Izumi (478), Makino (488), Mogro-Campero (491), and Nakashima (492).

Section 12 covers SOI structures produced by the implantation of nitrogen to form silicon nitride. We recommend the papers by Chang (529), Hemment (531), Hobbs (532) and Petruzzello (539).

Section 13 covers silicon-on-sapphire (SOS). This is the most mature SOI technology, but it is still being developed. We recommend the papers by Cristoloveaunu (547), Davis (549), Gupta (551,552) and Vasudev (560).

Materials Characterization Techniques

Auger Electron Spectroscopy: 136, 154, 248, 351, 364, 449, 459, 474, 476, 478, 497, 499, 530, 539

Electron Paramagnetic/Spin Resonance: 460, 488, 527, 532

Ellipsometry: 22, 250

Infrared Absorption: 154, 438, 478, 499, 528

Optical Microscopy: 115, 116, 140, 149, 154, 211, 222, 265, 319, 354, 499

Raman Spectroscopy: 14, 19, 20, 255, 259, 260, 261, 265

Reflectometry: 15, 461, 548

Rutherford Back Scattering: 137, 140, 438, 446, 452, 471, 474, 552

Scanning Electron Microscopy: 16, 222

Secondary Ion Mass Spectroscopy: 317, 438, 444, 446, 471, 472, 474, 475, 483, 484, 533, 535, 537, 538, 552

Transmission Electrom Microscopy: 99, 104, 112, 113, 125, 129, 137, 157, 194, 209, 252, 256, 258, 319, 341, 388, 407, 433, 438, 462, 468, 471, 474, 475, 483, 497, 499, 535, 537, 538

X-Ray Photospectroscopy: 438, 474, 476

X-Ray Diffraction Techniques: 124, 149, 150, 250, 263, 322, 408

3. SILICON-ON-INSULATOR

Generic

1). Three-Dimensional IC Trends.
Akasaka, Y.
Mitsubishi Electric Corp, Itami, Japan
Proceedings of the IEEE, Vol. 74, No. 12, 1703-1714, Dec. 1986 *EI*

2). Techniques for Producing SOI (Silicon on Insulator) Structures – General View.
Furukawa, S.
Tokyo Inst. of Technol., Tokyo, Japan
Oyo Buturi (Japan), Vol.53, No.1, 27, Jan. 1984

Silicon-on-insulators (SOI) for use as semiconductor-device substrates must satisfy the following requirements: (1) flatness, (2) high carrier mobility, (3) low effective dielectric constant, (4) low surface level density, (5) high thermal conductivity, (6) high insulation resistance, (7) high thermal stability, and (8) selective etching ability. The method for fabricating SOI must permit a low-temperature process, high productivity, low-cost fabrication, and process compatibility. *IN*

3). SOI by CVD: An Overview of Material Aspects and Implications of Device Properties.
Jastrzebski, L.; Kokkas, A.G.
RCA Labs., Princeton, NJ.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
3-6, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Two CVD techniques for producing monocrystalline SOI films, silicon-on-sapphire (SOS) and epitaxial lateral overgrowth (ELO), are described and the nature of the crystallographic defects in the films is discussed. The geometrical structure of SOI devices, device properties, dynamic characteristics, capacitance, and radiation hardness are then examined with emphasis on evaluating the potential of SOI technologies in future applications. *IN*

4). Recent Advances in Silicon-on-Insulator Technologies.
Lam, H.W.
Texas Instrum., Dallas, TX.
J. Vac. Sci. & Technol. A (USA), Vol.4, No.3, Pt.1, 1023-4, May-June 1986
Proceedings of the 32nd National Symposium of the American Vacuum Society
19-22 Nov. 1985, Houston, TX.

The author discusses the new SOI technologies that are being developed recently. The interest in SOI structures comes about because of the growing interest in using complementary metal-oxide-semiconductor (CMOS) circuits for VLSI. The new SOI technologies include implanted buried oxide layers, full isolation by oxidation of anodized silicon, epitaxial overgrowth, and beam recrystallization. *IN*

5). SOI Technology.
Nishimura, T.; Akasaka, Y.
LS1 Res. Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan
Oyo Butsuri, Vol. 54, No. 12, 1274-83, 1985 *CA*

• 6). Silicon-on-Insulator Technology.
Partridge, S.L.
GEC Res. Ltd., Hirst Res. Centre, Wembley, England

IEE Proc. I (GB), Vol.133, No.3, 66, June 1986

The last few years have seen considerable progress in the development of techniques for producing silicon-on-insulator (SOI) substrates suitable for fabrication of high performance devices/circuits. Among the most promising of the new ideas are those based on buried dielectric formation by ion implantation (oxygen or nitrogen), recrystallisation of deposited polycrystalline silicon-on-insulator (using lasers, electron beams, hot wires, strip heaters or incoherent light), and oxidation of porous silicon. A number of other techniques also show potential. The concept of SOI is not new, however. Attempts to grow single-crystal semiconductor films on insulating substrates data back almost 40 years with the first successes in the growth of silicon layers in the early 1960s. During that period epitaxial silicon-on-sapphire (SOS) emerged as a viable approach to SOI, since when it has become a well-established technology for MOS with a unique role to play in some important areas of application. The new substrate types promise to extend the range of applicability still further. Indeed, some workers predict a revolution, following which, for MOS technology at least, single-crystal silicon substrates will play a minor role in comparison to SOI. This paper outlines these different approaches to SOI and reviews their advantages for a number of important application areas, placing particular emphasis on MOS technology. *IN*

7). Silicon-on-Insulator Technology.
Partridge, S.L.
GEC Res. Ltd., Hirst Res. Centre, Wembley, England
IEE Proc. E (GB), Vol.133, No.3, 106-16, May 1986

The last few years have seen considerable progress in the development of techniques for producing silicon-on-insulator (SOI) substrates suitable for fabrication of high performance devices/circuits. The concept of SOI is not new, however. Attempts to grow single-crystal semiconductor films on insulating substrates date back almost 40 years. During that period epitaxial silicon-on-sapphire (SOS) emerged as a viable approach to SOI since when it has become a well-established technology for MOS with a unique role to play in some important areas of application. The new substrate types promise to extend the range of applicability still further. Indeed, some workers predict a revolution, following which, for MOS technology at least, single-crystal silicon substrates will play a minor role in comparison to SOI. This paper outlines these different approaches to SOI and reviews their advantages for a number of important application areas, placing particular emphasis on MOS technology. Applications such as VLSI, memory, structured, random and high speed logic, analogue circuit design, and defence electronics are considered. Recent developments in the preparation of SOI substrates have led to the successful realisation of a range of novel 'stacked' structures exploiting, for example, two (or more) independent layers of devices, common gates, or common device channels. Progress in and the potential of this exciting new field of three-dimensional integration is reviewed also. *IN*

8). Silicon-on-Insulator and Device Applications.
Partridge, S.L.
GEC Journal of Research, Vol. 4, No. 3, 165-173, 1986

The advantages of silicon-on-insulator (SOI) integrated circuits for a number of important application areas are reviewed, placing particular emphasis on MOS technology. The suitability of the main types of SOI for applications such as VLSI, high performance products and defence electronics are considered, and comparisons with single-crystal silicon substrates are made. Recent developments in three-dimensional silicon integrated circuits are also reviewed. *EI*

• 9). Silicon-on-Insulator Technologies, Are We Converging on a Technique of Choice?
Schott, J. T.; Shedd, W. M.
Rome Air Dev. Cent., Solid State Sci. Dir., Hanscom AFB, MA
IEEE Trans. Nucl. Sci., Vol. NS-33, No. 6, Pt. 1, 1366-71, 1986

This paper attempts to present an unbiased review and evaluation of the dozen or more techniques under development to fabricate SOI structures. *CA*

10). The Application of the Silicon-on-Insulator Structure to VLSI.
Tasch, A.F.; Hon Wai Lam
Central Res. Lab., Texas Instruments Inc., Dallas, TX.
11th European Solid State Device Research Conference (ESSDERC 81) and the 6th Symposium on Solid State Device Technology (SSSDT 81), 25, 1981
14-17 Sept. 1981, Toulouse, France
European Phys. Soc., Petit-Lancy, Switzerland

Various SOI approaches are described and the advantages and disadvantages, progress, and prospects are discussed for each approach. The authors conclude with an examination of the major issues which will determine the successful realization of the new approaches to silicon-on-insulator devices. *IN*

11). Assessment of Silicon-on-Insulator Technologies for VLSI.
Tsaur, B.Y.
Lincoln Lab., MIT, Lexington, MA
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 365-73, 1986 *CA*

12). Silicon-on-Insulator Electronic-Device Technology. Present State and Perspectives.
Wagner, S.
Tech. Hochsch. Karl-Marx-Stadt, Ger. Dem. Rep.
Nachrichtentech., Elektron., Vol. 36, No. 7, 270-2, 1986 *CA*

13). Silicon-on-Insulator Structures in Integrated Microelectronics.
Velchev, N.; Petkov, M.; Raicheva, Z.; Goranova, E.; Beshkov, G.
Bulg. EP, Elektroprom-st. Priborostr., Vol. 20, No. 11, 29-33, 1985 *CA*

14). Properties of Thin Films After Focused Beam Processing.
Campbell, I.H.; Fauchet, P.M.; Adar, F.
Dep. Electr. Eng., Princeton Univ., Princeton, NJ
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 311-16, 1986

A Raman microprobe was used to detect the changes in crystallinity, stress, and homogeneity of thin Si-on-insulator films irradiated by a single laser pulse. Maximum, isotropic, planar tensile stress increased from 5×10^9 to $12 \times 10^9 dyn/cm^2$ in the processed area and stress of $8 \times 10^9 dyn/cm^2$ was observed $20\mu m$ beyond the damage region. Crystallite sizes of 50 to > 300Å were observed inside the processed area. Results obtained with different pulsed laser frequencies are compared and significant differences in the processing effects are observed. *CA*

15). The Characterization of CVD Single-Crystal Silicon on Insulators: Heteroepitaxy and Epitaxial Lateral Overgrowth.
Cullen, G.W.; Duffy, M.T.; Jastrzebski, L.; Lagowski, J.
RCA Labs., Princeton, NJ.
J. Cryst. Growth (Netherlands), Vol.65, No.1-3, 415-38, Dec. 1983
Seventh International Conference on Crystal Growth (ICCG-7), 12-16, Sept. 1983, Stuttgart, Germany

In the development of the heteroepitaxial silicon technology, progress had been impeded because of the labor and time involved in the evaluation of the crystalline quality of the deposits by transmission electron microscopy and device performance. Therefore, an important part of the authors' program has been directed toward the development of rapid and non-destructive methods for the characterization of the silicon crystallinity. It is essential that the results of such methods relate to device performance. The authors update earlier reports on this effort. Emphasis has been placed on the use of UV reflectometry for probing the near-surface silicon quality, photovoltage spectroscopy for probing the 'bulk' of the film, interference photovoltage spectroscopy for probing the near-substrate portion of the silicon, and infrared multiple reflectometry to assess the crystalline quality of the substrate surface. The silicon-on-insulator effort has recently been extended on the growth of dielectrically isolated silicon by CVD epitaxial lateral overgrowth. The evaluation of these deposits by transmission electron microscopy is described. *IN*

16). Scanning Electron Microscopy Studies of Silicon on Insulator Devices (LCD Display).
Drake, D.J.; Fernquist, R.; Hawkins, W.G.
Webster Res. Center, Xerox Corp., NY.
Scanning Electron Microsc. (USA), Pt.4, 1579-84, 1984

Defect analysis of thin-film transistor driver matrices for actively addressed liquid crystal displays is performed in an SEM using a form of voltage contrast. Since these matrices are fabricated on transparent insulators, specimen charging takes place on the entire structure. By selectively grounding appropriate circuit elements, a number of circuit defects are revealed, including source and gate line open and short circuits. Additionally, a suitable range of electron-beam voltages and currents was found that allows nondestructive evaluation of these arrays. *IN*

17). Recombination Mechanisms in Si and Si Thin Films Determined by Picosecond Reflectivity Measurements Near Brewster's Angle.
Fauchet, P.M.; Nighan, W.L., Jr.
Dept. of Electr. Eng., Princeton Univ., NJ.
Appl. Phys. Lett. (USA), Vol.48, No.11, 721-3, 17 March 1986

A sensitive pump and probe method for measuring the transient carrier density in semiconductors is proposed and demonstrated in silicon. It relies on the magnified reflectivity changes when the

picosecond probe laser is incident close to Brewster's angle. The authors have measured the Auger recombination coefficient $\gamma = 2 \times 10^{-31} cm^6/s^{-1}$ and, in microcrystalline silicon films on insulator, the effective lifetime due to grain boundaries $\tau \simeq 100$ ps. Additionally, at much higher pump energies, upon melting, the reflectivity jumps by nearly one order of magnitude. *IN*

18). Thickness Determination for Silicon-on-Insulator Structures.
Kamins, T.I.; Colinge, J.-P.
Electronics Letters, Vol. 22, No. 23, 1236-1237, Nov. 1986

Optical interference at the interfaces of a silicon-on-insulator structure has been used for rapid, nondestructive determination of the silicon and oxide layer thicknesses. The technique is useful for determining the layer thicknesses for wafers in which devices and circuits are subsequently fabricated, especially for very thin silicon films in which the device characteristics depend strongly on the silicon thickness. *EI*

• 19). Optical Microanalysis of Small Semiconductor Structures.
Murphy, D.V.; Brueck, S.R.J.
Lincoln Lab., MIT, Lexington, MA.
Osgood, R.M.; Brueck, S.R.J.; Schlossberg, H.R. (Editors)
Laser Diagnostics and Photochemical Processing for Semiconductor Devices, Proceedings of a Symposium, 81-94, 1983, Nov. 1982, Boston, MA.
North-Holland, New York.

Raman spectroscopy is a powerful tool for evaluating semiconductor crystal characteristics with a diffraction-limited spatial resolution of approximately 0.5 μm, comparable to device structure dimensions. Examples are presented of the use of Raman scattering to measure stress variations across Si-on-insulator and Si-on-sapphire stripes with dimensions down to 2 μm and, to probe the spatial variation in the effectivness of annealing, of a Si layer deposited over metal device structures. Detailed measurements of the variation in the Raman spectra of thin crystalline Si films, with thicknesses down to 3.0 nm, are discussed. Measurements made on roughened Si surfaces are presented which show that surface morphology on a submicron spatial scale results in enhanced Raman intensities. *IN*

20). Minimization of Residual Stress in SOI Films.
Ogura, A.; Egami, K.; Kimura, M.
Fundam. Res. Lab., NEC Corp., Kawasaki, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 17th(Final Program Late News Abstr.), 10-11, 1985

Residual stress in Si films on structures with 1- to 3-μm thick SiO_2, phosphosilicate glass and AlN films as interlying insulators, and Si and sapphire as substrates were characterized by measuring Raman spectra. The stress in the Si film on a 3-μm thick AlN/Si substrate is lower than that on SiO_2, and microcracks were found in the Si film only on the SiO_2 layer. When the insulator thickness was 1 μm, no significant difference was observed. With Si substrates, the increase of AlN film thickness brings about no stress accumulation. With sapphire substrates, the residual stress is compressive and decreases with increasing thermal expansion coefficients of the insulating materials. A stress-free Si film can be obtained by using an underlayer (substrate and insulator) with a thermal expansion slightly larger than that of Si. *CA*

21). An Electrical Method to Measure SOI Film Thicknesses.
Whitfield, J.; Thomas, S.
Motorola Inc., Phoenix, AZ.
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.6, 347-9, June 1986

A method to nondestructively measure the silicon film thickness and the buried insulating film thickness is presented. The method is based on a silicon-on-insulator (SOI) MOSFET, operating in

the two regions where the threshold voltage depends on each of the film thicknesses. The method uses a feedback amplifier to hold the drain biases nearly constant while the body and/or the buried gate voltages are varied. Calculated threshold voltages from the top-gate voltages are used to calculate the film thicknesses. The method is illustrated on devices built in oxygen-implanted substrates. The electrical measurements compare well with SEM image measurements. *IN*

22). Study of Si SOI Optical Properties by Using Ellipsometric Four-Phase Model.
Zhu Wei-wen; Zhu Wen-yu; Wang Wei-yuan
Shanghai Inst. of Metall., Acad. Sinica, China
Acta Phys. Sin. (China), Vol.35, No.6, 797-802, June 1986

The ellipsometric parameters of LPCVD poly-Si on insulating SiO_2 (Si SOI) before or after annealing with laser- or rf-inducing graphite-strip heater were measured by spectroscopic ellipsometry over the wavelength interval 3000 to 5000 Å. The four-phase model of ellipsometric spectra was presented by matrix multiplication and the Monte Carlo simulation was used to calculate both ϵ_1 and ϵ_2 of Si SOI. The lattice perfection of Si SOI after annealing is discussed. *IN*

23). SOI Technologies for Integrated Circuits.
Akasaka, Y.; Cullen, G.W.; Gibbons, J.F.; Hill, C.; Vail, P.J.
Mitsubishi Electr. Corp., Japan;
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium, 3-6, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

There are a number of viable approaches to silicon-on-insulator (SOI) technologies, and a panel session has assembled a number of leaders in the SOI community for their views of 'SOI technologies for integrated circuits'. Their viewpoints were presented for general discussion in the session which was attended by about 150 people. Although SOI technologies are useful for many applications, most of the panelists agreed that the most appropriate near-term applications are for high-speed, high-density integrated circuits. Various SOI technologies, including silicon-on-sapphire (SOS), are currently in the running, but the majority of the panelists felt that for SOI technologies to be widely adopted, SOI must be available as a proven manufactured product within two for Si. *IN*

24). Silicon on an Insulating Material.
Auvert, G.; Bensahel, D.; Bomchil, G.; Colinge, J.-P.
Echo Rech. (France), No.114, 71-82, 1983

Technologies involving silicon and insulators have received new impetus and attention as a result of studies on porous silicon and the possibilities offered by 'transient' annealing using continuous or pulsed laser beams, lamps, or tapes of heated graphite. *IN*

25). The Various Methods of Silicon-on-Insulator Are Becoming Practical.
Goodenough, F.
Electron. Des. (USA), Vol.32, No.1, 74-80, 12 Jan. 1984

Silicon-on-insulator technology, which could succeed silicon-on-sapphire, portends low-cost dielectric isolation, high speeds, and even three-dimensional circuits. Four extremely different silicon-on-insulator techniques are appearing as alternatives to silicon-on-sapphire: beam recrystallization, implanted buried oxide, full isolation by porous oxidized silicon, and epitaxial overgrowth. *IN*

26). Comparison of Different SOI Technologies: Assets and Liabilities.
Jastrzebski, L.
RCA Labs., Princeton, NJ.
RCA Rev. (USA), Vol. 44, No. 2, 250-69, June 1983

Different methods used to obtain silicon-over-insulator (SOI) films are compared, based on the information available in the literature. All techniques are briefly outlined and their assets and liabilities are compared with special emphasis on application in different present and future processing technologies. It seems that at the present stage of development, the 'leader' cannot be clearly identified, and different technologies could favor different SOI approaches. *IN*

27). Silicon on Insulators: Different Approaches – A Review.
Jastrzebski, L.
RCA Labs., Princeton, NJ.
J. Cryst. Growth (Netherlands), Vol.70, No.1-2, 253-70, Dec. 1984
Sixth International Conference on Vapor Growth and Epitaxy and Sixth American Conference on Crystal Growth, 15-20 July 1984, Atlantic City, NJ.

Different methods used to obtain silicon-over-insulator (SOI) films are compared, based on the information available in the literature. All techniques are briefly outlined and their assets and liabilities are compared with special emphasis on application in different present and future processing

technologies. The CVD approach is discussed more than the others since it has been a focal point of work on SOI by the author. It seems that at the present stage of development the 'leader' cannot be clearly identified, and different technologies could favor different SOI approaches. *IN*

28). SOI Formation by Burying Oxide Layer.
Kajiyama, K.
Atsugi Electrical Communication Lab., NTT Public Corp., Tokyo, Japan
Oyo Buturi (Japan), Vol. 53, No. 1, 29, Jan. 1984

Three silicon-on-insulator techniques, SIMOX (separation by implanted oxygen), FIPOS (full isolation by porous oxidized silicon) and CEPIC (complementary epitaxial passivated integrated circuits), are described which bury an oxide film in a single-crystal silicon. The methods use the original single-crystal silicon as the element fabrication region, and an oxide film as the insulator. Large-scale ICS can be fabricated. *IN*

29). Comparison of SOI Technologies.
Lam, H.W.
Texas Instr. Inc., Dallas, TX.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
579-85, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Silicon-on-insulator (SOI) technologies are becoming more important as CMOS becomes the preferred technology for VLSI. The progress of the three most actively researched SOI technologies, beam-recrystallized SOI, implanted buried oxide, and full isolation by porous oxidized silicon are summarized. *IN*

30). Recent Advances in Silicon-on-Insulator Technologies.
Lam, H.W.
Texas Instruments Inc., Dallas, TX
Proceedings of the 1984 Custom Integrated Circuits Conference, 36-9
21-23 May 1984, Rochester, NY.
IEEE, New York.

The progress of the three most actively researched SOI technologies is reviewed. The technologies are beam-precrystallized SOI, implanted buried oxide, and full isolation by porous oxidized Si (FIPOS). Emphasis is given to those developments which lend themselves to CMOS VLSI applications. *IN*

31). Silicon on Insulating Substrates – Recent Advances.
Lam, H.W.
Texas Instruments Inc., Dallas, TX.
International Electron Devices Meeting 1983, Technical Digest, 348-51, 1983
5-7 Dec. 1983, Washington, DC.
IEEE, New York.

Silicon-on-insulator (SOI) technologies are becoming more important as CMOS becomes the preferred technology for VLSI. The progress of the three most actively researched SOI technologies, namely beam-recrystallized SOI, implanted buried oxide, and full isolation by porous oxidized silicon are summarized. *IN*

32). Analysis of the Si-on-Insulator Structure by Modeling of the Interface Atomic Arrangement.
Saito, T.; Yamakoshi, Y.; Ohdomari, I.

Sch. of Sci. and Eng., Waseda Univ., Tokyo, Japan
Baglin, J.E.E.; Campbell, D.R.; Chu, W.K. (Editors)
Thin Films and Interfaces II. Proceedings of the Symposium, 531-6, 1984
14-18 Nov. 1983, Boston, MA
North-Holland, New York.

A structure of interface between crystalline Si (c-Si) and underlying SiO_2 film formed by the Si-on-insulator technique has been analyzed by modeling of interface atomic arrangement. A ball-and-spoke model of a stoichiometrically abrupt c-Si/SiO_2 interface has been constructed by connecting a (100) c-Si lattice and a continuous random network model of amorphous SiO_2. A Keating-type potential has been used for the interatomic interactions. The bond-bending distortion energy of both Si and O atoms increases at the interface, while the bond-stretching energy is negligibly small. The amount of interface energy due to bond distortion is 0.20 J/m^2. *IN*

33). Research & Development of Three-Dimensional Integrated Circuits.
Tsurushima, T.
Electrotech. Lab., Ibaraki, Japan
J. Vac. Soc. Jpn. (Japan), Vol. 28, No. 1, 8-18, 1985

In implementing three-dimensional integrated-circuit chip fabrication, it is indispensable to well establish multilayered SOI structure fabrication technology and a process technique for fabricating basic circuit elements in the SOI structure. In these respects, this paper reviews the present technology and future development in three-dimensional circuit element fabrication, and outlines (1) semiconductor crystal layer formation on an insulator substrate, (2) stacked C-MOS element structure, (3) element integration in each layer, and (4) interlayer isolation processes. *IN*

34). A Thermal Model for Silicon-on-Insulator Multilayer Structure in Silicon Recrystallization Using Tungsten Lamp.
Chong Min Kyung
Dept. of Electr. Eng., Kaist, Seoul, Korea
J. Korea Inst. Electron. Eng., Vol.21, No.5, 90-9, Sept. 1984

A one-dimensional distribution of the temperature and the heat source in the SOI (silicon-on-insulator) multilayer structure illuminated by tungsten lamps from both sides was obtained by solving the heat equation in steady state on a finite difference grid using the successive over-relaxation method. The heat source distribution was obtained by considering such features as spectral components of the light source, multiple reflection at the internal interfaces, temperature and frequency dependence on the light absorption coefficient, etc. The front and back surface temperatures, which are boundary conditions for the heat equation, were derived from a requirement that they satisfy the radiation conditions. The radiation flux as well as the conduction flux was considered in modelling the thermal behaviour of the internal interfaces. Since the temperature and the heat source profiles are strongly dependent upon each other, the calculation of each profile was iterated using the updated profile of the other until they are consistent with each other. The experimental temperature at the front surface of the wafer as measured by pyrometer was about 1200 K, while the simulated temperature was 1120 K. *IN*

35). VLSI Materials: A Comparison Between Buried Oxide SOI and SOS.
Hamdi, A.H.; McDaniel, F.D.; Pinizzotto, R.F.; Matteson, S.; Lam, H.W.; Malhi, S.D.S.
Dept. of Phys., North Texas State Univ., Denton, TX.
IEEE Trans. Nucl. Sci. (USA), Vol. NS-30, No.2, 1722-5, April 1983

High-dose oxygen ion implantation in Si has been used to form a 0.48-μm thick buried oxide layer. The total dose was $2.1 \times 10^{18} O^{+}/cm^{2}$ implanted at 150 keV/atom. Epitaxial growth was employed to deposit a 0.38-μm thick layer on top of the implanted wafers. High-quality single-crystal Si on the entire 76-mm diameter wafer was achieved. The microstructure of the buried oxide SOI is compared to SOS material. *IN*

36). Isolation Process Technology in LSIS, II.
Muramoto, S.; Nakajima, S.
Atsugi Electrical Communication Lab., NTT Public Corp., Atsugi-Shi, Japan
J. Inst. Electron. and Commun. Eng. Jpn. (Japan), Vol. 66, No. 7, 729-35
July 1983

An isolation width of 1.5 μm to submicron is required for the implementation of megabit dynamic RAMs. Microisolation considerably affects MOS device properties. For latchup-free devices to be fabricated, element regions should be isolated perfectly by an insulator. The authors describe mask configuration for selective oxidation, isolation techniques using groove burying, silicon-on-insulator techniques using a buried oxidation film, and silicon-on-insulator techniques using annealing. *IN*

37). Improved Oxide Breakdown by Contoured Epitaxial Island Formation.
Policastro, S.G.; Sullivan, T.E.
RCA, Princeton, NJ.
RCA Tech. Not. (USA), No.1378, 1-2, 2 July 1986

The oxide breakdown voltage in semiconductor devices is extremely important in the design of large-scale integrated circuits. This is particularly true in the case of silicon-on-insulator (SOI) technology because of the large number of epitaxial island edges which must be crossed by layer of silicon oxide. Where the island edge is relatively sharp, the silicon oxide layer tends to be thinner or will experience cracks, both of which will adversely lower the breakdown voltage in that local

area. The present method rounds the relatively sharp edges of the epitaxial islands, thereby greatly reducing the incidence of failure of the oxide along these edges. *IN*

38). Beam Annealing Technology and Its Application to Device Fabrication.
Tokuyama, T.; Tamura, M.; Miyao, M.
Central Res. Lab., Hitachi Ltd., Kokubunji-Shi, Japan
J. Inst. Electron. and Commun. Eng. Jpn. (Japan), Vol.64, No.12, 1261-8
Dec. 1981

Recent data on dopant activation, thermal stabilisation, and dopant distribution are reviewed. In the rapidly developing field of silicon crystal growth on insulator (SOI), the two seedless growth methods, polysilicon island and graphoepitaxy, and the seeding method called bridging epitaxy are also treated. Problems of beam annealing are lack of heat annealing at the depth which the beam reaches, laser-induced defects distant to the contact surfaces and laser-beam-induced cracks in the SiO_2 of the SiO_2/Si surrounded windows and thus surface and contact characteristics are affected. Many device applications are examined in MOSFET, GaAs, and SOI devices. *IN*

39). A Three Dimensional Semiconductor Device.
Akasaka, Y.
LSI Dev. Lab., Mitsubishi Electr. Corp., Tokyo, Japan
Mitsubishi Electr. Adv. (Japan), Vol. 33, 18-19 Dec. 1985

The three-dimensional semiconductor device is a new silicon-on-insulator (SOI) circuit that stacks conventional VLSI elements to achieve high integration and high-speed operation. It promises to integrate a variety of powerful functions including parallel signal-processing, sensing, signal conversion, and storage. The three-dimensional device has triple-stacked active layers, and the basic operation of the memory, optical-sensor, and signal-processing circuits is covered. *IN*

40). Crosstalk Between Circuit Signals in 3-D Structure.
Akasaka, Y.; Nishimura, T.; Nakata, H.
Mitsubishi Electric Corp, Itami, Japan
IEEE Transactions on Electron Devices, Vol. ED-32, No. 11, Nov. 1985, 43rd Annual Device Res. Conf., Boulder, CO, June 17-19, 1985, 2550 *EI*

41). Lateral COMFET Made in Thin Silicon-on-Insulator Film.
Colinge, J.-P.; Chiang, S.-Y.
Hewlett-Packard Lab, Palo Alto, CA,
IEEE Electron Device Letters, Vol. EDL-7, No. 12, 697-699, Dec. 1986

Lateral conductivity-modulated FETs (COMFETs) have been fabricated using a silicon-on-insulator (SOI) CMOS process. High-speed low-voltage CMOS and medium-voltage COMFETs have thus been produced on the same chips. The COMFETs have an 80-V blocking capability both in the forward and in the reverse modes. Turn-off time of a few microseconds are obtained, which is comparable to values obtained in bulk COMFETs. Due to the thinness of the silicon film in which the devices are made, the linear current density is limited to approximately 10 μA/μm. *CA*

42). 3D Electronic Devices.
Furukawa, S.
Graduate School, Tokyo Inst. of Technol., Tokyo, Japan.
J. Inst. Telev. Eng. Jpn. (Japan), Vol. 36, No. 12, 1060-7, Dec. 1982

3D electronic devices have advantages in high integration/high density of circuits, speed and high performance. There are, however, some major problems in their development with the heat barrier, fabrication problems with SOI structure formation and interlayer connection through holes and test methods. 22 applications for 3D devices are listed. Current research in this area is reviewed including crystal layering techniques, SOI technolgy, SOS, SIMOX, FIPOS and especially 3D MOSFET with special emphasis on Japanese research. *IN*

• 43). A Comparison of the Radiation Hardness of Various VLSI Technologies for Defense Applications.
Gibbon, C.F.
Sandia Nat. Labs., Albuquerque, NM.
Impact of Very High Performance Integrated Circuits on Radar, Guidance and Avionics Systems. Avionics Panel 49th Symposium, 8/1-8, Oct. 1985
20-25 May 1985, Lisbon, Portugal
AGARD, Neuilly-sur-Seine, France

The author evaluates the radiation hardness of various potential very-large-scale integration (VLSI) IC technologies is evaluated. IC scaling produces several countervailing trends. Reducing vertical dimensions tends to increase total dose hardness, while reducing lateral feature sizes may increase

susceptibility to transient radiation effects. It is concluded that during the next decade at least, silicon complementary MOS (CMOS), perhaps on an insulating substrate (SOI), will be the technology of choice for VLSI in defense systems. *IN*

44). Floating Substrate Effects on the Switching Characteristics of SOI MOSFET.
Kato, K.; Taniguchi, K.
Toshiba Corp., Kawasaki, Japan
IEEE Transactions on Electron Devices, Vol. ED-32, No. 11, Nov.1985, 43rd Annual Device Res. Conf., Boulder, CO, June 17-19, 1985, 2549 *EI*

45). 3-D SOI/CMOS.
Nakano, M.
Fujitsu Ltd., Kawasaki, Japan
International Electron Devices Meeting, Technical Digest, 792-5, 1984
9-12 Dec. 1984, San Francisco, CA.
IEEE, New York.

Some of the properties of 3-D SOI/CMOS, such as fabricating processes, characteristics, and practical structures, are summarized. Attention is given to SOI techniques for 3-D devices, 3-D integration, and CMOS, and examples of 3-D SOI/CMOS. Three-dimensional SOI/CMOS is seen as an attractive candidate for future VLSIs. Laser recrystallization is thought to be the most suitable method of fabricating SOIs for 3-D devices because of the short heating time. It is pointed out that realization of future 3-D ICs will require improvements in many technologies. *IN*

46). A 3-D Integration Strategy in VLSI.
Satwinder, D.S.M.; Malhi, D.S.
Semiconductor Process & Design Center, Texas Instrum. Inc., Dallas, TX.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 147-8, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

With improved device design, it has been possible to build short-channel, p-channel, and n-channel MOSFETs with arbitrary threshold voltage and leakage current of the order of 1 pA/γm channel width. The channel mobility is about $10cm^2/V{\cdot}s$. The on-to-off current ratio is about seven orders of magnitude. Despite the low mobility, these devices are useful for a variety of high-density memory applications. The author has used p-channel devices built in small grain LPCVD polysilicon to develop a 2-μm stacked CMOS process. 64K static RAMs have been fabricated with this process. The cell size is 307 μm^2 and chip size is 55000 sq. mils. The access time is 120 ns. *IN*

• 47). SOI Technologies: Device Applications and Future Prospects.
Tsaur, B.-Y.
Lincoln Lab., MIT, Lexington, MA.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium, 641-52, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

Silicon-on-insulator (SOI) technologies have four major applications: very-large-scale integrated circuits (ICs), high-voltage ICs, large-area ICs, and vertical ICs. The author reviews the recent progress made in these areas and discusses the prospects of various SOI technologies for achieving commercialization. *IN*

48). SPICE Simulation of SOI MOSFET Integrated Circuits.
Veeraraghavan, S.; Fossum, J.G.; Eisenstadt, W.R.

Univ of Florida, Gainesville, FL
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. CAD-5, No. 4, 653-658, Oct. 1986

A five-terminal charge-based model for the thin-film silicon-on-insulator (SOI) MOSFET is implemented in SPICE2, thereby enabling, for the first time, proper simulation and computer-aided design of SOI MOS integrated circuits in which the unique floating-body and back-gate-bias effects can be significant. The implementation is achieved, without having to rewrite the circuit simulator, by developing a general method for incorporating new charge-based device models into SPICE2 that utilizes user-defined controlled sources. The utility and computing efficiency of the SOI MOSFET model implementation are demonstrated by simulating several representative SOI MOS circuits. *EI*

49). Three Dimensional Circuits: The Vertical Alternative to VLSI.
Veiga, E.R.
Mundo Electron. (Spain), No.157, 95-100, Dec. 1985

Limitations posed by micron and submicron VLSI circuits are basically on-chip electrical fields and power dissipation increased to intolerable levels, unless the supply voltage is reduced. Shrinking geometries maintaining the 5 V supply level would give rise to increased breakdown phenomena, whilst reducing operating voltages to allow smaller geometries reduces the switching speed of interfacing low-voltage CMOS circuits. On the other hand, the possibility of achieving a fast transition from the existing 5 V standard is blocked by economic factors – no market exists for sub-5 V chips-and technology. After reviewing typical phenomena that affect the reliability of VLSI devices and their solutions, SOI technologies are as a prelude to 3D devices, including a survey of experimental three-dimensional structures. *IN*

• 50). Half-Micrometre-Base Lateral Bipolar Transistors Made in Thin Silicon-on-Insulator Films.
Colinge, J.-P.
Hewlett-Packard Labs., Palo Alto, CA.
Electron. Lett. (GB), Vol.22, No.17, 886-7, 14 Aug. 1986

NPN and PNP lateral bipolar transistors having a base length shorter than 0.5 μm have been made in thin (100-nm) silicon-on-insulator films. Current gains of 75 and 40 have been obtained in NPN and PNP devices, respectively. Measurements indicate a base generation lifetime of 1 μs, and leakage currents of a fraction of a picoampere have been measured. The device fabrication is compatible with an SOI CMOS fabrication process. *IN*

51). Reduction of Floating Substrate Effect in Thin-Film SOI MOSFETs.
Colinge, J.-P.
Hewlett-Packard Labs., Palo Alto, CA.
Electron. Lett. (GB), Vol.22, No.4, 187-8, 13 Feb. 1986

The presence of a floating substrate in SOI transistors gives rise to a decrease of threshold voltage when drain voltage is increased. When the devices are made in a very thin silicon film, the latter is completely depleted when the device is in the 'on' state, and no part of the film can act as a floating substrate. This brings about a dramatic decrease of the so-called 'kink effect'. *IN*

52). Subthreshold Slope of Thin-Film SOI MOSFETs.
Colinge, J.-P.
Hewlett-Packard Labs., Palo Alto, CA.
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.4, 244-6, April 1986

Silicon-on-insulator (SOI) n-channel transistors have been made in thin (90-nm) silicon films. Both modelling and experimental results show that excellent subthreshold slopes can be obtained (62 mV/decade) when the silicon film thickness is smaller than the maximum depletion depth in the transistor channel. For comparison, the subthreshold slope of transistors made in thicker films is also reported. *IN*

53). Transconductance of Silicon-on-Insulator (SOI) MOSFETs.
Colinge, J.-P.
Hewlett Packard Labs., Palo Alto, CA.
IEEE Electron Device Lett. (USA), Vol.EDL-6, No.11, 573-4, Nov. 1985

The transconductance of n-channel silicon-on-insulator (SOI) MOSFETs has been measured with backside gate (substrate) bias as a parameter. For negative values of the backside gate bias, the transconductance of SOI transistors is similar to that of bulk devices. On the other hand, the transconductance exhibits an unusual behavior when the backside gate is positively biased. This is caused by mutual influence of the front- and backside gate-related depletion zones. Modeling of transconductance using numerical solution of Poisson's equation shows good agreement with experimental results. *IN*

54). Normally-Off MOS FETs Using Ultra Thin SOI Structured Silicon Film.
Hatori, F.; Sugano, T.
Dep. Electron. Eng., Univ. Tokyo, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 18th, 545-8, 1986 *CA*

55). New Method of Determination of the Flat-Band Voltage in SOI MOS Structures.
Iniewski, K.; Jakubowski, A.

Inst. of Electron Technol., Warsaw Tech. Univ., Poland
Solid-State Electron. (GB), Vol.29, No.9, 947-50, Sept. 1986

A new method to determine the flat-band voltage V_{FB} in an MOS structure has been proposed. It is based on measuring a voltage which corresponds to a capacitance equal to 0.9 of the oxide capacitance. The method is especially suited for SOI (silicon-on-insulator) structures, but could be useful in conventional types. In the latter case the error of determination of V_{FB} caused by an uncertainty in doping concentration is smaller than in the classical procedure, especially when the thickness of the dielectric is small. *IN*

56). Activation Energies of Oxide Charge Recovery in SOS or SOI Structures After an Ionizing Pulse.
Leray, J.-L.
CEA, Paris, France
IEEE Trans. Nucl. Sci. (USA), Vol.NS-32, No.6, 3921-8, Dec. 1985
1985 Annual Conference on Nuclear and Space Radiation Effects, 21-24 July 1985, Monterey, CA.

MOS transistors in either SOS technology with oxidation temperature variations or laser-recrystallized SOI have been exposed to an ionizing pulse in order to derive the activation energy of oxide charge recovery. A direct dependence of annealing activation energy on oxidation or on highest temperature and on electric field is found. In the case of SOI, the substrate oxide must also be considered. Models are discussed that are based on an exponential distribution of states above the valence band and/or on polaron effects. *IN*

• 57). Staggered CMOS: A Novel Three-Dimensional Technology.
Maby, E.W.; Antoniadis, D.A.
Dept. of Electr. Eng. & Comput. Sci., MIT, Cambridge, MA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 161-6, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

The authors report the fabrication of mutually self-aligned IGFETs in two silicon layers which are separated by a thin dielectric film. The transistors are configured such that the heavily doped source and drain regions of a transistor in one layer also serve as the gate electrodes for transistors in the other layer. One application of this three-dimensional technology is the implementation of a compact four-transistor 'staggered' CMOS latch circuit which can be used to form part of a static random-access memory cell. *IN*

58). SOI TFT's with Directly Contacted ITO.
Mimura, A.; Oohayashi, M.; Ohue, M.; Ohwada, J.; Hosokawa, Y.
Hitachi Ltd, Hitachi, Japan
IEEE Electron Device Letters, Vol. EDL-7, No. 2, Feb. 1986, 134-136

The fabrication of n-channel Al-gate thin-film transistors (TFTs) were fabricated on a silicon-on-insulator (SOI) is reported. Indium tin oxide (ITO) was deposited directly on the n^+ silicon layer of the TFT. The contact resistance between the ITO and the n^+ silicon layer increases with thermal annealing. The low-temperature (200°C) lift-off method of ITO is applied to achieve high-quality TFTs for active matrices in liquid crystal displays. *EI*

59). Radiation Damage in MOS Devices Underlying an Electron Beam Annealed SOI Structure.
Saitoh, S.; Higuchi, K.; Okabayashi, H.
Microelectronics Res. Labs., Nippon Electric Co. Ltd., Kawasaki, Japan
Jpn. J. Appl. Phys. Suppl. (Japan), 197-200, 1982

Proceedings of the 14th Conference (1982 International) on Solid State Devices, 24-26 Aug. 1982, Tokyo, Japan

Radiation damage due to electron-beam annealing has been investigated in MOS devices underlying an electron-beam-annealed silicon-on-insulator structure. A high degree of residual damage (surface state and positive charge) is found to exist in MOS devices. The damage can be easily annealed out by low-temperature (500 to 550°C) furnace annealing, when underlying MOS devices exist outside the electron-beam range. However, high-temperature furnace annealing at about 1000°C is necessary to eliminate the damage, when the electron bed penetrates through the gate oxides in the MOS devices. Use of a low-energy electron beam is recommended, based on these results, for the silicon-on-insulator formation for three-dimensional ICs. *IN*

60). TITE RAM: A New SOI DRAM Gain Cell for Mbit DRAMs.
Shichijo, H.; Malhi, S.D.S.; Shah, A.H.; Pollack, G.P.; Richardson, W.F., Elahy, M.; Banerjee, S.; Womak, R.; Chatterjee, P.K.
Semicond. Process & Design Centre, Texas Instruments Inc., Dallas, TX.
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 265-8, 1984, 30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

A new DRAM gain cell using SOI LPCVD polysilicon MOSFETs is proposed and experimentally demonstrated. This cell can realize a cell size of less than 15 μm^2 with 1-μm design rules for Mbit level MOS dynamic RAMs. Because the signal storage region is isolated by oxide, the cell is expected to be immune to soft errors and substrate disturbances. Typical signal retention times of 10 to 50 ms at room temperature, and 1 to 5 ms at 100°C are obtained. *IN*

61). Transient Effect in Thinned Silicon-on-Insulator Devices.
Vu, D.P.
CNET, CNS, Meylan, France
Electron. Lett. (GB), Vol.22, No.8, 412-13, 10 April 1986

In thin-film silicon-on-insulator devices, electrostatic coupling between the two Si-SiO_2 interfaces gives rise to transient drain-source current. This effect should be considered in devising three-dimensional circuits. *IN*

62). A Device Simulator for Silicon on Insulator MOSFETs.
Armstrong, G.A.; Davis, J.R.
Dept. of Electr. Eng., Queen's Univ. of Belfast, N. Ireland
Board, K.; Owen, D.R.J. (Editors)
Simulation of Semiconductor Devices and Processes. Vol.2., Proceedings of the Second International Conference, 449-67, 1986, 21-23 July 1986, Swansea, Wales
Pineridge Press, Swansea, Wales

A device simulator which predicts the DC characteristics of SOI MOSFETs has been developed. The simulator which is an extension of the MINIMOS program uses finite difference methods to solve the semiconductor equations in two dimensions for both carrier types. Accurate predictions of the onset of the 'kink' effect have been made for a range of devices with different gate lengths, fabricated in SOI films formed by buried oxygen implantation. The influence of carrier mobility and interface charge at the lower interface on the subthreshold behaviour has been considered. *IN*

• 63). A Seeded-Channel Silicon-on-Insulator (SOI) MOS Technology.
Baerg, W.; Sturm, J.C.; Hwa, T.L.; Lin, H.Y.; Siu, B.B.; Ting, C.H.; Tzeng, J.C.; Gibbons, J.F.
Intel Corp., Santa Clara, CA.
IEEE Electron Device Lett., Vol. EDL-6, No. 12, 668-70, Dec. 1985

An improved silicon-on-insulator (SOI) MOSFET transistor structure is presented. The structure retains the density and low-capacitance advantages of SOI, but places the transistor channel region in the single-crystal silicon substrate. This 'seeded-channel' configuration avoids floating-body effects and ensures that defects in the SOI will not affect the channel mobility. The technology has been used to successfully fabricate n-channel transistors. *IN*

64). Deep Depleted SOI MOSFETs With Back Potential Control: A Numerical Simulation.
Balestra, F.; Brini, J.; Gentil, P.
Lab. de Phys. des Composants a Semicond., ERA-CNRS, ENSERG, Grenoble, France
Solid-State Electron. (GB) Vol.28, No.10, 1031-7, Oct. 1985

The authors consider SOI MOSFET structures (N and P type) for which control of the back potential of the epi layer is obtained by using a back gate. The effect of interface parameters on the back and front threshold voltages is analysed in the case of a strong coupling between front and back interface (lightly doped epi layer). This analysis is carried out by a numerical integration of Poisson's equation throughout the structure. The authors thus obtain the potential profile and the electron and hole densities, as a function of the applied front (V_{G1}) and back (V_{G2}) gate voltages. They also derive the $I_D(V_{G1}, V_{G2})$ characteristics in the case of low drain voltage. This program allows them to examine the dependence of both front and back threshold voltages on the interfacial parameters. It is also used to examine the validity of the existing analytical models and to interpret experimental results obtained on MOS/SOS transistors. *IN*

65). Silicon on Insulator – New Insulation Method Yields Smaller Circuits (Integrated Circuits).
Bergstrom, S.
Eltek. Aktuell Elektron. (Sweden), No.14, 82-4, Sept. 1984

With good insulation between circuits, it is possible to pack them close together. Silicon-on-insulator is a common term for a number of new insulation methods. With some of these methods, it is possible to build three-dimensional integrated circuits. *IN*

66). Radiation Effects in Semiconductors: Technologies for Hardened Integrated Circuits.

Charlot, J.-M.
Service Electronique, CEA, Bruyeres-Le-Chatel, France
Rhoderick, E.H. (Editor)
Solid State Devices 1983, Thirteenth European Solid State Device Research Conference (ESSDERC) and the Eighth Symposium on Solid State Device Technology (SSSDT), 83-103, 1983, 13-16 Sept. 1983, Canterbury, Kent, England
IOP, Bristol, England

Various technologies are used to manufacture integrated circuits for electronic systems. But for specific applications, including those with a radiation environment, it is necessary to choose an appropriate technology or to improve a specific one in order to reach a definite hardening level. The author aims to present the main effects induced by radiation (neutrons and gamma rays) into the basic semiconductor devices, to explain some physical degradation mechanisms, and to propose solutions for hardened integrated circuit fabrication. The analysis involves essentially the monolithic structure of the integrated circuits and the isolation technology of active elements. In conclusion, the advantages of EPIC and SOS technologies are described and the potentialities of new technologies (GaAs and SOI) are presented. *IN*

67). Linear-Region Conductance of Thin-Film SOI MOSFET's with Grain Boundaries.
Fossum, J.G.; Lim, H.-K.; Ortiz-Conde, A.
Dept. of Electrical Engng., Univ. of Florida, Gainesville, FL.
IEEE Electron Device Lett. (USA), Vol.EDL-4, No.7, 239-42, July 1983

The linear-region conductance of silicon-on-insulator (SOI) MOSFETs is modeled by properly combining theoretical descriptions of the effects of grain boundaries in the channel region and of charge coupling between the front and back gates. The model is supported by measurements of thin-film SOI MOSFETs with and without grain boundaries. The theoretical-experimental analysis clearly distinguishes the charge-coupling effect from the grain-boundary effect, both of which can be beneficial to the MOSFET performance, and shows that the effects are not simply superimposed. *IN*

68). Analysis of Kink Characteristics in Silicon-on-Insulator MOSFETs Using Two-Carrier Modeling.
Kato, K.; Wada, T.; Taniguchi, K.
VLSI Res. Center, Toshiba Corp., Kawasaki, Japan
IEEE Trans. Electron Devices (USA), Vol.ED-32, No.2, 458-62, Feb. 1985

An exact SOI device simulator applicable to the prediction of the transistor characteristics in the high-current region is developed. In the simulator, the basic two-dimensional Poisson and current continuity equations are numerically solved under steady-state condition. To obtain a stable and rapid convergence in the numerical scheme, a newly developed alternative step solving method is implemented. Using this simulator, the drain current kink effect, a typical phenomenon for substrate floating devices, is exactly simulated for the first time. The physical mechanism of this phenomenon is also clarified. The simulated results indicate that kink effects are suppressed by using low lifetime SOI substrates. *IN*

69). Numerical Analysis of Switching Characteristics in SOI MOSFETs.
Kato, K.; Taniguchi, K.
Toshiba Corp., Kawasaki, Japan
IEEE Trans. Electron Devices (USA), Vol. ED-33, No.1, 133-9, Jan. 1986

By using a two-carrier and two-dimensional transient SOI simulator, calculated waveforms having good agreement with experimental results are obtained. Further analysis reveals the mechanism of switching characteristics. The motion of majority carriers plays a role in determining the switching characteristics for SOI devices in both the turn-on and turn-off stages, although the current overshooting time and the substrate potential recovery time are strongly affected by bias conditions.

The magnitude of drain current overshoot in the turn-on stage is also found to be a function of substrate impurity concentration. *IN*

70). Transient Analysis of Drain Current in Silicon-on-Insulator (SOI) MOSFETs.
Kato, K.; Wada, T.; Taniguchi, K.
VLSI Res. Center, Toshiba Corp., Kawasaki, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 68-9 supl, 1984, 30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

A MOSFET having channel length of 2 μm is fabricated on an SOI substrate in a standard process line. Gate oxide and SOI film thicknesses are 70 nm and 1 μm, respectively. The turn-on drain current overshoots by up to more than twice the steady-state value, and then decreases to a steady-state value in about 200 μs. The authors developed a rigorous two-carrier and transient SOI device simulator to analyze the switching characteristics. *IN*

71). A Novel Numerical Model for SOI Devices.
Lai, P.T.; Cheng, Y.C.
Dept. of Electr. Eng., Hong Kong Univ., Hong Kong
IEEE Electron Device Lett. (USA), Vol.EDL-6, No.9, 459-61, Sept. 1985

The Poisson's equation governing the potential distribution of semiconductor-on-insulator structures is solved by a novel numerical technique. In this efficient method, no grid-points need to be assigned for all the insulator regions such as the surface oxide layer, buried oxide layer, and sapphire layer. *IN*

72). Reduction of Problem Size for the Poisson Solver in Device Simulation.
Lai, P.T.; Cheng, Y.C.
Dept. of Electr. Eng., Hong Kong Univ., Hong Kong
IEEE Electron Device Lett. (USA), Vol.EDL-6, No.1, 6-7, Jan. 1985

A novel solution technique for the Poisson equation is demonstrated by using a mixed method, i.e., a direct algorithm for part or all of the insulator region and an iterative method for the remaining portion of the device structure. It is shown that the approach compares favorably to the corresponding iterative method, especially for devices with a larger proportion of insulator regions to semiconductor regions. By exploiting the linearity of the partial differential equation governing the insulator, it is possible to reduce the problem size and, therefore, the computer resources by an amount which increases with the proportion of grid nodes in the insulator region. As a result, the proposed solution method is well suited for device structures with thick field oxide and/or deep trench oxide, or for semiconductor-on-insulator structures. *IN*

73). A Charge-Based Large-Signal Model for Thin-Film SOI MOSFETs.
Lim, H.-K.; Fossum, J.G.
Dept. of Electr. Eng., Florida Univ., Gainesville, FL.
IEEE Trans. Electron Devices (USA), Vol.ED-32, No.2, 446-57, Feb. 1985

A charge-based large-signal model for thin-film SOI (Si-on-SiO_2) MOSFETs, intended for computer simulation of transient characteristics of SOI and 3-D circuits, is developed. The model emphasizes the structural uniqueness of the devices. Closed-form expressions for the quasi-static terminal charges, simpler than those for the bulk MOSFET because of the thin-film structure, are derived in terms of terminal voltages and device parameters, and are used to define the terminal currents. Equivalent circuits, developed from the charge-based model, show that the device can be accurately represented using only real reciprocal capacitances by explicitly accounting for the transient channel transport current I_{TT}. The analytical expression for I_{TT}, obtainable for the thin-film structure, makes it possible to evaluate the finite-carrier transit delay in the channel and the corresponding

charge nonconservation in the conventional reciprocal-capacitance MOSFET model that does not account for the delay. *IN*

74). Current-Voltage Characteristics of Thin-Film SOI MOSFETs in Strong Inversion.
Lim, H.-K.; Fossum, J.G.
Dept. of Electrical Engng., Univ. of Florida, Gainesville, FL.
IEEE Trans. Electron Devices (USA), Vol.ED-31, No.4, 401-8, April 1984

A simple analytic model for the steady-state current-voltage characteristics of strongly inverted silicon-on-insulator (SOI) MOSFETs is developed. The model, simplified by assuming that the inversion charge density is described well by a linear function of the surface potential, clearly shows the dependence of the drain current on the device parameters and on the terminal voltages, including the back-gate (substrate) bias. The analysis is supported by measurements of current-voltage characteristics of thin-film (laser recrystallized) SOI MOSFETs. The dependence of carrier mobility on the terminal voltages, especially the back-gate bias, is analyzed and shown to underlie discrepancies between the theoretical (constant mobility) and experimental results at high-gate voltages. The mobility dependence on the back-gate bias enhances the strong influence of the back gate on the drain current, especially when the device is saturated. *IN*

75). Transient Drain Current and Propagation Delay in SOI CMOS.
Lim, H.-K.; Fossum, J.G.
Dept. of Electrical Engng., Univ. of Florida, Gainesville, FL
IEEE Trans. Electron Devices (USA), Vol.ED-31, No.9, 1251-8, Sept. 1984

The transient overshoot in drain current that occurs in thin-film SOI (Si-on-SiO_2) MOSFETs because of the floating body is analyzed, and the benefit it can provide to propagation delay (speed) in SOI CMOS digital circuits is assessed. The analysis accounts for the charge-coupling between the front and back gates, and describes the dependence of the transient drain current (saturation) and propagation delay on the back-gate bias as well as on the switching frequency. Measurements of the transient current in recrystallized SOI MOSFETs and of propagation delay in SOI CMOS inverters and ring oscillators are described and shown to support the theoretical analysis. The current overshoot is especially beneficial in low-voltage circuits, although at high frequencies other floating-body effects can degrade the speed. *IN*

76). Back and Side Channel Leakage in SOI CMOS.
Oakley, R.E.
Plessey Res. Ltd., Caswell, Towcester, England
1983 Symposium on VLSI Technology. Digest of Technical Papers, 52-3, 1983
13-15 Sept. 1983, Maui, HI.
Business Centre for Acad. Soc. Japan, Tokyo, Japan

Source-to-drain leakage currents, flowing along the back and sides of the silicon islands, have been a problem in SOI technology from the earliest days of silicon on sapphire. These are particularly important in CMOS where they dominate the standby power and, with the advent of VLSI, they have become a major design consideration. N-channel and p-channel devices and CMOS circuits have been made on a variety of SOI substrates including silicon on sapphire, laser-recrystallized polysilicon, oxygen-implanted silicon, and strip-heater-recrystallized polysilicon as well as twin tub and conventional bulk CMOS processes. The emphasis has been on oxygen-implanted material with various doses and energies, both with and without epitaxy and on strip-heater-recrystallized polysilicon. *IN*

77). A Three-Dimensional DRAM Cell of Stacked Switching-Transistor in SOI (SSS).
Ohkura, M.; Kusukawa, K.; Sunami, H.; Hayashida, T.; Tokuyama, T.
Hitachi Ltd., Tokyo, Japan
International Electron Devices Meeting, Technical Digest, 718-21, 1985

1-4 Dec. 1985, Washington, DC.
IEEE, New York.

A new three-dimensional one-transistor dynamic RAM cell is presented. It has a trench capacitor fabricated in the Si substrate and a switching transistor fabricated in a laser-induced SOI layer formed on top of the capacitor area. The cell's advantages are a high capacitor capture ratio (capacitor area/cell area) and the possession of high capacitance even when the cell size is reduced to less than 5 μm^2, which is the anticipated size for a 16-Mb DRAM cell. The alpha-particle problem can be overcome by applying the Hi-C structure to the cell. *IN*

78). A Negative Drain Conductance Property in a Super-Thin Film Buried-Channel MOSFET on a Buried Insulator.
Omura, Y.; Sano, E.; Ohwada, K.
Musashino Electrical Communication Lab., NTT Public Corp., Tokyo, Japan
IEEE Trans. Electron Devices (USA), Vol.ED-30, No.1, 67-73, Jan. 1983

A negative drain conductance property in buried-channel MOSFETs on a buried insulator is demonstrated experimentally. The physical origin of the negative drain conductance is discussed theoretically. It is shown by a numerical analysis that the diffusion current of majority carriers, which flows against the drift current, is the origin of the negative drain conductance beyond the pinchoff stage. It is indicated that an intensely high convex profile of majority carriers near the drain is essential for that diffusion current, and that the profile is easily achieved when the conductive layer thickness is less than an extrinsic debye length. *IN*

79). A Simple Model for Short-Channel Effects of a Buried-Channel MOSFET on the Buried Insulator.
Omura, Y.
Electrical Communication Lab., NTT Public Corp., Tokyo, Japan
IEEE Trans. Electron Devices (USA), Vol.ED-29, No.11, 1749-55, Nov. 1982

A majority-carrier distribution model and a channel potential-profile model, in which the barrier-lowering effect is taken into account, are proposed for a buried-channel MOSFET (BC-MOSFET/-SOI). Simple expressions for threshold voltage and drain breakdown voltage were derived from the models for a short-channel BC-MOSFET/SOI. The comparison between theory and experimental results shows reasonable agreement. The physical concepts of short-channel effects on the threshold voltage and drain breakdown voltage have been compared with surface channel MOSFETs. Various scaling schemes are also discussed. *IN*

80). Modeling of 0.1-μm MOSFET on SOI Structure Using Monte Carlo Simulation Technique.
Throngnumchai, K.; Asada, K.; Sugano, T.
Dept. of Electron. Eng., Tokyo Univ., Japan
IEEE Trans. Electron Devices (USA), Vol.ED-33, No.7, 1005-11, July 1986

Simulation of 0.1-μm MOSFET characteristics using the Monte Carlo method is introduced. The device is a 0.1-μm MOSFET on an ultrathin, nearly intrinsic SOI structure that is thought to suppress short-channel effects. Intravalley scattering with acoustic phonon and intervalley inelastic scattering have been taken into account in the model. Surface roughness scattering has also been considered using a classical mode, which combines specular reflection and diffuse scattering. In order to take avalanche breakdown into account, a two-carrier many-particle Monte Carlo method has been used. A new model is proposed for the impact ionization probability, and also for the velocity distribution of both the primary electron and the generated electron-hole pairs. *IN*

81). Exact Modeling of Semiconductor-on-Insulator (SOI) Devices.
Yamaguchi, K.; Hagiwara, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan

Miller, J.J.H. (Editor)
NASECODE III. Proceedings of the Third International Conference on the Numerical Analysis of Semiconductor Devices and Integrated Circuits, 311-16
15-17 June 1983, Galway, Ireland
Boole Press, Dublin, Ireland

Numerical modeling of SOI devices by a bipolar carrier approach is proposed. Poisson's equation and the current continuity equations for electrons and holes are solved simultaneously. The former is solved in the whole area of devices, and electrostatic potential at the silicon-insulator interface is determined so as to fulfill Gauss's theorem. To achieve accurate numerical calculation and to obtain a stable convergence in the numerical scheme, a variable transformation is employed in the current continuity equation. Sample calculations demonstrate a quick and stable convergence in the numerical scheme, and clarify the operational mechanism of SOI devices. This modeling should become a helpful aid in SOI device design. *IN*

• 82). Mathematical Modeling of Semiconductor-on-Insulator (SOI) Device Operation.
Yamaguchi, K.
Hitachi Ltd., Tokyo, Japan
IEEE Trans. Electron Devices (USA), Vol.ED-31, No.7, 977-82, July 1984

Numerical modeling of SOI devices is proposed through the use of a bipolar carrier and time-dependent approach. Poisson's equation and the current continuity equations for electrons and holes are solved simultaneously. The former is solved over the whole area of the device in question, and the electrostatic potential at the silicon-insulator interface is determined so as to fulfil Gauss's theorem. To achieve accurate numerical calculations and to obtain a stable convergence in the numerical scheme, a variable transformation is used in the current continuity equation. That is, quasi-fermi potentials for electrons and holes rather than carrier densities are directly analyzed. An insulated layer is modeled in the current continuity equation using the zero intrinsic-carrier density and zero mobility to realize zero conductance in an insulator. *IN*

4. NOVEL TECHNIQUES: BONDING/ETCHBACK AND DEVICE TRANSFER

• 83). A Field-Assisted Bonding Process for Silicon Dielectric Isolation.
Frye, R.C.; Griffith, J.W.; and Wong, Y.H.
AT&T Bell Laboratories, Murray Hill, NJ
J. Electrochem. Soc.: Solid-State Science and Technology, Vol. 133, No. 8, 1673-1677, August 1986

We have developed a technique for bonding together two oxidized silicon wafers, resulting in a $Si/SiO_2/Si$ structure. The process consists of applying a moderate voltage between the wafers at a temperature of 1100°C–1200°C. Under these conditions, 3-in device wafers form a uniform, microscopically defect-free bond over their entire area. Our experiments indicate that water-related ionic charges in the steam-grown oxides are transported to the surface by electric field. These charges concentrate the potential drop into the gap between the wafers, giving rise to a large field and strong attractive force, even at low values of applied voltage. This technique can be used for the fabrication of dielectrically isolated silicon devices. The water-related impurities responsible for the bonding are annealed out during the process itself and do not pose any contamination problems in subsequent device processing. In addition, the bonded silicon wafers are found to be free of stress-induced dislocations and stacking faults which can degrade carrier lifetime. These advantages suggest that this technique offers a potential low-cost alternative to current dielectric isolation technology.

84). Device Layer Transfer Technique Using Chemi-Mechanical Polishing.
Hamaguchi, T.; Endo, N.; Kimura, M.; Ishitani, A.
NEC Corp., Kawasaki, Japan
Jpn. J. Appl. Phys. Part 2 (Japan), Vol.23, No.10, L815-17, Oct. 1984

A device layer transfer technique, a new technique for transferring a thin device layer fabricated on the silicon wafer onto an insulating substrate, is described. The fundamental processes supporting this technique are wafer thinning using chemi-mechanical polishing and wafer fastening. A 2-μm thick device layer with a 2-in diameter is formed on a quartz glass substrate without significant degradation in transistor characteristics. *IN*

85). Novel LSI/SOI Wafer Fabrication Using Device Layer Transfer Technique.
Hamaguchi, T.; Endo, N.; Kimura, M.; Nakamae, M.
NEC Corp., Kawasaki, Japan
International Electron Devices Meeting, Technical Digest, 688-91, 1985
1-4 Dec. 1985, Washington, DC.
IEEE, New York.

A device layer transfer technique, wherein a device layer already fabricated on a silicon wafer is transferred onto an insulating substrate, has been developed for achieving an LSI/SOI wafer. This technique is based on preferential polishing, newly developed with a more than 100 Si/SiO_2 polishing rate ratio. A bipolar LSI active layer, formed in a 1-μm thick epitaxial layer, has been successfully transferred to a 4-in diameter quartz glass. No change in $I_C - V_{CE}$ characteristics of the transistor and leakage current of the CB junction was observed. Isolation breakdown voltage was markedly improved after transfer. The device transfer technique is a promising method for realizing an LSI/SOI wafer with both large-diameter and high-crystal quality. *IN*

86). Epitaxial Film Transfer Technique for Producing Single Crystal Si Film on an Insulating Substrate.
Kimura, M.; Egami, K.; Kanamori, M.; Hamaguchi, T.
Fundamental Res. Labs., NEC Corp., Kawasaki, Japan
Appl. Phys. Lett. (USA), Vol.43, No.3, 263-5, 1 Aug. 1983

Epitaxial film transfer, a new technique for producing a single-crystal Si film with both large size and high quality on an insulating substrate, is demonstrated. The technique in which an epitaxial Si film is transferred to a secondary substrate by using three fundamental processes of epitaxial growth, bonding of two wafers, and substrate elimination can produce a 2-in single-crystal Si film as thin as 1.5 μm on an insulating substrate. Thickness variation can be controlled to $\pm 0.06\mu$m across a 2-in wafer. An epitaxial Si film is transferred without significant degradation in quality although a fine film waving exists. *IN*

87). Silicon-on-Insulator (SOI) by Bonding and Etch-Back.
Lasky, J.B.; Stiffler, S.R.; White, F.R.; Abernathey, J.R.
IBM Gen. Technol. Div., Essex Junction, VT.
International Electron Devices Meeting, Technical Digest, 684-7, 1985
1-4 Dec. 1985, Washington, DC.
IEEE, New York.

A silicon wafer bonding process is described in which only thermally grown oxide is present between wafer pairs. Bonding occurs after insertion into an oxidizing ambient. It is proposed that the wafers are drawn into intimate contact as a result of the gaseous oxygen between them being consumed by oxidation, thus producing a partial vacuum. The proposed bonding mechanism is polymerization of silanol bonds between wafer pairs. A preferential etch-back process is used to produce silicon-on-insulator (SOI) whose electrical quality is equal to that of bulk silicon. Capacitor measurements show a 27-μs minority carrier lifetime and low Q_{ss} at the SOI-'bottom oxide' interface. In addition, there is negligible charge within the bonding oxide. N-channel and p-channel FET devices show threshold voltages and mobilities equal to bulk controls. The subthreshold leakage is less than 1 fA per micron of channel width. *IN*

• 88). Wafer Bonding for Silicon-on-Insulator Technologies.
Lasky, J.B.
IBM Gen. Technol. Div., Essex Junction, VT.
Appl. Phys. Lett. (USA), Vol.48, No.1, 78-80, 6 Jan. 1986

A silicon wafer bonding process is described in which only thermally grown oxide is present between wafer pairs. Bonding occurs after insertion into an oxidizing ambient. It is proposed the wafers are drawn into intimate contact as a result of the gaseous oxygen between them being consumed by oxidation, thus producing a partial vacuum. The proposed bonding mechanism is polymerization of silanol bonds between wafer pairs. Silicon-on-insulator (SOI) is produced by etching away all but a few microns of one of the bonded pair. Capacitor measurements show a 27-μs minority-carrier lifetime and no degradation of the SOI-insulator interface. In addition, there is negligible charge at the bonding interface, making the technique attractive for three-dimensional as well as planar SOI applications. *IN*

89). A Technology for High-Performance Single-Crystal Silicon-on-Insulator Transistors.
Spangler, L.J.; and Wise, K.D.
Dept. of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI
IEEE Electron Device Letters, Vol.EDL-8, No.4, 137-139, April 1987

A process for forming transistors and circuits in a thin single-crystal silicon film on a glass substrate is presented. The process involves the electrostatic bonding of a silicon wafer to glass and the subsequent thinning of the wafer using doping-sensitive etchants to retain only the epitaxial layer. NMOS transistors have shown channel mobilities of 640 $cm^2/V{\cdot}s$, while leakage currents have been measured at less than $10^{-14}A/\mu m$.

5. EPITAXIAL OVERGROWTH

Comprehensive Treatment

90). Control of Lateral Epitaxial Chemical Vapor Deposition of Silicon Over Insulators.
Bradbury, D.R.; Kamins, T.I.; Tsao, C.-W.
J. Appl. Phys. (USA), Vol.55, No.2, 519-23, 15 Jan. 1984

Single-crystal silicon films have been grown over SiO_2-covered regions of a single-crystal silicon wafer by lateral epitaxial chemical vapor deposition (CVD). Nucleation of polycrystalline silicon on the SiO_2 is suppressed by adding HCl to the SiH_4 deposition gas. Sequential variation of the HCl partial pressure during different stages of the deposition process controls the relative deposition rates of the (100) and (110) planes and, consequently, the shape of the laterally advancing growth fronts, allowing the fronts from opposite sides of the SiO_2 region to join uniformly. A plane surface is obtained by increasing the HCl partial pressure after coalescence. A standard silicon CVD epitaxial reactor is used for the deposition. *IN*

91). An Epitaxial Regrowth of Polysilicon to Single Crystal Silicon by H_2 Annealing Process.
Hirofuji, Y.; Nomura, N.; Kugimiya, K.
Central Res. Lab., Matsushita Electr. Ind. Co. Ltd., Osaka, Japan
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 187-92, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Si epitaxial regrowth was realised through the thick interfacial oxide films of up to 2 nm by H_2 annealing. The epitaxy took place in a region when the oxide was reduced to about a half of its initial peak height, indicating that about half of the interfacial oxide films in area was completely reduced. In this region, redistribution or diffusion of super-saturated oxygen was also observed. A schematic model of the epitaxial regrowth by H_2 annealing is presented. *IN*

92). Solid-Phase Epitaxial Regrowth of Ion-Implanted Silicon on Sapphire Using Rapid Thermal Annealing.
Hodge, A.M.; Cullis, A.G.; Chew, N.G.
R. Signals & Radar Establ., Malvern, England
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984
Symposium, 393-9, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

Solid phase epitaxial regrowth of silicon on sapphire is used to improve the quality of as-received silicon films prior to conventional device processing. It has been shown that this is necessary, especially for layers of 0.3 μm and thinner, if the full potential of this particular silicon on insulator technology is to be realised. Si^+ ions are implanted at an energy and dose such that all but the surface of the silicon film is rendered amorphous. In this study, the layer is regrown using a rapid thermal annealer operated in the multi-second regime. A second shallower implant followed by rapid thermal annealing produces a further improvement. Characterisation of the material has been principally by cross-sectional transmission electron microscopy. The structures observed after different implant and regrowth treatments are discussed. *IN*

93). Lateral Solid Phase Epitaxy in Partially Doped Si Amorphous Layers onto Silicon Dioxide.
Ishiwara, H.; Furukawa, S.; Tanaka, M.; Ohta, K.
Tokyo Inst of Technology, Yokohama, Japan

IEEE Transactions on Electron Devices, Vol. ED-33, No. 11, 44th Annual Device Res. Conf., Amherst, MA, June 23-25, 1986, 1842-1843 *EI*

94). Lateral Solid Phase Epitaxy of Amorphous Si Films Onto Nonplanar SiO_2 Patterns on Si Substrates.
Ishiwara, H.; Tamba, A.; Furukawa, S.
Graduate Sch. of Sci. & Eng., Tokyo Inst. of Technol., Yokohama, Japan
Appl. Phys. Lett. (USA), Vol.48, No.12, 773-5, 24 March 1986

Lateral solid phase epitaxy (L-SPE) of amorphous Si (a-Si) films onto nonplanar SiO_2 pattern on Si (100) substrates was investigated. The patterns were formed by local oxidation of silicon (LOCOS) and the thickness of the SiO_2 films ranged from 60 to 470 nm. The L-SPE characteristics to those of planar patterns were observed in dense a-Si films prepared by high-temperature vacuum deposition and subsequent ion implantation. The maximum L-SPE lengths onto the LOCOS patterns were 4.5, 6.5, and 44 μm in undoped, B-doped, and P-doped samples, respectively. *IN*

95). Preparation of Thin (0.6 μm) Continuous Monocrystalline Silicon over Silica.
Jastrzebski, L.; Corboy, J. F.; Pagliaro, R., Jr.; Soydan, R.
RCA Lab., Princeton, NJ
J. Electrochem. Soc., Vol. 132, No. 12, 3056-7, 1985

The application was studied of oxide thinning to Si-on-insulator (SOI) films obtained by using the epitaxial lateral overgrowth (ELO) process. The Si epitaxial films were deposited on a SiO_2-patterned Si substrate in a chemical vapor deposition reactor by using a mixture of SiH_2Cl_2, HCl, and H_2 in a two-step growth cycle. The as-grown ELO films were 6 μm thick; after the epitaxial growth they were thinned by oxidation at 1100°C in HCl steam. SOI films thinned to 0.6 to 3.2 μm had the same flatness as the as-grown film. SiO_2 thickness versus oxidation time was also studied as a function of temperature and pressure in pyrogenic steam on (100) Si; results are tabulated for SiO_2 thickness of 0.5 to 6 μm. *CA*

• 96). Silicon CVD for SOI: Principles and Possible Applications.
Jastrzebski, L.
RCA Labs., Princeton, NJ.
Solid State Technol. (USA), Vol. 27, No. 9, 239-43, Sept. 1984

A CVD silicon epitaxial process for VLSI which can give good quality monocrystalline SOI films or silicon islands surrounded by oxide mask is discussed. The silicon film is seeded locally through openings in the SiO_2 mask from which it overgrows the oxide. Growth can be carried out until a continuous epitaxial SOI film is formed or may be stopped when windows in the SiO_2 mask are filled with silicon. This process could be used to obtain material for dielectrically isolated bipolar or CMOS circuits, three-dimensional structures, or as a new isolation method for MOS circuits. The effort is directed toward the improvement of packing density and performance. *IN*

97). Lateral Epitaxial Overgrowth of Silicon Over Recessed Oxide.
Jayadev, T.S.; Okazaki, E.; Petersen, H.; Millman, M.
Lockheed Palo Alto Res. Lab., Lockheed Missiles & Space Co., CA.
Electron. Lett. (GB), Vol. 21, No. 8, 327-8, 11 April 1985

There has been considerable interest in silicon-on-insulator (SOI) technology recently because of its potential applications in VLSI. CMOS circuits in SOI have higher speed because of the absence of substrate capacitance, and freedom from latch-up because of dielectric isolation. Recently, memory circuits like DRAMs have reached the physical limits of what is possible in two dimensions, and hence there is a growing need for 3-dimensional circuits. SOI offers a possible avenue to realize such 3-dimensional circuits and thus lead the way to the next generation of memories and integrated circuits. *IN*

98). Fabrication of Si-Gate MOSFET's on a Silicon-on-Insulator Formed by Lateral Solid Phase Epitaxy.
Katoh, T.; Hirashita, N.; Sasaki, M.; Onoda, H.
OKI Electric Industry Co, Hachioji, Japan
IEEE Transactions on Electron Devices, Vol. ED-33, No. 11, 44th Annual Device Res. Conf., Amherst, MA, June 23-25, 1986, 1843 *EI*

99). High-Resolution Electron Microscope Study of Silicon on Insulator Structure Grown by Lateral Solid Phase Epitaxy.
Kawarada, H.; Ueno, T.; Kunii, Y.; Horiuchi, S.; Ohdomari, I.
Waseda Univ, Tokyo, Japan
Jpn. J. Appl. Phys., Part 2, Vol. 25, No. 10, 814-817, Oct. 1986

Structural study of L-SPE grown (100)Si/SiO_2 interface after high-temperature annealing in Ar has been carried out using HRTEM. On an atomic scale the roughness at the (100)Si/SiO_2 interface is less than a few lattice planes (0.5 nm). When micro-twins are present in the L-SPE layer, almost all of them nucleate at the Si/SiO_2 interface. This is evidence for the formation of {111} growth planes near the interface during the L-SPE growth. The twin SiO_2 interface is not parallel to the substrate and forms atomically sharp {111} facets. This fact indicates that the interfacial energy for the (111) Si/SiO_2 interface is lower than that of the (100) Si/SiO_2 in solid phase. *EI*

100). Formation of a Silicon-on-Insulator Structure by Solid-Phase Epitaxy.
Kunii, Y.; Tabe, M.; Kajiyama, K.
Electr. Commun. Labs., NTT Public Corp., Kanagawa, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 209-30, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

A silicon-on-insulator (SOI) structure was formed by solid-phase epitaxy (SPE) of chemical vapor deposited (CVD) amorphous silicon (a-Si). Essential conditions for SPE were fulfilled utilizing a 'clean-CVD' process. In-reactor cleaning removed all interface layers between the a-Si film and Si substrate. Low deposition temperature and high deposition rate reduced micro-crystallites and foreign atoms in the a-Si film. The a-Si/SPE-layer facet was investigated and explained with an atomistic model. A principle for further improvement in lateral SPE is discussed. *IN*

101). Lateral-Epitaxy of CVD a-Si over SiO_2 Stripe-Area by Furnace-Annealing.
Kunii, Y.; Tabe, M.; Kajiyama, K.
Electrical Communication Labs., NTT Public Corp., Tokyo, Japan
Jpn. J. Appl. Phys. Suppl. (Japan), 605-6, 1982
Proceedings of the 14th Conference (1982 International) on Solid State Devices, 24-26 Aug. 1982, Tokyo, Japan

The authors have succeeded in fabricating an SOI structure by 'clean-CVD' of a-Si and furnace-annealing through lateral solid-phase-epitaxy (SPE) over SiO_2 stripe-area. The present fabrication process is simpler than the elaborate lateral-epitaxy methods reported previously, in-vacuum deposition, laser-annealing, and moving-strip-heater. *IN*

102). Solid-Phase Lateral Epitaxy of Chemical-Vapor-Deposited Amorphous Silicon by Furnace Annealing.
Kunii, Y.; Tabe, M.; Kajiyama, K.
Electrical Communication Labs., NTT Public Corp., Tokyo, Japan
J. Appl. Phys. (USA), Vol.54, No.5, 2847-9, May 1983

A single-crystalline silicon-on-insulator structure has been fabricated with solid-phase lateral epitaxy. Chemical-vapor-deposited amorphous silicon (CVD a-Si) deposited on an SiO_2 stripe is crystallized by furnace annealing. A new CVD technique (clean CVD) has met the conditions required for solid-phase epitaxy: clean interface and reduction of impurities and microcrystallites in the a-Si film. In the case of a 4-μm wide SiO_2 stripe parallel to the (100) direction, the entire deposited layer grows epitaxially by low-temperature furnace annealing (550 to 650°C). In the case of a 10-μm wide SiO_2 stripe, the whole surface region also grows epitaxially, although the deep region partially becomes polycrystalline in areas distant from the open substrate surface. The grown-layer crystallinity is improved by subsequent high-temperature annealing. *IN*

103). Lateral Solid-Phase Epitaxy of Vacuum-Deposited Amorphous Si Film Over Recessed SiO_2 Patterns.
Kunii, Y.; Tabe, M.
Atsugi Electr. Comm. Lab., NTT Public Corp., Kanagawa, Japan
Jpn. J. Appl. Phys. Part 2 (Japan), Vol.24, No.5, L352-4, May 1985

A single-crystal silicon-on-insulator structure has been fabricated by lateral solid-phase epitaxy (L-SPE) of vacuum-deposited amorphous Si (a-Si) film on Si (100) substrate with SiO_2 patterns. It is essential in L-SPE of vacuum-deposited a-Si that the substrate surface be planarized by recessing SiO_2 patterns. A 7-μm wide single-crystal area over recessed SiO_2 was grown by low-temperature annealing (575°C, 20 h). Only a polycrystalline area was formed over the unrecessed SiO_2 pattern. This is probably because of voids or the large stress field in a-Si film at the pattern edge step. *IN*

104). Lateral Solid Phase Epitaxy of Silicon on SiO_2 in a Silicon Molecular Beam Epitaxy System.
Lee, K.F.; Swartz, R.G.; Finegan, S.N.; Archer, V.D.; Hull, R.
AT&T Bell Labs., Holmdel, NJ.
IEEE; APS; Mater. Res. Soc.; Office of Naval Res.; American Vacuum Soc.
J. Vac. Sci. & Technol. B (USA), Vol. 3, No. 2, 739-40, March-April 1985
Proceedings of the Third International Conference on Molecular Beam Epitaxy, 1-3 Aug. 1984, San Francisco, CA.

The formation of silicon-on-insulator structures has been a subject of recent interest. Recently, Ishiwara et al. (1983) reported on the lateral solid phase epitaxy of amorphous silicon films over silicon oxide. Thermal anneal was done in a nitrogen ambient to induce epitaxial growth after the sample was taken out of the deposition chamber. The presence of lateral growth was found to depend critically on a post-deposition amorphization implant and the use of a thin (50-nm) silicon oxide layer. Since deposited amorphous silicon films may be porous, and exposure to atmosphere may be a source of absorption of gaseous contaminants, the authors present results obtained with the samples prepared by a postdeposition in-situ thermal anneal in vacuum. The deposition was performed in a silicon molecular beam epitaxy (MBE) system that has been used to produce test circuits. In samples that were simultaneously doped with an arsenic ion beam during deposition, lateral growth of 2 μm over a 100-nm silicon oxide layer has been observed. For stripes with lateral growth in a (110) or equivalent direction, however, only negligible lateral overgrowth was observed, in agreement with the results of Ishiwara et al. Such a difference is larger than the difference in solid phase epitaxial regrowth rate observed for (100) and (110) orientations in bulk silicon. The change in the extent of lateral growth was continuous, as evidenced in radial spoke patterns where the lateral directions of the stripe openings varied continuously from a (100) or equivalent direction. Samples were also examined by cross-section transmission electron microscopy (XTEM). *IN*

105). Formation of Si-on-Insulator Structure Under Solid Phase Growth.
Miyao, M.; Moniwa, M.; Warabisako, T.; Sunami, H.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)

Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 705-9, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

Two possible solutions to the problem of nucleus growth encountered in lateral solid-phase epitaxial growth over insulating films are discussed. A stress field originating from the thermal expansion coefficient for Si and SiO_2 acts as the driving force behind preferential nucleation. Utilization of underlying Si_3N_4 films successfully eliminated nuclei growth at topographically irregular portions. In addition, single crystallization of poly-Si nuclei was achieved on SOI structures for the first time. Lateral growth speed (ν (cm/s)) of 1.6×10^6 exp(−3.9/kT(eV)) was obtained during high-temperature annealing (≥1000°C). *IN*

106). Nucleation Control and Epitaxial Alignment in Silicon-on-Insulator Structure During Solid Phase Growth.
Miyao, M.; Moniwa, M.; Ichikawa, M.; Ishizaka, A.; Doi, T.; Sunami, H.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 511-14, 1984, 30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

Two possible solutions to the problem of nucleus growth encountered in lateral solid-phase epitaxial growth over insulating films are discussed. The driving force for preferential nucleation in amorphous-Si on SiO_2 films was found to be a stress field originating from the thermal expansion coefficient for Si and SiO_2. Utilization of underlying Si_3N_4 films successfully eliminated such nuclei growth. Additionally, high-temperature annealing (≥1000°C) crystallized poly-Si nuclei under lateral epitaxial alignment. Growth speed (V(cm/s)) was estimated to be 1.6×10^6 exp(−3.9/kT(eV)). *IN*

107). Preferential Nucleation Along SiO_2 Steps in Amorphous Si.
Moniwa, M.; Miyao, M.; Tsuchiyama, R.; Ishizaka, A.; Ichikawa, M.; Sunami, H.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Appl. Phys. Lett. (USA), Vol.47, No.2, 113-15, 15 July 1985

Annealing characteristics for amorphous Si film deposited on an SiO_2 layer were investigated with the hope that this would throw further light on aspects of solid phase epitaxy. Preferential nucleation, which initiated from the bottom region of deposited Si film, was found along SiO_2 steps. The activation energy for the growth speed of the nuclei was evaluated to be 1.7 eV. As this value is significantly smaller than 2.0 eV, the bond breaking energy of Si, stress originating mainly from the thermal expansion difference between SiO_2 and Si, is considered to be the driving force. *IN*

108). Lateral Solid Phase Epitaxy of Si over SiO_2 Patterns and Its Application to Silicon-on-Insulator Transistors.
Sasaki, M.; Katoh, T.; Onoda, H.; Hirashita, N.
VLSI Res. & Dev. Center, OKI Electric Ind. Co. Ltd., Tokyo, Japan
Appl. Phys. Lett. (USA), Vol.49, No.7, 397-9, 18 Aug. 1986

Lateral solid phase epitaxy (L-SPE) of vacuum-deposited amorphous Si over SiO_2 patterns for various substrate orientation and growth direction has been investigated and applied to fabrication of thin-film transistors on SiO_2. It has been confirmed that the L-SPE growth length depends strongly on both substrate orientation and growth direction. The maximum growth length of about 7 μm has been obtained in the L-SPE toward (100) direction on a (001) substrate. N-channel and p-channel transistors on the L-SPE layer have been developed and successfully fabricated for the first time. Channel mobilities of 380 $cm^2V \cdot s$ for n-channel transistors and 150 $cm^2V \cdot s$ for p-channel transistors have been obtained. *IN*

109). Integrated Circuits Fabricated on Multiple Silicon-Insulator Structures.
Sugiura, S.; Yoshida, T.; Kaneko, T.; Shono, K.; Dumin, D.J.
Sophia Univ., Tokyo, Japan
1984 Symposium on VLSI Technology. Digest of Technical Papers, 1984
10-12 Sept. 1984, San Diego, CA.
Japan Soc. Appl. Phys., Tokyo, Japan

The epitaxial growth of up to four multiple layers of silicon-insulator-on-silicon and SOS wafers is discussed. The high quality of the individual epitaxial silicon layers has been demonstrated by fabricating MOS ICs on each of the individual layers. The silicon quality, as determined by the transistor mobility, decreases as the number of layers increases. However, even the quality of the fourth layer on silicon is comparable to the quality of SOS wafers. It is concluded that the usefulness of the concept of single-crystal insulators in SOI structures has been demonstrated. *IN*

110). Seeding Lateral Epitaxy of Silicon on Insulator with Improved Seed and Cap Structure by Pseudoline Shaped Electron Beam Annealing.
Suguro, K.; Inoue, T.; Hamasaki, T.; Yoshii, T.; Yoshimi, M.; Takahashi, M.; Taniguchi, K.; Kashiwagi, M.; Tango, H.
VLSI Res. Center, Toshiba Corp., Kawasaki, Japan
Appl. Phys. Lett. (USA), Vol.47, No.7, 696-9, 1 Oct. 1985

Speeding lateral epitaxy for silicon films on an insulator, using pseudoline-shaped electron-beam annealing, has been investigated. Higher oscillation frequency, beam scanning velocity, and suitable oscillation amplitude were effective to achieve large uniform silicon-on-insulator (SOI) films with the aid of simulating temperature distribution in silicon substrate. Furthermore, improved seed with tapered edge and capping layer of tungsten/insulator were employed to obtain 300-μm by 1.3-mm single-crystal SOI films on a 1.3-μm SiO_2 layer. Stacked SOI devices were successfully fabricated with low-temperature planarization process. 218 ps/stage propagation-delay and 17 pJ power-delay product were obtained. *IN*

111). Solid Phase Epitaxy of UHV-Deposited Amorphous Si over Recessed SiO_2 Layer.
Tabe, M.; Kunii, Y.
Atsugi Electr. Commun. Lab., NTT Public Corp., Kanagawa, Japan
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 695-704, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

Lateral solid phase epitaxy (L-SPE) of ultra-high-vacuum (UHV) deposited amorphous Si (a-Si) over patterned SiO_2 has been studied to produce monocrystalline silicon-on-insulator (SOI) films. When employing UHV-deposited a-Si, it is essential for L-SPE to reduce step height at the pattern boundary. This is because low-density a-Si including columnar voids is formed at the step wall by the self-shadowing effects and the SPE region does not extend across the low-density a-Si area. L-SPE growth distance of 7 μm was achieved by low-temperature annealing (575°C, 20 h) on a planar substrate with recessed SiO_2 patterns. Another deposition technique of a-Si for SPE, i.e., chemical vapor deposition, is reviewed for comparison. *IN*

112). Characterization of Solid Phase Epitaxially Grown Si Films on SiO_2.
Tamura, M.; Miyao, M.; Tokuyama, T.; Yamamoto, H.; Ishiwara, H.
Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan.
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, 231-248, 1985.
Reidel, Dordrecht, Netherlands

Lateral solid phase epitaxial (L-SPE) films of vacuum-deposited Si on SiO_2 have been examined mainly through TEM observation, and compared with the case for (100) vertical solid phase epitaxial (V-SPE) films. Typical defects in L-SPE layers having a rough growth front are high-density twins and dislocations, the generation of which are independent of < 100 > and < 110 > laterally grown films. On the other hand, in V-SPE layers containing low-density short dislocations {111} facets are formed at the < 110 > directed oxide window edge. It is thought that this facet acts as a barrier for changing from V-SPE to L-SPE across the SiO_2 edge. Successive 1050°C high-temperature heat treatment generates interstitial type faulted and unfaulted dislocation loops in Si^+ ion-implanted V-SPE layers. This is in contrast to the reduced dislocation density resulting in L-SPE layers having no remaining amorphous regions after the first 600°C annealing. *IN*

113). Characterization of Solid-Phase Epitaxially-Grown Silicon Films on SiO_2.
Tamura, M.; Tokuyama, T.; Yamamoto, H.; Ishiwara, H.; Furukawa, S.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan;
Jpn. J. Appl. Phys. Part 1 (Japan), Vol.23, No.10, 1294-9, Oct. 1984

Lateral solid-phase epitaxial (L-SPE) films of vacuum-deposited Si on SiO_2 have been examined, mainly through TEM observation, and compared with (100) vertical solid-phase epitaxial (V-SPE) films. Typical defects in L-SPE layers with a rough growth front are high-density twins and dislocations, which are generated regardless of whether the films are (100) or (110) laterally-grown films. On the other hand, in V-SPE layers containing low-density short dislocations, (111) and (110) facets are formed at the (110) and (100) directed oxide window edges, respectively. The facets are thought to act as a barrier for the change from V-SPE to L-SPE across the SiO_2 edge. Successive 1050°C high-temperature heat treatment generates interstitial-type faulted and unfaulted dislocation loops in Si^+ ion implanted V-SPE layers. This is in contrast to the reduced dislocation density resulting in L-SPE layers containing no residual amorphous regions after the first 600°C annealing. *IN*

114). Solid Phase Processes for Semiconductor-on-Insulator.
Thompson, C.V.
Dept. of Mater. Sci. & Eng., MIT, Cambridge, MA.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984
Symposium, 711-19, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

A wide variety of techniques for producing device-quality semiconductor films on insulating substrates (SOI) is being studied. Processes which provide low defect density films at low temperatures and which do not require seeding from a single-crystal substrate would offer the greatest flexibility. While such processes do not currently exist, approaches based on crystallization of amorphous silicon or grain growth in polycrystalline silicon are being investigated. Development of either approach requires careful control of film properties and improved understanding of the fundamental materials processes involved. Theory and experiments on surface-energy-driven secondary grain growth (SEDSGG) are briefly reviewed. Controlled SEDSGG may provide a low-temperature means of obtaining low defect density films of a variety of materials on a common substrate. *IN*

115). Lateral Solid Phase Epitaxy of Evaporated Amorphous Si Films Onto SiO_2 Patterns.
Yamamoto, H.; Ishiwara, H.; Furukawa, S.; Tamura, M.; Tokuyama, T.
Dept. of Appl. Electron., Tokyo Inst. of Technol., Yokohama, Japan
Baglin, J.E.E.; Campbell, D.R.; Chu, W.K. (Editors)
Thin Films and Interfaces II. Proceedings of the Symposium, 511-16, 1984
14-18 Nov. 1983, Boston, MA.
North-Holland, New York.

Lateral solid phase epitaxy (L-SPE) of amorphous Si (a-Si) films vacuum-evaporated on Si substrates with SiO_2 patterns has been investigated, in which the film first grows vertically in the

regions directly contacted to the Si substrates and then grows laterally onto SiO_2 patterns. It has been found from transmission electron microscopy and Nomarski optical microscopy that use of dense a-Si films, which are formed by evaporation on heated substrates and subsequent amorphization by Si^+ ion implantation, is essentially important for L-SPE. The maximum L-SPE length of 5 to 6 μm was obtained along the (010) direction after 10-h annealing at 600°C. The kinetics of the L-SPE growth has also been investigated. *IN*

116). Lateral Solid Phase Epitaxy of Evaporated Amorphous Si Films Onto SiO_2 Patterns.
Yamamoto, H.; Ishiwara, H.; Furukawa, S.; Tamura, M.; Tokuyama, T.
Dept. of Appl. Electron., Tokyo Inst. of Technol., Yokohama, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 187-207, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Lateral solid phase epitaxy (L-SPE) of amorphous-Si (a-Si) films vacuum-evaporated on Si substrates with SiO_2 patterns has been investigated, in which the film first grows vertically in the regions directly contacted to the Si substrates and then grows laterally onto SiO_2 patterns. It has been found from transmission electron microscopy and Nomarski optical microscopy that use of dense a-Si films, which are formed by evaporation on heated substrates and subsequent amorphization by Si^+ ion implantation, is essentially important for L-SPE. The maximum L-SPE length of 5 to 6 μm was obtained along the (010) direction after 10-h annealing at 600°C. The kinetics of the L-SPE growth has also been investigated. *IN*

117). On the Mechanisms of Lateral Solid Phase Epitaxial Growth of Amorphous Si Films Evaporated on SiO_2 Patterns.
Yamamoto, H.; Ishiwara, H.; Furukawa, S.
Dept. of Appl. Electron., Tokyo Inst. of Technol., Yokohama, Japan
Jpn. J. Appl. Phys. Part 1 (Japan), Vol.24, No.4, 411-15, April 1985

Mechanisms of the lateral solid phase epitaxial (L-SPE) growth of amorphous Si films, which were vacuum-deposited on (100) Si substrates with SiO_2 patterns, are investigated using experimental data from cross-section transmission electron microscopy and other techniques, and results are compared with theory. In the case of the L-SPE growth along the (011) direction, it is concluded that the (111) facet is formed at the SiO_2 pattern edge during the vertical SPE stage and the L-SPE proceeds from the facet plane by microtwin-accelerated growth. For the growth along the (010) direction, it is found that the (110) facet plane is formed during the vertical SPE stage but changes to the folded (111) facet planes during the initial L-SPE growth. Growth models in the L-SPE along both directions are also presented. *IN*

118). Orientation Dependence of Lateral Solid-Phase-Epitaxial Growth in Amorphous Si Films.
Yamamoto, H.; Ishiwara, H.; Furukawa, S.
Dept. of Appl. Electron., Tokyo Inst. of Technol., Yokohama, Japan
Jpn. J. Appl. Phys. Part 1 (Japan), Vol.25, No.5, 667-72, May 1986

The characteristics of the lateral solid-phase-epitaxial (L-SPE) growth of undoped and p-doped amorphous Si (a-Si) films on SiO_2 patterns formed in various directions on (100) and (110) Si substrates were investigated. It was found that (1) the L-SPE growth length becomes a minimum in directions such that (111) facet planes can be formed parallel to the SiO_2 pattern edge and (2) the growth rates in these directions are constant. It was also found that the growth rates in other directions are faster in the initial stages of L-SPE, but decrease with the annealing time and reach the same saturated value as the above constant rate. The L-SPE growth rates were also compared with the growth rate of polycrystalline grains in p-doped a-Si films. *IN*

119). Device Characterization on Monocrystalline Silicon Grown over SiO_2 by the ELO (Epitaxial Lateral Overgrowth) Process.
Jastrzebski, L.; Ipri, A.C.; Corboy, J.F.
RCA Labs., Princeton, NJ.
IEEE Electron Device Lett. (USA), Vol.EDL-4, No.2, 32-5, Feb. 1983

MOS and lateral bipolar transistors have been fabricated on epitaxial silicon layers which have been laterally overgrown over SiO_2. These device characteristics were then compared to those measured on devices fabricated on homoepitaxial silicon and bulk silicon. The measurements indicate essentially identical MOS device characteristics for all three materials with a typical hole field-effect mobility of about $180 cm^2/V{\cdot}s$. Lifetime measurements using pulsed C-V techniques showed essentially the same values for ELO material and homoepitaxial material with the ELO value being about 20 μs for $10^{15} cm^{-3}$ doping level. These lifetime values correlate well with diode and bipolar transistor measurements. *IN*

120). Trench-Isolated Transistors in Lateral CVD Epitaxial Silicon-on-Insulator Films.
Kamins, T.I.; Bradbury, D.R.
Hewlett-Packard Labs., Palo Alto, CA.
IEEE Electron Device Lett. (USA), Vol.EDL-5, No.11, 449-51, Nov. 1984

Completely dielectrically isolated, p-channel MOS transistors have been obtained by lateral chemical vapor deposition epitaxial overgrowth of buried oxide layers and subsequent lateral isolation with refilled trenches. The transistor characteristics are similar to those in bulk control wafers. Isolation between the device island and the substrate is approximately $10^{12}\Omega$. *IN*

121). Dynamic Numerical Simulation of Melting and Resolidification Process in SOI Formation by Seeded Lateral Epitaxy.
Ohkura, M.; Ichikawa, M.; Miyao, M.; Sunami, H.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 503-6, 1984, 30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

Dynamic computer simulation of seeded lateral growth has been carried out, taking into account laser beam scanning and the melt/solidification process of the deposited poly-Si layer. Crystal growth direction over the SiO_2 layer was found to change depending on the thickness of the layer, with sufficient lateral growth occurring with a thicker SiO_2 layer. Lateral crystal growth velocity was estimated to be about 50 cm/s, which indicates the possibility of matching between beam scanning speed and growth velocity in obtaining large-area SOI structures. *IN*

122). Lateral Solid Phase Epitaxy of Silicon Over Oxide.
Roth, J.A.; Olson, G.L.; Hess, L.D.
Hughes Res. Labs., Malibu, CA.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium 431-42, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

The authors review recent progress in the growth of silicon-on-insulator films by lateral solid phase epitaxy. The temperature dependence of the rates of random crystallization and solid phase epitaxy are used to predict the maximum growth of Si over oxide achievable by this technique. Actual overgrowth distances of 10 μm obtained in UHV-deposited films are considerably less than the values predicted. Several possible causes of the difference between observed and predicted overgrowth are discussed. *IN*

123). Modeling of Interface Atomic Arrangement for Analysis of Solid Phase Epitaxy and Si-on-Insulator Structure.
Saito, T.; Ohdomari, I.
Sch. of Sci. & Eng., Waseda Univ., Tokyo, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 171-85, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

The authors have analyzed an atomic mechanism of solid phase epitaxy (SPE) by an amorphous Si/crystalline Si (a-Si/c-Si) interface model and Si-on-insulator structure by a c-Si/a-SiO_2 interface model. The a-Si/(100)c-Si interface model was constructed by building a continuous random network (CRN) model of a-Si on a (100)c-Si lattice. It consists of 121 atoms on the amorphous side and 230 atoms on the crystalline side. Using the interface model, they have quantitatively analyzed a bond rearrangement process (BRP) at the interface during SPE. They have studied a BRP based on the mechanism by Spaepen and Turnbull (1979). They have simulated nine steps of the BRP. The atomic coordinates at each step of the BRP have been calculated by the energy relaxation based on Keating potential. They have found that the atomic displacements during the BRP are smaller than Si-Si bond length. The BRP results in decrease in distortion energy mainly due to bond bending. The amount of decrease is in good agreement with the value evaluated by the experimental heat of crystallization. The c-Si/a-SiO_2 interface model has been constructed by connecting a c-Si lattice and a CRN model of a-SiO_2. It contains no dangling bonds and no SiO_2

transition region. They have found that the distortion of c-Si lattice is smaller in the c-Si/a-SiO_2 model than in the a-Si/c-Si interface model.

IN

124). Stress in Oxidized Porous Silicon Layers.
Barla, K.; Herino, R.; Bomchil, G.
Cent. Natl. Etud. Telecommun., CNS, Meylan, France
J. Appl. Phys., Vol. 59, No. 2, 439-41, 1986

Stress was determined in oxidized porous Si layers using x-ray diffraction to measure the substrate curvature. Stress is always compressive and its magnitude depends on oxide quality. The maximum value is reached when the oxide obtained from porous Si is densified by a high-temperature process and is equivalent to standard thermal SiO_2. The stress magnitude decreases when oxide porosity increases. An increase in layer thickness is always observed when oxidation conditions lead to a porous oxide or when the initial porosity of the layer is <56%, due to volumic expansion of SiO_2 relative to Si; otherwise the thickness decreases. *CA*

• 125). Dielectric Isolation Using Porous Silicon.
Baumgart, H.; Frye, R.C.; Phillipp, F.; Leamy, H.J.
Philips Lab., New York, NY.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 63-8, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

The fabrication of silicon-on-insulator structures was examined utilizing epitaxial growth of Si films on porous silicon and subsequent enhanced oxidation of the porous substrate. Porous silicon films have been formed by local anodic dissociation of silicon wafers in HF, while retaining the single crystalline structure. Low-temperature liquid phase epitaxy (LPE) from saturated Ga solutions as well as molecular beam epitaxy (MBE) and laser-induced epitaxy have been studied. Transmission electron microscopy (TEM) has demonstrated that all three techniques can achieve crystalline Si film growth on porous silicon. Surface smoothness and crystal perfection of the resulting epitaxial layers vary considerably with each technique. *IN*

• 126). Large Area, Uniform Silicon-on-Insulator Using a Buried Layer of Oxidized Porous Silicon.
Benjamin, J.D.; Keen, J.M.; Cullis, A.G.; Innes, B.; Chew, N.G.
R. Signals & Radar Establ., Great Malvern, England
Appl. Phys. Lett. (USA), Vol.49, No.12, 716-18, 22 Sept. 1986

The authors describe a process for the formation of silicon-on-insulator structures by selective anodization of a buried p-type layer to form porous silicon which is then oxidized. A buried n-type layer ensures that the flow of the anodizing current, and hence the formation of the porous silicon layer, is directed laterally rather than downwards. By this means they have produced defect-free, 200-nm thick and 40-μm wide silicon strips extending across the full width of device wafers and resting on 800 nm of silicon dioxide. This approach, which shows considerable promise for further enhancement, gives continuous large areas of high-quality isolated silicon with minimal wafer warpage compared with most existing silicon-on-silicon dioxide technologies. *IN*

127). The Formation of Porous Silicon and its Applications to Dielectric Isolation.
Frye, R.C.
AT&T Bell Labs., Murray Hill, NJ.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 53-62.
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Porous silicon is formed by the anodic dissolution of p-type silicon in aqueous hydrofluoric acid. Because of its very high porosity, this material can be rapidly oxidized to form thick (approximately 10-μm) oxide layers with minimal stress on the underlying silicon wafer. A remarkable property of porous silicon is that it preserves the crystalline orientation of the substrate despite removal of more than half of the silicon in the etched region, providing a suitable surface for the growth of epitaxial layers. Several schemes for dielectric isolation have been suggested which take advantage of these unique properties. The mechanism of porous silicon formation is presented and the relative advantages and disadvantages for practical device applications are discussed. *IN*

128). New Silicon-on-Insulator Technology Using a Two-Step Oxidation Technique.
Lin, T. L.; Wang, K. L.
Dep. Electr. Eng., Univ. California, Los Angeles, CA
Appl. Phys. Lett., Vol. 49, No. 17, 1104-6, 1986

Large Si-on-insulator (SOI) structures were obtained using a new two-step oxidation technique on a Si epitaxial film grown onto a porous Si sample. The first low-temperature oxidation step oxidizes the large-pore Si underlayer to avoid the collapse of the porous structure and thus secure the lateral O supply channels in the porous oxide. In the second step, a higher temperature is used to oxidize the remaining porous Si and the bottom part of the Si MBE overlayer with the O supplied through the oxidized porous Si layer which has a smaller porosity for the ease of subsequent Si epitaxial growth, and a second layer with a larger porosity which not only gives O supply channels during the SOI oxidation but also allows the volume expansion of the porous Si oxide to be accommodated. SOI sizes of 325 μm by 2 mm were successfully fabricated. The breakdown voltage of the SOI structures is ~400 V, and the leakage current densities between the SOI layer and the substrate are <3 nA cm^{-2} with a 10-V bias. N-channel MOSFETs were fabricated on the SOI structures with good characteristics, indicating that this technology may be suitable for VLSI circuits applications. *CA*

• 129). Crystalline Quality of Silicon Layer Formed by FIPOS Technology.
Imai, K.; Unno, H.; Takaoka, H.
Musashino Electrical Communication Lab., NTT Public Corp., Tokyo, Japan
J. Cryst. Growth (Netherlands), Vol.63, No.3, 547-53, Oct. 1983

The crystalline quality and electrical characteristics of isolated silicon layers fabricated by the FIPOS (Full Isolation by Porous Oxidized Silicon) technology have been studied. Transmission electron microscopy (TEM) was used to evaluate the crystalline quality and CMOS devices were used to determine the electrical characteristics of the isolated layers. Dislocations are generated in the isolated layers. These dislocations are caused by the thermal stresses present in the thick porous silicon layer during the oxidation process. Lowering the porous silicon density is effective in reducing the density of dislocations. The density of dislocations is two or three orders of magnitude lower than that in the silicon-on-sapphire (SOS) or in the epitaxial layer of the oxygen-implanted silicon. The field-effect mobility of n- and p-channel MOSFETs in the isolated silicon layer is the same as that in bulk silicon. The drain leakage currents of n- and p-channel MOSFETs are on the order of $10^{-13} to 10^{-14}$ A per 6.5-μm channel width. *IN*

• 130). FIPOS (Full Isolation by Porous Oxidized Silicon) Technology and Its Application to LSIS.
Imai, K.; Unno, H.
NTT Public Corp., Tokyo, Japan.
IEEE Trans. Electron Devices (USA) Vol.ED-31, No. 3, 297-302, March 1984.

FIPOS technology realizes a silicon-on-insulator structure, utilizing thick porous oxidized silicon and donors produced by proton implantation. New processing steps are proposed which provide small surface steps and are suitable for LSI fabrication. Formation conditions of thick porous oxidized silicon are established. CMOS devices are fabricated in isolated silicon layers and it is

shown that the characteristics of n-channel and p-channel MOSFETs are sufficient for application to CMOS LSIS. A FIPOS/CMOS logic array with 1.3 K gates is successfully fabricated, which shows a higher speed and lower power dissipation than the gates fabricated by bulk CMOS technology. *IN*

131). A New Silicon-on-Insulator Structure Using a Silicon Molecular Beam Epitaxial Growth on Porous Silicon.
Konaka, S.; Tabe, M.; Sakai, T.
Musashino Electrical Communication Lab., NTT Public Corp., Tokyo, Japan
Appl. Phys. Lett. (USA), Vol.41, No.1, 86-8, 1 July 1982

A new silicon-on-insulator (SOI) structure has been achieved by utilizing silicon molecular beam epitaxial (Si-MBE) growth on porous silicon, silicon island patterning, and the subsequent laterally enhanced oxidation of the porous silicon. The surface of Si-MBE film grown on porous silicon at 770°C without high-temperature preheating has a 7 by 7 superlattice structure when observed by a reflection high-energy electron diffraction (RHEED). Patterned Si-MBE film island, that is 7.0 μm wide and 0.35 μm thick, is successfully isolated by the laterally enhanced oxidation of porous silicon. *IN*

132). Advances in Oxidized Porous Silicon for SOI.
Nesbit, L.A.
IBM Gen. Technol. Div., Essex Junction, VT.
International Electron Devices Meeting, Technical Digest, 800-3, 1984
9-12 Dec. 1984, San Francisco, CA.
IEEE, New York.

The formation of a silicon-on-insulator (SOI) structure for VLSI applications by means of oxidized porous silicon (OPS) is attractive for both materials and device reasons. Despite these advantages, SOI by OPS may be liable to various processing constraints. These constraints include (a) limited silicon island size and geometry, (b) wafer warpage due to oxidation of the porous silicon, and (c) defects in the silicon islands that form during oxidation of the porous silicon. A process is presented which minimizes the first two problems and results in no observable defects in the silicon islands. Also, some preliminary device results are given from FETs fabricated in an SOI structure formed by OPS. *IN*

133). Defect-Free Silicon on Insulator by Oxidized Porous Silicon.
Nesbit, L.A.
IBM Corp., Armonk, NY.
IBM Tech. Disclosure Bull.(USA), Vol. 27, No. 8, 4632-3, Jan. 1985.

High-pressure oxidation can be used with oxidized porous silicon (OPS) techniques to produce defect-free, low warpage thin silicon-on-simulator (SOI) structures. *IN*

• 134). Porous Silicon Layers and Its Oxide for the Silicon-on-Insulator Structure.
Takai, H.; Itoh, T.
Sch. of Sci. & Eng., Waseda Univ., Tokyo, Japan
J. Appl. Phys. (USA), Vol.60, No.1, 222-5, 1 July 1986

Crystalline properties of Si films grown on porous Si layers were investigated. Based on the results obtained by Rutherford backscattering spectroscopy and cross-sectional transmission electron microscopy, a model of Si epitaxial growth on a porous Si layer is proposed. In the model, dominant defects in the region near the epitaxial layer/porous Si interface and in the one near the surface in the epitaxial layer are dislocations and stacking faults, respectively. The oxidation rate of the porous Si layers is about 80 to 130 times faster than that of the bulk Si, and the etching rate of the oxidized porous Si layers is almost equal to that of the bulk oxide. The effective dielectric constants of the oxidized porous Si layers have a close relation to the anodic current density, ranging from 3.8 to 4.0. *IN*

• 135). Silicon MBE: From Strained-Layer Epitaxy to Device Application.
Bean, J.C.
AT&T Bell Labs., Murray Hill, NJ.
J. Cryst. Growth (Netherlands), Vol.70, No.1-2, 444-51, Dec. 1984
Sixth International Conference on Vapor Growth and Epitaxy and Sixth American Conference on Crystal Growth, 15-20 July 1984, Atlantic City, NJ.

During the late 1970s, work in silicon MBE focused on optimal growth conditions, introduction of dopants, and film quality. This work yielded layers with qualities comparable to CVD epitaxy: zero stacking fault density line dislocation densities to 100-cm^2 bulk mobilities, minority carrier lifetimes to 100 μs, DLTS trap densities $< 10^{14} cm^2$, oxide interface state densities approximately $5 \times 10^{10} cm^2 \cdot V$. Investigators have since moved on to a variety of heteroepitaxial systems including silicon and insulator (Al_2O_3, $MgAl_2O_4$, ZrO_2, and CaF_2), silicon and metal (NiS_2 and $COSi_2$), and most recently, silicon and semiconductor (Ge and GaP). Work has now moved from MBE growth of discrete device structures to growth of both fully integrated structures and structures unique to the MBE process. *IN*

136). Silicon-MBE SOI.
Lin, T.L.; Chen, S.C.; Wang, K.L.; Iyer, S.
Dep. Electr. Eng., Univ. California, Los Angeles, CA
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 193-7, 1986

100-μm wide Si-on-insulator (SOI) structures were accomplished by utilizing Si molecular beam epitaxial (Si-MBE) growth on porous Si and subsequent lateral-enhanced oxidation of porous Si through pattern windows. A Si beam method was used for in-situ cleaning of the Si surface at 750°C, and the effectiveness of this method was demonstrated by using Auger electron spectroscopy and checked by determining the etch-pit density of the grown film. A two-step growth process of Si MBE was used to grow epitaxial layers of high quality. An electron mobility of 1300 cm$\cdot V^{-1} s^{-1}$ was obtained from van der Pauw measurements. *CA*

137). Si-MBE SOI Device and Circuits.
Lin, T.L.; Wang, K.L.; Iyer, S.
Dept. of Electr. Eng., California Univ., Los Angeles, CA.
Bean, J.C.; Iyer, S.S.; Kasper, E.; Shiraki, Y. (Editors)
Proceedings of the First International Symposium on Silicon Molecular Beam Epitaxy, 316-22, 1985, 14-17 May 1985, Toronto, Ont., Canada
Electrochem. Soc., Pennington, NJ.

A 100-μm wide silicon-on-insulator (SOI) structure has been achieved by utilizing silicon molecular beam epitaxial (Si-MBE) growth and porous oxidized silicon. A Si beam with flux density of $7.8 \times 10^{13} cm^{-2} s^{-1}$ was used to clean the sample surface at 750°C prior to MBE growth. The MBE Si film growth on porous Si at 750°C by a two-step growth process shows good crystallinity when checked by Rutherford backscattering spectroscopy (RBS) and transmission electron microscopy (TEM). SOI MOSFETs were successfully fabricated. *IN*

138). 100-μm-wide Silicon-on-Insulator Structures by Si Molecular Beam. Epitaxy Growth on Porous Silicon
Lin, T.L.; Chen, S.C.; Kao, Y.C.; Wang, K.L.; Iyer, S.
Dept. of Electr. Eng., California Univ., Los Angeles, CA.
Appl. Phys. Lett. (USA), Vol.48, No.26, 1793-5, 30 June 1986

100-μm silicon-on-insulator structures have been achieved by first utilizing silicon molecular beam epitaxial (Si MBE) growth on porous silicon and subsequently oxidizing the porous silicon through

the patterned Si MBE film windows. A Si beam method is used for the low-temperature surface cleaning of porous silicon prior to Si MBE growth. By using a two-step growth technique, the Si MBE film shows good crystallinity checked by Rutherford backscattering channeling spectroscopy and cross-sectional transmission electron microscopy. An electron mobility of 1300 $cm^2\ V^{-1}{}_s{}^{-1}$ with a doping concentration of $6 \times 10^{15} cm^{-3}$ has been achieved. *IN*

139). Si-Gate CMOS Devices on a $Si/CaF_2/Si$ Structure.
Onoda, H.; Katoh, T.; Hirashita, N.; Sasaki, M.
OKI Electr. Ind. Co. Ltd., Tokyo, Japan
International Electron Devices Meeting, Technical Digest, 680-3, 1985
1-4 Dec. 1985, Washington, DC.
IEEE, New York.

A heteroepitaxial $Si/CaF_2/Si$ structure has been formed by molecular bean epitaxy (MBE), and Si-gate CMOS integrated circuits (100-stage inverter chains and 1/8 dynamic frequency dividers) have been successfully fabricated on that structure for the first time. For device fabrication, an improved CMOS process has been developed. Low-temperature processes (maximum 950°C) have been chosen in order not to degrade the crystalline quality of the overgrown Si. The fabricated circuits have an inverter delay of 360 ps per stage at V_{DD}=5 V, and a maximum divider frequency of 370 MHz at V_{DD}=7 V. *IN*

140). Formation of SOI-GaAs on $(Ca,Sr)F_2/GaAs$ Structures.
Tsutsui, K.; Lee, H.C.; Ishiwara, H.; Asano, T.; Furukawa, S.
Grad. Sch. of Sci. & Eng., Tokyo Inst. of Technol., Yokahama, Japan
Fujimoto, M. (Editor)
Gallium Arsenide and Related Compounds 1985. Proceedings of the Twelfth International Symposium, 109-14, 1986, 23-26 Sept. 1985, Karuizawa, Japan
Adam Hilger, Bristol, England

$GaAs/Ca_{0.43}/Sr_{0.57}F_2/GaAs$ ((100) and (111)) SOI structures were fabricated using MBE growth. The SOI-GaAs layers were investigated by He ion channeling and backscattering spectroscopy (RBS) and Nomarski optical microscope. It was found that the temperature dependences of the crystalline quality and the surface morphology were different between the layers on (100) and (111) substrates. The channeling minimum yield (χ_{min}) of 5.5% was obtained in a layer grown on the (111) substrate using a two-step growth technique. *IN*

8. SILICON ON CALCIUM FLUORIDE, CUBIC ZIRCONIA, GARNET, AND MAGNESIUM OXIDE

141). Fabrication of MOSFETs in $Si/CaF_2/Si$ Heteroepitaxial Structures.
Asano, T.; Kuriyama, Y.; Ishiwara, H.
Graduate Sch. of Sci. & Eng., Tokyo Inst. of Technol., Yokohama, Japan
Electron. Lett. (GB), Vol. 21, No. 9, 386-7, 25 April 1985

Aluminium-gate n-channel MOSFETs have been fabricated in $Si/CaF_2/Si$ heteroepitaxial silicon-on-insulator structures. The MOSFETs were fabricated by a process including thermal oxidation in wet oxygen ambient for the formation of the gate oxide. The maximum field-effect electron mobility as high as 580 $cm^2V \cdot s$ was obtained. *IN*

142). Low Temperature Fabrication of SOI-MOSFETs in $Si/CaF_2/Si$ Heteroepitaxial Structures.
Asano, T.; Wakabayashi, S.; Ishiwara, H.
Graduate Sch. of Sci. & Eng., Tokyo Inst. of Technol., Yokohama, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 519-22, 1984, 30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

The epitaxial growth of Si films on CaF_2/Si heteroepitaxial structures and characteristics of MOSFETs fabricated in the $Si/CaF_2/Si$ structures are investigated. Both the growth of the $Si/CaF_2/Si$ structures and the fabrication of MOSFETs are performed at temperatures below 800°C. For the growth of Si films, a new growth method, which involves in-situ deposition of a thin ($\leq 10nm$) Si onto the CaF_2 surface at room temperature prior to deposition of Si at elevated temperatures, has been developed in order to prevent interfacial reaction between deposited Si and underlying CaF_2. Al gate n-channel MOSFETs, which are electrically isolated from the substrates, have been fabricated by utilizing plasma-enhanced CVD SiO_2 as the gate insulator. The maximum field-effect mobility of about 180 $cm^2V \cdot s$ has been obtained. *IN*

143). Silicon-on-Insulator Technology by Heteroepitaxial Growth of Fluorides.
Farrow, R.F.C.
Almaden Res. Cent., IBM, San Jose, CA
Proc. SPIE-Int. Soc. Opt. Eng., 623(Adv. Process. Charact. Semicond. 3), 175-82, 1986 *CA*

144). Integration of Semiconductor and Magnetic Bubble Devices: SOI on Garnet.
Greve, D.W.; Kryder, M.H.; Rasky, P.H.L.
Dep. Electr. Comput. Eng., Carnegie-Mellon Univ., Pittsburgh, PA
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 375-82, 1986

Si-on-insulator (SOI) technology is used for a process in which field-effect transistors are fabricated in recrystallized polysilicon on a magnetic bubble substrate. The characteristics of the field-effect transistors and the effect of the necessary processing steps on the magnetic properties of the substrate are presented. A memory constructed in this hybrid technology would have very high density, multiple detectors for high speed, and direct logic level outputs. *CA*

• 145). Characteristics of MOSFET Prepared on $Si/MgO{:}Al_2O_3SiO_2Si$ Structure.
Hokari, Y.; Mikami, M.; Egami, K.; Tsuya, H.; Kanamori, M.
NEC, Kanagawa, Japan
IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 1, 173-177, Feb. 1985

A new silicon-on-insulator (SOI) wafer with epitaxial-Si/epitaxial- $MgO:Al_2O_3(0.1\mu m)/SiO_2(0.5\mu m)$-/(100)Si structure has been developed. The present structure has such advantages as (1) low parasitic capacitance and high-voltage tolerance between the top silicon layer and bulk silicon by using a thick SiO_2 film and (2) freedom from strain in the top silicon layer. An n-channel MOSFET (W/L = 100/100μm, t_{ox} = 300 Å) was prepared successfully on the present SOI wafers with 0.6- to 3-μm thick top silicon epitaxial layer. MOSFET static characteristics were evaluated and compared with those observed in the FETs prepared on conventional silicon on sapphire (SOS) and bulk silicon wafers. Channel electron mobility showed higher values for thicker silicon films. The highest value of 440 cm^2/V-s was obtained for a 3-μm thick top silicon layer. This value was 20% greater than that obtained for an SOS wafer (370 cm^2/V-s), though the value was slightly inferior to that for bulk Si (550 cm^2/V-s). Tailing factor and p-n junction leakage current obtained for 3-μm thick silicon layer were almost the same as those for SOS FETs. It is concluded that the new SOI wafer with an over 3-μm thick silicon layer is quite promising for realizing SOI devices. *EI*

146). Characteristics of MOSFET Prepared on $Si/MgO.Al_2O_3SiO_2Si$ Structure.
Hokari, Y.; Mikami, M.; Egami, K.; Tsuya, H.; Kanamori, M.
VLSI Dev. Div., NEC Corp., Kanagawa, Japan
IEEE Trans. Electron Devices (USA), Vol.ED-32, No.2, 253-7, Feb. 1985

A new silicon-on-insulator (SOI) wafer with epitaxial-Si/epitaxial-$MgO:Al_2O_3$(0.1 μm)/SiO_2(0.5 μm)/(100)Si structure has been developed. The present structure has been developed. The present structure has such advantages and (1) low parasitic capacitance and high-voltage tolerance between the top silicon layer and bulk silicon by using a thick SiO_2 film and (2) freedom from strain in the top silicon layer. An n-channel MOSFET (W/L=100/100 μm, T_{ox} = 300 Å) was prepared successfully on the present SOI wafers with 0.6- to 3-μm thick top silicon epitaxial layer. MOSFET static characteristics were evaluated and compared with those observed in the FETs prepared on conventional silicon on sapphire (SOS) and bulk silicon wafers. Channel electron mobility showed higher values for thicker silicon films. The highest value of 440 $cm^2V{\cdot}s$ was obtained for a 3-μm thick top silicon layer. This value was 20% greater than that obtained for an SOS wafer (370 $cm^2V{\cdot}s$), though the value was slightly inferior to that for bulk Si (550 $cm^2V{\cdot}s$). Tailing factor and p-n junction leakage current obtained for 3-μm thick silicon layer were almost the same as those for SOS FETs. It is concluded that the new SOI wafer with an over 3-μm thick silicon layer is quite promising for realizing SOI devices. *IN*

147). Vapor Phase Epitaxial Growth of Silicon on Insulating Material on Silicon.
Ihara, M.
Fujitsu Lab. Ltd., Atsugi, Japan
Oyo Buturi (Japan), Vol.53, No.1, 28 Jan. 1984

A silicon-on-insulator technique using a vapor-phase epitaxial method and vacuum deposition method is described which is capable of a high-quality silicon single-crystal silicon active layer on a single-crystal insulator. The method can construct a $Si/MgO-Al_2/O_3/Si$ structure having a high-quality silicon active layer suitable for use as a bipolar IC material. *IN*

148). Formation of Epitaxial SOI Structures Using Alkaline Earth Fluoride Films.
Ishiwara, H.; Asano, T.
Grad. Sch. Sci. Eng., Tokyo Inst. Technol., Yokohama, Japan
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 129-36, 1986

This report reviews recent research on heteroepitaxial Si-on-insulator (SOI)-type structures such as $SiCaF_2Si$ and $GeCaF_2Si$ structures. Structural and electrical properties of an alkaline earth fluoride films on Si substrates are discussed. Growth conditions, structural properties, and device applications of the $SiCaF_2Si$ structures are presented. *CA*

149). Si on Cubic Zirconia.
Manasevit, H.M.; Golecki, I.; Moudy, L.A.; Yang, J.J.; Mee, J.E.
Microelectronics Res. and Dev. Center, Rockwell Internat., Anaheim, CA.
J. Electrochem. Soc. (USA), Vol.130, No.8, 1752-8, Aug. 1983

Epitaxial growth of single-crystal Si films has been realized on the (100), (110), and (111) crystallographic planes of yttria-stabilized, cubic zirconia single crystals. The Si films were grown by chemical vapor deposition, using the pyrolysis of SiH_4 at temperatures in the range 950 to 1075°C and at deposition rates of 0.08 to 1.2 μm/min. A predeposition annealing procedure has been developed, resulting in a quasi-stable, oxygen-deficient zirconia surface. A model is presented to explain the dependence of oxygen kinetics in cubic zirconia on temperature and yttria content. The heteroepitaxial Si films have been characterized by optical and scanning electron microscopies, reflection electron diffraction, x-ray diffraction, Rutherford backscattering and channeling, and surface electrical conductivity and Hall effect measurements. Several 0.4- to 0.5-μm thick (100)- and (110)-oriented Si films on cubic zirconia were found to be of higher crystal quality than commercial (100) Si on sapphire films of similar thickness. *IN*

150). Formation of Si Epi./$MgO>Al_2/O_3$ Epi./SiO_2/Si and Its Epitaxial Film Quality.
Mikami, M.; Hokari, Y.; Egami, K.; Tsuya, H.; Kanamori, M.
NEC Corp., Kawasaki, Japan
Extended Abstracts of the 15th Conference on Solid State Devices and Materials, 31-4, 1983, 30 Aug.-1 Sept. 1983, Tokyo, Japan
Japan Soc. Appl. Phys., Tokyo, Japan

A new type silicon-on-insulator with $Si/MgO>Al_2/O_3/SiO_2/Si$ structure has been developed. An $MgO>Al_2/O_3$ (spinel) epitaxial film is grown on a (100) Si substrate by chemical vapor deposition. Amorphous SiO_2 is formed by thermal oxidation of the Si substrate through spinel film. The Si epitaxial film is grown on $MgO>Al_2/O_3/SiO_2/Si$ by SiH_4 pyrolysis. A strain-free Si epitaxial film is attained. The Si film crystalline quality evaluated by the x-ray rocking curve is equivalent to that in SOS. *IN*

151). Silicon-on-Insulator Heterostructures.
Poate, J. M.
AT&T Bell Lab., Murray Hill, NJ
Simonne, J.J.; Buxo, J. (Editors)
Insul. Films Semicond., Proc. Int. Conf. INFOS 85, Meeting Date 1985, 41-8,
North-Holland: Amsterdam, Neth., 1986 *CA*

9. POLYSILICON

Comprehensive Treatment

152). SOI Edge Parasitics and Their Couplings.
Chen, C.-E.
Texas Instruments Inc, Dallas, TX
IEEE Transactions on Electron Devices, Vol. ED-33, No. 11, 44th Annual Device Res. Conf., Amherst, MA, June 23-25, 1986, 1843 *EI*

153). Polysilicon Super-Thin-Film Transistor (SFT).
Hayashi, H.; Noguchi, T.; Oshima, T.
Semicond. Group, Sony Corp., Atsugi, Japan
Jpn. J. Appl. Phys. Part 2 (Japan), Vol.23, No.11, L819-20, Nov. 1984

N-channel MOS FETs have been fabricated in super-thin polysilicon film on quartz substrates. The thickness of the film had an important role in improving the electrical properties. Moreover, grain boundary passivation by the hydrogen from a plasma-SiN film has been developed to increase the field-effect mobility. The field-effect mobility is more than 20 $cm^2/V{\cdot}s$ at the polysilicon thickness of 150 to 200 Å, and threshold voltage and leakage current are reduced to 6 V and $10^{-13} A/\mu m$, respectively. The device obtained in this work can be used not only for flat panel matrix displays but also for other applications. *IN*

154). Thermal Annealing Behaviour of Si/SiO_2 Structures.
Lifshits, V.G.; Kaverina, I.G.; Korobtsov, V.V.; Saranin, A.A.; Zotov, A.V.
Inst. of Autom. & Control Processes, Acad. of Sci., Vladivostok, USSR
Thin Solid Films (Switzerland), Vol.135, No.1, 99-105, 2 Jan. 1986
Sixth International Conference on 'Thin Films', 13-17 Aug. 1984, Stockholm, Sweden

The interaction of vacuum-deposited silicon films with the underlying oxide at annealing temperatures of 1050 to 1250°C was studied by means of low-energy electron diffraction, Auger spectroscopy, IR spectroscopy, and optical and electron microscopy. The deposition of silicon onto SiO_2-covered silicon substrates and the annealing of the samples were carried out in ultrahigh vacuum. The results obtained revealed that the silicon and oxide layers are etched away by heat treatment. The dependence of the etching on the thickness of the silicon film, the thickness of the SiO_2 layer, and the annealing temperature was determined. A qualitative model of the etching process is proposed. *IN*

155). Enhanced Leakage Current Due to a High-Gain Stray Bipolar Transistor in Accumulation-Mode SOI MOSFET's.
Madan, S.
MIT, Cambridge, MA
IEEE Transactions on Electron Devices, Vol. ED-32, No. 11, Nov 1985, 43rd Annual Device Res. Conf., Boulder, CO, June 17-19, 1985, 2549-2550 *EI*

156). Leakage Current Mechanisms in Hydrogen-Passivated Fine-Grain Polycrystalline Silicon on Insulator MOSFETs.
Madan, S.K.; Antoniadis, D.A.
Dept. of Electr. Eng. & Comput. Sci., MIT, Cambridge, MA.
IEEE Trans. Electron Devices (USA), Vol.ED-33, No.10, 1518-28, Oct. 1986

The action of a parasitic bipolar transistor that can amplify the leakage current due to the thermally generated carriers has been confirmed and characterized. A current gain (β) of more than 6 for the parasitic bipolar transistor has been measured in accumulation-mode devices, in spite of the

presence of a large number of defects. This high gain is attributed to the presence of the vertical electric field which separates the carriers, thus reducing the probability of recombination. The presence of field-enhanced generation is shown to be the cause of the observed increase in the leakage current with positive front or back-gate bias for p-channel accumulation-mode devices. Reasonable agreement has been obtained between experimental data and theory based on field-enhanced generation due to Poole-Frenkel barrier lowering. *IN*

157). Polysilicon Grain Growth by Rapid Isothermal Annealing.
Pinizzotto, R.F.; Clark, F.Y.; Malhi, S.D.D.; Shah, R.R.
Ultrastructure Inc., Richardson, TX.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 169-78, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

One method of reducing the area occupied by a RAM cell is to stack the p- and n-channel devices on top of one another. This 'stacked CMOS' structure is a first step towards three-dimensional integration. The simplest approach is to use polysilicon as the substrate for the top transistors. The authors describe the results of grain growth studies of samples annealed by rapid isothermal annealing. The temperature varied from 1100 to 1400°C and the anneal time varied from 10 to 480 s. TEM was used to examine the microstructure of the material. The grain growth was found to be film thickness limited; i.e., the final growth size was approximately the same as the initial film thickness. As a result, the kinetics of grain growth cannot be described by a simple logarithmic time law. There also is a velocity dependent drag contribution to the growth kinetics that implies impurities play an important role. Thicker oxides lead to faster growth, probably by reducing the heat flow to the silicon substrate. A capping layer was found to have no effect on the grain size. The above results indicate that it is possible to obtain large grains in short times using isothermal annealing. This process may be useful for fabricating stacked polysilicon layers in three-dimensional integrated circuits. *IN*

158). Comparison of Different Techniques for Passivation of Small-Grain Poly-Si MOSFET's.
Rodder, M.; Madan S.
MIT, Cambridge, MA
IEEE Transactions on Electron Devices, Vol. ED-32, No. 11, Nov. 1985, 43rd Annual
Device Res. Conf., Boulder, CO, June 17-19, 1985, 2548-2549 *EI*

159). Effects of Grain Boundaries on the Channel Conductance of SOI MOSFETs.
Fossum, J.G.; Ortiz-Conde, A.
Dept. of Electrical Engng., Univ. Of Florida, Gainesville, FL.
IEEE Trans. Electron Devices (USA), Vol.ED-30, No.8, 933-40, Aug. 1983

A physical model that describes the effects of grain boundaries on the linear-region (strong-inversion) channel conductance of SOI (polysilicon on silicon-dioxide) MOSFETs is developed and supported experimentally. The model predicts an effective turn-on characteristic that occurs beyond the strong-inversion threshold, and henceforth defines the 'carrier mobility threshold voltage' and the effective field-effect carrier mobility in the channel, which typically is higher than the actual (intragrain) mobility. These parameters, which are defined by the properties of the grain boundaries, can easily be misinterpreted experimentally as the threshold voltage and the actual carrier mobility. *IN*

160). Effects of Grain Boundaries on Channel Conduction in Thin Film Polysilicon On Silicon-Dioxide Metal Oxide Semiconductor Field Effect Transistors (SOI MOSFETs).
Fossum, J.G.; Ortiz, A.; Lim, H.-K.; Lam, H.-W.
Dept. of Electrical Engng., Univ. Of Florida, Gainesville, FL.
Proc. Spie Int. Soc. Opt. Eng. (USA), Vol.385, 65-75
Laser Processing of Semiconductor Devices, 18-19 Jan. 1983
Los Angeles, CA.

A physical model that describes the effects of grain boundaries on the linear-region, strong-inversion channel conductance of SOI (polysilicon on silicon-dioxide) MOSFETs is developed and is supported by measurements of laser-recrystallized devices. The model predicts an effective turn-on characteristic that occurs beyond the strong-inversion threshold, and henceforth defines the 'carrier mobility threshold voltage' and the effective (transconductance) carrier mobility in the channel, which typically is higher than the actual (intragrain) mobility. These parameters, which are defined by the properties of the grain boundaries, can easily be misinterpreted experimentally as the threshold voltage and the actual carrier mobility. The actual threshold voltage is defined by the charge coupling between the front and back gates of the thin-film transistor. This coupling is discussed and a closed-form expression for the threshold voltage, which depends on the back-gate bias and on the properties of the back Si-SiO_2 interface, is given. *IN*

161). Effects of Grain Boundaries on the Current-Voltage Characteristics of SOI MOSFETs.
Fossum, J.G.; Ortiz-Conde, A.
Dept. of Electr. Eng., Florida Univ., Gainesville, FL.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 199-206
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

A physical model that describes the steady-state current-voltage characteristics of field-effect transistors (MOSFETs) fabricated in (poly)silicon-on-insulator (SOI) is described. The model predicts that a single high-angle grain boundary, especially one traversing the channel near the drain, can control the conduction properties of the MOSFET for all (weak-to-strong) inversion conditions in all (linear-to-saturation) regions of operation. *IN*

162). Scaling of SOI/PMOS Transistors.
Singh, H.J.; Saraswat, K.C.; Shott, J.D.; McVittie, J.P.; Meindl, J.D.
Integrated Circuits Lab., Stanford Univ., Stanford, CA.

International Electron Devices Meeting 1983, Technical Digest, 67-70, 1983
5-7 Dec. 1983, Washington, DC.
IEEE, New York.

Results are reported from a study including the weak inversion behavior of p-channel MOS transistors fabricated in polycrystalline silicon. The devices have a wide range of channel dopings, with channel lengths and widths down to 1.25 μm. The use of very thin polysilicon enables the gate to modulate the channel conductivity of devices in fine-grain polysilicon with gate voltage excursions of under 5 V. The devices have a slow turn-on and exhibit an extended weak-inversion region. Weak-inversion currents increase with applied drain voltages up to about 5 V, with long-channel devices also showing this phenomenon. Short-channel effects are seen as the channel length approaches 2 μm and are mitigated by using a higher channel doping. Device currents drop sharply below a channel width of 2 μm, although the narrow-width effect is not as pronounced as the short-channel effects. *IN*

10. RECRYSTALLIZATION TECHNIQUES

GENERIC

Comprehensive Treatment

163). Optically-Heated Zone Crystal Growth of Silicon Thin Films on Amorphous Substrates.
Biegelsen, D.K.; Hawkins, W.G.; Fennell, L.E.; Johnson, N.M.; Moyer, M.D.
Xerox Palo Alto Res. Center, CA.
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 129-36, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

The authors review the current understanding of issues relevant to the crystallization of silicon thin films on amorphous substrates. They treat in particular the case of radiant heating (e.g., lasers, lamps, strip-heaters, etc.). Semiconducting silicon becomes metallic and more highly reflecting on melting. Therefore, there is a natural negative feedback mechanism associated with optical coupling to the film. This results in inhomogeneous melting, which in turn leads to several very beneficial, as well as mildly deleterious, consequences for crystal growth. On the positive side, the melting process is stabilized (robust) and texturing (specific crystal planes lying parallel to the substrate) occurs readily. On the other hand, undercooling is prevalent and can lead to growth instabilities. They describe a model for the phenomena of texturing and in-plane axial orientation. They then discuss mechanisms of defect formation (e.g., low-angle grain boundaries, twinning – and in the extreme – amorphous solidification). Finally, they discuss methods for stacking devices, and by permitting substrate biasing. *IN*

164). Thermal Stress During Zone-Melting-Recrystallization of Silicon on Insulator Films: The Origin of Subboundaries and In-Plane Orientation of SOI.
Gibson, J.M.; Pfeiffer, L.N.; West, K.W.; Joy, D.C.
AT&T Bell Lab., Murray Hill, NJ
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 289-99, 1986

The effect of thermal stress during zone-melting recrystallization of Si-on-insulator SOI films is considered. New experimental results from graphite-strip-heated films are drawn upon. Low-angle grain boundaries exhibit an inverse dependence between spacing and tilt angle. This is explained semi-quantitatively by a model in which thermal stress-induced film buckling is responsible for the existence of low-angle grain boundaries. The predominance of the {100} orientation in these films is partly due to thermal stress and the elastic anisotropy of Si. Thus thermal stress is proposed as the origin of the two major features of zone-melted films. *CA*

165). Beam Recrystallized Silicon-on-Insulator Devices.
Lam, H.W.
Central Res. Labs., Texas Instruments Inc., Dallas, TX.
Appleton, B.R.; Celler, G.K. (Editors)
Laser and Electron Beam Interactions with Solids. Proceedings of the Materials Research Society Annual Meeting, 471-82, 1982, 16-19 Nov. 1981, Boston, MA.
North-Holland, Amsterdam, Netherlands

Beam-recrystallized silicon-on-insulator is an attractive material for VLSI integrated circuit and flat panel display applications. This paper describes the electrical characteristics that are unique to MOSFETs fabricated in this material. The back-interface between the silicon and the insulator significantly affects the leakage current by acting as a possible leakage path, depending on the

charge at the back interface and the doping concentration in the silicon close to the back interface. In addition, enhanced arsenic diffusion along grain boundaries can cause short circuits between the source and the drain of an n-channel MOSFET. Evidence of such enhanced diffusion is presented as well as means to reduce the impact of the problem. It is shown that molecular hydrogen can be used to passivate the grain-boundaries in the recrystallized silicon material, thereby increasing the carrier mobility. A profile of the carrier mobility as a function of depth from the surface of the silicon is presented, showing that the carrier mobility is not reduced significantly, even close to or at the back interface. *IN*

• 166). Microstructural Defects in Laser Recrystallized, Graphite Strip Heater Recrystallized and Buried Oxide Silicon-on-Insulator Systems: A Status Report.
Pinizzotto, R.F.
Central Res. Labs., Texas Instruments Inc., Dallas, TX
J. Cryst. Growth (Netherlands), Vol. 63, No. 3, 559-82, Oct. 1983.

Laser recrystallized silicon-on-oxide, graphite-strip-heater-recrystallized silicon-on-oxide and buried oxide by high dose oxygen ion implantation are three of the silicon-on-insulator technologies that are currently being evaluated for VLSI and VHSIC applications. The status report compares the microstructures of these materials. The main defects in both the laser- and graphite-strip-heater-recrystallized material are subgrain boundaries. The misorientations across the boundaries are normally less than 1 deg. The boundaries are formed by dislocation coalescence. The dislocations are generated by the stresses caused by the volume expansion during solidification of silicon droplets trapped in the solid silicon matrix. The droplets are caused by constitutional supercooling. Buried oxide SOI formed by high dose oxygen ion implantation has fewer crystallographic defects than the other two materials. The entire ion-implanted area is a single crystal after high-temperature annealing. The primary defects in epitaxial layers grown on implanted substrates are dislocations. *IN*

167). Microstructural Characterization of Silicon-on-Insulator Structures.
Pinizzotto, R.F.
Central Res. Labs., Texas Instrum. Inc., Dallas, TX
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications.
US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 251-61.
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Laser-recrystallized silicon-on-oxide, graphite-strip-heater-recrystallized silicon-on-oxide, and buried oxide by high dose oxygen ion implantation are three of the silicon-on-insulator technologies currently being evaluated for VLSI and VHSIC applications. This report compares the microstructures of these materials. The main defects in both the laser- and graphite-strip-heater-recrystallized material are subgrain boundaries. The misorientations across the boundaries are normally less than 1 deg. The boundaries are formed by dislocation coalescence. The dislocations are generated by the stresses caused by volume expansion during solidification of silicon droplets trapped in the solid silicon matrix. The droplets are caused by constitutional supercooling. Buried oxide SOI formed by high dose oxygen ion implantation has fewer crystallographic defects than the other two materials. The entire ion implanted area is a single crystal after high-temperature annealing. The primary defects in epitaxial layers grown on implanted substrates are dislocations. The oxide/silicon interfaces are abrupt if the dose is large enough. The sharp interfaces are formed by an internal oxidation mechanism. The minimum MeV He ion-channeling yield from epitaxial silicon layers grown on buried oxide is about 2.5%, the lowest of any SOI material. *IN*

168). Crystallization of Deposited Silicon on Insulators for Device Applications.
Ryssel, H.; Gotzlich, J.
Fraunhofer-Inst. fur Festkorpertechnol., Munchen, Germany

Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.
Proceedings of the Conference, 369-82, Vol.2
25-28 Sept. 1984, Dresden, Germany
Akad. Wissenschaften DDR, Dresden, Germany

The different techniques used for crystallization of polycrystalline silicon layers on insulating substrates are reviewed and compared in respect to the possible fabrication of 3-dimensional structures. Devices fabricated in such layers are described and further developments mentioned. *IN*

169). SOI Technologies at the CNET.
SOI Group, CNET, Meylan, France
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
539-49, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

For the recrystallization of poly-Si films deposited on oxidized Si wafers, CNET focus their research on lamp and cw laser systems. They have obtained large single-crystal films using both techniques. 'Selective annealing' allows localization of the remaining defects in the recrystallized films. Crystallographic as well as electrical characterization confirm the device-worthy potential of this material. *IN*

• 170). Scanned Microzone Recrystallization to Form Single Crystal Silicon on Amorphous Insulators – A Review.
Sedgwick, T.O.
IBM Thomas J. Watson Res. Center, Yorktown Heights, NJ.
Kaldis, E. (Editor)
Crystal Growth of Electronic Materials. 229-44
5th International Summer School on Crystal Growth and Materials Research.
3-10 Sept. 1983, Davos, Switzerland
North-Holland, Amsterdam, Netherlands

Microzone recrystallization of Si on amorphous insulator structures using a variety of scanned point and line energy sources is reviewed. The main topics covered are: heat flow nucleation geometric factors, serpentine scanning of point sources with seeding, line sources for large-area recrystallization, and geometric and constitutional supercooling models of subboundary formation. *IN*

171). A Steady-State Temperature Model for Silicon Recrystallization Using Light Sources.
Kyung, C.M.; Yang, Y.Y.
Dept. of Electr. Eng., Korea Adv. Inst. of Sci. & Technol., Seoul, Korea
IEEE Trans. Electron Devices (USA), Vol.ED-33, No.6, 864-5, June 1986

A simplified yet accurate temperature calculation scheme is proposed for silicon-on-insulator (SOI) recrystallization using light sources. The assumption is made that the total amount of heat generated per unit area in the SOI wafer by the light absorption is balanced by the total outgoing radiation flux. It is shown that this assumption significantly reduces the CPU time to calculate the steady-state wafer temperature. The calculation results of this model agree fairly well with those of the rigorous and time-consuming Poisson solver (see C.M. Kyung, ibid., Vol.ED-31, No.12, pp. 1845-51, 1984) with less than 3 K of temperature discrepancy for a typical case. *IN*

172). Large Area Subgrain-Boundary-Free SOI Induced by Thermal Gradient Control of Transitional Seeded-Growth.
Lee, E.-H.
Monsanto Electron. Mater. Co., St. Peters, MO.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium 471-6, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

The transitional region of subgrain-boundary-free crystal to subgrain-boundary-laced crystal formed during the initial stage of energy-beam-induced seeded recrystallization of thin-film silicon on an insulator has been examined to study the primary cause of subgrain boundary formation and the conceptual basis of its suppression. Observations include the systematic variation of faceted, cellular, and dendritic features; subgrain boundary directions and spacings; and the stable growth distance as a function of silicon film thickness and energy-beam density. A temperature gradient argument based on constitutional supercooling theory has been used to explain these observations. There are indications that an increased thermal gradient at the solidification front can suppress the onset of growth instability for large-area, defect-free growth of SOI. *IN*

173). Solid-Liquid Interface Instability in the Energy-Beam Recrystallization of Silicon on Insulator.
Lee, E.-H.
Monsanto Electron. Mater. Co., St. Peters, MO.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 563-73, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

An attempt has been made to systematically sort out the characteristic modes of the morphological transition in energy-beam-recrystallized thin-film silicon on insulating substrates, and to relate them to the mechanisms of solid-liquid interface stability breakdown. Stable to unstable breakdown modes include faceted, cellular, and dendritic configurations as well as transient and composite configurations. These primary modes of breakdown then lead to the secondary modes of breakdown which constitute subboundary formation. The mechanics of the primary (interface) breakdown and that of the secondary (subboundary) breakdown must be clearly differentiated in understanding the breakdown process. Constitutional supercooling and absolute supercooling models have been used to explain the various interface instabilities. *IN*

174). Threshold Voltage Of Thin-Film Silicon-on-Insulator (SOI) MOSFETs.
Lim, H.-K.; Fossum, J.G.

Dept. of Electrical Engng., Univ. of Florida, Gainesville, FL.
IEEE Trans. Electron Devices (USA), Vol.ED-30, No.10, 1244-51, Oct. 1983

The charge coupling between the front and back gates of thin-film silicon-on-insulator (SOI: e.g., recrystallized Si on SiO_2) MOSFETs is analyzed, and closed-form expressions for the threshold voltage under all possible steady-state conditions are derived. The expressions clearly show the dependence of the linear-region channel conductance on the back-gate bias and on the device parameters, including those of the back silicon-insulator interface. The analysis is supported by current-voltage measurements of laser-recrystallized SOI MOSFETs. The results suggest how the back-gate bias may be used to optimize the performance of the SOI MOSFET in particular applications. *IN*

175). Temperature Distribution of Silicon-on-Insulator Systems During Recrystallization Processing.
Miaoulis, I.N.; Mikic, B.B.
Dept. of Mech. Eng., MIT, Cambridge, MA, USA
J. Appl. Phys. (USA), Vol. 59, No. 5, 1663-6, 1 March 1986

The temperature distribution during melting-recrystallization processing of thin silicon films for electronic devices was calculated numerically and is presented in graphical form. Two methods of high-quality recrystallization are analyzed: the antireflective coating method and the stepwise thickness variation of the silicon dioxide. The controlling parameters were determined and their effects on temperature distributions are presented. *IN*

176). Thin Bulk Effects in SOI Structure.
Wang Shouwu; Xia Yongwei; Kong Lingkun; Zhang Dongxuan
Inst. of Semicond., Acad. Sinica, China
Chin. J. Semicond. (China) Vol.6, No.3, 225-35, May 1985

The potential and carrier distribution in different parts of a SOI structure are studied by using computer simulation. The results show that thin bulk effects occur in a SOI structure, with uniformly doped P-type recrystallization silicon film, when the thickness of the film is less than the maximum thickness of the depletion layer. The higher the threshold voltage, the thicker the recrystallization film when the thickness of the inner dioxide is constant; whereas the lower the threshold voltage, the thicker the inner dioxide when the film thickness is constant. The threshold voltage decreases as the inner dioxide thickness increases and finally becomes a constant value not dependent on the thickness of inner dioxide. The interface states with positive charge in the SOI structure further decrease the threshold voltage. Simulation analysis show that the principal design rule to prevent thin bulk effects in a SOI structure is to make the thickness of the recrystallization film exceed the maximum thickness of the depletion layer, and to use low-doping density silicon films and thick inner dioxide so as to decrease the influence of thin bulk effects when the film thickness is less than the maximum thickness of the depletion layer. The simulation presupposes that it is possible to develop new MOS thin-film transistors with crystal silicon substrate and lower threshold voltage. The simulation shows that the expression of threshold voltage for a SOI structure, using the depletion approximation, is very simple and more accurate. *IN*

177). Modes of Growth Stability Breakdown in the Seeded Crystallization of Microzone-Melted Silicon on Insulator.
Lee, E.-H.; Rozgonyi, G.A.
Monsanto Electron. Mater. Co., St. Peters, MO.
J. Cryst. Growth (Netherlands), Vol.70, No.1-2, 223-9, Dec. 1984
Sixth International Conference on Vapor Growth and Epitaxy and Sixth American Conference on Crystal Growth, 15-20 July 1984, Atlantic City, NJ.

Some of the characteristic modes of growth breakdown as observed in the energy-beam recrystallized thin-film silicon on insulating substrates are discussed from a solid-liquid interface stability point of view. Observations include elemental modes of breakdown, such as faceted, cellular, and dendritic configurations, as well as transient and composite configurations thereof. Each of these primary modes of breakdown then leads to a secondary mode of breakdown which constitutes the sub-boundaries. The outcome of each primary and secondary mode of breakdown seems to depend on the local thermal conditions and crystal growth directions. *IN*

• 178). Defect Characterization in Monocrystalline Silicon Grown Over SiO_2.
McGinn, J.T.; Jastrzebski, L.; Corboy, J.F.
RCA Labs., Princeton, NJ.
J. Electrochem. Soc. (USA), Vol.131, No.2, 398-403, Feb. 1984

Crystallographic defect structures in monocrystalline silicon films grown over SiO_2 layers have been characterized by cross-section and planar transmission electron microscopy. Overgrowths of epitaxial silicon films on SiO_2 layers have been seeded from single-crystal substrates through openings in the SiO_2 layers. Defect structures have been studied as a function of substrate orientation, seeding procedure, and growth temperature. Defect densities have been dramatically reduced through first-order optimization of the above parameters. *IN*

179). Technique for Radiation Effects Measurements of SOI.
Miller, W.M.; Tsao, S.S.; Pfeiffer, L.
Sandia Natl. Lab., Albuquerque, NM
IEEE Trans. Nucl. Sci., Vol. NS-33, No. 6, Pt. 1, 1381-4, 1986

A technique was developed and tested for measuring the radiation response of the interfaces of Si-on-insulator (SOI) materials. The approach uses deconvolution of capacitance-voltage (C-V) data of full and etched-back SOI structures to provide the C-V curves of each of the three interfaces. From these curves, the changes in the voltage due to oxide trapped charge and interface states were determined. The technique was designed to provide a comparison of the radiation responses of different SOI materials. The total dose effects were studied for SOI material prepared by melt recrystallization. *CA*

180). Single Crystal Silicon Films on Amorphous Insulators: Growth by Lateral Nucleated Epitaxy Using Scanning Laser and Electron Beams and Evaluation by Electron Backscattering Contrast.
Sedgwick, T.O.; Geiss, R.H.; Depp, S.W.; Hanchett, V.E.; Huth, B.G.; Graf, V.; Silvestri, V.J.
IBM Res., San Jose, CA.
J. Electrochem. Soc. (USA), Vol.129, No.12, 2802-8, Dec. 1982

Electron backscattering contrast has been used to study the mode and extent of single-crystal silicon film growth on amorphous insulators. Using nucleated lateral epitaxy and a scanning argon ion laser beam or an electron beam, single-crystal films up to 1 mm by 70 μm in area were grown over thin silicon nitride or silicon dioxide layers on silicon substrates. Elevated substrate temperatures and the use of capping layers promoted large area growths and reduced damage to the structure.

Electron channeling micrographs easily reveal that after 70 to 100 μm of scan progression the single-crystal growth of laser-scanned samples terminates in either a uniformly nucleated polycrystalline growth front or in random nucleated large twins propagating along (110) direction. Electron-beam-produced overgrowths revealed extensive twin formation both in the nonovergrowth and overgrowth regions. *IN*

181). Measurement and Reduction of Interface States at the Recrystallized Silicon-Underlying Insulator Interface.
Sturm, J.C.; Plummer, J.D.; Gibbons, J.F.
Electron. Labs., Stanford Univ., CA.
Appl. Phys. Lett. (USA), Vol.46, No.12, 1171-3, 15 June 1985

Deep level transient spectroscopy and capacitance-voltage measurements have been performed on an inverted metal-oxide-semiconductor (MOS) capacitor structure to measure the interface state density at the recrystallized silicon-underlying insulator interface. The effects of different recrystallization caps, annealing steps, and different underlying oxides have been investigated. An interface state density in the mid 10^{10} cm^{-2} eV^{-1} range can be consistently obtained, enabling well-behaved MOS transistor channels on the bottom of the recrystallized films. *IN*

• 182). Characterization of Beam-Recrystallized Si Films and Their Si/SiO_2 Interfaces in Silicon-on-Insulator Structures.
Vu, D.P.; Pfister, J.C.
CNET, Meylan, France
Appl. Phys. Lett. (USA), Vol.48, No.1, 50-2, 6 Jan. 1986

A technique equivalent to the conventional C-V measurement is developed for silicon-on-insulator technology. A depletion-mode transistor is used. The $I_D/(V_G)$ characteristic and its derivative, i.e., the transconductance, allow the determination of the doping of the Si film, the oxide thickness, the fixed oxide charge at both Si/SiO_2 interfaces. The device can be used in process control without any extra process steps. *IN*

183). Determination of Minority-Carrier Generation Lifetime in Beam-Recrystallized Silicon-on-Insulator Structure by Using a Depletion-Mode Transistor.
Vu, D.P.; Pfister, J.C.
CNET, Meylan, France
Appl. Phys. Lett. (USA), Vol.47, No.9, 950-2, 1 Nov. 1985

The authors describe a technique for measuring minority-carrier lifetime on a very small area of material and apply this technique to recrystallized silicon layers on an insulating substrate where the localization of the crystalline defects gives rise to small defect-free regions actually used for devices. The method uses a depletion-mode transistor in which drain-source conductance yields a signal equivalent to capacitance signal, thus allowing measurements equivalent to conventional Zerbst transient capacitance to be made in the defect-free regions. *IN*

184). Beam-Recrystallised Silicon-on-Insulator Films: Can Devices Live with Grain Boundaries?
Colinge, J.-P.
CNET, Meylan, France
Microelectron. J. (GB), Vol.14, No.6, 58-65, Nov.-Dec. 1983

Current techniques in which polysilicon films deposited on an insulator are recrystallised have not yet shown the ability to produce large areas of grain boundary-free material. Grain boundaries have been demonstrated to be paths of rapid dopant diffusion, giving rise to shorts in devices. Grain boundaries occurring in the channel of transistors shift the device threshold voltage in an uncontrolled manner. It is, however, possible to control the location of these defects with accuracy and to place them where they will not preclude circuit operation, i.e., in the field area of the circuits. Single-crystal stripes of silicon-on-insulator can be obtained, with no other defects than the localised ones. Good device performances have been obtained using this material, in which the mobility is the same as in bulk silicon. *IN*

185). Recrystallization of Polycrystalline Silicon Islands on Fused Silica.
Kobayashi, Y.; Fukami, A.; Suzuki, T.
Hitachi Res. Lab., Hitachi Ltd., Ibaraki, Japan
Extended Abstracts of the 15th Conference on Solid State Devices and Materials, 35-8, 1983, 30 Aug.-1 Sept. 1983, Tokyo, Japan
Japan Soc. Appl. Phys., Tokyo, Japan

Cracks in zone melting recrystallized silicon on fused silica could be eliminated by recrystallizing polycrystalline silicon which was previously etched to form islands of silicon. The islands must be less than 250 by 500 μm^2 in size when silicon thickness is 0.5 μm and 50 by 100 μm^2 when silicon thickness is 1.0 μm. The recrystallized silicon islands were a single crystal with some subgrain boundaries consisting of arrays of discrete dislocations. The orientation of crystals was (111) in almost all cases. The electron field-effect mobilities of devices on recrystallized silicon were 300 to 700 $cm^2/V{\cdot}s$, the same as that of devices on bulk silicon with an orientation of (111) when the device threshold voltages were the same. *IN*

186). Nucleation and Crystal Growth Characteristics in Energy Beam Crystallization of Silicon Islands.
Kugimiya, K.; Akiyama, S.; Yoshii, N.
Central Res. Lab., Matsushita Electr. Ind. Co. Ltd., Osaka, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 47-66, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Nucleation and crystal growth controls in recrystallization of isolated Si islands embedded in insulators have been studied. It was observed that isolated single-scannings of polysilicon films by energy beams resulted in the preferred orientation of (110) surface and (111) approximately (113) growth directions. Overlapped multiscannings were destructive to this preferred orientation and resulted in random orientation which was due to unstable and random nucleation at Si/melt-Si/SiO_2 interfaces and also due to crystal break-ups caused by large stresses. In crystallization of islands, the (110) and (111) preferred orientation was also observed. The (110) surface orientation was assumed to reflect the high (110) anisotropy of as-deposited LPCVD polysilicon films and/or the stress-enhanced growth accompanied with (112) pseudo-twins. A model was constructed and showed that pseudo-twins extending to (111) directions were nucleation sites for the very fast growth and accommodated

impurities like oxygen, effectively reducing stresses. At melt-Si/SiO_2 interfaces, nucleation was almost suppressed reflecting preferred temperature profiles. These observations pointed out that islands embedded in insulators with grooves and traced by isolated single scannings resulted in the best grain boundary control and better single-crystal islands. *IN*

187). Multilevel SOI Recrystallization Using a Novel Seed Structure.
Hamasaki, T.; Inoue, T.; Ysohimi, M.; Yoshii, T.; Tango, H.
VLSI Res. Cent., Toshiba Corp., Kawasaki, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 18th, 569-72, 1986 *CA*

188). Effective Defect Entrainment in Lamp Zone Melting of Silicon Films on Insulator.
Haond, M.; Dutartre, D.; Bensahel, D.
Cent. Natl. Etud. Telecommun., Meylan, France
J. Cryst. Growth, Vol. 79, No. 1-3, Pt. 2, 578-82, 1986

Si-on-insulator (SOI) films prepared by zone melting contain grain or subgrain boundaries which result from the freezing front instabilities. If device-worthy films are to be used, these line defects have to be confined to locations where no active areas of devices will be placed. The authors present the two main entrainment techniques they have studied. They are based on thermal modulation and interfacial energy modulation. An in-situ observation helps the understanding of the actual mechanisms involved in the breakdown of the freezing front. *CA*

189). Modifying Crystallographic Orientations of Polycrystalline Si Films Using Ion Channeling.
Kung, K.T.-Y.; Iverson, R.B.; Reif, R.
Dept. of Electr. Eng. & Comput. Sci., MIT, Cambridge, MA.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 727-32, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

Polycrystalline silicon films 4800 Å thick deposited via low-pressure chemical vapor deposition on oxidized silicon wafers have been amorphized by silicon ion implantation and subsequently recrystallized at 700°C. Due to channeling of the ions through grains whose (110) axes were sufficiently parallel to the beam, these grains survived the implantation step and acted as seed crystals for the solid-phase epitaxial regrowth of the film. This work suggests the feasibility of combining ion implantation and furnace annealing to generate large-grain, uniformly oriented polycrystalline films on amorphous substrates. It is a potential low-temperature silicon-on-insulator technology. *IN*

190). Seed Selection Through Ion Channeling to Modify Crystallographic Orientations of Polycrystalline Si Films on SiO_2: Implant Angle Dependence.
Kung, K.T.-Y.; Iverson, R.B.; Reif, R.
Dept. of Electr. Engng. & Comput. Sci., MIT, Cambridge, MA.
Appl. Phys. Lett. (USA), Vol.46, No.7, 683-5, 1 April 1985

Polycrystalline silicon films 4800 Å thick deposited by low-pressure chemical vapor deposition at 620°C on oxidized silicon wafers have been amorphized by implantation with 210-keV Si^{28} ions to a dose of $10^{15} cm^{-2}$ at 0, 1, 3, 5, or 7 deg from normal incidence and subsequently recrystallized at 700°C. The as-deposited film was (110) textured with the (110) directions within ±20 deg of the surface normal. After the 0-, 1-, or 3-deg implant and subsequent recrystallization, most of the (110) directions were confined to within ±4 deg of the corresponding implant direction. For the 5- and 7-deg implants, the (110) directions in the recrystallized layers became randomly oriented; that is, the films lost their (110) texture. These results can be explained by the process of seed selection through ion channeling (SSIC): the grains that survived the 0-, 1-, or 3-deg implant due to ion channeling acted as seeds during recrystallization. The fact that the direction of the (110) axes

in the recrystallized films was coincident with the implant angle strongly supports the existence of the SSIC process. *IN*

191). Understanding the Transitional Seeded-Growth Mechanism for Large Area Crystallization of Subgrain-Boundary-Free SOI.
Lee, E.-H.
Monsanto Electron. Mater. Co., St. Peters, MO.
Bean, K.E.; Rozgonyi, G.A. (Editors)
VLSI Science and Technology-1984. Proceedings of the Second International Symposium on Very Large Scale Integration Science and Technology. Materials for High Speed/High Density Applications, 250-66, 1984
6-11 May 1984, Cincinnati, OH.
Electrochem. Soc., Pennington, NJ.

The breakdown transition mechanism from a stable to an unstable growth of thin film silicon on insulating substrates is discussed for conceptual approaches of achieving large-area, defect-free silicon-on-insulator (SOI) materials. Morphological, thermodynamic, chemical, and microstructural analyses suggest that constitutional supercooling might be responsible for the stability breakdown, although other types of supercoolings are not ruled out. There are indications that stable growth distance can be extended with increased thermal gradients. The concept of incubation distance has been useful to set up a semi-quantitative model for estimating the stable growth distance. *IN*

192). The Forming of Si Single Crystal Layer Structures on Insulating Substrates.
Scharff, W.; Erben, J.-W.; Hoppner, K.; Wolf, A.; Voelskow, M.; Matthai, J.
Sektion Phys., Tech. Hochschule, Karl-Marx-Stadt, Germany
Wiss. Z. Tech. Hochsch. Karl-Marx-Stadt (Germany),Vol.27, No.2, 256-64 1985.

The growth of Si layer on insulator substrate at varied rates is reported, and the effect of small angle shift of grain boundaries on different optical and electrical parameters is discussed. Reproducible single-crystal structures with (100) orientation and carrier mobility comparable to that in bulk semiconductor material are quoted. *IN*

Comprehensive Treatment

193). Characterization of the Dual E-Beam Technique for Recrystallizing Polysilicon Films.
Davis, J.R.; McMahon, R.A.; Ahmed, H.
Dept. of Eng., Cambridge Univ., England
J. Electrochem. Soc. (USA), Vol.132, No.8, 1919-24, Aug. 1985

Detailed materials properties of silicon-on-insulator films produced by dual electron-beam recrystallization of polysilicon films are reported. By scanning a line electron beam parallel to the edges of an array of narrow seeding windows, large areas (several square centimeters) of precisely oriented single-crystal silicon have been formed. The optimum beam conditions and substrate geometry to achieve the best recrystallization have been investigated, and it has been found that using a fast scan speed (approximately 35 cm/s) allows seeded regrowth without melting the substrate below the isolating oxide. Using these conditions, complete wafers may be recrystallized in around 30 s without introducing strain or wafer warping. Remaining crystallographic defects include dislocations midway between seeding windows and an occasional twinning of the regrowth when the windows are aligned along $< 110 >$. *IN*

194). A TEM Study of Silicon-on-Insulator Films Produced by the Dual Electron Beam Recrystallisation of Polycrystalline Silicon.
Hockly, M.; Davis, J.R.
British Telecom Res. Labs., Martlesham Heath, Ipswich, England
Cullis, A.G.; Holt, D.B. (Editors)
Microscopy of Semiconducting Materials, 1985. Proceedings of the Royal Microscopical Society Conference, 83-8, 1985, 25-27 March 1985, Oxford, England
Adam Hilger, Bristol, England

Cross-sectional TEM studies have been carried out which show that low-defect density single-crystal silicon-on-oxide films have been produced using the dual electron-beam recrystallisation technique, which employs the seeded lateral regrowth of deposited polysilicon layers. Control of the movement of the melting and solidification fronts is shown to be crucial to the success of the technique. A localised characteristic defect has been identified and its mechanism of formation determined. *IN*

195). Silicon Film Recrystallization Using E-Beam Line Source.
Rensch, D.B.; Chen, J.Y.
Hughes Res. Labs., Malibu, CA.
Microelectron. J. (GB), Vol. 14, No. 6, 66-73, Nov.-Dec. 1983

Lateral zone melting from a fast-scanning (50 to 30 cm/s) e-beam line source has been used to grow single-crystal films with an area limited only by the e-beam scan field. Electron backscattering contrast and etch pit techniques have been used to study the crystallographic orientation and extent of single-crystal silicon film growth on SiO_2-coated silicon wafers. (100) textured films have been grown on these (0.35- to 1.0-μm thick) SiO_2 layers containing periodic openings to permit seeding during recrystallization. Recrystallization of non-seeded polysilicon produced (111)-textured films. Enhancement-mode n-channel MOSFETs have been made in both types of films. Channel mobility as high as 600 $cm^2/V{\cdot}s$ has been measured in the (100) textured films. *IN*

196). Silicon on Insulator Films Produced by Electron Beam Recrystallization of Polysilicon.
Davis, J.R.; McMahon, R.A.; Ahmed, H.; Hopper, G.F.
British Telecom Res. Labs., Martlesham Heath, England;
Br. Telecom Technol. J. (GB), Vol. 3, No. 1, 63-9, Jan. 1985

A dual electron-beam technique has been developed which is able to convert films of fine-grained polycrystalline silicon, deposited on an oxide, into single-crystal form. By seeding the regrowth of the film from a single-crystal substrate which is partially covered by a thick isolating oxide, silicon-on-insulator (SOI) films with precisely controlled orientation can be obtained. CMOS transistors and simple circuits fabricated in these films show them to have electron and hole mobilities comparable to those of bulk silicon, and much better than those of silicon on sapphire (SOS) films. The technique is thus a strong contender for producing SOI substrates for high-speed CMOS circuits and also for applications requiring high-voltage isolation. *IN*

197). Silicon-on-Insulator CMOS Transistors in Dual Electron Beam Recrystallised Polysilicon.
Hopper, G.F.; Davis, J.R.; McMahon, R.A.; Ahmed, H.
Hirst Res. Centre, GEC, Wembley, England
Electron. Lett. (GB), Vol.20, No.12, 500-1, 7 June 1984

Discrete MOS transistors and CMOS test circuits have been fabricated on silicon-on-insulator substrates prepared by recrystallisation of polysilicon on silicon dioxide by the dual electron-beam technique. Channel mobilities in seeded material are found to be equal to those obtained in bulk silicon devices. In unseeded material, hole mobility remains the same, but electron mobility is lower. *IN*

198). Characteristics of MOS Devices in Electron Beam-Recrystallized Silicon on Insulator.
Ohmura, Y.; Shibata, K.; Inoue, T.; Yoshii, T.; Horiike, Y.
Toshiba Randd Center, Toshiba Corp., Kawasaki, Japan
International Electron Devices Meeting, Technical Digest, 429-32, 1982
13-15 Dec. 1982, San Francisco, CA.
IEEE, New York.

N-Channel MOS devices have been fabricated in an electron beam-recrystallized silicon film on a $Si_3N_4/SiO_2/(100)$ silicon substrate. The threshold voltage for MOS transistors is well controlled by B or As channel-implantation. The electron mobility of 410 $cm^2/V{\cdot}s$ has been obtained for As-implanted transistors. However, the electron mobility decreases drastically for unimplanted and B-implanted transistors, which is suggestive of the excessive surface scattering due to the rough surface morphology. The 25-stage E/E and E/D ring oscillators have operated with minimum supply voltages of 5.4 and 13.4 V, respectively. The propagation delay for an E/E ring oscillator with fan out of 1 composed of L=4 μm transistors is 5.6 ns/stage at V_{dd}=5.5 V with a power dissipation of 0.38 mW/stage. *IN*

• 199). N-Channel MOS Ring Oscillators Fabricated in Electron-Beam Recrystallized Silicon-on-Insulator.
Ohmura, Y.; Shibata, K.; Inoue, T.; Yoshii, T.; Horiike, Y.
Toshiba Corp., Kawasaki, Japan
IEEE Electron Device Lett. (USA), Vol.EDL-4, No.3, 57-9, March 1983

Both 25-stage N-MOS enhancement driver/enhancement load (E/E) and enhancement driver/depletion load (E/D) ring oscillators with a fan out of one composed of 4-μm channel length transistors have been successfully fabricated in cw electron-beam recrystallized polysilicon/$Si_3N_4/SiO_2/(100)$

silicon substrates. The minimum supply voltage for the oscillation is 5.4 V for an E/E ring oscillator with a transistor threshold voltage of about 1 V, while that for the E/D ring oscillator is as high as 13.4 V, which seems to be due to incorrect B- and As-implantation doses for the threshold-voltage control of the driver and load transistors, respectively. Propagation delays of 3.0 ns/stage at a supply voltage of 6 V with a power dissipation of 0.5 mW/stage and 7.2 ns/stage at a supply voltage of 14 V with a power dissipation of 2.1 mW/stage are obtained for the E/E and E/D ring oscillators, respectively. *IN*

200). Growth of Large Grained Silicon on Insulator by Electron Beam Annealing and Performance of MOS Devices.
Shibata, K.; Ohmura, Y.; Inoue, T.; Kato, K.; Horiike, Y.; Kashiwagi, M.
Toshiba Res. and Dev. Center, Toshiba Corp., Kawasaki, Japan
Jpn. J. Appl. Phys. Suppl. (Japan), 213-16, 1982
Proceedings of the 14th Conference (1982 International) on Solid State Devices, 24-26 Aug. 1982, Tokyo, Japan

An electron-beam-annealing (EBA) system with high current electron-emitter and oil-free pump evacuated chamber was developed. Parameters in grain growth of silicon-on-insulator (SOI) were analysed, and large grained-poly-Si with dimensions of 20 μm by several millimeters was stably and reproducibly obtained on Si_3N_4 film. MOSFETs (L=1.5 to 50 μm), inverters, and ring oscillators with well-controlled threshold voltages were successfully fabricated in the recrystallised SOI. Back interface conductions were clarified by drain current (I_d)-back gate voltage (V_{bg}) measurements. A hysteresis loop was found in the $I_d - V_{bg}$ relation, which is considered due to charge injection into Si_3N_4 layer. *IN*

201). Stacked SOI CMOS Fabricated with Seeding Lateral Epitaxy.
Yoshimi, M.; Suguro, K.; Takahashi, M.; Hamasaki, T.; Inoue, T.; Yoshii, T.; Taniguchi, K.; Tango, H.
Toshiba Corp., Kawasaki, Japan
1985 Symposium on VLSI Technology, Digest of Technical Papers, 26-7, 1985
14-16 May 1985, Kobe, Japan
Bus. Center Acad. Soc. Japan, Tokyo, Japan

The first successful fabrication of stacked devices using pseudoline electron beam (PLEB) is reported. A new seeding lateral epitaxy (SLE) method was used for SOI growth. The method utilizes improved seed structure and has the capability of growing large single crystals with high yield. In the device fabrication, low-temperature and planar processes were used to achieve downscaling of device dimension. The performance of the fabricated stacked CMOS, along with the influence of the SLE process on bottom layer devices, is described. *IN*

202). E-Beam-Induced Lateral Seeded Epitaxy of Silicon on Insulator.
Angelucci, R.; Lulli, G.; Merli, P.G.
Istituto Lamel, CNR, Bologna, Italy
Mater. Lett. (Netherlands), Vol.4, No.4, 185-8, June 1986

Lateral seeded recrystallization of polysilicon films deposited on SiO_2 was performed by a scanning e-beam annealing system. It was observed that the melting of the film depends on the energy absorption into the target, proceeding from seed openings to the islands, if the maximum of the energy-loss profile lies under the SiO_2 insulating layer. Recrystallized (100) monosilicon films with low defect density were obtained for a seed spacing of 20 μm. Experiments performed with various kinds of capping layers, in order to avoid the formation of ridges, exhibit a large amount of damage in the recrystallized films due to the instability of the capping layers under e-beam irradiation. *IN*

203). New Electron Beam Process – A Challenge to SOS.
Dance, B.
New Electronics, Vol. 18, No. 5, 61, Mar. 5, 1985

A dual electron-beam technique was developed which can convert films of fine-grained polycrystalline silicon deposited on a oxide layer into the single-crystal form. A seeding technique is used to produce silicon-on-insulator (SOI) films with precisely controlled orientation. Devices fabricated in these films have mobilities similar to those in bulk silicon and considerably greater than those of silicon-on-saphire (SOS) films. The new technique shows great promise for the production of SOI substrates for high-speed CMOS circuits and for high-voltage applications. *EI*

204). Techniques for Producing Defect-Free SOI by Dual Electron Beam Heating of Deposited Polysilicon.
Davis, J.R.; McMahon, R.A.; Ahmed, H.
Dept. of Engng., Cambridge Univ., Cambridge, England
J. Phys. Colloq. (France), Vol. 44, No. C-5, C5/337-41, Oct. 1983
Laser-Solid Interactions and Transient Thermal Processing of Materials
25-27 May 1983, Strasbourg, France

Advances in the dual electron-beam recrystallization technique arising from the fast scanning of a line beam parallel to the edges of narrow seeding windows are described. The resultant recrystallized layers are essentially defect-free, have good surface flatness, and cover large areas. *IN*

205). Crystal Orientations for Unseeded SOI Films Recrystallized by a MM Long CW Line-Source Electron Beam.
Hada, H.; Saitoh, S.; Okabayashi, H.
Microelectron. Res. Lab., NEC Corp., Kawasaki, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 17th, 139-42, 1985 *CA*

206). Amplitude Modulated Pseudo-Line Electron Beam Recrystallization for Large Area SOI Growth.
Hamasaki, T.; Inoue, T.; Higashinakagawa, I.; Yoshii, T.; Kashiwagi, M.; Tango, H.
VLSI Res. Cent., Toshiba Corp., Kawasaki, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 17th, 135-8, 1985 *CA*

207). Highly Controllable Pseudoline Electron-Beam Recrystallization of Silicon on Insulator.

Hamasaki, T.; Inoue, T.; Higashinakagawa, I.; Yoshii, T.; Tango, H.
VLSI Res. Center, Toshiba Corp., Kawasaki, Japan
J. Appl. Phys. (USA), Vol.59, No.8, 2971-6, 15 April 1986

A new electron-beam-annealing technique, an amplitude-modulated pseudoline electron beam, has been proposed for recrystallization of large-area silicon layers on insulating materials (SOI). The technique utilizes an amplitude-modulated sinusoidal wave for high-frequency beam oscillation. Through computer simulation of the temperature distribution for the sample surface, precise control of the position probability density profile of the line beam proved to be essential in realizing wide and uniform annealing. An optimum oscillation waveform was determined from the simulation. A large-area SOI, 4-mm square operator, was successfully recrystallized. *CA*

208). Line-Shaped Electron Beam System and SOI Films Prepared by the System.
Hayafuji, Y.; Shibata, A.; Yanada, T.; Sawada, A.; Usui, S.; Kawado, S.; Hayashi, H.
Sony Corp. Res. Center, Yokohama, Japan
Appleton, B.R.; Eisen, F.H.; Sigmon, T.W. (Editors)
Ion Beam Processes in Advanced Electronic Materials and Device Technology, 311-16, 1985, 15-18 April 1985, San Francisco, CA.
Mater. Res. Soc., Pittsburgh, PA.

The line-shaped electron-beam-annealing system which generates an electron beam of a length of 4 cm and a width of less than 100 μm with a high-energy density exceeding well over 100 kW/cm^2 was developed for the first time with a purpose of SOI processing as its primary application. An acceleration voltage of up to 20 kV can be used in this system. Seeded single-crystalline islands with areas several mm long and 30 to 100 μm in width were obtained by a single scan of the electron beam. The electron beam is generated in a pulsed way in the system due to the power restriction of the power supplies. An area of 4 by 5 cm^2 was processed by a single scan of an electron beam at a sample speed of 530 cm/s and a beam duration of 9.5 min. The scanning area for one scan is determined by the beam length and the duration of the beam and sample speed. The present system could give single-crystalline silicon films without any grain boundaries. The electron mobility of the electron-beam-recrystallized films, obtained from FETs made as a vehicle to test the electrical properties of the films, was comparable to that of the bulk silicon. A very rapid migration of silicon atoms in solid polycrystalline silicon films, which is controllable by process parameters, was also found with a migration speed of the order of 1 m/s in a capped structure. The present electron-beam system is useful in studying basic mechanisms of crystal growth in thin films. The system can have a very high throughput, a desirable feature in semiconductor industry. The present system can also be used to study the rapid thermal treatment of materials other than semiconductors including rapidly solidified materials. *CA*

• 209). Recrystallization of Polycrystalline Si Over SiO_2 Through Strip Electron-Beam Irradiation.
Hayafuji, Y.; Yanada, T.; Usui, S.; Kawado, S.; Shibata, A.; Watanabe, N.; Kikuchi, M.; Hayashi, H.; Williams, K.E.
Sony Corp. Res. Center, Yokohama, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 85-97, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Polycrystalline silicon on SiO_2 islands was successfully recrystallized by rapid scanning with a strip electron beam. The electron beam was focused on the samples in a strip measuring 3 cm by 60 μm, with a voltage of 10 kV and with peak current densities up to 70 A/cm^2. Samples with a poly-Si(001)Si, poly-Si/SiO_2/(001)Si and poly-Si/striped SiO_2/(001)Si structure were prepared. In the

poly-Si/striped SiO_2/(001)Si structure, lateral epitaxial growth in the scanned direction extended as much as 70 μm from the seeded area at the edge of the 100-μm wide stripe. The regrowth speed was estimated to be about 200 cm/s. TEM analysis showed that the recrystallized area on the SiO_2 stripe was (001) single-crystalline film which included small-angle boundaries. The surface appearance depended on the regrowth direction and the (110) direction was found to be the preferential direction. Encapsulation of the samples with silicon nitride film effectively smoothed the recrystallized surface, although small-angle boundaries still were in evidence. *IN*

210). Characterization of Subgrain Boundaries in Laterally Seeded Epitaxial SOI Films Recrystallized by an Electron Beam.
Horita, S.; Ishiwara, H.
Dep. Appl. Electron., Tokyo Inst. Technol., Yokohama, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 18th, 573-6, 1986 *CA*

211). E-Beam Recrystallized SOI.
Ishiwara, H.
Graduate School of Sci. and Engng., Tokyo Inst. of Technol., Yokohama, Japan
Extended Abstracts of the 15th Conference on Solid State Devices and Materials, 97-100, 1983, 30 Aug.-1 Sept. 1983, Tokyo, Japan
Japan Soc. Appl. Phys., Tokyo, Japan

Recrystallization of Si films on SiO_2/Si structures by an electron beam is reviewed. In order to produce the concave trailing edge of the molten zone, a spot beam is scanned faster than the thermal response time of the substrates either along a straight line sinusoidally or along a 'V' shape. It was found from Nomarski optical microscopy that both scanning methods were effective to obtain large single-crystal grains. The maximum grain size with flat surface was about 20 by 450 μm^2. *IN*

212). Recrystallization of Silicon-on-Insulator Structures by an Electron-Beam with Fast Sinusoidal X- and Slow Linear Y-Scans.
Ishiwara, H.; Nakano, M.; Yamamoto, H.; Furukawa, S.
Graduate School of Sci. and Engng., Tokyo Inst. of Technol., Yokohama, Japan
Jpn. J. Appl. Phys. Suppl. (Japan), 607, 1982
Proceedings of the 14th Conference (1982 International) on Solid State Devices, 24-26 Aug. 1982, Tokyo, Japan

Growth of crystalline Si films onto amorphous insulating substrates has attracted attention for fabrication of high-speed LSIs as well as 3-dimensional LSIs. A considerable amount of work has been devoted to increasing the grain size in Si films and recently a general principle that laser and electron-beam-induced molten zones are necessary to have concave trailing edges has been found. So far, the concave edge has been realized by varying the optical absorption with thin-film structures and by shaping laser spot. In these samples, however, width of a single-crystal grain is limited by the laser spot. On the contrary, electron-beam annealing has an advantage that the temperature profile in the substrate can be controlled over a larger area by electrical scanning of the beam. The authors present a novel recrystallization technique by an electron beam with fast sinusoidal x- and slow linear y-scans, which has the potential to produce a wider molten zone with the concave trailing edge. The maximum single-crystal grain size so far obtained is 20 by 450 μm^2. *IN*

213). Recrystallization of Silicon-on-Insulator Structures by Sinusoidally-Scanned Electron Beams.
Ishiwara, H.; Ohyu, K.; Horita, S.; Furukawa, S.
Graduate Sch. of Sci. & Eng., Tokyo Inst. of Technol., Yokohama, Japan
Jpn. J. Appl. Phys. Part 1 (Japan), Vol. 24, No. 2, 126-32, Feb. 1985

The recrystallization by an electron beam of Si films deposited on SiO_2/Si structures is described. To achieve pseudo-line-shaped heating, a spot beam was scanned along a line at frequencies of up to 10 kHz. It is predicted theoretically that the temperature profile along the line can be controlled by the scanning waveform and that a concave molten zone edge is obtained with a sinusoidal scan. It was found experimentally that the recrystallization conditions required for forming a large single-crystal area with a flat surface are rather restricted in the sinusoidal-scan method, since the Si films are broken up or deformed by the temperature gradient along the line. It was also found that overlapping scans of the pseudo-line-shaped beam are effective in increasing the single-crystal area. A nearly single-crystalline Si film of 300 by 200 μm^2 was produced on an SiO_2/Si structure by overlapping scans. *IN*

214). Growth of Si on Insulators Using Electron Beams.
Knapp, J.A.; Picraux, S.T.
Sandia Nat. Labs., Albuquerque, NM.
J. Cryst. Growth (Netherlands), Vol.63, No.3, 445-52, Oct. 1983

The use of electron beams for melting and crystallizing polycrystalline silicon layers in silicon-on-insulator structures is described. The formation of single-crystal Si films with low-angle grain boundaries or of large parallel grains has been achieved, similar to results for other beam and radiant heat source techniques. However, the electron-beam approach has been much less thoroughly investigated than other heating sources. The advantages and disadvantages of electron beams, relative to other heat sources, are discussed, as well as the current state of application. *IN*

215). Growth of Silicon-on-Insulator Films Using a Line-Source Electron Beam.
Knapp, J.A.; Picraux, S.T.
Sandia Nat. Labs., Albuquerque, NM.
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 557-62, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

A swept line-source electron beam has been used to study unseeded Si-on-insulator crystallization at beam scan speeds of 150 to 1500 cm/s. For a particular sample configuration a maximum linear crystallization velocity of 350 cm/s was observed. At higher sweep speeds, competing nucleation occurred at intervals across the film. Both the limit in crystallization velocity and the intervals between nucleation are tentatively explained by a simple model. *IN*

216). Silicon-on-Insulator Structures Formed by a Line-Source Electron Beam: Experiment and Theory.
Knapp, J.A.
Sandia Nat. Labs., Albuquerque, NM.
J. Appl. Phys. (USA), Vol.58, No.7, 2584-92, 1 Oct. 1985

A line-source electron beam has been used to melt and recrystallize isolated Si layers to form Si-on-insulator structures. Heat flow calculations for these layered structures have been developed which correctly predict the observed recrystallization. Using sample sweep speeds of 100 to 600 cm/s and peak power densities up to 75 kW/cm^2 in the 1- by 20-mm beam, the authors have obtained single-crystal areas as large as 50 by 350 μm. Seed openings to the substrate are used to control the orientation of the regrowth and the heat flow in the recrystallization film. *IN*

217). Recrystallization of Si Films on Thermal SiO_2-Coated Si Substrates Using a High-Speed E-Beam Line Source.
Rensch, D.B.; Chen, J.Y.
Hughes Res. Labs., Malibu, CA.
IEEE Electron Device Lett. (USA), Vol.EDL-5, No.2, 38-40, Feb. 1984

Lateral zone melting from a fast-scanning (5- to 30-cm/s) electron-beam line source has been used to grow single-crystal films with an area limited only by the electron-beam scan field. Electron backscattering contrast and etch pit techniques have been used to study the crystallographic orientation and the extent of single-crystal silicon film growth on thermal SiO_2-coated silicon (SOI) wafers. (100) textured films have been grown on these (0.35- to 1.0-μm thick) SiO_2 layers containing periodic openings to permit seeding during recrystallization. The seeded recrystallized films contained subgrain-free areas measuring 50 by 125 μm^2. Recrystallization of nonseeded polysilicon produced (111)-textured films. Enhancement-mode n-channel MOSFETs have been made in both types of films. Channel mobility as high as 600 $cm^2/V{\cdot}s$ has been measured in the (100) textured films. *IN*

218). Silicon Film Recrystallization by Line Electron Beam.
Saitoh, S.; Okabayashi, H.; Higuchi, K.
Microelectronics Res. Labs., NEC Corp., Kawasaki, Japan
Extended Abstracts of the 15th Conference on Solid State Devices and Materials, 101-3, 1983, 30 Aug.-1 Sept. 1983, Tokyo, Japan
Japan Soc. Appl. Phys., Tokyo, Japan

Ion-implanted Si and SOI films were recrystallized by using a line electron-beam-annealing system, operated in a cw-mode. In annealing ion-implanted Si films, an area about 3.5 mm wide was uniformly annealed in one beam scan. In the seeded SOI recrystallization case, SOI islands 200 μm square over an area 1.6 mm on a side were recrystallized without any grain boundaries in one-beam scan. *IN*

219). Electron Beam Recrystallized SOI Structures.
Shibata, K.; Inoue, T.; Kato, K.; Kashiwagi, M.
Res. & Dev. Center, Toshiba Corp., Kawasaki, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 29-39, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Electron-beam recrystallization of silicon films on silicon dioxide has been studied in three principal subjects. The first, with coalescence of dislocations, grain boundaries were generated at strain concentrated regions in the recrystallized silicon film. The second, measuring the transient temperature profile, it was confirmed that when the electron-beam scanning rate was above 5 mm/s, the temperature profile has a convex tailing. The third, ultra-high vacuum-deposited silicon films were used for laterally seeded epitaxial growth on silicon dioxide. The maximum epitaxial growth length and silicon film quality were improved in comparison with the results of chemically vapor deposited polycrystalline silicon films. *IN*

220). Recrystallization of Silicon on Insulator by Electron Beam Annealing.
Shibata, K.
Toshiba Corp., Kawasaki, Japan
Oyo Buturi (Japan), Vol. 53, No. 1, 32, Jan. 1984

There are two electron-beam-annealing methods: (1) the pulse method in which discharges charges from a capacitor, and (2) the continuous irradiation method in which continuously flows a constant beam current. Electron-beam annealing has advantages in being able to control beam output and scanning precisely and provide a desired annealing depth according to acceleration voltage setting. An inherent disadvantage is to electrify the surface of the specimen being annealed. *IN*

221). Use of the Line-Shaped Electron Beam in Silicon-on-Insulator (SOI) — A New Opportunity in Semiconductors.

Shibata, A.
Sony Res. Center, Yokohama, Japan
Radiat. Phys. Chem., Vol. 25, No. 4-6, 817-19, 1985

A thin layer of polycrystalline Si is deposited on an insulator such as SiO_2 grown on a Si wafer (active elements may be built on it) or a glass substrate, and then it is melted to regrow into a single-crystallized film of device quality, on which active elements are fabricated. Various energy sources are used in this process including a C heater, spot and shaped laser, or electron beams. The line-shaped electron beam with a very high-energy density of $> 1 MW/cm^2$ is apparently the most promising one due to its capability of generating fewer crystalline defects, negligible thermal effects to the underlying substrate, and a high through-put, the most desirable features for three-dimensional integration which should resolve difficulties encountered in the present two-dimensional integration. *CA*

222). A Study of Melting and Resolidification of Silicon-on-Insulator Structures Formed by Lateral Epitaxy.
Williams, D.A.; McMahon, R.A.; Hasko, D.G.; Ahmed, H.; Hopper, G.F.; Godfrey, D.J.
Microelectron. Res. Lab., Univ. Cambridge, Cambridge, United Kingdom
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 15-20, 1986

The formation of Si-on-insulator structures, by recrystallizing polycrystalline Si films with a dual-electron-beam technique, was studied over a wide range of conditions. The quality of the layers was assessed by examining cross sections in the SEM and optical microscopy of the surface after a Secco etch. The range of line powers which gives device-worthy single-crystal material becomes greater as the sweep speed increases and as the background temperature is reduced. The extent of melting into the substrate in the seed windows and below the isolating oxide was determined from the movement of an As implant. The experimental results are compared with the predictions from a one-dimensional model for the heat flow. *CA*

223). Large Area SOI Growth by Electron Beam Recrystallization.
Yoshii, T.; Hamasaki, T.; Inoue, T.; Higashinakagawa, I.; Tango, H.
VLSI Res. Center, Toshiba Corp., Kanagawa, Japan
J. Crystallogr. Soc. Jpn. (Japan), Vol.28, No.2, 83-91, March 1986

Recent progress in SOI growth by electron-beam recrystallization is described. Emphasis was placed on pseudo-line electron-beam (PLEB) technique with lateral seeded epitaxy. Through computer simulation of the temperature distribution of the sample during electron-beam irradiation, amplitude modulation of a high-frequency oscillation wave is proved to be useful for obtaining large-area SOI. Agglomeration of SOI near the seed region can be suppressed by using a seed structure with tapered edge and narrow seed width of 2 μm, which leads to the realization of single-crystalline SOI with well-controlled crystallographic orientation. A large-area SOI growth, 4 mm^2, is successfully carried out. *IN*

224). Silicon-on-Insulator Crystal Growth Shows Promise for 3-Dimensional ICs.
Yoshii, T.; Inoue, T.; Suguro, K.; Hamasaki, T.; Tango, H.; Kashiwagi, M.
VLSI Res. Center, Toshiba Corp., Kanagawa, Japan
JEE (Japan), Vol. 22, No. 220, 64-6, 68, April 1985

Work by Toshiba Corporation engineers for electron-beam annealing, to build silicon-on-insulator devices, and the use of other processes results in prototypes of encouraging, double-layer 3-D products. It is possible that 3-D devices could have high speed, functions, and other features hardly possible with two-dimensional LSIs. To create 3-D devices, however, numerous problems must be solved. In view of the present state of SOI crystal growth technology that constitutes

the most important device technique, the authors describe the method being developed – SOI crystal growth by electron-beam annealing. It thus becomes necessary to develop better annealing equipment and methods on the basis of fundamental knowledge about crystal growth, applying the developed techniques to 3-D ICs for feedback of problems with them. *IN*

225). Recrystallization of SOI Structures by a 2-Dimensionally Scanned Pseudo-Line Electron Beam.
Horita, S.; Ishiwara, H.
Grad. Sch. Sci. Eng., Tokyo Inst. Technol., Yokohama, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 17th, 131-4, 1985 *CA*

226). Electron-Beam Recrystallization of Silicon Layers on Silicon Dioxide.
Inoue, T.; Shibata, K.; Kato, K.; Yoshii, T.; Higashinakagawa, I.; Taniguchi, K.; Kashiwagi, M.
Res. and Dev. Center, Toshiba Corp., Kawasaki, Japan
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium 523-31, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Recent progress of SOI growth by electron-beam recrystallization is described. Transient temperature profile on the recrystallizing sample surface was analyzed experimentally by direct observation with a thermovision, which is essential for the understanding of crystal growth mechanism. SOI growth was performed by a spot-beam annealing and a pseudo-line-shaped beam annealing. The line-shaped electron beam has been proved to be useful for large-area crystallization. Emphasis was placed on lateral seeded recrystallization of silicon layer evaporated in an ultra high vacuum. Silicon layers with the seed area grown epitaxially during the evaporation and above 1-μm thickness were successfully recrystallized, resulting in reproducible lateral epitaxy. The pseudo-line-shaped electron beam formed by very high-frequency oscillation enabled dimensional enlargement of lateral epitaxial growth. Crystalline properties were characterized by analyses of Rutherford backscattering and electron channeling pattern. *IN*

227). Line-Source E-Beam Crystallization of Silicon-on-Insulator Films.
Knapp, J.A.; Picraux, S.T.
Sandia Nat. Labs., Albuquerque, NM.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium 533-7, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Silicon-on-insulator films have been formed using a 20 mm by 1 mm line-source electron beam, with sample sweep speeds of 100 to 500 cm/s and peak beam power densities up to 75 kW/cm^2. Films were formed over 1- and 2-μm thick SiO_2 isolating layers on 4-in diameter Si $< 100 >$ wafers, with stripe openings of 5- to 100-μm width for seeding the crystallization from the substrate. Films consisted of Si layers from 0.4- to 1.0-μm thickness, with a capping layer of 2-μm SiO_2. By sweeping the beam parallel to the long axis of the seed openings, smooth, oriented films were obtained, with low-angle grain boundaries confined to midway between seed openings. Best results were obtained for $< 50 - \mu$m spacing between seed openings. *IN*

• 228). Si-on-Insulator Formation Using a Line-Source Electron Beam.
Knapp, J.A.
Sandia Nat. Lab., Albuquerque, NM.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing, Symposium, 619-22, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

A line-source electron beam has been used to melt and recrystallize isolated Si layers to form Si-on-insulator structures, and the process is simulated by heat flow calculations. Using sample sweep speeds of 100 to 600 cm/s and peak power densities up to 75 kW/cm^2 in the 1- by 20-mm beam, the authors has obtained single-crystal areas as large as 50 by 350 μm. Seed openings to the substrate are used to control the orientation of the regrowth and the heat flow in the recrystallizing film. A finite-element heat flow code has been developed which correctly simulates the experimental results and which allows the calculation of untried sample configurations. *IN*

229). Silicon-on-Insulator Technology by Crystallization on Quartz Substrates.
Baumgart, H.
Philips Lab., North Am. Philips Corp., Briarcliff Manor, NY
Proc. SPIE-Int. Soc. Opt. Eng., 623 (Adv. Process. Charact. Semicond. 3), 211-23, 1986 *CA*

• 230). Laser-Induced Crystallization of Silicon on Bulk Amorphous Substrates: An Overview.
Biegelsen, D.K.; Johnson, N.M.; Hawkins, W.G.; Fennell, L.E.; Moyer, M.D.
Xerox Palo Alto Res. Centers, Palo Alto, CA.
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 537-48, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

The authors review the current understanding of laser-induced silicon thin-film crystal growth on bulk amorphous substrates. They propose a model for oriented nucleation and show that the silicon reflectivity jump on melting coupled with radiant heating lead naturally to this autonucleation mechanism. They then survey various techniques for control of lateral epitaxial growth and conclude with the results of some recent electrical device characterization. *IN*

231). A Model for CW Laser Recrystallization Including Reflectivity Effects.
Calder, I.D.
Northern Telecom Electron. Ltd., Ottawa, Ont., Canada
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium 507-12, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

A simple, practical model is developed for cw laser recrystallization of silicon and SOI structures, taking into account spatial variations in optical reflectivity. The power absorption is assumed to be uniform within each of three regions: the central molten spot, the annular two-phase region, and an outer annulus to account for absorption in the solid phase. Analytic expressions are obtained for the radial and depth dependence of the temperature, for the melt depth, the melt radius, the melt threshold, the crystallization threshold, and the substrate melt threshold. SOI structures are considered and comparison with some experimental results shows excellent agreement. *IN*

• 232). Laser Crystallization of Thin Si Films on Amorphous Insulating Substrates.
Celler, G.K.
Bell Labs., Murray Hill, NJ.
J. Cryst. Growth (Netherlands), Vol. 63, No. 3, 429-44, Oct. 1983

Crystalline Si films on insulating substrates are advantageous for high-performance large-scale integrated circuits and for large-area circuits used in flat-panel displays. Such films have been successfully formed by selective melting and recrystallization of polycrystalline Si deposited from the vapor on oxidized Si wafers and on bulk fused silica. Depending on the precursor structure and on the melting procedure, large crystallites or single-crystalline layers are achieved. Si recrystallization with cw and Q-switched lasers is described. Transistor fabrication in recrystallized films is reviewed, and the influence of residual grain boundaries and other defects on device performance is evaluated. *IN*

233). Laser Recrystallization and 3D Integration.

Colinge, J.-P.
CNET, Meylan, France
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984
Symposium, 653-62, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

There are various methods for producing device-grade silicon-on-insulator films; most, however, are unsuitable for fabrication of 3D integrated structures. The laser recrystallization technique is currently the only one which has produced single-crystal devices for 3D ICs. Improvements on this technique have been such that defects such as grain boundaries can be localized and even eliminated. High-speed CMOS circuits with VLSI features have been realized as well as new devices which take advantage of the 3D arrangement of vertically integrated structures. Although 3D integration is still in the early stages of development, it has already opened up new perspectives for applications such as high-speed circuits, dense memories, and sensors. *IN*

234). Grain Boundary Confinement in SOI Films Using Patterned AR Coatings and Seeded Oscillatory Growth.
Drowley, C.I.; Zorabedian, P.; Kamins, T.I.
Hewlett-Packard Labs., Palo Alto, CA.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
465-70, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Regular arrays of grain-boundary-free silicon strips several hundred microns long have been produced in a silicon-on-insulator (SOI) structure by using a patterned anti-reflection (AR) coating in combination with seeded oscillatory growth techniques. The AR coating pattern consists of a series of parallel stripes (typically 10 μm wide, separated by 10-μm spaces) starting from a seeding window. A laser beam (typically a 50- by 250-μm elliptical beam) is scanned perpendicular to the stripes, with the long axis of the beam parallel to the scan direction. The beam is stepped 1 to 2 μm between successive scans to advance the single crystal along the direction of the AR stripes. Grain boundaries are confined to the region under the AR stripes. Stereographic analysis of KOH etch pits formed in the single-crystal strips has shown that the orientation of the stripes gradually rotates from (001) (1 > 1 > 0) to (013) (3 > 3 > 1) as the crystal propagates away from the seed. MOS transistors formed in the single-crystal strips have mobilities comparable to devices formed in bulk films. These mobilities are approximately 20% higher than those found in devices formed in large-grain recrystallized polysilicon films. *IN*

235). Laser Recrystallization of Silicon Stripes in SiO_2 Grooves with a Polycrystalline Silicon Sublayer.
Egami, K.; Kimura, M.; Hamaguchi, T.
Fundamental Res. Labs., NEC Corp., Kawasaki, Japan
Appl. Phys. Lett. (USA), Vol.43, No.11, 1023-5, 1 Dec. 1983

A new substrate structure has been proposed for obtaining laser-recrystallized silicon on quartz glass. Single-crystal Si stripes as large as 12 by 500 μm, dielectrically isolated with a width as small as 1.5 μm, have been obtained by use of the new structure, in which polysilicon stripes are placed in SiO_2 grooves and a polycrystalline silicon sublayer is inserted between the SiO_2 layer and quartz glass to improve the thermal profile in recrystallization. The proposed structure is useful for realizing both enlargement and positional control of Si grains. *IN*

236). Device Applications of Beam Crystallized Silicon-on-Insulators.
Gibbons, J.F.
Stanford Univ., Stanford, CA.

1982 IEEE International Solid-State Circuits Conference Digest of Technical Papers, 233-6, 1982, 10-12 Feb. 1982, San Francisco, CA.
IEEE, New York.

Both enhancement- and depletion-mode MOSFETs can be fabricated on 0.5-μm LPCVD polysilicon films that have deposited on either SiO_2 or Si_3/N_4 and then recrystallized with a cw scanning laser. This result has led to a great deal of activity at a number of laboratories aimed at understanding and controlling the recrystallization process and exploring the potential of beam-crystallized silicon-on-insulators for device and IC fabrication. The author reviews the central results in this field and the direction of the current research. *IN*

237). CW Laser Crystallization of SOI: Thermal Analysis of the Most Critical Parameters.
Hode, J.M.; Joly, J.P.; Jeuch, P.
Leti, CEA, Grenoble, France
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium, 513-19, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

The authors present an overview of the thermal modeling of cw laser-induced crystallization of SOI. The dynamical case for a three-layer structure is derived. Effects of the phase change (increase in reflectivity, latent heat) are also treated. Analytical expressions are given and the models are compared to experiment. *IN*

238). Thermal Modeling of CW Laser-Crystallization of SOI.
Hode, J.M.; Joly, J.P.
Leti, CEA, Grenoble, France
J. Phys. Colloq. (France) Vol.44, No.C-5 C5/343-50 Oct. 1983
Laser-Solid Interactions and Transient Thermal Processing of Materials
25-27 May 1983, Strasbourg, France

The authors present analytical thermal models for cw laser-crystallization of SOI, taking account of various physical parameters (thermal conductivity, reflectivity, latent heat). The influence of these parameters is evaluated and compared to experiment. *IN*

• 239). Laser-Recrystallized SOI Devices: Promises and Pitfalls.
Kamins, T.I.
Hewlett-Packard Labs., Palo Alto, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 109-18
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, Amsterdam.

Recrystallized SOI structures offer possibilities for new classes of devices, as well as improved performance of more conventional circuitry. Single-layer and multilayer circuits are possible. For large-geometry devices unseeded films should be satisfactory, but seeding is required for high-performance, small-geometry circuits. In addition to the quality of the recrystallized film and the substrate, the properties of the interfaces must be optimized. The characteristics of each potential heat source must be considered when selecting one for a specific SOI structure; different sources are optimum for different applications. The evolution of SOI device structures can be seen by considering different realizations of CMOS cells. SOI structures can be applied to conventional circuits and also should allow efficient integration of entire systems with closely interacting functions. *IN*

240). Laser-Recrystallized Silicon-on-Oxide – The Ideal Silicon-on-Insulator Structure for VLSI?
Lam, H.W.

Central Res. Labs., Texas Instruments Inc., Dallas, TX.
International Electron Devices Meeting, Technical Digest, 556-8, 1980
8-10 Dec. 1980, Washington, DC.
IEEE, New York.

The development of the laser recrystallization technology of deposited polysilicon on a 1-μm thick oxide layer grown on a silicon wafer has enhanced the hope of achieving a silicon-on-insulator (SOI) material system that is far superior to that of silicon-on-sapphire (SOS) and is suitable for VLSI application. Surface mobility measured in devices fabricated in the laser-recrystallized SOI material approaches that fabricated in bulk silicon. The bottom silicon and silicon dioxide interface had been shown to be device-worthy. *IN*

241). Three Dimensional Thermal Analysis for Laser Annealing and Its Application to the Design of the SOI Structures.
Morishita, T.; Miyajima, T.; Kudo, J.; Koba, M.; Awane, K.
Semicond. Res. Labs., Sharp Corp., Nara, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 499-502, 1984
30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

Laser annealing (LA) has recently been used to obtain recrystallized silicon films, where 3D devices could be realized. The precise process control required in their applications encourages the construction of a computer model for the temperature rise caused by LA. The authors simulated the stationary temperature profiles induced by a moving cw laser beam in multi-layered SOI structures. In order to improve the crystal quality, they proposed the SOI structures capped with polysilicon and applied this simulation to the design of these structures. *IN*

242). Two-Dimensional Dynamic Numerical Simulation of an SOI Formation Process in Laser-Induced Seeded Lateral Growth.
Ohkura, M.; Ichikawa, M.; Miyao, M.; Sunami, H.; Tokuyama, T.
Hitachi Ltd., Tokyo, Japan
IEEE Trans. Electron Devices (USA), Vol.ED-32, No.7, 1347-52, July 1985

Dynamic computer simulation of seeded lateral growth has been carried out, taking into account laser-beam scanning and the melt/solidification process of the deposited poly-Si layer. Crystal growth direction over the SiO_2 layer is found to change depending on the thickness of the layer, with sufficient lateral growth occurring with a thicker SiO_2 layer. Lateral crystal growth velocity depends strongly on laser irradiation conditions and sample structures. It was estimated to be about 50 cm/s when the scan speed was set at 100 cm/s with a specified sample structure. This indicates the possibility of matching the beam scanning speed and the growth velocity in obtaining large-area SOI structures by optimizing these parameters. *IN*

243). Line-Source Processing of SOI Structures with Laser and Electron Beam.
Palkuti, J.L.; Pang, C.-S.
Adv. Res. & Appl. Corp., Sunnyvale, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 93-9, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Line-shaped laser and electron beams in combination with halogen-lamp substrate heating were used to fabricate single-crystal SOI films. Electron-beam and laser systems were developed to achieve a minimum beam cross section of 10 to 100 μm and aspect ratios up to 70. Unseeded SOI films were fabricated with a (100) textured single-crystal structure. Seeded films were recrystallized with 20- by 80-μm single-crystal islands with no low-angle grain boundaries. A process window of

1 to 10% in electron-beam power was measured. Single-crystal films were obtained at a line-scan velocity up to 2 cm/s suggesting a potential throughput of about 100 wafers per hour. The high scan velocity allows for minimizing the high-temperature cycle to under 30 seconds that the wafer is exposed to during recrystallization. This short-temperature cycle is compatible with the fabrication of three-dimensional devices, since unwanted diffusion and substrate damage are minimized. *IN*

244). Laser Recrystallized SOI.
Tamura, M.; Ohkura, M.; Natsuaki, N.; Miyao, M.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan.
Extended Abstracts of the 15th Conference On Solid State Devices and Materials, 23-6, 30 Aug.-1 Sept. 1983, Tokyo, Japan.
Japan Soc. Appl. Phys., Tokyo, Japan.

Si-on-insulator (SOI) technology has developed rapidly in recent years. Most techniques concentrate on transformation of polycrystalline Si films deposited on dielectric coated (SiO_2 or Si_3N_4) crystalline Si wafers by radiation sources. The major recrystallization methods are discussed, with emphasis on laser-irradiated SOI structures. Discussion focuses primarily on crystal-growth-related phenomena, since a reliable SOI technology must be established to obtain device-worthy crystal quality. *IN*

245). Laser Recrystallized SOI and Its Application to Device Fabrication.
Tamura, M.; Miyao, M.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Nishizawa, J. (Editor)
Semiconductor Technologies 1984, 137-50
North-Holland, Amsterdam, Netherlands

Si-on-Insulator (SOI) technology has been rapidly developing in recent years. Most techniques have concentrated on transformation of polycrystalline Si films deposited on dielectric coated (SiO_2 or Si_3N_4) crystalline Si wafers using radiation sources. The major recrystallization methods are discussed with emphasis on laser-irradiated SOI structures. The discussion primarily focuses on crystal growth phenomena, since a reliable SOI technology must be established to obtain device-worthy crystal quality. The electronic properties of the grown layer are also discussed in connection with crystal quality with some novel device structures realized by SOI technology. *IN*

246). Rapid Laser Scanning for Si-on-Insulator Devices.
Trimble, L.E.; Celler, G.K.
Bell Labs., Murray Hill, NJ.
Mater. Lett. (Netherlands), Vol. 1, No. 5-6, 184-8, April 1983

Rapid scanning (1- to 10-m/s) crystalline Si on SiO_2 with cw argon lasers offers practical means of forming Si-on-insulator devices. The short dwell times minimize heat losses by diffusion and allow recrystallization of at least one 3-in wafer/min. Moreover, simultaneous crystallization of Si over thermally dissimilar substrate regions becomes possible. This is demonstrated for stacked transistor structures, where the Si film for the upper transistors is recrystallized over the gate oxide and over the 10 times thicker field oxide. Large thermal stresses caused by rapid scanning often lead to micro-fracture in the films. The authors detailed study determined the optimum range of substrate temperatures, scan velocities, and line overlaps necessary to eliminate this problem. *IN*

247). High-Voltage Electron Microscopy Investigation of Subgrain Boundaries in Recrystallized Silicon-on-Insulator Structures.
Baumgart, H.; Phillipp, F.
Div. of North American Philips Corp., Briarcliff Manor, NY.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 593-8, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

The microstructure of high-quality recrystallized Si films on SiO_2 substrates produced by CO_2 laser-induced zone-melting has been investigated by high-voltage electron microscopy (HVEM). Subgrain boundaries represent the major defects in these recrystallized films. The origin of the subboundaries has been traced to periodic internal stress concentrations occurring at the faceted growth interface. These highly localized stresses cause plastic deformation of the growing single-crystal film by nucleation of an array of slip dislocations. The mechanism responsible for the formation of subgrain boundaries has been revealed to be polygonization, where thermally activated dislocations rearrange themselves into the lower energy configuration of the low-angle grain boundary. *IN*

248). Structural Properties of Dielectric Layers Following CO_2 Laser Irradiation of SOI Structures.
Baumgart, H.; Arnold, E.; Petruzzello, J.; McGee, T.F.; Frommer, M.H.
Philips Labs., New York, NY.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 87-92, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Semi-insulating polycrystalline silicon films have been used as matching layers in micro-zone-melting recrystallization experiments of silicon-on-insulator (SOI) structures. The effect of the laser irradiation on the structural composition and crystallographic properties has been investigated by transmission electron microscopy and Auger electron spectroscopy. CO_2 laser processing has been shown to lead to redistribution of oxygen and interface segregation of thin oxide and silicon zones. *IN*

• 249). Crystallographic Orientation Control of Silicon Stripes in SiO_2 Grooves Using a New Double Laser Annealing Technique.
Egami, K.; Kimura, M.; Hamaguchi, T.
Fundamental Res. Labs., NEC Corp., Kawasaki, Japan
Appl. Phys. Lett. (USA), Vol.44, No.10, 962-4, 15 May 1984

Crystallographic orientation control using a new double laser annealing of silicon stripes in SiO_2 grooves is presented. In the laser recrystallization of silicon stripes in the structure consisting of SiO_2 grooves/polysilicon sublayer/quartz glass substrates, first a part of the Si stripe is intentionally recrystallized by a cw ND:yttrium aluminum garnet laser to obtain (100) texture with a small grain size. Next, using these (100) oriented Si grains as seed crystals, (100) oriented large Si stripes are obtained by scanning a cw Ar ion laser along the stripe direction. This double laser-annealing technique for orientation control can potentially be used to fabricate three-dimensional devices. *IN*

250). Laser Treatment of the Silicon Wafer Surface.
Gorushko, V.A.; Danilovich, N.I.; Lesnikova, V.P.; Pilipenko, V.A.; Semenov, L.G.; Sterzhanov, N.I.; Chigir, G.G.
Minsk Radio Eng. Inst., Belorussian, SSR
Poverkhn. Fiz. Khim. Mekh. (USSR), 1984
Phys. Chem. & Mech. Surf. (GB), Vol.3, No.7, 2125-35, 1985

The effects of laser treatment on the quality of the silicon wafer surface structure, the properties of the silicon-dielectric interface, and the defect structure of the epitaxial layers grown on the laser-treated substrates have been studied. The data of laser ellipsometry, electron microscopy, and x-ray and metallographic analyses have shown that laser pretreatment of the silicon wafer surface improves the structure of the surface layer, reduces the charge at the silicon-insulator interface, and lowers the defect concentration in the epitaxial layers. *IN*

251). Electronic Deep Levels in Laser-Crystallized Silicon Thin-Film MOS Capacitors on Fused Silica.
Johnson, H.M.; Moyer, M.D.
Xerox Palo Alto Res. Center, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 101-8, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Residual electronic deep levels in fully-processed, cw laser-crystallized silicon thin films on fused silica were measured by transient capacitance spectroscopy, supplemented with capacitance-voltage techniques. The test devices were metal-oxide-silicon thin-film capacitors with p-type conductivity. The hole emission spectra are dominated by a continuous distribution of deep levels in the lower half of the silicon band gap which are associated with the Si-SiO_2 interface; the spectra also display the effects of surface generation. The interface-state density near midgap is estimated to be $6 \times 10^{10} eV^{-1} cm^{-2}$, and there are no detectable bulk deep levels with densities $> 1 \times 10^{14} cm^{-3}$. *IN*

252). Electrical Characterization of Laser/Energy-Beam Recrystallized Thin Film Silicon-on-Insulator (SOI).
Lee, E.-H.; Ruprecht, D.J.
Monsanto Electron. Mater. Co., St. Peters, MO.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 139-44, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Spreading resistance has been measured for various types of grain boundaries formed on graphite-heater-recrystallized SOI samples (G-SOI) or laser-strip-beam-recrystallised SOI samples (L-SOI) in order to identify the characteristic relation between the morphological/structural variation of the boundary defects and their electrical transport properties. In general, the resistance values across L-SOI sub-boundaries are higher than those across G-SOI sub-boundaries. TEM analyses reveal evidence of a higher degree of crystallographic mismatch (up to 10 deg) in L-SOI sub-boundaries than that (1 to 2 deg) in G-SOI sub-boundaries. The measurement also revealed the evidences of counter-doping near the seed areas where the epitaxial growth initiated. *IN*

• 253). Laser Recrystallized, Faceted, Cellular and Dendritic Morphologies of Thin Film Silicon-on-Insulator.
Lee, E.-H.
Monsanto Electron. Mater. Co., St. Peters, MO.
Mater. Lett. (Netherlands), Vol.3, No.3, 73-7, Jan. 1985

Configurations of faceted, cellular, and dendritic growth morphologies, as observed on laser-beam-recrystallized thin-film silicon on amorphous, insulating substrates, are reported. These configurations are viewed as first-order growth stability breakdown, from which the sub-boundaries develop. The cause of breakdown is discussed in terms of constitutional supercooling and absolute (bath) supercooling. *IN*

254). Study on the Transitional Seeded Crystallization Variation of Silicon on Insulator

Using Gaussian Laser Beams.
Lee, E.-H.
Monsanto Electron. Mater. Co., St. Peters, MO
J. Appl. Phys., Vol. 59, No. 1, 263-5, 1986

Variable distances of the transitional, defect-free, seeded crystallization of thin-film Si on insulating substrates were investigated using energy beams of Gaussian intensity distribution. Phenomenologically, defect-free crystals from the seed formed Gaussianlike contours with respect to subboundary-laced crystals. The results are attributed to the thermal gradient effect upon the crystallization stability. This study bears a significant implication in the current efforts to increase the subboundary-free crystallization region over extended distances. *CA*

• 255). Characterization of the Effects of Different Capping Layer Structures on the Laser Recrystallization of Silicon by Using Electrical Test Structures and Raman Spectroscopy.
Lu, H.E.; Boyd, J.T.; Jackson, H.E.; Janning, J.L.
Dep. Electr. Comput. Eng., Univ. Cincinnati, Cincinnati, OH
J. Appl. Phys., Vol. 60, No. 12, 4273-6, 1986

Polycrystalline Si-on-insulator is laser-recrystallized by using three different capping layer structures on separate wafers. The capping layer structures used include a 6-nm nitride layer, a combination of 64-nm nitride and 20-nm oxide layers, and 50-nm nitride antireflection periodic stripes oriented parallel to the direction of laser scanning. Electrical characteristics were measured by metal-oxide-semiconductor (MOS) Si-on-insulator (SOI) test structures fabricated in the laser-recrystallized Si films. Measurement of carrier mobilities, MOS interface properties, leakage currents, and ring oscillator delay times were compared for wafers having different capping layer structures. Stress in each case is characterized using a Raman spectrometer with microprobe. *CA*

256). TEM Investigation of Laser Recrystallized Thin Films of Amorphous Silicon Deposited on Various Substrates.
Mirouh, K.; Gaboriaud, R.J.; Desoyer, J.C.; Fogarassy, E.
Lab. de Metall. Phys., Poitiers, France
Pinard, P.; Kalbitzer, S. (Editors)
Poly-Micro-Crystalline and Amorphous Semiconductors, 221-6, 1984.
5-8 June 1984, Strasbourg, France
Editions de Phys., Les Ulis, France.

Thin layers (1,000 to 2,000 Å) of amorphous undoped silicon have been deposited by CVD on two types of substrates: $< 100 >$ oriented silicon single crystals and silicon oxide SiO_2 (SOI), and recrystallized by means of a pulsed ruby laser (20 ns, 1 to 2 J/cm^2) and a pulsed and scanned YAG laser (100 ns, 10 kHz, 1 to 2.5 J/cm^2). The annealed layers have been investigated by TEM, using both plane-viewed and cross-sectional samples. The major observations made during these investigations are qualitatively discussed. The best results are obtained with scanned laser (YAG and CO_2) on SOI structures. *IN*

257). Characterization and Application of Laser Induced Seeded-Lateral Epitaxial Si Layers on SiO_2.
Miyao, M.; Ohkura, M.; Warabisako, T.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 499-510, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

Electrical and crystal properties of seeded lateral epitaxial Si are evaluated as a function of distance from seeding area with the aid of a micro-probe RHEED and MOSFET fabrication. The results

indicate that the quality of a grown layer is as good as that of bulk Si crystal for most of the epitaxial layer. However, at the SiO_2 edge, electrical properties are somewhat poor due to the existence of dislocations and residual stresses. Element devices useful for SOI structures are fabricated. Electrical properties of MOSFETs with double active area indicate that surface and bottom regions of the epitaxial layer are all of device-worthy quality. Insulated control gate bipolar type transistors are proposed and some preliminary results are shown. *IN*

258). Dendritic Growth Induced in Thin Silicon Films by CO_2 Laser Irradiation.
Mock, P.; Bugiel, E.
Inst. for Semicond. Phys., Acad. of Sci., Frankfurt, Germany.
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.
Proceedings of the Conference, 411-14, Vol. 2, 1985.
25-28 Sept. 1984 Dresden, Germany.
Akad. Wissenschaften DDR, Dresden, Germany.

Laser recrystallized silicon films on SiO_2 are a possible material for SOI applications. A 0.5-μm thick polycrystalline silicon film on a SiO_2 layer of 1-μm thickness on bulk silicon is recrystallized with a scanning cw-CO_2 laser working in the TEM_{00} mode. The samples are covered by 1-μm CVD-SiO_2. The irradiation produces a silicon melt, in which homogeneous nucleation occurs and crystallites grow to dimensions up to $150 \times 20 \times 0.5\mu m^3$. The structure of the recrystallized region is investigated by TEM in order to examine the growth process. *IN*

259). Characterization of Laser Recrystallized SOI.
Nakashima, S.
Dept. of Appl. Phys. Osaka Univ., Suita, Japan
Extended Abstracts of the 15th Conference on Solid State Devices and Materials, 39-42, 1983, 30 Aug.-1 Sept. 1983, Tokyo, Japan
Japan Soc. Appl. Phys., Tokyo, Japan

A Raman microprobe technique has been applied to the characterization of laser-annealed polycrystalline silicon films on insulating substrates. The crystalline perfection and residual strain in the annealed films are evaluated by Raman parameters such as the Raman intensity, bandwidth, peak frequency, and polarization properties. The observation has revealed that the crystallinity can be characterized with a spatial resolution of $< 1\mu$m. The structural perfection of lateral seeding epitaxial films has also been examined by the measurements of Raman intensity profile under different polarization configurations. *IN*

• 260). Raman Image Measurements of Laser-Recrystallized Polycrystalline Si Films by a Scanning Raman Microprobe.
Nakashima, S.; Mizoguchi, K.; Inoue,Y.; Miyauchi, M.; Mitsuishi, A.; Nishimura, T.; Akasaka, Y.
Dept. of Appl. Phys., Osaka Univ., Japan
Jpn. J. Appl. Phys. Part 2 (Japan), Vol.25, No.3, L222-4, March 1986

The authors measured two-dimensional Raman intensity images of laser-recrystallized polycrystalline silicon islands on insulators by a scanning Raman microprobe. It is found that crystallites with about 10-μm-size grow along the scanning direction of an annealing laser. The crystallographic orientations of the crystallites have been determined by Raman-microprobe polarization measurements. *IN*

261). Laser Crystallization of Polycrystalline Silicon by Controlling Lateral Thermal Profile.
Nishimura, T.; Akasaka, Y.; Nakata, H.; Sugahara, K.; Isu, T.
LSI Res. & Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan

Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 21-8, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

The thickness variation of the silicon dioxide layer underlying polycrystalline silicon (polysilicon) causes the effective thermal profile in the polysilicon film for controlling the nucleation process during laser recrystallization. The obtainable grains are rectangular in shape as large as 8μm by 500μm. Raman microprobe is used to measure local strain at various points. The observation indicates that the residual tensile stress in the recrystallized silicon films on the structured oxide layer in this study is about 1/3 as small as that in laser-recrystallized polysilicon films on a flat oxide layer. *IN*

262). The Effects of Selectively Absorbing Dielectric Layers and Beam Shaping on Recrystallization and FET Characteristics in Laser Recrystallized Silicon on Amorphous Substrates.
Possin, G.E.; Parks, H.G.; Chiang, S.W.; Liu, Y.S.
General Electric Res. and Dev. Center, Schenectady, NY.
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 549-56, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

Selective absorption, using patterned dielectric films, and beam shaping were used as means for improving the recrystallization of LPCD polysilicon islands on fused quartz. IR imaging of the laser-heated region was used to optimize and control the recrystallization. MOSFETs were fabricated in laser-recrystallized silicon islands on amorphous substrates using a standard n-channel poly-gate process. Devices with various channel lengths and widths were fabricated, and the dependence of threshold voltage, channel mobility, and leakage on recrystallization conditions and device dimensions was studied. *IN*

263). X-Ray Studies of Strain in Laser-Crystallized SOI Films.
Rivier, M.; Reidinger, F.; Goetz, G.; McKitterick, J.
IBM France, Corbeil-Essonnes, France
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 681-5, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

The authors have used x-ray diffraction to measure the strain perpendicular to the substrate surface in laser-crystallized silicon films on oxidized silicon and fused quartz substrates. The dependence of the strain on grain orientation was determined and the influence of the scan speed, the insulating oxide thickness, and subsequent high-temperature exposure was examined. Maximum strain was obtained for grains oriented with the (100) plane parallel to the substrate surface. The strain decreased with increasing angle between the surface plane and the (100) plane of the grains. The stress parallel to the surface in the variously oriented grains was calculated from the stiffness tensor, assuming an isotropic, in-plane stress, and a variation similar to the strain was found. The strain found on oxidized wafers was about half that on fused quartz. Its dependence upon the oxide thickness (0.2 μm to 1.00 μm) was not significant for scan speeds under 10 cm/s. Similarly, the variation in strain with scan speed was very small for speeds below 10 cm/s. Scan speeds above 50 cm/s caused significant increases in the strain. The measured strain was reduced by high-temperature anneals. A 1100°C anneal reduced the average strain by 60% and caused a clear reduction in grain imperfection (as determined by diffracted beam width). However, a 900°C anneal increased the diffracted beam widths even though the average strains was reduced by about 30%. *IN*

264). EBIC Measurement and Grain-Boundary Recombination in SOI Polycrystalline Silicon.
Wu, K.; Dutton, R.W.; Johnson, N.M.
Stanford Electron. Lab., Stanford Univ., CA.
IEEE Trans. Electron Devices (USA), Vol.ED-33, No.7, 1020-7, July 1986

The grain boundary recombination phenomenon in laser-recrystallised silicon-on-insulator (SOI) polycrystalline silicon thin-film material has been measured using the electron-beam-induced-current (EBIC) technique. Unusual EBIC appearances are observed in the arsenic-doped N^+ region. A channel-collection model, based on both experimental evidence and process simulation, is proposed to account for the phenomena. Using this mode, typical values of the effective grain-boundary recombination velocity in the N^+ region are found to be about 10^5 cm/s where grain size is in the range of 1 to 5 μm. *IN*

265). Measurement of Local Stress in Laser-Recrystallized Lateral Epitaxial Silicon Films Over Silicon Dioxide Using Raman Scattering.
Zorabedian, P.; Adar, F.
Hewlett-Packard Labs., Palo Alto, CA.
Appl. Phys. Lett. (USA), Vol.43, No.2, 177-9, 15 July 1983

Raman microprobe measurements of stress have been performed on a laser-recrystallized, seeded, lateral epitaxial silicon film on an oxidized silicon wafer. The direction-averaged, planar tensile stress increased from $2\times10^9 dyn/cm^2$ in the seed region to $5\times10^9 dyn/cm^2$ in the silicon-on-insulator region at distances greater than 20 μm from the seed/silicon-on-insulator boundary. Grain-boundary nucleation observed by optical Nomarski microscopy occurred approximately 11 μm from the seed edge in this film. Depth variations of the stress were observed by comparing measurements using 457-nm and 514.5-nm excitation wavelengths. *IN*

266). High Speed CMOS Devices Fabrication on Laser-Recrystallized Polycrystalline Silicon Island.
Akasaka, Y.; Nishimura, T.; Nakata, H.
Mitsubishi Electric Corp., Itami, Japan
1983 Symposium on VLSI Technology. Digest of Technical Papers, 48-9, 1983
13-15 Sept. 1983, Maui, HI.
Business Centre for Acad. Soc. Japan, Tokyo, Japan

CMOS devices were fabricated on laser-crystallized polysilicon islands. Both n-channel and p-channel MOSFETs having channel length of 2 μm were obtained with good uniformity and reproducibility. 19-stage CMOS ring oscillators with channel lengths of 3 μm were fabricated with a good functional yield. The speed performance was 280 ps/gate. *IN*

267). Integrated MOS Devices in Double Active Layers.
Akasaka, Y.; Kusunoki, S.; Sugahara, K.; Nishimura, T.; Nakata, H.
Mitsubishi Electr. Corp., Hyogo, Japan
1984 Symposium on VLSI Technology. Digest of Technical Papers
90-1, 1984, 10-12 Sept. 1984, San Diego, CA.
Japan Soc. Appl. Phys., Tokyo, Japan

Integrated MOS devices in stacked double active layers were designed and fabricated. The integrated devices consisted of CMOS devices on SOI film formed by the selective laser-recrystallization technique and underlying NMOS devices on bulk silicon. The device structure and processing parameters were carefully determined in order to obtain single-crystalline SOI as a top layer and avoid any influence of the laser recrystallization process on the performance of the already completed NMOS devices on the bottom layer. *IN*

268). Device Performances of a Submicron SOI Technology.
Auberton-Herve, A.J.; Joly, J.P.; Jeuch, P.; Gautier, J.; Hode, J.M.
LETI-IRDI, CEA, Grenoble, France
International Electron Devices Meeting, Technical Digest, 808-11, 1984
9-12 Dec. 1984, San Francisco, CA.
IEEE, New York.

A fully CMOS bulk compatible technology involving the laser zone-melting-recrystallization of silicon-on-insulator has been developed. Using a seeding technique, submicron MOS transistors (L=0.3 μm to 3 μm) have been processed in a grain-boundary-free SOI layer, showing a back leakage current <0.2 pA/μm channel width. A 101-stage ring oscillator exhibited propagation delay per stage of 93 ps for a supply voltage of 5 V. *IN*

269). Subboundary Free Submicronic Devices on Laser-Recrystallized Silicon on Insulator.
Auberton-Herve, A.J.; Joly, J.P.; Hode, J.M.; Castagna, J.C.
CEA, CENG, Grenoble, France
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984
Symposium, 607-12, 26-3, Mater. Res. Soc., Pittsburgh, PA.

Seeding from bulk silicon (lateral epitaxy) has been used in Ar^+ laser recrystallization to achieve subboundary free silicon-on-insulator areas. On these areas CMOS devices have been made using almost entirely the standard processing steps of a bulk micronic CMOS technology. N-MOS transistors with channel length as small as 0.3 μm have shown very small leakage currents. This is attributed especially to the lack of subboundaries. A 40% increase in the dynamic performances in comparison with equivalent size CMOS bulk devices has been obtained (93 ps of delay time per stage for a 101-stage ring oscillator with 0.8 μm of channel length). This is the best result presented

so far for crystallized SOI. No serial requirements are needed in the layout of the circuit with the chosen seed structure. Furthermore, an industrial processing rate for the laser recrystallization processing has been achieved using an elliptical laser beam, a high scan velocity (30 cm/s) and a 100-μm line to line scan step (a 4-in wafer in 4 minutes). *IN*

270). NMOS Silicon Gate Transistors in Large-Area Laser-Crystallised Silicon Layers.
Bosch, M.A.; Chin, G.M.; Herbst, D.; Grogan, J.K.; Lemons, R.A.; Tennant, D.M.; Tewksbury, S.K.
Bell Labs., Holmdel, NJ.
IEE Proc. I (GB), Vol.131, No.4, 121-4, Aug. 1984

The properties of NMOS polycrystalline silicon gate transistors, fabricated in large-area laser-crystallised silicon layers on an insulating substrate, are described. The transistor characteristics reveal the influence of parasitic side transistors. The influence of the side-channel transistors becomes more pronounced with decreasing channel width, and has to be considered in the mobility calculations. The electron mobility is channel-length dependent, and varies from 780 $cm^2/V^{-1}/s^{-1}$ at L=5 μm to 200 $cm^2/V^{-1}s^{-1}$ at L=100 μm. Leakage currents at V_d=4.9 V are typically 15 pA/μm, although 20% of transistors with channel length less than 10 μm show leakage currents in excess of 1 μA. The threshold voltage depends on the drain voltage, as is typical for silicon-on-insulator structures. *IN*

271). Transistors Made in Laser Recrystallized Polysilicon on Insulator Films.
Chandrasekhar, S.; Apte, P.R.; Roy, S.K.
Tata Inst. of Fundamental Res., Bombay, India
Bull. Mater. Sci. (India), Vol.8, No.3, 391-6, June 1986
Proceedings of the Symposium on Thin Film Science and Technology, 9-11 Jan. 1985, India

LPCVD polycrystalline silicon films were deposited on thermally oxidized silicon as well as on LPCVD silicon nitride deposited on silicon. A cw argon ion laser was used to recrystallize the polysilicon film into large grains (grain size from 5 μm to 40 μm). Boron was then implanted and a standard n-channel silicon gate process and a n-channel metal gate process were carried out to realise MOSFETs on this material. Channel mobilities up to $450cm^2/V{\cdot}s$ for electrons have been measured. This thin-film MOSFET has a four-terminal structure with a top and a bottom gate and the influence of one gate on the drain current due to the other gate has been investigated. Comparison of the $I_D - V_D$ curves of the devices with physical models was found in good agreement. *IN*

272). Devices and Circuits in Laser-Crystallized Silicon Thin Films on Fused Silica.
Chiang, A.; Johnson, N.M.
Xerox Palo Alto Res. Center, CA.
Bean, K.E.; Rozgonyi, G.A. (Editors)
VLSI Science and Technology-1984. Proceedings of the Second International Symposium on Very Large Scale Integration Science And Technology.
Materials for High Speed/High Density Applications, 267-71.
6-11 May 1984, Cincinnati, OH.
Electrochem. Soc., Pennington, NJ.

Nearly defect-free silicon thin films on fused silica can be obtained by laser crystallization with a tilted melt interface. Optimization of NMOS thermal cycles has resulted in leakage currents and voltage thresholds appropriate for depletion-load NMOS logic circuits. The ensuing demonstration of the first high-speed dynamic shift registers on bulk amorphous substrate indicates the viability of applying this SOI technology to large-area electronics. *IN*

273). High-Performance Thin Film Transistors in CO_2 Laser Crystallized Silicon on

Quartz.
Chiang, A.; Meuli, W.P.; Johnson, N.M.; Zarzycki, M.H.
Xerox Palo Alto Res. Centers, Palo Alto, CA.
Proc. Spie Int. Soc. Opt. Eng. (USA), Vol.385, 76-9, 1983
Laser Processing of Semiconductor Devices, 18-19 Jan. 1983, Los Angeles, CA.

High-performance thin-film transistors (TFTS) have been fabricated in single-crystal silicon thin films on fused quartz substrates. The single-crystal islands for device fabrication are produced from patterned and encapsulated polysilicon films crystallized with a scanning CO_2 laser. The authors report for the first time their work on depletion-mode as well as enhancement-mode devices fabricated with a polysilicon-gate NMOS process. These devices have channel lengths of 6 to 20 μm. Channel mobilities of $> 900 cm^2/V{\cdot}s$ are again indicative of single-crystal islands. Leakage currents of =1 pA are achieved by back channel ion implantation. Voltage thresholds vary by <0.3 V, and the yield for working devices is 98%. The results anticipate the achievement of a high-performance integrated SOI circuit technology. *IN*

274). NMOS Dynamic Shift Registers in CO_2 Laser-Crystallized Silicon Thin-Films on Fused Quartz.
Chiang, A.; Zarzycki, M.H.; Meuli, W.P.; Johnson, N.M.
Xerox Palo Alto Res. Center, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 119-26, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

High-speed NMOS depletion-load ring oscillators and dynamic shift registers have been fabricated from laser-crystallized silicon thin-film transistors (TFTs) on fused quartz. The authors report on optimization of circuit fabrication process involving ion implantation and high-temperature cycles to achieve inverter gains, logic thresholds, and input noise margins appropriate for logic operation. Characteristics of discrete devices are also used to evaluate a process simulator and a device simulator as tools for future designs. *IN*

275). P-I-N Photodiodes Made in Laser-Recrystallized Silicon-on-Insulator.
Colinge, J.-P.
Hewlett-Packard Labs., Palo Alto, CA.
IEEE Trans. Electron Devices (USA), Vol. ED-33, No. 2, 203-5, Feb. 1986

Lateral p-i-n photodiodes made in laser-recrystallized silicon-on-insulator are investigated. Dark reverse currents of 0.1 pA/μm are obtained (5-V reverse voltage), as well as an efficiency of more than 5% in the green part of the visible spectrum. The influence of a back gate (the mechanical substrate) on the intrinsic zone of the diode is discussed. The carrier lifetime is found to be approximately 8 μs in the intrinsic zone, and the photogenerated current is proportional to incident light power over more than 5 decades. *IN*

276). Transistors Made in Single-Crystal SOI Films.
Colinge, J.-P.; Demoulin, E.; Bensahel, D.; Auvert, G.; Morel, H.
CNET, Meylan, France
IEEE Electron Device Lett., Vol. EDL-4, No. 4, 75-7, April 1983

Test transistors with gate lengths ranging from 10 to 4 μm were made in laser-recrystallized silicon-on-insulator films. A capping layer of patterned antireflecting stripes of Si_3N_4 was used to grow large single crystals of silicon. MOS transistors show good electrical characteristics and a surface mobility up to 650 $cm^2/V{\cdot}s$ for electrons. With the exception of the recrystallization procedure, the wafers followed a fully standard NMOS process, including the growth of a LOCOS field oxide. *IN*

277). Total Dose Radiation-Bias Effects in Laser-Recrystallised SOI MOSFETs.

Davis, G.E.; Hughes, H.L.; Kamins, T.I.
Naval Res. Lab., Washington, DC.
IEEE Trans. Nucl. Sci. (USA), Vol.NS-29, No.6, 1685-9, Dec. 1982
IEEE Annual Conference on Nuclear and Space Radiation Effects, 20-22 July 1982, Las Vegas, NV.

Laser-recrystallised polysilicon over an insulating layer, such as silicon dioxide, provides a new approach for the fabrication of active devices which are dielectrically isolated from the substrate. The authors deal with initial radiation studies for gamma radiation doses from 1 Krad to 1 Mrad(Si) on n- and p-channel MOSFETs fabricated in such laser-crystallised silicon. The n-channel devices were used to investigate the effect of interfacial charge trapping at both the gate oxide- and underlying oxide-recrystallised silicon interface. Data on radiation-induced leakage currents and threshold shifts are presented as a function of radiation dose for worst-case irradiation-bias conditions and for various substrate biases during irradiation. Additionally, the effect of a deep boron implant is presented. *IN*

278). Offset-Gate Structures for Increased Breakdown Voltages in Silicon-on-Insulator Transistors.
Drowley, C.I.; Kamins, T.I.
Hewlett-Packard Lab., Palo Alto, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 133-8, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

An offset-gate structure was used to fabricate p-channel MOS transistors in laser-recrystallized silicon-on-insulator (SOI) films. The breakdown voltage increased from about −18 V with a conventional gate structure to about −38 V with the offset gate and was then limited by bulk breakdown in the film, rather than by the high fields near the gate drain overlap region. Simulations indicate that breakdown voltages of about −60 V can be achieved in the structure used, provided that the back-surface fixed-charge density is limited to $1 \times 10^{11} cm^{-2}$. *IN*

279). A Configurable CMOS SRAM Using a Seeded, Laser Recrystallized Polysilicon on Insulator Process.
Ganousis, D.; Collins, G.; Sritharan, S.; Cooper, D.
Colorado State Univ., Fort Collins, CO.
Proceedings of the IEEE 1986 Custom Integrated Circuits Conference, 55-8, 1986, 12-15 May 1986, Rochester, NY.
IEEE, New York.

A configurable CMOS static random-access memory (SRAM) has been implemented in a seeded, laser recrystallized polysilicon-on-insulator process. In addition to satisfying the design criteria of a fast-access, low-power SRAM circuit design, the silicon-on-insulator bipolar CMOS technique, named CSU/SOI BiCCMOS I, permits elimination of latch-up, increased packing density, and the capability of merging CMOS and bipolar transistors. *IN*

280). Island-Edge Effects of Transistors Fabricated in Large-Area Laser Micro-Zone Crystallized Si on Insulator.
Herbst, D.; Bosch, M.A.; Tewksbury, S.R.
Bell Labs., Holmdel, NJ.
IEEE Electron Device Lett., Vol. EDL-4, No. 8, 280-2, Aug. 1983

Device-quality isolated silicon layers on crystalline silicon wafers have been grown by laser microzone crystallization. Device fabrication revealed that the lateral isolation of devices is nontrivial. Transistors with various edge configurations exhibit very different electrical characteristics.

Parasitic side transistors in island-edge devices are responsible for an early turn-on in n-channel transistors. Their effect has to be taken into account for mobility calculations. *IN*

281). SOI/CMOS Gate Array by Laser Recrystallization.
Izawa, T.; Kawamura, S.; Sasaki, N.; Nakano, M.; Wada, K.; Ashida, M.
IC Dev. Div., Fujitsu Ltd., Kawasaki, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 70-1 supl, 1984, 30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

The authors describe 440-gate CMOS gate arrays fabricated by a laser-recrystallized SOI (silicon-on-insulator) technology for the first time. The gate array has 440 fundamental elements named Basic Cells (BC). A BC consists of two pairs of p-channel and n-channel MOSFETs with L=2.8 μm and W=30 μm. *IN*

282). Single-Crystal Silicon Transistors in Laser-Crystallized Thin Films on Bulk Glass.
Johnson, N.M.; Biegelsen, D.K.; Tuan, H.C.; Moyer, M.D.; Fennell, L.E.
Xerox Palo Alto Res. Center, Palo Alto, CA.
IEEE Electron Device Lett., Vol. EDL-3, No. 12, 369-72, Dec. 1982

High-performance thin-film transistors (TFT) have been fabricated in single-crystal silicon thin films on bulk fused silica. Deposited films of polycrystalline silicon were patterned to control nucleation and growth of single-crystal material in pre-selected areas and encapsulated with a dielectric layer (e.g., SiO_2) in preparation for laser crystallization. The patterned silicon layer was crystallized with a scanning CO_2 laser, which produced islands with preferred crystal orientation. The single crystallinity of the islands was established with transmission electron microscopy after transistor evaluation. The silicon islands were processed with conventional microelectronic techniques to form metal-oxide-semiconductor field-effect transistors operating in the n-channel enhancement mode. The devices display exceptional electrical characteristics with 'low-field' channel mobilities >1000 $cm^2/V{\cdot}s$ and leakage currents <10 pA, for a channel length of 12 μm and width of 20 μm. Achievement of high-performance TFTs with the combined features of microcrack suppression, preferred orientation, and selected-area crystallization render CO_2-laser processing of silicon films a viable and versatile basis for a silicon-on-insulator technology. *IN*

283). Thin-Film Transistors in CO_2-Laser Crystallized Silicon Films on Fused Silica.
Johnson, N.M.; Tuan, H.C.; Moyer, M.D.; Thompson, M.J.; Biegelsen, D.K.; Fennell, L.E.; Chiang, A.
Xerox Palo Alto Res. Centers, Palo Alto, CA.
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 605-11, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

Thin-film transistors (TFT) have been fabricated in scanned CO_2 laser-crystallized silicon films on bulk fused silica. In n-channel enhancement-mode transistors, it is demonstrated that an excessively large leakage current can be electric-field modulated with a gate electrode located beneath the silicon layer. This dual-gate configuration provides direct verification on bulk glass substrates of back-channel leakage as has recently been demonstrated for beam-crystallized silicon films on thermal oxides over silicon wafers. With the application of deep-channel ion implantation to suppress back-channel leakage, high-performance TFTs have been fabricated in single-crystal silicon films on fused silica. The results demonstrate that scanned CO_2 laser processing of silicon films on bulk glass can provide the basis for a silicon-on-insulator technology. *IN*

284). Electrical Characteristics of Three-Dimensional SOI/CMOS ICs.
Kawamura, S.; Sasaki, N.; Iwai, T.; Mukai, R.; Nakano, M.; Takagi, M.

Fujitsu Ltd., Kawasaki, Japan
IEEE Electron Device Lett. (USA), Vol.EDL-5, No.7, 248-50, July 1984

Seven-stage ring oscillators fabricated in the three-dimensional (3-D) structure by using laser recrystallization with a cross-scan method have a propagation delay of 430 ps per stage at 5 V. Uniform operating characteristics and high-speed performance are observed for chips covering a significant portion of 4-in-diameter SOI films, indicating the possibility of 3-D ICs for future VLSIs. The electrical characteristics of devices fabricated in the underlying bulk silicon are not degraded by the recrystallization of the silicon layer directly above. *IN*

285). Laser Recrystallized SOI and Its Application to Three-Dimensional CMOS Integrated Circuits.
Kawamura, S.
IC Dev. Div., Fujitsu Ltd., Kawasaki, Japan.
Nishizawa, J. (Editor)
Semiconductor Technologies 1984, 215-33.
North-Holland, Amsterdam, Netherlands.

Several techniques are presented using laser-beam recrystallization to obtain large-area single-crystalline silicon films over insulators (SOI). These films are of technological interest as a potential material for three-dimensional integration. The techniques utilize either the shaping of the laser beam or varying of the power absorption on various regions of the substrate, leading to enhancement of the crystal growth mechanism of the SOI under laser irradiation. Application of SOI technologies to three-dimensional integrated circuits as well as two-dimensional ones is also presented. A three-dimensional SOI/CMOS ring oscillator fabricated by laser-beam recrystallization exhibits good electrical characteristics with a minimum propagation delay time approaching that of single-crystal Si devices. *IN*

286). 3-Dimensional Gate Array with Vertically Stacked Dual SOI/CMOS Structure Fabricated by Beam Recrystallization.
Kawamura, S.; Sasaki, N.; Iwai, T.; Mukai, R.; Nakano, M.; Takagi, M.
Fujitsu Ltd., Kawasaki, Japan
1984 Symposium on VLSI Technology, Digest of Technical Papers,
44-5, 1984, 10-12 Sept. 1984, San Diego, CA.
Japan Soc. Appl. Phys., Tokyo, Japan

The fabrication of an advanced 3-D device composed of a vertically stacked dual SOI structure is described. To demonstrate the possibility of the practical application of 3-D ICs for future VLSIs, a CMOS gate array cell composed of a 2-input NAND with a dual SOI/CMOS structure has been fabricated by using laser-beam recrystallization and a new contact hole technique. *IN*

287). 3-Dimensional SOI/CMOS IC's Fabricated by Beam Recrystallization.
Kawamura, S.; Sasaki, N.; Iwai, T.; Mukai, R.; Nakano, M.; Takagi, M.
Fujitsu Ltd., Kawasaki, Japan
International Electron Devices Meeting 1983, Technical Digest, 364-7
1983, 5-7 Dec. 1983, Washington, DC.
IEEE, New York.

A three-dimensional CMOS IC with a structure in which one type of transistor is fabricated directly above a transistor of the opposite type with separate gates and an insulator in between has been fabricated using laser-beam recrystallization. Seven-stage ring oscillators fabricated in the 3-D structure have a propagation delay of 430 ps/stage at a supply voltage of 5 V, which is comparable to that of single-crystal Si devices. This CMOS structure and the process technologies developed in this work can be the basis for realizing a multilayered 3-D IC composed of vertically stacked transistors with separate gates and an insulating layer in between. *IN*

288). Vertical Dual Gate CMOS Structure in Two Laser-Recrystallized Silicon Layers Over Oxidized Silicon Substrate.
Kenyon, P.; Dressel, H.; Negri, A.
GTE Labs. Inc., Waltham, MA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 155-60, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

A seven-mask CMOS process that provides vertically integrated structures which joint gates is described. The structures have been characterized as individual NMOS and PMOS transistors. An implant technique is described which may permit the fabrication of fully self-aligned CMOS structure. *IN*

• 289). Gamma-Ray Irradiation Effects on VLSI Geometry MOSFETs Fabricated on Laser Recrystallised SOI Wafers.
Kim, J.S.; Bluzer, N.
Advanced Technol Labs., Westinghouse Electric Corp., Baltimore, MD.
IEEE Trans. Nucl. Sci. (USA), Vol.NS-29, No.6, 1690-5, Dec. 1982
IEEE Annual Conference on Nuclear and Space Radiation Effects, 20-22 July 1982, Las Vegas, NV.

The authors have investigated the effects of radiation on the characteristics of NMOS and PMOS FETs having different channel length (1.3 μm to 5 μm). The FETs were fabricated on SOI wafers where the silicon (0.5-μm) film was laser recrystallised. Gamma-irradiation (up to 200 krad(Si)) was performed at 300 K while the devices were under bias (+10, 0, −10 V). Radiation produced severe increases in the NMOS FET subthreshold leakage currents. Smaller increases with irradiation were observed in the PMOS FET subthreshold leakage currents. Radiation caused increases in the PMOS FET threshold voltage with the largest shifts occurring for the +10 V gate bias. The threshold voltage in NMOS devices decreased with exposure to ionising irradiation. All the observed threshold shifts are consistent with net hole trapping in the SiO_2. They observed a monotonic dependence of the radiation-induced threshold voltage shifts on the channel length of PMOS devices. Smaller threshold shifts were obtained for the short-channel devices. *IN*

290). MOSFETs Fabricated in (100) Single Crystal Silicon-on-Oxide Obtained by a Laser-Induced Lateral Seeding Technique.
Lam, H.W.; Sobczak, Z.B.; Pinizzotto, R.F.; Tasch, A.F., Jr.
Central Res. Labs., Texas Instruments Inc., Dallas, TX.
International Electron Devices Meeting, Technical Digest, 559-61, 1980
8-10 Dec. 1980, Washington, DC.
IEEE, New York.

A laser-induced lateral seeding process has been developed to recrystallize LPCVD polysilicon deposited on a 1-μm thick oxide substrate to form (100) silicon. The lateral seeding is a zone melting process performed in a micro scale. The seed is provided by inducing epitaxial regrowth in selected regions of the deposited polysilicon layer that are in contact with the (100) silicon substrate. The single crystal grows laterally by as much as 80 μm into the oxide substrate region from the epitaxial seed region. N-channel MOSFET devices have been fabricated in the laterally seeded SOI materials. Surface electron mobilities of 540 $cm^2/V{\cdot}s$ have been measured, which is an improvement over that obtained in SOS. *IN*

291). Characterization of SOI Double Si Active Layers Through Fabrication of Elementary Devices.
Miyao, M.; Ohkura, M.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan

Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 269-81, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Various active regions in seeded lateral epitaxial Si layers obtained by cw scanning Ar laser irradiation are characterized by fabricating elementary devices. P-n diodes in the seeding area show a forward current with an ideality factor of 1.2 to 1.4 and a reverse current level of $6\times10^{-8}A/cm^2$ at 0.1 V. Electrical properties of MOSFETs located at the SiO_2 edge are somewhat poor ($\mu = 450cm^2/V\cdot s.$, $V_{th} = 1.0V$) due to the existence of dislocations and residual stress. However, the dislocations escape to the sample surface along the inclined plane of the SiO_2 edge during lateral growth. Thus, no crystal defects are observed in the Si layers grown over the SiO_2. The MOSFETs located on the front and back side of the SOI layer show high electron mobility (600 $cm^2/V\cdot s$) and a reasonable threshold voltage (0.5 V). A novel device structure where the diode forward current is controlled by a MOS gate is also presented. Unsaturated, triode-type characteristics are observed. *IN*

292). Effect of Grain Boundaries on the I-V Characteristics of P-Channel MOSFET/SOI.
Nishimura, T.; Sugahara, K.; Kusunoki, S.; Akasaka, Y.
LSI Res. Dev. Lab., Mitsubsihi Electr. Corp., Itami, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 17th, 147-50, 1985 *CA*

293). Characteristics of Short-Channel MOSFETs in Laser Crystallized Si-on-Insulator.
Ng, K.K.; Celler, G.K.; Povilonis, E.I.; Trimble, L.E.; Sze, S.M.
Bell Labs., Murray Hill, NJ.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
559-65, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Data are reported on short-channel MOSFETs fabricated in laser-crystallized silicon-on-insulator (SOI) structures. In this experiment, special effort was made to minimize enhanced diffusion of dopants from the source-and-drain regions along grain boundaries. Instead of the standard anneal used for the implant activation, rapid thermal annealing and low-temperature furnace annealing was used. These modified processes yielded functional MOSFETs with channel lengths as short as 1.5 μm, and ring oscillators of 2.0 μm. A speed of 115 ps per stage was obtained in these ring oscillators which is not only the fastest ever reported on any SOI structure, but also a factor of 2 faster than that from the same circuits in bulk Si. The results demonstrate quantitatively the speed improvement of SOI over bulk material due to reduced parasitic capacitance. *IN*

294). Comparison of Enhancement/Depletion Inverter Speed in Bulk Si and SOI Circuits.
Ng, K.K.; Taylor, G.W.; Celler, G.K.; Trimble, L.E.; Bayruns, R.J.;
Povilonis, E.I.
Bell Labs., Murray Hill, NJ.
International Electron Devices Meeting 1983, Technical Digest, 356-9
5-7 Dec. 1983, Washington, DC.
IEEE, New York.

The speed performance in bulk Si and SOI structures is compared both experimentally and theoretically, using ring oscillators as a basis for comparison. Short-channel devices were obtained in laser-crystallized poly-Si, using rapid thermal annealing for source-and-drain implant activation to avoid grain boundary diffusion. For a 2.0-μm design rule ring oscillator, a propagation delay per stage of 115 ps was obtained, which is not only the fastest ever achieved with an SOI structure, but also a factor of 2 faster than the same circuit in bulk Si. A recently developed propagation delay

model was applied to analyze the ring oscillator delay for SOI and bulk Si. The results demonstrate quantitatively the speed improvement due to reduced parasitic capacitance in the SOI structure. *IN*

295). High Speed SOI-CMOS Devices by Laser Recrystallization Technique.
Nishimura, T.; Akasaka, Y.; Nakata, H.
LSI Res. & Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 263-8, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

CMOS devices are fabricated on laser-recrystallized polysilicon islands on an insulating layer. Both n-channel and p-channel MOSFETs having a channel length of 2 μm exhibit normal operation by controlling the grain boundary direction in the channel region. The low field electron and hole mobilities are 580 $cm^2/V{\cdot}s$ and 220 $cm^2/V{\cdot}s$, respectively. 19-stage CMOS ring oscillators with nominal channel lengths of 3 μm are fabricated. The minimum propagation delay is 280 ps/stage at supply voltage of 10 V, and the minimum power delay product is 0.13 pJ/stage. *IN*

296). SOI-CMOS Devices on Beam-Recrystallized Polysilicon.
Nishimura, T.; Akasaka, Y.; Nakata, H.
LSI Res. and Dev. Lab., Mitsubishi Electric Corp., Itami, Japan
Microelectron. Eng. (Netherlands), Vol.1, No.3, 209-33, Nov. 1983.

Control of the grain boundary direction in the recrystallized polycrystalline silicon (polysilicon) island is achieved by the direction of the laser scanning. By using this technique, the source-to-drain short in a short-channel MOSFET is almost eliminated, and MOSFETs with channel lengths of 2- to 3-μm level in both n-channel and p-channel mode are fabricated with a good uniformity and reproducibility. The low-field electron and hole mobilities are 580 $cm^2/V{\cdot}s$ and 220 $cm^2/V{\cdot}s$, respectively. 19-stage CMOS ring oscillators with nominal channel lengths of 3 μm are fabricated. The minimum propagation delay is 280 ps/stage at a supply voltage of 10 V, and the minimum power delay produce is 0.13 pJ/stage. *IN*

297). Vertically Integrated MOS Devices With Double Active Layers.
Nishimura, T.; Sugahara, K.; Akasaka, Y.; Nakata, H.
LSI Res. & Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 527-30, 1984, 30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

The integrated MOS device in stacked double active layers is designed and fabricated by using the improved selective laser recrystallization technique and the VLSI technology. The 15-μm wide single-crystalline silicon-on-insulator (SOI) stripes in between straight grain boundaries can be obtained on the already completed MOS devices without any degradation of their electrical characteristics. MOS devices fabricated on this top layer exhibit quite the same electrical characteristics as those of bulk silicon devices, and also the good stability against the potential variation at the underlying device layer. The performance of the MOS devices in double active layers verifies the designed structure and the technologies used in this work provide the good feasibility of the future three-dimensional LSI. *IN*

298). A Three-Dimensional DRAM Cell of Stacked Switching-Transistor in SOI (SSS).
Ohkura, M.; Kusukawa, K.; Sunami, H.; Hayashida, T.; Tokuyama, T.
Hitachi Ltd., Tokyo, Japan
International Electron Devices Meeting, Technical Digest, 718-21, 1985,
1-4 Dec. 1985, Washington, DC.

IEEE, New York.

A new three-dimensional one transistor dynamic RAM cell is presented. It has a trench capacitor fabricated in the Si substrate and a switching transistor fabricated in a laser-induced SOI layer formed on top of the capacitor area. The cell's advantages are a high capacitor capture ratio (capacitor area/cell area) and the possession of high capacitance even when the cell size is reduced to less than 5 μm^2, which is the anticipated size for a 16-Mb DRAM cell. The alpha-particle problem can be overcome by applying the Hi-C structure to the cell. *IN*

299). Moderate Inversion in SOI MOSFETs with Grain Boundaries.
Ortiz-Conde, A.; Fossum, J.G.
Dept. of Electrical Engng., Univ. of Florida, Gainesville, FL.
IEEE Electron Device Lett. (USA), Vol.EDL-4, No.10, 344-6, Oct. 1983

The authors' previous model for effects of grain boundaries on the strong-inversion (linear region) conductance of Silicon-on-Insulator (SOI) MOSFETs (IEEE Trans. Electron Devices, Vol. ED-30, No. 8, pp. 933-940, 1983) is extended to account for moderate inversion. The extension, which is supported by measurement of laser-recrystallized devices, predicts a nearly exponential dependence for the conductance on the (front) gate voltage that is controlled by the grain boundaries. *IN*

300). 1.1 K-Gate CMOS/SOI Gate Array by Laser Recrystallization Technique.
Sakashita, K.; Nishimura, T.; Kusunoki, S.; Kuramitsu, Y.; Akasaka, Y.
Mitsubishi Elec. Corp., Itami, Japan
1985 Symposium on VLSI Technology, Digest of Technical Papers,
32-3, 1985, 14-16 May 1985, Kobe, Japan
Bus. Center Acad. Soc. Japan, Tokyo, Japan

The newly developed selective laser-recrystallization technique has been successfully applied to the fabrication of a 1.1 K-gate CMOS/SOI gate array. The 8-bit parallel array multiplier constructed in this gate array is the first application of CMOS-LSI on a recrystallized SOI. The operation of the 8-bit parallel array multiplier is described. *IN*

301). 3-Dimensional Integration Fabricated by Using Seeded Lateral Epitaxial Film on SiO_2.
Sasaki, N.; Iwai, T.; Kawamura, S.; Mukai, R.; Wada, K.; Nakano, M.
Div. of IC Dev., Fujitsu Ltd., Kasawaki, Japan
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium,
149-54, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Seeded lateral epitaxial laser-recrystallization of silicon film on SiO_2 is applied to fabricate 3-dimensional (3-D) integrations: 3-D CMOS 7-stage ring oscillators. Top p-channel Si-gate SOI MOSFETs are fabricated in the seeded recrystallized silicon directly above bottom n-channel Si-gate bulk MOSFETs with an insulator in between. The recrystallized silicon at the seed region can be utilized for a buried contact to interconnect bottom and top MOSFETs. At the arsenic implantation step to fabricate source and drain of the bottom MOSFETs, ions are not implanted into the seed region to prevent heavy doping and crystal disorder there; otherwise the dopant diffuses laterally and residual crystal disorder disturbs the epitaxial recrystallization. After the laser-recrystallization, the seed region is implanted with phosphorus to interconnect the top and bottom MOSFETs. The Ar^+ laser irradiation is performed with 10 W power, a 50-μm spot size, a 13 cm/s scanning speed and a 13-μm step at 400°C in air. Propagation delay of 460 ps is obtained for the seven stage 3-D CMOS ring oscillator at a power supply voltage of 17 V for a channel length of 3 μm and a channel width of 18 μm. In the seeded SOI films, grain boundary generation and crystal orientation can be controlled. *IN*

302). Three-Dimensional SRAM-Cell Fabricated with a Laser-Recrystallization Technology.
Sasaki, N.; Kawamura, S.; Iwai, T.; Nakano, M.; Wada, K.; Takagi, M.
IC Dev. Div., Fujitsu Ltd., Kawasaki, Japan
Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, 72-3 supl, 1984
30 Aug.-1 Sept. 1984, Kobe, Japan
Business Centre for Acad. Sci. Japan, Tokyo, Japan

SRAM cells have been fabricated with a three-dimensional (3-D) CMOS-IC technology, where an n-channel SOI-MOSFET is fabricated directly above another p-channel bulk-MOSFET insulator in between, for the first time. The memory cell contains 5 MOSFETs. A flip-flop of the memory cell consists of two 3-D inverters and a transfer gate consists of an n-channel SOI-MOSFET placed in the vicinity of the flip-flop. The sense amplifier is also formed with a 3-D inverter. *IN*

303). CMOS/SOI Devices Fabricated on Ar^+ Laser Recrystallized Polysilicon Films.
Shen Zong-yong; Lin Cheng-lu; Zou Shi-chang
Shanghai Inst. of Metall., Acad. of Sinica, China
Acta Electron. Sin. (China), Vol.14, No.2, 30-4, March 1986

CMOS/SOI devices are fabricated on Ar^+ laser recrystallized polysilicon islands on SiO_2 isolating layers. Both n-channel and p-channel MOSFET exhibit good output characteristics. The low field electron and hole mobilities of MOSFET with a channel length of 4 μm are $510cm^2/V{\cdot}s$ and $142cm^2/V{\cdot}s$, respectively. Six-stage CMOS inverters have fine static and transient characteristics. Nine-stage CMOS ring oscillators with p-channel transistors of (W/L)=(112 μm/6 μm) and n-channel transistors of (W/L)=(52 μm/6 μm) are fabricated. The minimum propagation delay is 2.8 ns/stage, and the minimum power delay product is 2.6 pJ/stage. The speed performance of these CMOS/SOI devices is superior to those of the same CMOS devices fabricated on bulk silicon. *IN*

304). Vertical Bipolar Transistors in Laser-Recrystallized Polysilicon.
Sturm, J.C.; Gibbons, J.F.
Stanford Electron. Labs., Stanford Univ., CA.
IEEE Electron Device Lett. (USA), Vol. EDL-6, No.8, 400-2, Aug. 1985

Vertical bipolar n-p-n transistors with a base width of 0.2 μm have been fabricated in laser-recrystallized poly-Si films on thermally oxidized Si substrates. With proper hydrogen-annealing steps, common-emitter current gains on the order of 100 were possible. Recombination in the base-emitter space-charge region was found to be the dominant source of base current. *IN*

305). SOI/SOI/Bulk-Si Triple-Level Structure for Three-Dimensional Devices.
Sugahara, K.; Nishimura, T.; Kusunoki, S.; Akasaka, Y.; Nakata, H.
Mitsubishi Electric Corp., Mizuhara, Itami, Japan
IEEE Electron Device Lett. (USA), Vol. EDL-7, No. 3, 193-5, March 1986

The fabrication procedure of the SOI/SOI/bulk-Si triple-level structure is developed by using the improved selective laser-recrystallization technique and MOS LSI technology. The enlarged crystal stripes sandwiched by straight grain boundaries are produced on the planarized insulating film which overlies the device structure in bulk-Si, and also the SOI/bulk-Si double-layered structure. The basic characteristics of MOSFETs in a triple-level structure are evaluated. *IN*

306). Three-Dimensional CMOS IC's Technology and Characteristics.
Tsien, P.; Ma, T.; Shan, J.; Zhao, Y.; Chen, B.; Lin, H.
Tsinghua Univ., China
Pan Tao T'i Hsueh Pao/Chinese Journal of Semiconductor, Vol. 7, No. 6, 582-588, Nov. 1986

This paper reports a three-dimensional (3-D) CMOS IC technology and characteristics. N-MOS transistors have been fabricated on a p-type single-crystal silicon substrate. P-MOS transistors have been fabricated using n-type silicon-on-insulator films prepared by use of CW Ar^+ laser beam recrystallization. A LPCVD SiO_2 layer is an insulator between N-MOS and P-MOS transistors. Nine-stage 3D-CMOS ring oscillators with a 5-μm channel length are made with a propagation delay of 2.7 ns each. *EI*

307). Characterization of Laser-SOI Double Si Active Layers By Fabricating Elementary Device Structure.
Warabisako, T.; Miyao, M.; Ohkura, M.; Tokuyama, T.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
International Electron Devices Meeting, Technical Digest, 433-6, 1982
13-15 Dec. 1982, San Francisco, CA.
IEEE, New York.

Various active regions in a silicon-on-insulator (SOI) structure, prepared by seeded lateral-epitaxy using a scanned cw Ar laser, are characterized by fabricating MOSFETs and diodes. The MOSFETs on both sides of the SOI layer exhibit a channel mobility of higher than 600 $cm^{-8}A/cm^2$ at 0.1 V. A novel device structure is also presented where the diode forward current is controlled by a MOS gate. *IN*

308). Recrystallization of Silicon Film on Insulating Layers Using a Laser Beam Split by a Birefringent Plate.
Aizaki, N.
Fundamental Res. Labs., NEC Corp., Kawasaki, Japan
Appl. Phys. Lett. (USA), Vol.44, No.7, 686-8, 1 April 1984

20-μm wide, 1-mm long, single-crystal Si films on SiO_2 have been produced using a cw Ar laser beam split by a birefringent quartz plate. The single-scan recrystallized region width has been widened by multiple-beam splitting. The resultant single-crystal region obtained by multiple scan from the seed is a 90-μm wide and 100-μm long area with rare grain boundaries. This split-beam method uses the stable and highly efficient TEM_{00} mode and needs no prepatterned antireflection layers. *IN*

309). Recrystallization of SOI Structures by Split Laser Beam.
Aizaki, N.
Fundamental Res. Labs., NEC, Kawasaki, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 41-6, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

To obtain a large-area recrystallized single-crystal silicon layer on insulator, a birefringent quartz plate has been used to optimize the annealing laser beam shape. 20-μm wide 1-mm long single-crystal Si films on SiO_2 have been produced with a two-peak cw Ar laser beam. The single-scan recrystallized region width has been widened by multiple-beam splitting. Using a four-peak beam, the resultant single-crystal region by multiple scan from the seed is a 100-μm wide and 100-μm long area with rare grain boundaries. This split-beam method uses the stable and highly efficient TEM_{00} mode and needs no pre-patterned antireflection layers. *IN*

310). Adhesion Effects on the Recrystallization of Silicon Films.
Bleil, C.E.; Troxell, J.R.
Dept. of Electron., Gen. Motors. Res. Labs., Warren, MI.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing, Symposium, 687-92, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

Laser processing of thin films of amorphous or polycrystalline silicon on insulator substrates, such as the glass normally used for liquid crystal displays, frequently leads to film thickness variations which are unacceptable for device fabrication. Some thickness variations are caused by the high surface tension of molten silicon and the poor adhesion of the silicon to the substrate. Techniques to reduce this problem by increasing the adhesion of the film to silicon-dioxide-coated Corning 7059 glass substrates have been investigated. Two different approaches were used. First, silicon ions were implanted into the silicon-glass interface to increase the direct bonding of the silicon to the silicon dioxide. Second, layers of material known to exhibit better adhesion to both silicon and silicon dioxide were introduced between the silicon films and the glass substrate. Both techniques produced films which, after subsequent laser processing, showed significantly reduced thickness variations. These procedures make it possible to laser process thin films of silicon on Corning 7059 glass substrates under conditions which produce large grain polysilicon films without producing unacceptably large thickness variations or film cracking. *IN*

311). Influence of Crystalline Structure on Performance of Thin Film Transistors.

Celler, G.K.; Ng, K.K.; Trimble, L.E.; Povilonis, E.I.
AT&T Bell Labs., Murray Hill, NJ.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium,
127-32, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

The authors have developed a procedure to optimize electron mobility and leakage currents in MOSFETs fabricated in laser-recrystallized polysilicon films on SiO_2. A shaped laser beam was used to obtain grain boundaries aligned with the current flow in MOS transistors. To suppress grain boundary diffusion, rapid thermal annealing replaced all high-temperature processing steps subsequent to source-and-drain implantation. By combining these two approaches, functional transistors as short as 1.5 μm were obtained, and also 2-μm-channel 19-state ring oscillators with 115 ps/stage propagation delay. *IN*

312). Fabrication of Thin Silicon-on-Insulator Films Using Laser Recrystallization.
Colinge, J.-P.; Hu, H.K.; Peng, S.
Hewlett-Packard Labs., Palo Alto, CA, USA
Electron. Lett. (GB), Vol. 21, No. 23, 1102-3, 7 Nov. 1985

This paper describes a technique to obtain thin (130-nm) silicon-on-insulator (SOI) films. A 550-nm thick film of silicon is first deposited on an insulating oxide and recrystallized using an argon laser. Owing to the combined use of seeding windows and antireflection patterns, the recrystallized film is single crystal. The SOI film is then planarised using thick resist spinning and plasma etch. Finally, the film thickness is reduced to 130 nm by thermal oxidation. *IN*

313). Growth of Large Areas of Grain Boundary-Free Silicon-on-Insulator.
Colinge, J.-P.; Bensahel, D.; Alamome, M.; Haond, M.; Pfister, J.C.
CNET, Meylan, France
Electron. Lett. (GB), Vol.19, No.23, 985-6, 10 Nov. 1983

A technique combining a raster laser scan, selective annealing using patterned antireflection stripes and a seeding window has been successfully used to grow large single crystals of silicon-on-insulator. The raster-scanned laser spot simulates an advancing linear heat source and the antireflection stripes modulate the trailing edge in such a way that parasitic random nucleation is avoided. The seeding gives the film its crystal orientation. *IN*

314). Transistors Made in Single-Crystal SOI Films.
Colinge, J.-P.; Demoulin, E.; Bensahel, D.; Auvert, G.
CNET, Meylan, France
J. Phys. Colloq. (France), Vol. 44, No. C-5, C5/409-13, Oct. 1983
Laser-Solid Interactions and Transient Thermal Processing of Materials,
25-27 May 1983, Strasbourg, France

Transistors have been realized in laser-recrystallized silicon-on-insulator films. Antireflecting stripes of silicon nitride were used to shape the trailing edge of the silicon as it quenches under laser scan which allows accurate control of the grain boundary location. The grain boundaries were oxidized into a standard LOCOS process which left single-crystal silicon stripes completely embedded in the oxide. N-channel transistors as well as ring oscillators were made in the recrystallized material. A surface mobility of 650 $cm^2/V{\cdot}s$ was observed in the transistors, and a 1-ns delay per stage was measured in the ring oscillators (L=5 μm). *IN*

315). The Use of Selective Annealing for Growing Very Large Grains in Silicon on Insulator Films.
Colinge, J.-P.; Demoulin, E.; Bensahel, D.; Auvert, G.
CNET, Meylan, France

Jpn. J. Appl. Phys. Suppl. (Japan), 205-8, 1982
Proceedings of the 14th Conference (1982 International) on Solid State Devices, 24-26 Aug. 1982, Tokyo, Japan

The selective annealing technique (laser annealing under patterned antireflecting coating) has been successfully applied to the growth of very large (20 μm 3000 μm) silicon single crystals. The grain boundary location is controlled by a conventional lithography step, and the grains obtained have a nearly perfect rectangular shape. *IN*

316). Use of Selective Annealing for Growing Very Large Grain Silicon on Insulator Films.
Colinge, J.-P.; Demoulin, E.; Bensahel, D.; Auvert, G.
CNET, Meylan, France
Appl. Phys. Lett. (USA), Vol.41, No.4, 346-7, 15 Aug. 1982

The selective annealing technique (laser annealing under a patterned antireflecting coating) has been successfully applied to the growth of very large (20 by 400 μm) silicon single crystals on SiO_2. The grain boundary location is controlled by a conventional lithography step, and the grains obtained have a nearly perfect rectangular shape. *IN*

317). Oxygen and Nitrogen Incorporation During CW Laser Recrystallization of Polysilicon.
Drowley, C.I.; Kamins, T.I.
Hewlett-Packard Labs., Palo Alto, CA.
Narayan, J.; Brown, W.l.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 511-16, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

The incorporation of nitrogen and oxygen in polysilicon has been examined by SIMS. The analysis, combined with C-V measurements and ion implantation, has been used to correlate the incorporation of the two species with the fixed-charge density at the back polysilicon/SiO_2 interface. Laser recrystallization with a silicon-nitride encapsulation layer results in the inclusion of 2 to $4\times10^{17}cm^3$ nitrogen atoms in the polysilicon. If an oxide capping layer is used, the nitrogen level observed is at the background of the SIMS system ($= 10^{15}cm^{-3}$). Either type of capping layer results in 3 to $4\times10^{18}cm^{-3}$ oxygen atoms being incorporated into the polysilicon. Implantation of nitrogen into the polysilicon before recrystallization increases the fixed-charge density ($N_{f,b}$) at the back interface, while implanted oxygen decreases $N_{f,b}$. The high $N_{f,b}$ found with a nitride capping layer is attributed to deposition of nitrogen of SiN_x at the back interface. *IN*

318). CO_2 Laser Recrystallization of LPCVD Polysilicon.
Dudenis, J.; Pranevicius, L.; Urbelis, A.
Kaunas Politech. Inst., USSR
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.
Proceedings of the Conference, 415-19, Vol.2, 1985
25-28 Sept. 1984, Dresden, Germany
Akad. Wissenschaften DDR, Dresden, Germany

Laser recrystallization of polysilicon on insulating substrates (SOI) is a widely recognized technique. The use of cw CO_2 laser ($\lambda = 10.6\mu m$) to produce SOI structures is quite rare, although promising results have been achieved in the recrystallization of polysilicon on absorbing quartz or using a tuned 9.3-μm CO_2 laser to heat SiO_2 layers surrounding polysilicon. Also CO_2 laser annealing (LA) of ion implantation damage in crystal Si has proved to be successful. The main problem concerning cw CO_2 LA is poor energy absorption which is sometimes enhanced using thermal preannealing or UV light. Low-pressure chemical-vapour-deposited (LPCVD) polysilicon was produced at 650°C on 0.25-μm thick SiO_2 thermally grown on (100) silicon wafers. Polysilicon layers were made 0.4

and 0.8 μm thick. Laser annealing was performed in the air with a cw CO_2 laser having maximum output power of 31 W. *IN*

319). CW Argon(1+) Laser Crystallization of Hydrogenated Amorphous Silicon on Insulating Substrates.
Huang, X.; Bao, X.; Chen, J.; Gao, W.
Dep. Phys., Nanjing Univ., Nanjing, Peop. Rep. China
Nanjing Daxue Xuebao, Ziran Kexue, Vol. 22, No. 4, 695-700, 1986

Hydrogenated amorphous Si produced by glow discharge was crystallized by cw Ar^+ laser. The structure and morphology of the crystallized film were examined by optical microscopy and TEM, and plasma etching was used to determine the degree of crystallization. The substrate temperature during crystallization was 240°C. The laser-beam spot size was 40μm with $\sim$ 50% overlap. The structure of the crystallized film depends on substrate temperature, and laser power conditions for producing polycrystalline Si film for SOI devices were discussed. *CA*

320). Recrystallization of Silicon on Insulator With a Heat-Sink Structure.
Kawamura, S.; Sasaki, N.; Iwai, T.; Nakano, M.; Takagi, M.
IC Dev. Div., Fujitsu Ltd., Kawasaki, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 67-84, 1985, 20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

A new method for obtaining complete single-crystalline silicon films on SiO_2 with cw-Ar laser recrystallization is presented. The method utilizes the difference in thermal resistivity between the device regions with thin SiO_2 layers which act as a heat-sink and the surrounding regions with thick SiO_2 layers, thus controlling the nucleation and growth during resolidification process. 19-stage SOI/CMOS ring oscillators fabricated in the heat-sink structure have a propagation delay of 950 ps per stage at a supply voltage of 7 V. These results indicate that desired control of thermal profiling during resolidification process can be achieved by adjusting the structure of SOI. *IN*

321). Laser Recrystallization of Si Over SiO_2 with a Heat-Sink Structure.
Kawamura, S.; Sasaki, N.; Nakano, M.; Takagi, M.
Fujitsu Ltd., IC Dev. Div., Kawasaki, Japan
J. Appl. Phys. (USA), Vol.55, No.6, Pt.1, 1607-9, 15 March 1984

Complete single-crystalline silicon films over SiO_2 have been produced with a heat-sink structure designed for best utilization of temperature gradients during resolidification process induced by an incident cw Ar laser beam. The structure includes device regions with thin SiO_2 layers which act as a heat sink to the substrate and the peripheral regions with thick SiO_2 layers. By using this technique, residual grain boundaries in the laser recrystallized silicon over insulator can be eliminated. N-channel metal-oxide-semiconductor field-effect transistors fabricated in the recrystallized silicon films with a heat-sink structure exhibit good device characteristics, having a surface electron mobility of 500 $cm^2/V{\cdot}s$ which is comparable to that of bulk devices. *IN*

322). Effect of Oxygen in Atmosphere on (100) Texture of Laser-Recrystallized Silicon on Fused Quartz.
Kimura, M.; Egami, K.; Kanamori, M.
Fundamental Res. Labs., NEC Corp., Kanagawa, Japan
Appl. Phys. Lett. (USA), Vol.46, No.1, 57-9, 1 Jan. 1985

Effect of oxygen in an atmosphere on (100) texture formed by laser melting has been quantitatively examined using x-ray diffraction method. It has been found that oxygen content over several percentage is necessary to be included in an atmosphere during recrystallization for preventing the agglomeration of silicon and achieving strong (100) texture, but that capping with an SiO_2 layer

does not induce such strong (100) texture as that produced with air and no capping. An oxide layer seems not to be necessarily important for strong (100) texture formation. *IN*

323). Study on the Transitional Seeded Crystallization Variation of Silicon on Insulator Using Gaussian Laser Beams.
Lee, E.-H.
Monsanto Electron. Mater. Co., St. Peters, MO.
J. Appl. Phys. (USA), Vol.59, No.1, 263-5, 1 Jan. 1986

Variable distances of the transitional, defect-free, seeded crystallization of thin-film silicon on insulating substrates have been investigated using energy beams of Gaussian intensity distribution. Phenomenologically, defect-free crystals from the seed have been found to form Gaussian-like contours with respect to sub-boundary-laced crystals. The results are attributed to the thermal gradient effect upon the crystallization stability. This study bears a significant implication in the current efforts to increase the sub-boundary-free crystalline region over extended distances. *IN*

324). Lateral Epitaxy of SOI Under Laser Radiation.
Lin Huiwang; Tsien Peihsin; MA Tengge; Li Zhijian
Inst. of Microelectronics, Tsinghua Univ., China
Chin. J. Semicond. (China), Vol.4, No.3, 287-90, May 1983

The cw-Ar^+ laser recrystallization of polysilicon-on-oxide with lateral seed is investigated. The experimental results show substantial effects of laterally seeded epitaxy. The largest grains observed are about 50 μm by 40 μm. The recrystallized silicon layer has the same orientation with the seed; their orientations are all (100). The increasing of grain size after laser recrystallization without lateral seed is also observed, but the crystal orientations are random. *IN*

325). Indirect Laser Annealing of Polysilicon for Three-Dimensional IC's.
Mukai, R.; Sasaki, N.; Iwai, T.; Kawamura, S.; Nakano, M.
Fujitsu Ltd., Kawasaki, Japan.
International Electron Devices Meeting 1983, Technical Digest, 360-3,
5-7 Dec. 1983, Washington, DC.
IEEE, New York.

A laser-annealing technique for producing single-crystal silicon islands on an amorphous insulating layer has been developed using a Si cap for three-dimensional ICs. A stable temperature gradient eliminates grain boundaries in recrystallized Si islands; the interior of the islands is kept cooler than the periphery and crystal growth begins from the interior. This temperature gradient is realized because the Si islands are indirectly heated by an argon ion laser beam. Laser power is absorbed in a Si cap and heat flow to the Si islands takes place laterally as well as vertically through a separation cap from the high-temperature Si cap. Field-effect mobility of 460 $cm^2/V{\cdot}s$ is obtained for SOI/MOSFETs fabricated in the silicon islands. *IN*

326). Single Crystalline Si Islands on an Amorphous Insulating Layer Recrystallized by an Indirect Laser Heating Technique for Three-Dimensional Integrated Circuits.
Mukai, R.; Sasaki, N.; Iwai, T.; Kawamura, S.; Nakano, M.
Fujitsu Ltd., Kawasaki, Japan
Appl. Phys. Lett. (USA), Vol.44, No.10, 994-5, 15 May 1984

A new laser-recrystallizing technique for producing single-crystalline Si islands on an amorphous insulating layer has been developed. Si islands are recrystallized by indirect Ar ion laser heating utilizing a Si cap. This technique is an effective recrystallizing method for fabricating three-dimensional integrated circuits. During recrystallization, this technique easily and stably produces a desired temperature profile to eliminate grain boundaries in recrystallized Si islands; the interior of the Si islands is kept cooler than the periphery and crystal growth begins from the interior. This desired temperature profile is realized because an Ar ion laser power is absorbed in the Si

cap and heat flow takes place to the Si islands laterally as well as vertically from the heated Si cap through a separation cap. Damage to the underlying layer is not observed, which suggests that the laser-beam power is cut in the Si cap. No grain boundaries are observed in more than 90% of the Si islands recrystallized with such an arrangement that laser-beam traces include Si islands; the size of the islands is 20 by 60 μm. Field-effect mobility of 460 $cm^2/V{\cdot}s$ is obtained for Si on insulator/metal-oxide-semiconductor field-effect transistors fabricated in the recrystallized Si islands with this technique. *IN*

327). Single Crystalline SOI Square Islands Fabricated by Laser Recrystallization Using a Surrounding Antireflection Cap and Successive Self-Aligned Isolation Utilizing the Same Cap.
Mukai, R.; Sasaki, N.; Iwai, T.; Kawamura, S.; Nakano, M.
Div. of IC Dev., Fujitsu Ltd., Kawasaki, Japan
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing, Symposium, 663-8, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

A new laser recrystallizing technique has been developed for high density SOI-LSIs. This technique produces single-crystalline silicon islands on an amorphous insulating layer without seed. Square windows are opened at arbitrary places in an antireflection cap over a polycrystalline film on an amorphous insulating layer. Grain boundaries of the polycrystalline Si in the window are removed completely at the subsequent laser-recrystallization step. Single-crystalline silicon islands are formed by self-aligned etching of the silicon films which was covered by the antireflection cap. This technique is an effective method for fabricating high density SOI-LSIs, since the single-crystalline islands can be fabricated at arbitrarily selected places. Yield of the grain-boundary-free islands was 95%; the size of the island is 10 by 20 μm, and the irradiation overlap of laser-beam traces is 70%. *IN*

328). Study of the Laser-Recrystallized Film with a Control of Grain Boundary Location by Using Surrounding Antireflection Cap Method.
Mukai, R.; Sasaki, N.; Nakano, M.
Fujitsu Ltd, Kawasaki, Japan
Journal of Electronic Materials, Vol. 15, No. 6, 339-343, Nov. 1986

A modified technique for unseeded laser-recrystallization of poly-crystalline silicon films deposited on amorphous insulators has been developed whereby grain boundary location in the recrystallized silicon film can be controlled. In this technique, the silicon film is encapsulated with an antireflection cap with windows and then recrystallized by cw-Ar ion laser irradiation. Grain boundaries are removed from the silicon film at the place where the window is opened because of a temperature gradient due to a change in laser-beam absorption in the silicon film. The $< 100 >$ texture is observed in the grain-boundary-free areas although the silicon shows $< 110 >$ texture before the recrystallization. An SOI/MOSFET has been fabricated in the recrystallized film. The channel regions of MOSFET's are aligned in the window regions. Field-effect mobility of 490 cm^2/V-s is obtained for n-channel MOSFETs. Source-to-drain leakage current of 5 $fA/\mu m$ is obtained at drain voltage of 5 V and back-gate voltage of -100 V for the $W/L = 10\ \mu m/2\mu m$ MOSFET. *EI*

329). Minimization of Residual Stress in SOI Films by Using AlN Interlaid Insulator.
Ogura, A.; Egami, K.; Kimura, M.
Fundamental Res. Lab., NEC Corp., Kawasaki, Japan
Jpn. J. Appl. Phys. Part 2 (Japan), Vol.24, No.8, L669-71, Aug. 1985

It was found that residual stress in SOI film recrystallized by laser annealing depends on both substrates and interlaid insulator materials. For a stress-free Si film, a thermal expansion coefficient of the underlaid material, comprising of a substrate and an interlaid insulator should be slightly

larger than that of Si. AlN was found to be a very effective interlaid insulator. In the structure of resolidified-Si/3-μm thick insulator/Si substrate, the residual stress in SOI films on AlN ($5 \times 10^9 dyn/cm^2$) was lower than that on SiO_2 ($7 \times 10^9 dyn/cm^2$). *IN*

330). Laser Annealing of Polysilicon Films with an Applied Electric Field.
Okamoto, K.; Suzunaga, H.; Kitagawa, Y.
Univ of Electro-Communications, Faculty of Communication Engineering, Chofu, Japan
Electron Commun. Japan, Part 2, Vol. 69, No. 1, 37-42, 1986 *EI*

331). Orientation Controlled SOI by Line-Shaped Laser-Beam Seeded Lateral Epitaxy for CMOS Stacking.
Ohkura, M.; Kusukawa, K.; Sunami, H.; Tokuyama, T.
Cent. Res. Lab., Hitachi Ltd., Kokubunji, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 17th, 143-6, 1985 *CA*

332). Reduced Subboundary Misalignment in SOI Films Scanned at Low Velocities.
Pfeiffer, L.; West, K.W.; Joy, D.C.; Gibson, J.M.; Gelman, A.E.
AT&T Bell Lab., Murray Hill, NJ
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 29-38, 1986

Silicon-on-insulator (SOI) films on SiO_2 scan-melted at low velocities (20 to 300 μm/s) with reduced thermal gradients at the melt-freezing interface have qualitatively different properties from similar films melt-scanned at higher gradients and scan velocities. The transition between the two regimes appears to be abrupt. Scanning at intermediate velocities often results in an admixture of patches containing one or the other type of material. The slow scan regime is characterized by long straight non-branched subboundaries having a lateral spacing 50 to 60 μm, and very small tile misalignments of ≤ 0.1. These slow scan subboundaries consist largely of threading dislocations in contrast to conventional subboundaries which are tilt boundaries of ≤ 3 °C and typically consist of edge dislocations running in the plane of the film. *CA*

333). Addressing the Problems of Agglomeration, Surface Roughness and Crystal Imperfection in SOI Films.
Ramesh, S.; Martinez, A.; Petruzzello, J.; Baumgart, H.; Arnold, E.
Philips Lab., North Am. Philips Corp., Briarcliff Manor, NY
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 45-51, 1986

Under a wide variety of laser-recrystallization conditions, a reliable encapsulation structure that prevents agglomeration and enables recrystallization of SOI (Si-on-insulator) films over a 100% wafer area was designed and experimentally tested. The experiments indicate that the wetting characteristics of the structure can also improve the surface planarity of the recrystallized Si. A dramatic reduction in defect density and the nonoccurrence of the characteristic branched subgrain boundary pattern under appropriate conditions of laser recrystallization is reported. *CA*

334). Melt-Width Enhancement in the Recrystallization of Polycrystalline Silicon-on-Insulator by Twin-Laser-Beam-Induced Substrate Interheating.
Sasaki, N.; Mukai, R.; Izawa, T.; Nakano, M.; Takagi, M.
IC Dev. Div., Fujitsu Ltd., Kawasaki, Japan
Appl. Phys. Lett. (USA), Vol.45, No.10, 1098-100, 15 Nov. 1984

A new method to recrystallize polycrystalline silicon on amorphous insulating layers is developed using twin cw argon laser beams. It is found that the melt width of twin beams can exceed that of a single beam by a factor of 4. This effect is explained by a model of substrate interheating between

twin laser spots. Using this technique, a large silicon single-crystalline grain as large as 1.8 mm long and 20 μm wide was obtained on thermal-oxide-coated silicon wafers even for the substrate kept at room temperature during laser irradiation. *IN*

335). Polycrystalline Silicon Recrystallization by Combined CW Laser and Furnace Heating.
Shappir, J.; Adar, R.
School of Appl. Sci. and Technol., Hebrew Univ. of Jerusalem, Jerusalem, Israel
J. Electrochem. Soc. (USA), Vol.131, No.4, 902-5, April 1984

A modified cw argon laser-induced lateral recrystallization of polycrystalline silicon is described. Holding the sample in a furnace at elevated temperature of about 1000°C resulted in significantly reduced thermal gradients and stresses. A wider range of power is allowed for proper recrystallization both on oxide and substrate areas simultaneously. Preferred thermal profiles enabled larger lateral epitaxy of 50 μm per single scan. The higher substrate temperature resulted also in wider melted areas and high scan rates of 80 cm/s enabling much shorter processing time. *IN*

336). Laser Recrystallized CMOS/SOI Devices.
Shen Zong-yong; Lin Cheng-lu; Fang Fang; Zou Shi-chang
Shanghai Inst. of Metall., Acad. Sinica, China
Kexue Tongbao (Sci. Bull.) (China), Vol.31, No.15, 1070-3, Aug. 1986

SOI (silicon-on-insulator) is an ideal material for developing high-speed complementary metal-oxide-semiconductor and three-dimensional large-scale integrated circuits. The authors have made use of a cw Ar^+ laser to recrystallize polysilicon films on SiO_2 insulating layers. The experimental results show a significant increase in grain size from 200 to 500 Å to 20 to 30 μm in length and 5 to 10 μm in width and an improvement in electrical properties. The surface smoothness of the recrystallized polysilicon films meets the requirement of the planar technology of silicon integrated circuits. 6-stage CMOS inverters and 9-stage CMOS ring oscillators were successfully fabricated on the laser recrystallized polysilicon. *IN*

337). Lateral Impurity Transport in Silicon Films on Insulators During Laser Recrystallization.
Sugahara, K.; Nishimura, T.; Akasaka, Y.; Nakata, H.
LSI Res. & Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan
Appl. Phys. Lett. (USA), Vol.48, No.5, 356-8, 3 Feb. 1986

The lateral transport of dopants in silicon films on insulators during laser recrystallization is investigated. The dopants implanted locally in silicon films on insulators are found to be transported in the forward direction of the laser scan as well as in the backward direction. Both transport lengths from the originally implanted region are measured as a function of the laser scan velocity. The transport mechanism is explained by taking into account a liquid phase diffusion and a segregation of impurities depending on the crystallization speed. The diffusion coefficients of $(1.2 \pm 0.2) \times 10^{-4}$ and $(1.3 \pm 0.4) \times 10^{-4} cm^2/s$ for arsenic and boron, respectively, in molten silicon are obtained. *IN*

338). Orientation Control of SOI Film by Laser Recrystallization.
Sugahara, K.; Kusunoki, S.; Inoue, Y.; Nishimura, T.; Akasaka, Y.
LSI Res. Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan
Ext. Abstr. Conf. Solid State Devices Mater., 18th, 565-8, 1986 *CA*

339). Recrystallization of Thin Polycrystalline Films Using CO_2-Laser Beam Irradiation.
Tillack, B.; Reinboth, R.; Mock, P.; Bugiel, E.; Winkler, R.
Inst. for Semicond. Phys., Acad. of Sci., Frankfurt, Germany
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.

Proceedings of the Conference, 406-10, Vol.2, 1985
25-28 Sept. 1984, Dresden, Germany
Akad. Wissenschaften DDR, Dresden, Germany

Recently, the recrystallization of thin amorphous or polycrystalline films has been the subject of numerous investigations with the aim of producing large-area single-crystalline silicon on insulating layers (SOI). The authors study the application of CO_2 lasers to lateral melting of silicon on SiO_2-coated wafers. *IN*

340). A Seeded Channel Approach to Silicon-on-Insulator Technology.
Ting, C.H.; Baerg, W.; Lin, H.Y.; Siu, B.; Hwa, T.; Sturm, J.C.; Gibbons, J.F.
Intel Corp., Santa Clara, CA
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 77-82, 1986

A seeded channel approach was developed to avoid the shortcomings of the conventional SOI (Si-on-insulator) structure such as grain or sub-grain boundaries in the channel region, floating substrate effects, etc. The gate of each FET is located above its own seed window to ensure that single-crystalline material is obtained for the channel region. The source and drain regions, however, are located in the recrystallized Si over SiO_2 for improved isolation and minimizing junction capacitance. Recrystallization was obtained in 4-in Si wafers by using an Ar laser and a computer-controlled x-y stage with heated substrate holder. Problems encountered in laser recrystallization, such as reflectivity variations over seed and SOI regions, surface ripples, pittings, etc., were eliminated by optimizing the thin-film thickness of the isolation oxide, polysilicon, and the capping oxide. This technology was used successfully to fabricate FET devices by using a standard production n-MOS process. Good device characteristics were obtained by using 400 Å gate oxide and channel length of 1 to 50 μm. The measured electron mobility in the channel region is, however, still lower than the ideal bulk values. *CA*

341). Growth Mechanisms and Defects in Si Layers Grown on SiO_2 by Bridging (Lateral Seeded) Epitaxy.
Tokuyama, T.; Tamura, M.; Natsuaki, N.; Ohkura, M.; Ichikawa, M.; Miyao, M.
Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 3-19, 1985
20-24 June 1983, Oiso, Japan

Mechanisms for lateral seeding growth of Si layers on SiO_2, and defect structures in the regrown layers are discussed based on TEM and micro-probe-RHEED observations. The seeding area essential for lateral epitaxial growth is found to be as small as 0.5 μm wide. It is also found that defects in the regrown layers are related to the time interval during cooling, but are also related to sample structure and laser irradiation conditions. Using 1- to 2-μm (size and spacing) circular or square seeding patterns, uniform and defect-free regrown layers are developed over a considerably large surface area. *IN*

342). Laser Annealing Method.
Tsuya, H.
NEC Corp., Tokyo, Japan
Oyo Buturi (Japan), Vol.53, No.1, 31 Jan. 1984

Laser-annealing equipment for silicon-on-insulator (SOI) device fabrication is described which is equipped with a television monitor for recrystallization process observation. Major parameters affecting the temperature distribution on a specimen are beam-spot diameter, irradiation intensity

distribution, scanning speed, and substrate heating temperature. Beam scanning on the equipment is performed by moving its scanning optical system by means of a motor. *IN*

343). In Situ Investigation of Controlled Explosive Crystallization Processes in Amorphous Silicon Layers.
Wagner, M.; Glaser, E.; Andra, G.; Gotz, G.
Friedrich-Schiller-Univ., Jena, Germany
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.
Proceedings of the Conference, 485-91, Vol.2, 1985
25-28 Sept. 1984, Dresden, Germany
Akad. Wissenschaften DDR, Dresden, Germany

SOI-techniques are of growing interest with regard to a production of IC-configurations with several active layers. Explosive crystallization processes in amorphous silicon layers might provide a technology to realize single-crystalline layers on amorphous substrates. For controlling such processes, it is necessary to understand the dynamics of the crystallization process and the phase front movement as well as the ignition conditions. Due to the high speed of explosive crystallization for an investigation, suitable in-situ techniques are required. Using time-resolved reflectivity measurements (TRRM), it is possible to determine the velocity of moving phase fronts and the temperature during explosion. Recently, the velocity under cw-laser irradiation was measured by studying the crystal structure in dependence on the scanning parameters. However, the yield of precise data on the dependence of the crystallization velocity on the temperature, the heat losses, the latent heat available, and other parameters requires a large-area heating of the amorphous layer combined with a controlled ignition of the explosion. The present paper presents a special irradiation and testing technique to solve these problems. *IN*

344). Beam Shaping for CW Laser Recrystallization of Polysilicon Films.
Zorabedian, P.; Drowley, C.I.; Kamins, T.I.; Cass, T.R.
Hewlett-Packard Labs., Palo Alto, CA.
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials,
523-8, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

A shaped laser beam has been used for laterally seeded recrystallization of polysilicon films over oxide. Direct maps of the shaped-beam intensity distribution in the wafer plane are correlated with the grain structure of the recrystallized polysilicon. Using 60% overlapping of shaped-beams scans along (100) directions, the authors have obtained seeded areas one mm wide and 50 to 500 μm long. These consist of 40-μm wide adjacent single-crystal strips regularly separated by low-angle grain boundaries extending laterally away from the seed openings. The spacing between grain boundaries is equal to the scan spacing, providing a means for controlling the location of grain boundaries in otherwise defect-free, single-crystal films. *IN*

345). Laser Scan Registration for Lateral Epitaxy of Silicon-on-Insulator Stripes on Silicon Substrates.
Zorabedian, P.; Kamins, T.I.; Drowley, C.I.
Hewlett-Packard Labs., Palo Alto, CA.
J. Appl. Phys. (USA), Vol.57, No.12, 5262-7, 15 June 1985

An improved technique for seeded laser recrystallization of silicon-on-insulator stripes has been developed using a slanted elliptical beam and a computer-controlled system to register laser scans to alignment marks on the silicon wafer. After the wafer position is automatically determined by searching for alignment marks with a low-power beam, a raster is generated parallel to the device features, and the aligned laser beam is swept across the wafer. The dependence of the defect

structure of the recrystallized films on the parameters used for scanning and the resulting thermal gradients are defect-free, single-crystal silicon films over oxide stripes up to 65 μm wide have been obtained. *IN*

346). Lateral Seeding of Silicon-on-Insulator Using an Elliptical Laser Beam: A Comparison of Scanning Methods.
Zorabedian, P.; Kamins, T.I.
Hewlett-Packard Labs., Palo Alto, CA.
Lam, H.W.; Thompson, M.J. (Editors).
Comparison of Thin Film Transistor and SOI Technologies Symposium, 81-6
26-28 Feb. 1984 Albuquerque, NM.
North-Holland, New York.

Two scanning methods for laterally-seeded recrystallization of striped silicon-on-insulator/seed structures with an elliptical laser beam are discussed. One method requires repeated remelting of the silicon film and is controlled by the temperature of the substrate, which is locally heated by the beam. This method results in very few defects and single-crystal silicon-on-insulator stripes up to 50 μm wide. The second method involves little remelting and is primarily controlled by the lateral offset of the beam with respect to the stripes. Single-crystal silicon-on-insulator stripes up to 40 μm wide have been obtained, with defects consisting primarily of stacking faults and twins, as well as some grain boundaries. These defects show little effect on MOS transistor leakage current. *IN*

347). Zone-Melting Recrystallization of Thick Silicon on Insulator Films.
Atwater, H.A.; Smith, H.I.; Thompson, C.V.; Geis, M.W.
Dept. of Electrical Engng. and Computer Sci., MIT, Cambridge, MA.
Mater. Lett. (Netherlands), Vol.2, No.4A, 269-73, March 1984

The authors report 'unseeded' zone-melting recrystallization of encapsulated Si films, up to 60 μm thick, on SiO_2. The crystallographic texture of the films changes from (100) to random as the thickness is increased beyond 5 μm. The subboundary spacing increases with film thickness and two regimes of thickness dependence are observed. They report a vertical-constriction patterning technique which enables a uniform (100) texture to be achieved in thick films. *IN*

348). Annealing of Ion-Implanted Silicon-on-Insulator Films Using a Scanned Graphite Strip Heater.
Banerjee, S.K.; Lee, B.; Baker, J.E.; Reed, D.A.; Streetman, B.G.
Dept. of Electrical Engng., Univ. of Illinois at Urbana-Champaign, Urbana, IL.
Thin Solid Films (Switzerland), Vol.115, No.1, 19-26, 4 May 1984

Solid-phase and liquid-phase incoherent radiation annealing of boron- or phosphorus-implanted silicon-on-oxide films using a scanning graphite-strip heater has been examined. Excellent electrical activation with little dopant redistribution is observed for solid phase transient annealing. The silicon films are uniformly doped on liquid phase annealing. An absence of zone-refining effects during liquid-phase annealing is observed and is attributable to the high scan velocities employed during the annealing process. *IN*

349). Twin Stabilized Planar Growth of SOI Films.
Baumgart, H.; Phillipp, F.; Ramesh, S.; Khan, B.; Martinez, A.; Arnold, E.
Philips Lab., North Am. Philips Corp., Briarcliff Manor, NY
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 65-70, 1986

The microstructure of beam-recrystallized Si-on-insulator (SOI) film is strongly dependent on nucleation and growth processes during zone-melt propagation. In general, the recrystallization takes place along the (100) plane and in the {001} direction and in this case subgrain boundaries form the only major defects in the material. Stable growth regimes were identified that produce predominantly twin boundaries, when the SOI films recrystallize with their surface parallel to the (110) planes. The twin formation process is attributed to growth twinning characteristic for FCC and diamond structures. The majority of these boundaries consists of coherent twins. In this manner (110) textured SOI films can be grown which contain almost entirely twin boundaries as structural defects. The crystallography of coherent twin boundaries in SOI films and their dependence on growth parameters is presented. *CA*

350). Device-Worthy Silicon on Insulator Films Prepared by Lamp-Zone-Melting.
Bensahel, D.; Haond, M.; Dutartre, D.; Vu, D.P.
Cent. Natl. Etud. Telecommun., Meylan, France
Phys. Semicond. Devices, Proc. Int. Workshop, 3rd, 282-90.
World Sci.: Singapore, 1985

A technique for the fabrication of 4-in wafers of monocrystalline Si-on-insulator with a halogen lamp system is described. This technique makes use of a surface relief etched in the oxide grown on a Si wafer. With this heat-sink structure, the remaining defects of the recrystallized film are located within narrow strips (4 μm wide), leaving defect-free areas (36 μm wide). Complementary

MOS devices realized in the defect-free areas show that the electrical quality of the recrystallized film is similar to that of bulk monocrystalline Si. *CA*

351). Capping Techniques for Zone-Melting-Recrystallized Si-on-Insulator Films.
Chen, C. K.; Pfeiffer, L.; West, K. W.; Geis, M. W.; Darack, S.;
Achaibar, G.; Mountain, R. W.; Tsaur, B. Y.
Lincoln Lab., MIT, Lexington, MA
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 53-8, 1986

To prepare Si-on-insulator (SOI) films by graphite-strip-heater zone-melting recrystallization (ZMR), a capping technique must be used to ensure wetting by the molten Si zone. Two new capping techniques are demonstrated that result in reproducible wetting without degrading the crystallographic texture of the recrystallized film: annealing SiO_2-capped Si films in NH_3 and depositing two SiN_x layers with carefully controlled compositions on the SiO_2 capping layer. Wetting is promoted by the incorporation of trace amounts of N at the Si-SiO_2 interface. Both N implantation experiments and Auger spectroscopy studies establish that the presence of less than a monolayer of N at this interface is sufficient to ensure wetting. *CA*

• 352). New Capping Technique for Zone-Melting Recrystallization of Silicon-on-Insulator Films.
Chen, C.K.; Geis, M.W.; Finn, M.C.; Tsaur, B.-Y.
Lincoln Lab., MIT, Lexington, MA.
Appl. Phys. Lett. (USA), Vol.48, No.19, 1300-2, 12 May 1986

A new capping technique employing high-temperature NH_3 annealing has been developed to ensure uniform wetting by the molten Si zone during zone-melting recrystallization of Si-on-insulator films. By using this technique, the authors have reproducibly prepared 0.5-μm thick films with (100) crystalline texture that are greatly improved in smoothness, void density, and thickness uniformity. In addition, recrystallized 1-μm thick films have been obtained with large areas that are free of subboundaries, containing only threading dislocations at densities of less than $2 \times 10^6 cm^{-2}$. *IN*

• 353). Recent Advances in Si and Ge Zone-Melting Recrystallization.
Chen, C.K.; Geis, M.W.; Choi, H.K.; Tsaur, B.-Y.; Fan, J.C.C.
Lincoln Lab., MIT, Lexington, MA.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 613-18, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

By improving the thermal uniformity and stability of their graphite-strip heater oven, the authors have been able to significantly improve the overall quality of ZMR Si films. They have observed unbranched subboundaries and new types of defects that are less extended so that the total warp is less than 4 μm for 3-in wafers. The ZMR technique has also been utilized for producing thin Ge-on-insulator films. *IN*

• 354). A Single-Crystal Silicon Thin Film Formed by Secondary Recrystallization.
Cline, H.E.
General Electric Corporate Res. and Dev., Schenectady, NY.
J. Appl. Phys. (USA), Vol.55, No.12, 4392-7, 15 June 1984

Thin encapsulated silicon films were zone heated in the solid state just under the melting point with a quartz-iodine lamp over a range of speeds between 0.005 and 0.05 cm/s. The recrystallized thin films were examined with electron channeling, transmission electron microscopy, scanning and optical microscopy. The recrystallized 1/2-μm thick film was essentially a single crystal with large equiaxed subgrains oriented with the (100) nearly normal to the plane of the film and the

(010) direction along the growth direction at growth velocities below 0.01 cm/s. Misorientations between adjacent large 100-μm subgrains were of the order of 1 deg. The driving force of grain growth in the silicon thin film was determined to be the surface energy anisotropy of the silicon oxide interface from observations of grain boundary grooves that were pinned by a few micron-size included grains. Both the mechanism of recrystallization and the potential for producing silicon-on-insulator material by solid-state recrystallization are discussed. *IN*

355). In Situ Observation of Lamp Zone Melting of Si Films on Patterned SiO_2.
Dutartre, D.
CNET, Meylan, France
Appl. Phys. Lett. (USA), Vol.48, No.5, 350-2, 3 Feb. 1986

Using video recording equipment, the authors are able to visualize and study both the melting and freezing interfaces in lamp zone melting recrystallization of silicon-on-insulator (SOI) films. A so-called 'explosive' melting has been observed, corresponding to a noncontinuous advance of the front. They also show the effectiveness of an etched pattern in the underlying SiO_2 on the modulation of the solidification front. They thereby confirm the entrainment effect of this pattern. They observe then the effect of the scan speed on the liquid/solid interface morphology together with the entrainment efficiency. *IN*

356). Effects of Heating-Temperature Gradient and Scanning Direction on Crystallographic Properties of Zone-Melting Recrystallized Silicon on Square-Shaped Fused Quartz.
Fujita, S.; Okamoto, M.; Yamamoto, H.; Sasaki, A.
Dept. of Electr. Eng., Kyoto Univ., Japan
J. Appl. Phys. (USA), Vol.56, No.10, 2986-8, Nov. 1984

A new system in which a sample is heated by three different lower strip heaters was used for zone-melting recrystallization of Si on square-shaped fused-quartz substrates. By heating the two side heaters to a temperature higher than that of the center, and/or by recrystallizing the sample from the corner, the crystallographic properties (i.e., alignment of crystallographic axes and grain size) can be improved. Grain size as large as 1.15 by 10 mm was successfully obtained by simultaneously applying the two techniques described above. *IN*

357). Elimination of Subboundaries from Zone-Melting-Recrystallized Silicon-on-Insulator Films.
Geis, M.W.; Chen, C.K.; Smith, H.I.; Nitishin, P.M.; Tsaur, B.Y.; Mountain, R.W.
Lincoln Lab., MIT, Lexington, MA
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 39-44, 1986

Since the introduction of zone-melting recrystallization (ZMR) for Si-on-insulator (SOI) films, subboundaries (low-angle grain boundaries) have been the major crystallographic defects in recrystallized films. By using an improved ZMR procedure, subboundaries are eliminated over large areas. The improvements include the use of 1-μm thick polycrystalline-Si films deposited on 2-μm thick thermal SiO_2 film (instead of 0.5-μm thick Si and SiO_2 films), a new encapsulation technique, and improved control of the thermal gradient during ZMR. Recrystallized SOI films without subboundaries contain isolated dislocations with densities $< 2 \times 10^6 cm^{-2}$. *CA*

358). Three-Dimensional Device Fabrication Using Zone-Melting Recrystallization with a Graphite Strip Heater.
Geis, M.W.; Chen, C.K.; Mountain, R.W.; Economou, N.P.; Lindley, W.T.; Hower, P.L.
MIT, Lexington, MA

IEEE Transactions on Electron Devices, Vol. ED-32, No. 11, Nov. 1985, 43rd Annual Device Res. Conf., Boulder, CO, June 17-19, 1985, 2547-2548 *EI*

359). Zone-Melting Recrystallization of Semiconductor Films.
Geis, M.W.; Smith, H.I.; Tsaur, B.-Y.; Fan, J.C.C.; Silversmith, D.J.; Mountain, R.W.; Chapman, R.L.
Lincoln Lab., MIT, Lexington, MA.
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 477-89, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

The use of zone melting recrystallization (ZMR) to prepare large-grain (and in some cases single-crystal) semiconductor films is reviewed, with emphasis on recent work on Si on SiO_2. Encapsulants are generally required to minimize contamination and decomposition, induce a crystalline texture, improve surface morphology and prevent agglomeration. In the case of Si, the solid-liquid interface is faceted, which gives rise to subboundaries. These can be entrained by laterally modulating the temperature through the use of an optical absorber on top of the encapsulant. Control of thermal gradients and in-plane crystallographic orientation are important for reliable entrainment. *IN*

360). Zone-Melting Recrystallization of Si Films with a Moveable-Strip-Heater Oven.
Geis, M.W.; Smith, H.I.; Tsaur, B.-Y.; Fan, J.C.C.; Silversmith, D.J.; Mountain, R.W.
Lincoln Lab., MIT, Lexington, MA.
J. Electrochem. Soc. (USA), Vol. 129, No. 12, 2812-18, Dec. 1982

Recent work on zone-melting recrystallization of Si on amorphous insulating substrates using a moveable-strip heater oven is described in detail for the first time. A (100) texture is obtained if the Si is encapsulated with SiO_2 or a composite of $SiO_2/Si_3/N_4$. An encapsulation layer of 2 μm SiO_2/30 nm Si_3/N_4 prevents agglomeration and ensures a smooth surface. Several theories explaining the predominance of (100) texture in the transition region and the tendency of solidification from (100) textured seeds to occlude other orientations are discussed. Both effects are believed due to minimum interfacial tension between Si (100) and SiO_2. Grain boundaries can be eliminated by a variety of techniques, but subboundaries remain which have a minimal effect on majority carrier conduction. The spacings between subboundaries are found to increase with film thickness, approximately as the first power, and to increase with molten zone speed, approximately as the square root. *IN*

361). The {100} Single Crystal SOI Films Obtained on Four Inch Wafers Using Halogen Lamps.
Haond, M.; Dutartre, D.; Bensahel, D.
Cent. Natl. Etud. Telecommun., Meylan, France
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 83-8, 1986

By using a halogen lamp recrystallization system, it is shown that a patterning of the underlying oxide of SOI (Si-on-insulator) structures allows a high yield of localization of the remaining defects generally encountered in zone-melting recrystallization. The influence of the scan speed and grain orientation on the efficiency of the entrainment was investigated. Moreover, a quasi-single crystal can be obtained if a combination of seeding and oxide patterning is used. *CA*

362). Fabrication of Thick Films of Silicon-on-Insulator Substrates by Using a Scanning Halogen Lamp System.
Haond, H.; Bensahel, D.; Dutartre, D.
CNET, Meylan, France
Electron. Lett. (GB), Vol.20, No.24, 991-3, 22 Nov. 1984

Electron. Lett. (GB), Vol.20, No.24, 991-3, 22 Nov. 1984

A technique for preparing thick films of silicon-on-insulating substrates is presented. The authors start with a classical deposition of a thin film of polysilicon on patterned stripes of SiO_2 grown on Si wafers. The energy of the focused light of a halogen lamp induces a deep melting in the upper part of the substrate. This results in a controlled sinking of the SiO_2 strips in the molten silicon. By scanning the molten zone, the silicon solidifies at the leading edge, and the resulting film is made of 20- to 40-μm thick stripes of defect-free Si-on-SiO_2 separated by seeding areas. *IN*

363). Improved Heat-Sink Structure Providing Single-Crystal SOI Films Prepared by Lamp Zone Melting.
Haond, M.; Dutartre, D.; Bensahel, D.
CNET, Meylan, France
Mater. Lett. (Netherlands), Vol.4, No.1, 13-16, Nov. 1985

In order to localize the remaining defects encountered in lamp-zone-melting recrystallization of silicon-on-insulator (SOI) films, the authors have used an improved heat-sink technique. It consists of a periodic surface relief etched down into the underlying SiO_2 and extending along 4-in wafers. The resulting film contains SOI stripes separated by narrow lines where the defects are localized. This technique also avoids the de-wetting of the liquid silicon with the large molten zone used. By using a combination of seeding with the heat-sink structure, the authors obtain a quasi-single-crystal film on 4-in wafers. *IN*

364). Improvement of Wetting of Silicon on Insulator During Lamp Zone Melting Using Plasma Nitridation.
Haond, M.; Dutartre, D.; Pantel, R.; Straboni, A.; Vuillermoz, B.
Cent. Natl. Etud. Telecommun., CNS, Meylan, France
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 59-64, 1986

In the preparation of Si-on-insulator films by zone-melting recrystallization (ZMR), a cap layer is necessary to avoid the beading up of a Si film when it is molten over Si. This is a consequence of a bad wetting of liquid Si on SiO_2. A successful application of a plasma nitridation treatment of the capping oxide is reported. The behavior of the liquid Si films during ZMR is compared for different capping structures. The modification of the interface is investigated by using Auger analysis. A range of N accumulation at the interface provides a good wetting. *CA*

365). Recrystallization of Si on Insulating Substrates by Using Incoherent Light Sources.
Haond, M.
CNET, Meylan, France
J. Phys. Colloq. (France), Vol.44, No.C-5, C5/327-36, Oct. 1983
Laser-Solid Interactions and Transient Thermal Processing of Materials
25-27 May 1983, Strasbourg, France

The author reviews the main results obtained to date in the recrystallization of thin silicon-on-insulator films by means of incoherent light sources. Different sources such as graphite heaters, halogen tungsten filament lamps, and mercury arc lamps have been investigated. Large-area monocrystalline (100) Si films have been obtained using these various means. The defects remaining in the films are discussed, i.e., grain and/or subgrain boundaries, precipitates, and strain. Electrical measurements are also reported. Current research is devoted first to the design of appropriate set-ups and shaping of the energy beams and, second, to film patterning in an aim to reject grain boundaries out of the active areas of devices. *IN*

• 366). Strip Heater Recrystallized SOI Structures.
Higuchi, K.; Saitoh, S.; Okabayashi, H.
Microelectron. Res. Labs., NEC Corp., Kawasaki, Japan

Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications. US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 151-7, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Si films recrystallization on SiO_2 was performed using the strip-heater method. The recrystallized Si films crystallinity was found to be dependent on the width of SOI islands surrounded by a seeding area, based on electron channeling pattern observations. SOI islands with less than 200-μm width were recrystallized into single crystals. In a few mm wide SOI islands, subgrain growth was observed, although each subgrain oriented in nearly seed crystal orientation. Large angle grains, which contained many subgrains, were grown for the sample with a seeding area at one side. *IN*

367). Electrical and Physical Properties of Rapid-Zone-Recrystallized SOI Made Using a Pulsed Arc Lamp.
Hunt, C.E.; Frey, J.
Sch. Electr. Eng., Cornell Univ., Ithaca, NY
Ext. Abstr. Conf. Solid State Devices Mater., 18th, 561-4, 1986 *CA*

368). Epitaxial Regrowth of Amorphous or Polycrystalline Silicon Layers on Silicon Single Crystals and Bridging Epitaxy by Flash Lamp Irradiation.
Klabes, R.; Matthai, J.; Voelskow, M.; Wieser, E.; Erben, J.-W.; Scharff, W.; Weissmantel, C.
Zentralinst. Fur Kernforschung, Akad. Der Wissenschaften, Rossendorf, Germany; Phys. Status Solidi A (Germany), Vol.82, No.2, K121-3, 16 April 1984

The liquid phase regrowth of amorphous and polycrystalline layers on single-crystal silicon using flash lamp pulses is reported. With respect to silicon-on-insulator devices, it is of great interest to extend these investigations to samples where the amorphous silicon film is deposited on a SiO_2 layer with open windows to the single-crystal substrate (seeding or bridging epitaxy). Here, the corresponding possibilities of flash lamp irradiation are investigated. *IN*

369). Recrystallization of Polycrystalline Silicon on Fused Silica Using an RF-Heated Carbon Susceptor.
Kobayashi, Y.; Fukami, A.; Suzuki, T.
Res. Lab., Hitachi Ltd., Ibaraki, Japan
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 137-50, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

A new zone-melting recrystallization method that uses an rf-heated carbon susceptor in fabrication of SOI (silicon-on-insulator) structures has been developed. In this method, a 0.5- to 1.0-μm thick polycrystalline silicon film, encapsulated with a 1.2-μm thick CVD-SiO_2 layer, was deposited on a fused silica substrate. The substrate was moved across the carbon susceptor, which had a narrow, high-temperature zone. The continuous silicon films produced had grains in the recrystallized silicon film of several tenths to a few mm wide and a few cm long, and a film orientation of (100). In the grains, there were many small angle grain boundaries which consisted of discrete dislocations. There were some cracks in the silicon film. In the silicon islands, recrystallized silicon was a single crystal with an orientation of (111) and there were no cracks. In order to obtain silicon without cracks and with an orientation of (100), a method that connects the polycrystalline silicon islands was proposed. *IN*

370). Zone Melting Recrystallization Method.

Kobayashi, Y.
Hitachi Res. Lab., Hitachi Ltd., Tokyo, Japan
Oyo Buturi (Japan), Vol. 53, No. 1, 30, Jan. 1984

Silicon-on-insulator (SOI) techniques based on zone-melting recrystallization (ZMR) are described which are used for monocrystallization of silicon on a SiO_2 film or silica substrate. The ZMR method permits large-grain crystallization with the use of no seed crystal. There is, however, the possibility of impurity segregation during recrystallization. *IN*

371). Temperature Profile of a Silicon-on-Insulator Multilayer Structure in Silicon Recrystallization with Incoherent Light Source.
Kyung, C.M.
Bell Labs., Murray Hill, NJ.
IEEE Trans. Electron Devices (USA), Vol.ED-31, No.12, 1845-51, Dec. 1984

A one-dimensional distribution of the temperature and the heat source in an SOI (silicon-on-insulator) multilayer structure illuminated by tungsten lamps from both sides was obtained by solving the heat equation in steady state on a finite difference grid using a successive over-relaxation method. The heat source distribution was obtained by considering such features as spectral components of the light source, multiple reflection at the internal interfaces, temperature and frequency dependence of the light absorption coefficient, etc. The front and back surface temperatures, which are boundary conditions for the heat equation, were derived from a requirement that they satisfy the radiation conditions. The radiation flux, as well as the conduction flux, was considered in modeling the thermal behavior at the internal interfaces. Since the temperature and the heat source profiles are strongly dependent on each other, the calculation of each profile was iterated using the updated profile of the other until they were consistent with each other. *IN*

372). Improved Crystal Perfection in Zone-Recrystallized Si Films on SiO_2.
Pfeiffer, L.; West, K.W.; Paine, S.; Joy, D.C.
AT&T Bell Lab., Murray Hill, NJ.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 583-92, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

The authors review recent results of their graphite-strip-heater Si-on-Insulator (SOI) effort: (1) recrystallization of SOI films on 100-mm wafers, (2) model of subboundary pattern formation in SOI films, (3) low-defect density SOI films by ultra slow scanning of the melt zone, (4) low-defect density SOI films by patterned openings in the cap oxide overlayer. *IN*

373). Si-on-Insulator Films of High Crystal Perfection by Zone Melting Under a SiO_2 Cap Provided With Vent Openings.
Pfeiffer, L.; Kovacs, T.; West, K.W.
AT&T Bell Labs., Murray Hill, NJ.
Appl. Phys. Lett. (USA), Vol.47, No.2, 157-9, 15 July 1985

The authors observe a marked improvement in the crystal perfection of zone melted thick Si-on-insulator films that were prepared for melt processing by etching an array of openings in the SiO_2 capping layer. Chemical defect etching and Rutherford backscattering measurements reflect this improvement, which the authors believe is due to the creation of new venting paths that reduce the level of excess dissolved SiO_2 in the molten Si before recrystallisation. *IN*

374). Incoherent Light Recrystallization of Silicon-on-Insulator Films.
Robinson, McD.; Celler, G.K.; Lischner, D.J.
Epsilon Technol. Inc., Tempe, AZ.
Lam, H.W.; Thompson, M.J. (Editors)

Comparison of Thin Film Transistor and SOI Technologies Symposium, 71-80, 1984, 26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Energy sources used to convert polycrystalline silicon-on-insulator films to single crystal through melting and recrystallization have included electron beams, lasers, graphite-strip heaters, and incoherent light from tungsten halogen and vapor arc lamps. The author focus on incoherent light recrystallization of polycrystalline silicon, comparing tungsten filament and vapor arc lamp sources, and linear zone melting versus uniform illumination. The discussion includes material redistribution, defect formation, and the dynamics of melting. *IN*

375). Focused Lamp Zone Melting Recrystallization of Silicon on Insulating Substrates.
Sakurai, J.
Div. of Adv. Technol., Fujitsu Ltd., Kawasaki, Japan
J. Electrochem. Soc. (USA), Vol.133, No.7, 1485-8, July 1986

Zone-melting recrystallization (ZMR) of silicon-on-insulator (SOI) has been performed by a pair of focused lamps. Distinction from conventional ZMRs is located instantaneous heating with focused beams on front and back surfaces of SOI wafers, instead of keeping the entire wafer uniformly at the high-temperature 0.4-μm thick poly-Si films over 2-μm thick insulating layer on the Si substrate are recrystallized without an appreciable redistribution of arsenic atoms implanted, $2 \times 10^{15} ions/cm^2$, 150 keV through 50-$\mu$m thick Si_3/N_4 films on the Si substrate which suggests that the focused lamp ZMR can be compatible with the three-dimensional devices. The unseeded Si film recrystallization on grooved quartz wafers is crack-free, large-grained with (100) texture across several chips. For seeded samples, the lateral epitaxy takes place completely over the SiO_2 islands of $100 \times 180 \mu m^2$ in size without any subgrain boundaries, in which displacement of the SiO_2 island during ZMR can be avoided by connecting the islands to each other with narrow SiO_2 bridges. Major remaining problems for SOI are the warpage of Si wafers and the subgrain boundaries. *IN*

376). Growth of Single-Crystalline Regions on Amorphous Insulating Substrates by Zone-Melting Recrystallization.
Scharff, W.; Erben, J.-W.; Wolf, A.; Heber, M.; Hamann, C.; Weissmantel, C.; Voelskov, M.; Matthai, J.; Kogler, R.; Klabes, R.; Wieser, E.
Sektion, Phys./Elektronische, Bauelemente, Tech. Hochschule Karl-Marx-Stadt, Karl-Marx-Stadt, Germany;
Phys. Status Solidi A (Germany), Vol.82, No.1, K5-9, 16 March 1984

The growth of single-crystal silicon films or islands on insulating substrates (SOI) offers new interesting possibilities for the further development of electronic and opto-electronic devices. The authors discuss the growth of silicon islands which are embedded into a SiO_2 structure, so that a planar surface was formed by the SiO_2 layer and the silicon island. Crystals grown in this manner might be most useful in technological applications. *IN*

377). Preparation of Single-Crystalline Silicon Film Structures on Insulating Substrates.
Scharff, W.; Erben, J.-W.; Hoeppner, K.; Wolf, A.; Voelskow, M.; Matthaei, J.
Sekt. Phys./Elektron. Bauelemente, Tech. Hochsch., Karl-Marx-Stadt, Ger. Dem. Rep.
Wiss. Z. - Tech. Hochsch. Karl-Marx-Stadt, 27(2), 256-64, 1985

The recrystallization of poly-Si layers on SiO_2 or quartz glass by scanning with a halide lamp on the backside of the Si or quartz substrate was studied. Small-angle grain boundaries and dislocation loops are observed in the recrystallized Si on SiO_2. Dendritic growth is observed in Si islands on SiO_2. Dendrite growth is observed on quartz glass. *CA*

378). Silicon Films on Amorphous Substrates: Influence of Boundaries and Barriers.
Scharff, W.; Weissmantel, C.
Sekt. Phys., Tech. Hochsch., Karl-Marx-Stadt 9010, Ger. Dem. Rep.

J. Vac. Sci. Technol., A, Vol. 4, No. 6, 3160-4, 1986

Silicon-on-insulator (SOI) structures were produced by recrystallization of polycrystalline silicon deposited on thermally grown SiO_2 using either a single-flash lamp pulse or light strip scanning. In the latter case of lateral zone melting, encapsulating coatings of Si_3N_4/SiO_2 were found to be necessary to obtain closed films. Examination by electron microscopy revealed the formation of subgrain boundaries that can be entrained under light-absorbing strips of Si or $MoSi_2$. In conclusion, of basic considerations concerning the stability of the system during recrystallization, a major influence of the wetting behavior at the interface between the encapsulating layer and the molten silicon was deduced, and a rough interface and/or the addition of some monolayers of carbon was found to be favorable. Measurements performed with SOI test circuits confirmed the device-worthy quality of the films, for which first applications in optoelectronic memories have been realized. *CA*

379). Silicon-on-Insulator by Graphoepitaxy and Zone-Melting Recrystallization of Patterned Films.
Smith, H.I.; Geis, M.W.; Thompson, C.V.; Atwater, H.A.
Electrical Engng. and Computer Sci., MIT, Cambridge, MA.
J. Cryst. Growth (Netherlands), Vol. 63, No. 3, 527-46, Oct. 1983

Graphoepitaxy and zone-melting recrystallization of patterned films are reviewed, with emphasis on their application to silicon-on-insulator (SOI). In the case of Si graphoepitaxy by partial melting with a laser or stationary strip-heater, orientation is explained on the basis of preferential retention of those grains that have (100) texture and have (100) directions parallel to the grating axis. Graphoepitaxy encompasses a wide variety of film formation methods and mechanisms of orientation. Oscillatory CVD and solid-state surface-energy-driven secondary recrystallization are low-temperature approaches which may be able to provide SOI in those situations where the high temperature of melting (1412°C) cannot be tolerated, such as multilevel integrated electronics and flat-panel displays. Zone-melting recrystallization of patterned Si films has yielded: large-area, single-grain Si films on SiO_2 via an hourglass technique; entrainment of subboundaries, grain boundaries and impurities along straight lines separated by $=100$ μm; and orientation filtering by growth-velocity competition. *IN*

380). Zone Melting Recrystallization of Patterned Films and Low-Temperature Graphoepitaxy.
Smith, H.I.; Thompson, C.V.; Geis, M.W.; Atwater, H.A.; Yonehara, T.; Wong, C.C.
Lincoln Labs, MIT, Cambridge, MA.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing. Processing of the Symposium, 459-464, 1984.
14-17 Nov. 1983, Boston, MA.
North-Holland, NY.

Zone-melting recrystallization (ZMR) of Si films on SiO_2 has produced large-area films with electrical properties approaching those of bulk wafers. The mechanisms of film formation and the use of patterning to control orientation and defect distribution are briefly reviewed. Some examples of the use of patterning are: single-grain films have been produced by means of planar constrictions; subboundaries and impurities have been entrained to lie along straight lines separated by $\sim 100\mu$m through the use of lithographically-defined grating patterns; a vertical-constriction technique has enabled (100) texture to be achieved in 50-μm thick Si films; a lithographically-defined orientation filter, which takes advantage of growth-velocity anisotropy, has been used to select a predetermined azimuthal orientation. *IN*

381). Thickness Dependence of SiO_2 Capping Layers on Recrystallization of Germanium

Islands on Insulator.
Takai, M.; Tanigawa, T.; Gamo, K.; Namba, S.
Faculty of Engng. Sci., Osaka Univ., Toyonaka, Osaka, Japan
Jpn. J. Appl. Phys. Part 2 (Japan), Vol.23, No.6, L357-9, June 1984

The thickness of SiO_2 capping layers has been varied to suppress agglomeration and surface rounding of germanium layers of SiO_2 during zone-melting recrystallization. It was found that SiO_2 capping with a thickness of more than 1 μm could suppress agglomeration and surface rounding successfully and most of the islands were single crystalline with flat surfaces. The predominant orientation of germanium islands was found to be (100). *IN*

382). Zone-Melting Recrystallization of Si Films on SiO_2.
Tsaur, B.-Y.
Lincoln Lab., MIT, Lexington, MA, USA
Furukawa, S. (Editor)
Silicon-on-Insulator: Its Technology and Applications, US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics,' 101-28, 1985
20-24 June 1983, Oiso, Japan
Reidel, Dordrecht, Netherlands

Large-area, device-quality Si films on SiO_2 have been prepared by zone-melting recrystallization using graphite-strip heaters. A composite $SiO_2/Si_3/N_4$ encapsulation layer prevents agglomeration of the molten Si, ensures a smooth film surface, and induces (100) texture. The recrystallized films contain widely-spaced grain boundaries, which can be eliminated by seeded growth techniques, and many sub-boundaries within each grain. Sub-boundaries can be entrained along parallel lines underneath a photolithographically defined optical absorber or reflector pattern. Extensive electrical measurements have been made on the recrystallized films. Sub-boundaries have no significant effect on MOSFET device performance, and high-yield CMOS test circuits have been made in films on 2-in diameter wafers. Radiation-hardened CMOS devices, lateral bipolar transistors, and dual-gate MOSFETs have been fabricated in recrystallized films. *IN*

383). Zone-Melting Recrystallization of LPCVD-Silicon Films Using a Movable Halogen Lamp.
Voelskow, M.; Matthai, J.; Stagemann, K.-H.; Gerisch, D.; Mutze, S.
Centralio Inst. for Nucl. Res., Acad. of Sci., Rossendorf, Germany
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.
Proceedings of the Conference, 402-5, Vol. 2, 1985
25-28 Sept. 1984, Dresden, Germany
Akad. Wissenschaften DDR, Dresden, Germany

During the last few years, various methods for production of single-crystalline or large-grained silicon films on insulating substrates (SOI) have been developed. SOI is attractive for high-density MOS-integrated circuits, and in particular for CMOS-technology. The SOI-technique also offers new possibilities to produce 3D-integrated circuits, flat plate displays, and inexpensive solar cells. The authors have used the zone-melting recrystallization technique (ZMR) for production of large-grained silicon films. *IN*

384). Oriented Growth of Silicon Films on Insulating Materials.
Weissmantel, C.
Sektion Phys., Tech. Hochschule, Karl-Marx-Stadt, Germany
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.
Proceedings of the Conference, 383-91, Vol.2.
25-28 Sept. 1984 Dresden, Germany

This paper deals with the state of the art in preparing oriented silicon layers by recrystallization of amorphous or polycrystalline films deposited on amorphous and insulating substrates, in particular oxidized silicon or fused silica. Following a discussion on the incentives and the experimental problems, results obtained in the author's laboratory by using the techniques of (1) graphoepitaxy and (2) lateral zone-melting recrystallization are presented and discussed in comparison with the findings by other groups. Further trends in film preparation as well as emerging applications are outlined.

IN

385). A Simple Mathematical Model for the Description of the Zone Melting Process of SOI-Structures.
Andra, H.; Streit, U.; Weinelt, W.; Wolf, A.; Hoppner, K.; Scharff, W.
Tech. Hochschule Karl-Marx-Stadt, Germany
Exp. Tech. Phys. (Germany), Vol.34, No.1, 1-9, 1986

The growth of device-worthy silicon crystal films on insulating substrates would offer a new type of semiconductor technology. The crystallization of continuous silicon layers on thermally oxidized silicon wafers was performed by a zone-melting process. To describe the recrystallization process of SOI-structures, a simple mathematical model is given and the numerical calculation of the one-dimensional temperature profile is carried out by a difference method. *IN*

386). Two Dimensional Numerical Thermal Analysis of Silicon on Insulator Recrystallization Processes by a Moving Heat Source.
Chang, C.Y.; Fang, Y.K.; Wu, B.S.; Chen, R.M.
Inst. of Electr. and Comput. Eng., Nat. Cheng Kung Univ., Tainan, Taiwan
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
497-505, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

The moving-zone-melt recrystallization of polysilicon-on-insulator substrate has been studied with computer simulation methods. The most important parameters such as upper strip heater moving velocity, the power of upper strip heater, substrate temperature were investigated. Generally speaking, temperature profile in multilayer and melt depth of poly Si are difficult to be visualized, but are still important for recrystallization process. Therefore,by using two-dimensional finite difference method, a numerical analysis of moving-melt-zone recrystallization processes has been developed. Through this analysis, the temperature profile in multilayer and melt depth of poly-Si are depicted. *IN*

387). The Role of Oxygen in Zone-Melting Recrystallization of Silicon-on-Insulator Films.
Fan, J.C.C.; Tsaur, B.-Y.; Chen, C.K.; Dick, J.R.; Kazmerski, L.L.
Lincoln Lab., MIT, Lexington, MA.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
477-89, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Using secondary-ion mass spectroscopy, the authors have found that oxygen is strongly concentrated at the sub-boundaries in zone-melting-recrystallized silicon-on-insulator films prepared by the graphite-strip-heater technique. This observation suggests that the formation of sub-boundaries during recrystallization may be caused by constitutional supercooling resulting from the presence of oxygen that is dissolved into the molten Si zone from the adjacent SiO_2 layers. Since all zone-melting-recrystallized films to date have been bordered by SiO_2 layers, regardless of the heating techniques employed, the sub-boundaries almost always present in these films may well have dissolved oxygen as their common origin. *IN*

388). Characterization, Control, and Reduction of Subboundaries in Silicon on Insulators.
Geis, M.W.; Chen, C.K.; Smith, H.I.; Mountain, R.W.; Doherty, C.L.
Lincoln Lab., MIT, Lexington, MA.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1986
Symposium, 26-30 Nov. 1984, Boston, MA.

Mater. Res. Soc., Pittsburgh, PA.

Subboundaries are the major crystalline defects in thin semiconductor films produced by zone-melting recrystallization (ZMR). Using transmission electron microscopy (TEM) and chemical etching, the authors have analyzed the angular discontinuity and defect structure of subboundaries in ZMR Si films. Annealing in oxygen has resulted in the elimination of dislocation bands from sizeable regions of some films. Calculations suggest that cellular growth due to constitutional supercooling may not occur in some Si ZMR. *IN*

389). Thermal Profiles in Silicon-on-Insulator (SOI) Material Recrystallized With Scanning Light Line Sources.
Kubota, K.; Hunt, C.; Frey, J.
Cornell Univ. Sch. of Electr. Eng., Ithaca, NY.
Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 629-34, 1985, 26-30 Nov. 1984, Boston, MA.
Mater. Res. Soc., Pittsburgh, PA.

A two-dimensional solution of the classical heat equation is obtained and used to predict thermal profiles during line source zone-melting recrystallization of silicon on insulators. A macroscopic solidification model is used to find the extent of the molten zone in multilayered structures. The problems of convergence associated with moving phase boundaries are reduced by using the transformed temperature and the enthalpy model. The resultant isotherms obtained at varying zone scan speeds indicate optimum experimental conditions. *IN*

• 390). Thermal Profiles During Recrystallization Of Silicon On Insulator With Scanning Incoherent Light Line Sources.
Kubota, K.; Hunt, C.E.; Frey, J.
Cornell Univ. Sch. of Electr. Eng., Ithaca, NY.
Appl. Phys. Lett. (USA), Vol.46, No.12, 1153-5, 15 June 1985

The classical heat equation is solved in one and two dimensions to obtain temperature profiles during recrystallization of silicon thin films on insulators with scanning incoherent light sources. The extent of the Si molten region in multilayered structures is predicted using a macroscopic approach. The enthalpy method incorporates the latent heat of fusion into the temperature-enthalpy relation for Si; the Kirchhoff transformation takes the temperature dependence of the thermal conductivities for the materials into account. The calculations yield the Si melt depths and temperatures and are intended to establish proper experimental conditions. *IN*

391). CMOS Circuits Made in Lamp-Recrystallised Silicon-on-Insulator.
Vu, D.P.; Leguet, C.; Haond, M.; Bensahel, D.; Colinge, J.-P.
CNET, Meylan, France
Electron. Lett. (GB), Vol.20, No.7, 298-9, 29 March 1984

Polysilicon film was deposited on 100-mm oxidised silicon wafers. The film was recrystallised using a focused halogen lamp and served as substrate material for CMOS circuit fabrication. A mobility of 480 and 180 $cm^2/V{\cdot}s$ is found in n- and p-channel MOS transistors, respectively, and the threshold voltage spread is very low. 65-stage ring oscillators were also realised, which exhibit a 6-ns delay per stage at 5 V supply voltage. *IN*

392). Characterization of Silicon on Insulator Films Realized via Zone Melting Recrystallization.
Bensahel, D.; Haond, M.; Dutarte, D.
CNET, Meylan, France
Cullis, A.G.; Holt, D.B. (Editors)
Microscopy of Semiconducting Materials, 1985. Proceedings of the Royal Microscopical Society Conference, 73-82, 1985, 25-27 March 1985, Oxford, England
Adam Hilger, Bristol, England

The macroscopical defects encountered during the recrystallization of poly-Si films on insulator by zone melting are described. The behaviour of microscopic defects and their possible localization are then reviewed. *IN*

• 393). Localization of Defects on SOI Films Via Selective Recrystallisation Using Halogen Lamps.
Bensahel, D.; Haond, M.; Vu, D.P.; Colinge, J.-P.
CNET, Meylan, France
Electron. Lett. (GB), Vol.19, No.13, 464-6, 23 June 1983

Selective annealing by means of an incoherent light system has been employed to grow single-crystal Si on oxide. This technique allows control of the location of the remaining defects (subgrain boundaries) in the (100) recrystallised film. *IN*

• 394). Origin of Oriented Crystal Growth of Radiantly Melted Silicon on SiO_2.
Biegelsen, D.K.; Fennell, L.E.; Zesch, J.C.
Xerox Palo Alto Res. Center, Palo Alto, CA.
Appl. Phys. Lett. (USA), Vol.45, No.5, 546-8, 1 Sept. 1984

The authors demonstrate directly that (100) texturing of lamellae in radiantly melted silicon on SiO_2 derives from precursor seeds in the as-deposited solid film. The anisotropic interfacial free energy between crystalline silicon and SiO_2 controls the orientation. *IN*

395). Minority Carrier Lifetime Studies in Halogen Lamp Recrystallized SOI Films.
Chantre, A.; Ronzani, D.; Vu, D.P.
Cent. Natl. Etud. Telecommun., Meylan, France
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 349-55, 1986

Minority carrier generation processes were studied in detail in halogen lamp recrystallized Si-on-insulator (SOI) films. Various kinds of materials were analyzed in order to assess the roles of the different crystallographic imperfections present in the layers (precipitates, subgrain boundaries, interfaces). Generation lifetimes in precipitate-free material are controlled by subgrain boundaries, and 100-μs lifetimes can be measured in defect-free regions of SOI obtained by using a defect localization technique. *CA*

• 396). Topographic Imperfections In Zone Melting Recrystallized Si Films On SiO_2.
Chen, C.K.; Geis, M.W.; Tsaur, B.-Y.; Chapman, R.L.; Fan, J.C.C.
Lincoln Lab., MIT, Lexington, MA.
J. Electrochem. Soc. (USA), Vol.131, No.7, 1707-11, July 1984

The principal topographic imperfections in Si films recrystallized on SiO_2 by the graphite-strip-heater technique have been examined. Wafer warpage has been reduced to less than 4 μm for 2-in diameter samples. The protrusion density decreases with finer subboundary spacing; this

can be understood in terms of the thermal gradient present at the liquid-solid interface. *IN*

397). Silicon Thin Films Formed on an Insulator by Recrystallization.
Cline, H.E.
General Electric Corporate Res. and Dev., Schenectady, NY.
J. Appl. Phys. (USA), Vol.55, No.8, 2910-15, 15 April 1984

Encapsulated silicon thin films were both zone heated and uniformly pulse heated over a range of rates and temperatures with quartz-iodine lamp heat sources. Large 100-μm size grains were observed after zone heating in the solid state just below the melting point. In contrast, 10-μm grain sizes were found in comparable pulse heat treatments in the same material. Zone melting results in a columnar subgrain structure. The mechanisms of grain growth, crystal growth, from the liquid film , and agglomeration are discussed in view of these experiments at relatively low growth rates. A silicon-on-insulator material may be produced at rates less than 0.025 cm/s by directional grain growth. *IN*

• 398). Study of the Solidification Front of Si Films in Lamp Zone Melting Controlled by Patterning the Underlying SiO_2.
Dutartre, D.; Haond, M.; Bensahel, D.
CNET, Meylan, France
J. Appl. Phys. (USA), Vol.59, No.2, 632-5, 15 Jan. 1986

A periodic heat-sink structure has been tested in lamp recrystallization of thin polycrystalline silicon films deposited on oxidized wafers. The defects generally encountered in this type of recrystallization, grain and subgrain boundaries, are localized in specifically designed areas. This localization technique and especially the occurrence of unlocalized defects are interpreted, taking into account the breakdown of the solidification front. Beside faceting effects, constitutional supercooling due to impurity segregation is found to play a major role in this type of recrystallization. *IN*

• 399). Oxygen in Zone-Melting-Recrystallized Silicon-on-Insulator Films: Its Distribution and Possible Role in Sub-Boundary Formation.
Fan, J.C.C.; Tsaur, B.-Y.; Chen, C.K.; Dick, J.R.; Kazmerski, L.L.
Lincoln Lab., MIT, Lexington, MA.
Appl. Phys. Lett. (USA), Vol.44, No.11, 1086-8, 1 June 1984

Using secondary-ion mass spectroscopy, the authors have found that oxygen is strongly concentrated at the sub-boundaries in zone-melting-recrystallized silicon-on-insulator films prepared by the graphite-strip-heater technique. This observation suggests that the formation of sub-boundaries during recrystallization may be caused by constitutional supercooling resulting from the presence of oxygen that is dissolved into the molten Si zone from the adjacent SiO_2 layers. *IN*

400). Crystallinity of Recrystallized Si on SiO_2 by Zone Melting Method.
Higuchi, K.; Saitoh, S.; Okabayashi, H.
Microelectronics Res. Labs., NEC Corp., Kawasaki, Japan
Extended Abstracts of the 15th Conference on Solid State Devices and Materials, 27-30, 1983, 30 Aug.-1 Sept. 1983, Tokyo, Japan
Japan Soc. Appl. Phys., Tokyo, Japan

Si film recrystallization on SiO_2 was performed using the zone melting technique. The recrystallized Si films crystallinity was found to be dependent on the width of SOI islands surrounded by a seeding area, based on electron channeling pattern observations. *IN*

401). Detection of Electronic Defects in Strip-Heater Crystallized Silicon Thin Films.
Johnson, N.M.; Moyer, M.D.; Fennell, L.E.; Maby, E.W.; Atwater, H.

Xerox Palo Alto Res. Centers, Palo Alto, CA.
Narayan, J.; Brown, W.L.; Lemons, R.A. (Editors)
Laser-Solid Interactions and Transient Thermal Processing of Materials, 491-7, 1983, 1-4 Nov. 1982, Boston, MA.
Elsevier, New York.

Electronic defects in strip-heater-crystallized silicon thin films have been investigated with capacitance-voltage (C-V), deep-level spectroscopic, and scanning-electron microscopic techniques. For electrical characterization, the crystallized silicon films were used to fabricate inverted metal-oxide-silicon capacitors in which degenerately doped bulk silicon substrates provided the gate electrode. High-frequency C-V characteristics yield effective fixed-charge densities in the oxide of $> 2 \times 10^{11} cm^{-2}$. Trap-emission spectra, recorded with deep-level transient spectroscopy on both p-type and n-type capacitors, indicate a continuous distribution of deep levels throughout the silicon bandgap. The Si-SiO_2 interface is considered to be the principal source of this deep-level continuum, since the films are essentially single crystal with a low density of subgrain boundaries; the effective interface-state density is $> 2.5 \times 10^{10} eV^{-1} cm^{-2}$. A discrete energy level, detectable above the background continuum, appears in the upper half of the silicon bandgap; it may identify a point defect in the bulk of the silicon film with a spatially uniform density of approximately $1 \times 10^{13} cm^{-3}$. On lateral p-n junction diodes, electron-beam-induced-current images reveal enhanced diffusion of arsenic along structural defects intersecting the junction. *IN*

402). Lateral Zone Growth and Characterization of Device Quality Silicon-on-Insulator Wafers.
Lam, H.W.; Pinizzotto, R.F.; Malhi, S.D.S.; Vaandrager, B.L.
Central Res. Labs., Texas Instruments Inc., Dallas, TX.
Appl. Phys. Lett. (USA), Vol.41, No.11, 1053-5, 1 Dec. 1982

A lateral zone-melting process has been developed whereby (100) silicon-on-insulator wafers can be obtained. Small-angle grain boundaries exist extensively in the recrystallized silicon, with a maximum variation in the orientation between adjacent grains of 0.3 deg. A SiC coating prevents the dusting of carbon from the moving heater from contaminating the silicon film. It has been found that enhanced arsenic diffusion along the small-angle grain boundaries in this material is significantly less than that in the grain boundaries in laser-recrystallized silicon-on-insulator material. Furthermore, it was found that the small-angle grain boundaries do not significantly affect the carrier mobility, probably because of the relatively low surface trapping state density at the small-angle grain boundaries. Complementary-metal-oxide-semiconductor devices fabricated in this material exhibit characteristics that are comparable to those of bulk devices. *IN*

403). (100) and (111) Textures in Unseeded, Strip Heater Recrystallized Silicon-on-Insulator.
Lee, E.-H.
Monsanto Electron. Mater. Co., St. Peters, MO.
Appl. Phys. Lett. (USA), Vol.48, No.2, 180-2, 13 Jan. 1986

The graphite-strip-heater technique was used to obtain strongly preferred (100) or (111) textures for thin-film silicon recrystallized on amorphous oxide and nitride substrates. Whereas (100) textures have been obtained in the liquid phase, (111) textures have been obtained in the solid phase at near-melting temperatures. Films of (100) orientation displayed the usual subboundaries, but (111) films revealed grainy textures mixed with pond ripple features. The lateral epitaxy model and the birth and spread model have been useful in distinguishing the two growth mechanisms. Films on Si_3N_4 substrates had characteristics similar to those on SiO_2 substrates. *IN*

404). Extended Growth of Subgrain-Boundary-Free Silicon-on-Insulator Via Thermal Gradient Variation.
Lee, E.-H.

Monsanto Electronic Materials Co., ST. Peters, MO.
Appl. Phys. Lett. (USA), Vol.44, No.10, 959-61, 15 May 1984

Morphological variations of graphite-strip-heater-recrystallized silicon-on-insulator formed in the initial stage of seeded growth have been analyzed to examine the thermal gradient effect upon the growth stability. Systematic transition of the stable growth into an orderly breakdown of faceted, cellular, and dendritic configurations has been attributed to the decreasing temperature gradient in this region. There are indications that constitutional supercooling could be responsible for the interface stability breakdown and that increased thermal gradients can suppress the onset of breakdown and maintain the stable growth over an extended distance. *IN*

405). Electron-Beam-Induced Current Measurements in Silicon-On-Insulator Films Prepared by Zone-Melting Recrystallization.
Maby, E.W.; Atwater, H.A.; Keigler, A.L.; Johnson, N.M.
MIT, Cambridge, MA.
Appl. Phys. Lett. (USA), Vol.43, No.5, 482-4, 1 Sept. 1983

Enhanced diffusion of arsenic along grain boundaries and subboundaries in zone-recrystallized silicon-on-insulator films has been measured by electron-beam-induced current analysis of lateral pn junctions fabricated in the films. A 4-h diffusion at 1100°C resulted in protrusions of arsenic at the junction edges which measured approximately 3 to 5 μm along the grain boundaries and only 1 to 2 μm along the subboundaries. The results suggest that under more ordinary thermal processing conditions, field-effect transistors with channel lengths greater than about 1.5 μm can be randomly positioned with respect to the more numerous subboundaries, but grain boundaries should be avoided. *IN*

406). Sub-Boundary Formation and Suppression in Silicon Films Recrystallized by Scanned Zone Melting.
Pfeiffer, L.; Gibson, J.M.; Kovacs, T.
AT&T Bell Labs, Murray Hill, NJ.
Baglin, J.E.E.; Campbell, D.R.; Chu, W.K. (Editors)
Thin Films and Interfaces II. Proceedings of the Symposium, 505-510, 1984
14-18 Nov. 1983, Boston, MA.
North-Holland, NY.

We observe that the formation of low-angle grain boundaries (sub-boundaries) depends strongly on the thickness of the recrystallized Si film. The average lateral spacing between adjacent sub-boundaries increases from 40 μm for 4000-Å films to 500 μm for unseeded Si films 30 μm thick. For seeded 30-μm Si films on 1.6 mm by 1.6 mm buried oxide islands, areas exceeding 1.0 mm by 1.0 mm have been recrystallized which are free of all sub-boundaries, but which contain dislocations in other configurations. *IN*

407). TEM-Investigations of Recrystallized Silicon Films on Insulators by Zone Melting and Flash Lamp Irradiation.
Scharff, W.; Erben, J.-W.; Hoppner, K.; Wolf, A.; Klabes, R.;
Matthai, J.; Voelskow, M.; Wieser, E.
Sektion Phys., Tech. Hochschule, Karl-Marx-Stadt, Germany.
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors).
Energy Pulse Modification of Semiconductors and Related Materials. Proceedings of the Conference, 397-401, Vol.2, 25-28 Sept. 1984, Dresden, Germany.
Akad. Wissenschaften DDR, Dresden, Germany.

The recrystallization of flat polycrystalline silicon films on insulating substrates by the zone-melting process is a well-established technology for electronic device applications. For the authors' recrystallization experiments, polycrystalline silicon films deposited on thermally grown silicon dioxide

and encapsulated with a combination of silicon dioxide and silicon nitride layers were recrystallized by zone melting using the focused light of a rod-like halogen lamp in an elliptical aluminium mirror. *IN*

408). Display Quality SOI by Recrystallization of Bridged Silicon Islands on Quartz.
Bak, C.S.; Braatz, P.O.; Margerum, J.D.
Hughes Res. Lab., Malibu, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 215-20, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Arrays of single-crystal thin-film silicon islands were prepared of fused quartz substrates by a zone-melting recrystallization of bridged island patterns of poly-Si. A scanning graphite-strip-heater technique was used, with the Si islands connected ('bridged') in the scanning direction by narrow Si strips. These strips generated a self-seeding effect in the crystalline growth, and the recrystallized Si islands were good quality SOI with (100) orientation as shown by x-ray and etch-pit analysis. Protuberances, film cracking, and impurity segregation were greatly suppressed in this bridged island SOI as compared to defects normally observed in recrystallized continuous Si films on quartz. MOSFETs were fabricated in the SOI islands, using n-channel enhancement-mode devices with a gate length of 5 μm and a gate width of 50 μm. The average carrier mobility measured on these SOI devices was $470 \pm 70 cm^2/V{\cdot}s$, which was twice as high as the mobility measured in MOSFETs fabricated concurrently in SOS. Good MOSFETs in the SOI islands showed a switching ratio of about 10^7 at 6 V and a leakage of less than 2 pA/μm. These results indicate that high-performance drive circuits for liquid crystal displays can be fabricated in SOI recrystallized from bridged island patterns on transparent quartz substrates. *IN*

409). Use of Zone-Melting Recrystallization to Fabricate a Three-Dimensional Structure Incorporating Power Bipolar and Field-Effect Transistors.
Geis, M.W.; Chen, C.K.; Mountain, R.W.; Economou, N.P.; Lindley, W.T.; Hower, P.L.
MIT Lincoln Lab., Lexington, MA.
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.1, 41-3, Jan. 1986

Three-dimensional (3-D) structures were fabricated incorporating power bipolar transistors in a Si substrate and metal-oxide-semiconductor field-effect transistors (MOSFETs) in an overlying silicon-on-insulator (SOI) film that was zone-melting recrystallized with a graphite-strip heater. Both n-p-n and p-n-p bipolar transistors were used. The n-p-n devices exhibited no significant change in transistor characteristics after zone-melting recrystallization (ZMR), while the p-n-p devices showed a substantial reduction in breakdown voltage. The MOSFETs exhibited electron mobilities comparable to those in similar devices fabricated in single-crystal Si wafers. The bipolar transistor yield is approximately 90%. The unusually high device quality and yield for 3-D structures obtained by the ZMR technique demonstrates the feasibility of fabricating monolithic structures incorporating both logic functions and relatively high-current high-voltage power switches. *IN*

410). Characteristics of a 1.2-μm CMOS Technology Fabricated on an RF-Heated Zone-Melting Recrystallized SOI.
Kobayashi, Y.; Fukami, A.; Nagano, T.
Res. Lab., Hitachi Ltd., Ibaraki, Japan
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.6, 350-2, June 1986

A 0.7- to 5-μm CMOSFET were fabricated on SOI which was recrystallized using an rf-heated zone-melting recrystallisation method. Their performance characteristics are presented. The leakage currents of n-channel MOSFETs having gate lengths between 5- and 0.7-μm range between 10^{-14} and $10^{-12} A/\mu m$ and show no dependence on channel length. Those of the p-channel MOSFETs were $10^{-14} - 10^{-12} A/\mu m$ when the gate lengths were longer than 1.2 μm, and increased when the

gate lengths were shorter than 1.0 μm. The propagation delay time of the CSMOSFET inverter was 0.13 ns per stage at a supply voltage of 3.5 V. *IN*

411). Improvement of SOI/MOSFET Characteristics by Recrystallizing Connected Silicon Islands on Fused Silica.
Kobayashi, Y.; Fukami, A.
Hitachi Ltd., Ibaraki, Japan.
IEEE Electron Device Lett. (USA), Vol. EDL-5, No.11, 458-60, Nov. 1984

N-channel MOSFETs were fabricated on isolated and connected islands which were recrystallized on fused silica substrates using a rf-heated zone-melting recrystallization method. The field-effect mobility of the device fabricated on the connected silica island was about 900 $cm^2/V{\cdot}s$, which was twice that of the device fabricated on the isolated island, and its leakage current was $10^{-13}A/\mu m$, which was two orders lower than that of the latter. These observations were attributed to realization of (100) oriented silicon and decrease of positive charge density at the silicon/fused silica interface by recrystallizing the connected polycrystalline silicon island. *IN*

412). RF Recrystallization of Polycrystalline Silicon on Fused Silica for MOSFET Devices.
Kobayashi, Y.; Fukami, A.; Suzuki, T.
Hitachi Res. Lab., Hitachi Ltd., Ibaraki, Japan
J. Electrochem. Soc. (USA), Vol.131, No.5, 1188-94, May 1984

A new zone-melting recrystallization method that uses an rf-heated carbon susceptor in fabrication of silicon-on-insulator (SOI) structures has been developed. A fused silica substrate, on which a 0.5- to 1.0-μm thick polycrystalline silicon film had been deposited, was encapsulated with a 1.2-μm thick CVD-SiO_2 layer. This was moved across the carbon susceptor, which had a narrow high-temperature zone. The continuous silicon films that were recrystallized had grains several tenths to a few millimeters wide, a few centimeters long, and a film orientation of (100). The electron mobility of MOSFETs fabricated on the films was about 700 to 1000 $cm^2/V{\cdot}s$, which was higher than that of (100) orientated bulk single-crystal silicon. However, as some cracks occurred in the film, it was formed as islands and then the islands were recrystallized. This recrystallized silicon was a single crystal with an orientation of (111) and showed no cracks. The electron field-effect mobility of the islands was about 300 to 600 $cm^2/V{\cdot}s$, which was smaller than that of the recrystallized continuous film because of the (111) orientation. In order to obtain silicon without cracks and with an orientation of (100), a method that connected the polycrystalline silicon islands with narrow strips was proposed based on a thermal connection of silicon. *IN*

413). SOI CMOS Circuit Performance on Graphite Strip Heater Recrystallized Material.
Malhi, S.D.S.; Lam, H.W.; Pinizzotto, R.F.
Texas Instruments Inc., Dallas, TX.
International Electron Devices Meeting, Technical Digest, 441-3, 1982
13-15 Dec. 1982, San Francisco, CA.
IEEE, New York.

A CMOS Process has been implemented on graphite-strip-heater recrystallized silicon substrates. The low field electron mobility of 660 $cm^2/V{\cdot}s$ and hole mobility of 220 $cm^2/V{\cdot}s$ is obtained. For a gate length of 5 μm and gate oxide thickness of 500 Å, the average inverter delay is 1.85 ns, as obtained from 39-stage ring oscillators with a fan-in and fan-out of 1, operated at 5 V. *IN*

414). Silicon-on-Insulator Bipolar Transistor.
Rodder, M.; Antoniadis, D.A.
MIT, Cambridge, MA.
IEEE Electron Device Lett. (USA), Vol.EDL-4, No.6, 193-5, June 1983

Thin-film lateral n-p-n bipolar transistors (BJT) have been fabricated in moving melt-zone recrystallized silicon on a 0.5-μm silicon dioxide substrate thermally grown on bulk silicon. Current-voltage characteristics of devices with different base widths (5 and 10 μm) have been analyzed. The use of a metal gate over the oxide covering the base region has allowed the devices to be operated as n-channel MOSFETs as well, thus surface effects on device characteristics have been investigated under varying gate-bias voltages. Maximum dc current gain values of 2.5 were achieved with a 5-μm base width and values around 0.5 with a 10-μm base width. Higher gain values were impeded by onset of high-level injection which occurred at low currents because of light base doping of these devices. *IN*

415). Slant-Scanning and Interstice-Bridging Methods Used to Produce Highly Uniform ZMR Si Films on Quartz Wafers.
Tomita, H.; Usui, S.
Sony Corp, Research Cent, Yokohama, Japan
IEEE Electron Device Letters, Vol. EDL-7, No. 6, 356-358, June 1986

Two methods applied to zone-melting recrystallization using a graphite-strip heater to produce highly uniform and high-quality Si films on 3-in quartz wafers are presented. The characteristics of MOSFETs fabricated in 2/V-s Si films are also reported. The slant-scanning method was used to prepare grain-boundary-free recrystallized Si films in 180-μm wide stripes separated by 20 μm. The interstice-bridging method was used to reduce the $< 111 >$ texture generation to less than 1%. The average electron mobility and the average threshold voltage for MOSFETs were 960 cm^2/V-s with a standard deviation of 43 cm^2/V-s and 1.38 V with a standard deviation of 0.25 V, respectively. *EI*

416). Effects of Ionizing Radiation on SOI/CMOS Devices Fabricated in Zone-Melting-Recrystallized Si Films on SiO_2.
Tsaur, B.-Y.; Mountain, R.W.; Chen, C.K.; Turner, G.W.; Fan, J.C.C.
Lincoln Lab., MIT, Lexington, MA.
IEEE Electron Device Lett. (USA), Vol.EDL-5, No. 7, 238-40, July 1984

The effects of ionizing radiation on SOI/CMOS devices fabricated in zone-melting-recrystallized Si films on SiO_2-coated Si substrates have been investigated as a function of the negative bias applied to the substrate during irradiation and measurement. For these devices, which have a thin-gate oxide 10 nm thick, the optimum substrate bias is -5 V. For total doses up to 10^7 rad(Si), with this bias they exhibit low subthreshold leakage currents ($< 0.2 - pA/\mu$m channel width), small threshold voltage shifts ($\leq$0.18 V for n-channel devices and $\leq$0.46 V for p-channel devices), and very little transconductance degradation (<5%). *IN*

417). Fully Isolated Lateral Bipolar-MOS Transistors Fabricated in Zone-Melting-Recrystallized Si Films on SiO_2.
Tsaur, B.-Y.; Silversmith, D.J.; Fan, J.C.C.; Mountain, R.W.
Lincoln Lab., MIT, Lexington, MA.
IEEE Electron Device Lett. (USA), Vol.EDL-4, No.8, 269-71, Aug. 1983

A four-terminal device that can be operated either as a lateral n-p-n bipolar transistor or as a conventional n-channel MOSFET has been fabricated in silicon-on-insulator films prepared by graphite-strip-heater zone-melting recrystallization. Common-emitter current gain close to 20 and emitter-base breakdown voltage in excess of 10 V have been obtained for bipolar operation. As a MOSFET, the device exhibits well-behaved enhancement-mode characteristics with a field-effect mobility of 600 $cm^2/V{\cdot}s$ and drain breakdown voltage exceeding 15 V. *IN*

418). Merged CMOS/Bipolar Technologies and Microwave MESFETs Utilizing Zone-Melting-Recrystallized SOI Films.
Tsaur, B.-Y.; Choi, H.K.; Chen, C.K.; Chen, C.L.; Mountain, R.W.; Fan, J.C.C.
Lincoln Lab., MIT, Lexington, MA.

International Electron Devices Meeting, Technical Digest, 812-15, 1984
9-12 Dec. 1984, San Francisco, CA.
IEEE, New York.

Two merged CMOS/bipolar technologies utilizing SOI structures have been demonstrated. In each case, a single sequence of processing steps was used to fabricate fully isolated CMOS devices and vertical bipolar transistors on the same Si wafer. The CMOS devices were fabricated in a zone-melting-recrystallized SOI film, while the bipolar devices were fabricated either in the SOI film or in epitaxial Si layers grown selectively on the Si substrate. Good electrical characteristics were obtained for the CMOS devices and for both SOI and epitaxial bipolar devices. In addition, microwave MESFETs have been fabricated in zone-melting-recrystallized Si films on bulk fused-silica substrates. These devices exhibited maximum frequency of oscillation of 8 to 14 GHz. At 1.2 GHz, an optimum noise figure of 2.5 dB and associated gain of 10.4 dB were measured. *IN*

419). Merged CMOS/Bipolar Technologies Utilizing Zone-Melting-Recrystallized SOI Films.
Tsaur, B.-Y.; Mountain, R.W.; Chen, C.K.; Fan, J.C.C.
Lincoln Lab., MIT, Lexington, MA.
IEEE Electron Device Lett. (USA), Vol. EDL-5, No. 11, 461-3, Nov. 1984

Merged CMOS/bipolar technologies utilizing SOI (silicon-on-insulator) structures have been demonstrated. In each case, a single sequence of processing steps was used to fabricate fully isolated CMOS devices and vertical bipolar transistors on the same Si wafer. The CMOS devices were fabricated in zone-melting-recrystallized SOI film, while the bipolar devices were fabricated either in the SOI film or in epitaxial Si layers grown selectively on the Si substrate. Good electrical characteristics were obtained for the CMOS devices and for both SOI and epitaxial bipolar devices. *IN*

• 420). Radiation-Hardened JFET Devices and CMOS Circuits Fabricated in SOI Films.
Tsaur, B.Y.; Sferrino, V.J.; Choi, H.K.; Chen, C.K.; Mountain, R.W.;
Schott, J.T.; Shedd, W.M.; LaPierre, D.C.; Blanchard, R.
Lincoln Lab., MIT, Lexington, MA
IEEE Trans. Nucl. Sci., Vol. NS-33, No. 6, Pt. 1, 1372-6, 1986

The effects of total-dose radiation were investigated for the first complementary JFETs fabricated in zone-melting-recrystallized (ZMR) Si films on SiO_2-coated Si substrates. With a –5 V bias applied to the Si substrate during irradiation and device operation, both n- and p-channel devices show low threshold-voltage shift, low leakage currents, and small transconductance degradation for total doses up to 10^8 rad(Si). Fully functional CMOS 1 K static RAMs and 1.2 K gate arrays were fabricated in both ZMR and O-implanted (SIMOX) Si-on-insulator (SOI) films. The ZMR circuits are superior in speed performance to the SIMOX circuits because parasitics are smaller for the ZMR structure. Excellent transient-radiation hardness was demonstrated for both ZMR and SIMOX SRAMs, which showed no logic upset for dose rates up to 7×10^{10} rad(Si)/s. *CA*

• 421). Radiation-Hardened Silicon-on-Insulator Complementary Junction Field-Effect Transistors.
Tsaur, B.-Y.; Choi, H.K.
MIT Lincoln Lab., Lexington, MA.
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.5, 324-6, May 1986

The effects of total-dose radiation have been investigated for complementary junction field-effect transistors fabricated in zone-melting recrystallized Si films in SiO_2-coated Si substrates. With a –5 V bias applied to the Si substrate during irradiation and device operation, both n- and p-channel devices show low threshold-voltage shift ($\leq$ 0.09 and $\leq$ 0.12 V, respectively), low leakage currents (≤ 1 and $< 3 - pA/\mu m$ channel width, respectively), and small transconductance degradation (<15%) for total doses up to 10^8 rad (Si). *IN*

422). Silicon-on-Insulator MOSFETs Fabricated in Zone-Melting-Recrystallized Poly-Si

Films on SiO_2.
Tsaur, B.-Y.; Geis, M.W.; Fan, J.C.C.; Silversmith, D.J.; Mountain, R.W.
Lincoln Lab., MIT, Lexington, MA.
Appleton, B.R.; Celler, G.K. (Editors)
Laser and Electron Beam Interactions with Solids. Proceedings of the Materials Research Society Annual Meeting, 585-90, 1982
16-19 Nov. 1981, Boston, MA.
North-Holland, Amsterdam, Netherlands.

N- and p-channel enhancement-mode MOSFETs have been fabricated in Si films prepared by zone-melting recrystallization of poly-Si deposited on SiO_2-coated Si substrates. The transistors exhibit high surface mobilities, in the range of 560 to 620 $cm^2/V{\cdot}s$ for electrons and 200 to 240 $cm^2/V{\cdot}s$ for holes, and low leakage currents of the order of 0.1 $pA/\mu m$. Uniform device performance with a yield exceeding 90% has been measured in tests of more than 100 devices. The interface between the Si film and the SiO_2 layer on the substrate is characterized by an oxide charge density of 1 to $2\times10^{11}cm^{-2}$ and a high surface carrier mobility. N-channel MOSFETs fabricated in Si films recrystallized on SiO_2-coated fused quartz substrates exhibit surface electron mobilities substantially higher than those of single-crystal Si devices because the films are under a large tensile stress. *IN*

423). SOI/CMOS Circuits Fabricated in Zone-Melting-Recrystallized Si Films on SiO_2-Coated Si Substrates.
Tsaur, B.Y.; Fan, J.C.C.; Chapman, R.L.; Geis, M.W.; Silversmith, D.J.; Mountain, R.W.
Lincoln Lab., MIT, Lexington, MA.
IEEE Electron Device Lett. (USA), Vol.EDL-3, No.12, 398-401, Dec. 1982

A CMOS test circuit chip containing six arrays of 360 to 533 parallel transistors, two 1-stage ring oscillators, and two inverter chains has been designed for evaluating SOI wafers prepared by using the graphite strip-heater technique for zone-melting recrystallization of poly-Si films on SiO_2-coated Si substrates. One 2-in diameter wafer has been evaluated in detail by testing all the circuits on each of 98 chips fabricated in the recrystallized film. These measurements reveal a good yield of functional circuits, and most of the failures can be explained by obvious metallization defects. The operating characteristics of each type of circuit are quite uniform from chip to chip. For the ring oscillators, which have a 5-μm gate length and fan in and out of 1, at a supply voltage of 5 V the switching delay time is about 2 ns per stage and the power-delay product is 0.2 to 0.3 pJ per stage. *IN*

424). Submicrometer CMOS Devices in Zone-Melting-Recrystallized SOI Films.
Tsaur, B.; Chen, C.K.
MIT Lincoln Lab., Lexington, MA.
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.7, 443-5, July 1986

CMOS devices with effective channel lengths ranging from 0.7 to 4.0 μm have been fabricated in zone-melting-recrystallized silicon-on-insulator films prepared by the graphite-strip-heater technique. Low-temperature processing was utilized to minimize dopant diffusion along subboundaries in the films. Both n- and p-channel devices have low leakage current ($< 0.1 - pA/\mu m$ channel width) and good subthreshold characteristics. For ring oscillators with a transistor channel length of 0.8 μm, the propagation delay is 95 ps at a supply voltage of 5 V. *IN*

425). Electrical Characterization of Beam-Recrystallized SOI Structures Using a Depletion Mode Transistor.
Vu, D.P.; Chantre, A.; Ronzani, D.; Pfister, J.C.
Cent. Natl. Etud. Telecommun., Meylan, France
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 357-61, 1986

A depletion-mode transistor, a very versatile tool for the electrical characterization of Si-on-insulator (SOI) structures, is applied to Si thin films recrystallized by using a zone-melting technique in which grain-boundaries are localized. Apart from the transport parameters, one can get from drain-source current the information usually determined from a MOS capacitor. Due to the existence in such a transistor of two MOS structures, both Si-SiO_2 interfaces, as well as the "bulk" of the Si film, could be characterized. *CA*

11. SIMOX

Comprehensive Treatment

426). Formation of Buried Insulating Layers by High Dose Oxygen Implantation under Controlled Temperature Conditions.
Bruel, M.; Margail, J.; Stoemenos, J.; Martin, P.; Jaussaud, C.
CEN, Lab d'Etudes et de Technologie de l'Informatique, Grenoble, France
Vacuum, Vol. 35, No. 12, 589-593, Dec. 1985

A sample holder is described for preparing Si-on-insulator structures by high-dose O implantation. A molten Sn layer is used as a thermal contact. The optimum annealing conditions for forming Si-SiO_2 structures for integrated circuits are described. *CA*

427). An Overview of SOI by Implantation of Oxygen: Materials, Devices and Circuits.
Burnham, M.E.; Wilson, S.R.
Semicond. Res. & Dev. Labs., Motorola Inc., Phoenix, AZ.
Proc. SPIE Int. Soc. Opt. Eng. (USA), Vol.530, 240-50, 1985
Advanced Applications of Ion Implantation, 23-25 Jan. 1985, Los Angeles, CA.

Silicon-on-insulators (SOI) formed by ion implantation of oxygen has been examined by several researchers including the present authors. This paper gives a brief review of this subject. The advantages of SOI versus silicon on sapphire (SOS) and bulk Si are discussed. The materials properties and the effects of ion implantation and anneal conditions are reviewed. Device modeling as it applies to SOI has been presented. Characteristics of devices built in SOI formed by ion implantation of oxygen are examined. *IN*

• 428). Improved SOI Films by High Dose Oxygen Implantation and Lamp Annealing.
Celler, G.K.; Hemment, P.L.F.; West, K.W.; Gibson, J.M.
AT&T Bell Lab., Murray Hill, NJ
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 227-32, 1986

Ion-beam synthesis of a buried SiO_2 layer is an attractive Si-on-insulator (SOI) technology for high-speed complementary MOS circuits and radiation-hardened devices. A new annealing procedure at 1405°C is demonstrated that produces Si films of excellent quality, essentially free of O precipitates and with sharp interfaces between the Si and the SiO_2. *CA*

• 429). Silicon-on-Insulator Films by Oxygen Implantation and Lamp Annealing.
Celler, G.K.
AT&T Bell Labs., Murray Hill, NJ.
Solid State Technol. (USA), Vol. 30, No. 3, 93-8, Mar. 1987

Ion-beam synthesis of a buried SiO_2 layer is an attractive silicon-on-insulator (SOI) technology for high-speed CMOS circuits and radiation-hardened devices. Recent progress in achieving high-quality SOI structures, essentially free of oxygen precipitates and with sharp interfaces between the Si and the SiO_2, is reviewed here.

430). Silicon on Insulator Formed by Oxygen(1+) or Nitrogen(1+) Ion Implantation.
Hemment, P.L.F.
Dep. Electron. Electr. Eng., Univ. Surrey, Guildford/Surrey, United Kingdom
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 207-21, 1986

The synthesis of buried layers of SiO_2 and Si_3N_4 by ion implantation is reviewed. This process, which may be used to form device-worthy Si on-insulator structures, involves (1) implantation of

O^+ or N^+ and (2) high-temperature processing to achieve defect annealing and chemical segregation of the implanted species. *CA*

431). Silicon on Insulator Structures Formed by Ion Implantation.
Hemment, P.L.F.
Univ. of Surrey, Guildford, United Kingdom
Vacuum, Vol. 35, No. 10-11, Oct.-Nov. 1985, Proc. of the SIRA Int. Seminar on Thin Film Prep. and Process Technol., Brighton, UK, Mar. 26-28, 1985, 509 *EI*

432). RANDD Project on Future Electron Devices in Japan.
Kawashima, M.
Res. and Dev. Assoc. for Future Electron Devices, Tokyo, Japan
Penfield, P., Jr. (Editor)
Proceedings, Conference on Advanced Research in VLSI, 123, 1984
23-25 Jan. 1984, Cambridge, MA.
MIT, Cambridge, MA.

The eight- to ten-year RANDD project on future electron devices was established in 1981 by the Japanese government with the aim of developing basic technoloty in the 1990s. It consists of three research items: superlattice devices, three-dimensional ICs, and hardened ICs for extreme conditions. The organization and plans of this project are first briefly described. Some recent results are then discussed in connection with the major research targets for each device, which are (for the first three- to four-year period): superlattices – fine control of crystal growth to several atomic layers; 3-D ICs – development of SOI and related technology for 2- to 3-layer structures; hardened ICs – improvement of processes and devices to withstand 2 to 10×10^4 rad device characterization. *IN*

433). Effect of Background Doping on the Superficial Silicon Layer of SOI Wafers Synthesized by Oxygen Implantation.
Krause, S. J.; Jung, C. O.; Wilson, S. R.
Dep. Mech. Aerosp. Eng., Arizona State Univ., Tempe, AZ
Proc. - Electrochem. Soc., 86-4(Semicond. Silicon 1986), 642-51, 1986

The effect was studied of background dopant and dopant level on the structure of O-implanted Si-on-insulator (SOI) material by TEM. All wafers, when O-implanted, either unheated or with a 400°C substrate temperature, developed a heavily damaged superficial Si layer above a buried oxide layer. After annealing, all wafers had a superficial layer with a precipitate-free region at the surface which was located above a precipitate-rich region. During annealing, the buried oxide layer grew toward the surface in lightly B- or P-doped wafers, but did not grow at all in heavily doped As or Sb wafers. In the As- and the Sb-doped wafers implanted unheated, a thin, sharply bounded amorphous layer developed in the superficial layer above the buried oxide. Upon annealing, the amorphous layer transformed into two thin bands, above the buried oxide, of polycrystalline Si with precipitates and precipitate-free single-crystal Si. Overall, the major effects of heavy background doping were to inhibit growth of the buried oxide layer during annealing and to produce a unique structure at the interface region of the superficial Si and buried oxide layers. *CA*

434). A Review of Silicon-on-Insulator Formation by Oxygen Ion Implantation.
Pinizzotto, R.F.
Mater. Sci. Lab., Texas Instrum. Inc., Dallas, TX.
Hubler, G.K.; Holland, O.W.; Clayton, C.R.; White, C.W. (Editors)
Ion Implantation and Ion Beam Processing of Materials. Proceedings of the Symposium, 265-74, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

Silicon-on-insulator structures will be an important technological advance used in future VLSI, VHSIC, and three-dimensional integrated circuits. The most mature SOI technology other than

silicon-on-sapphire is SIMOX, or separation by implanted oxygen. High-energy oxygen ions are implanted into single-crystal silicon until stoichiometric buried silicon dioxide layer is formed. After implantation, the material is annealed at high temperature to remove implantation-induced defects. The structure is completed by the growth of a thin epitaxial silicon layer. Devices and complex circuits have been successfully fabricated by several research groups. This paper reviews the development of this buried oxide SOI technology from 1973 to 1983. The five major sections discuss the advantages of SOI, the basics of buried oxide formation, the literature published between 1973 and 1983, key issues that must be solved before large-scale implementation takes place, and finally, predictions of future characterization that confirm the device-worthy potential of this material. *IN*

435). A Review of Silicon-on-Insulator Formation by Oxygen Ion Implantation.
Pinizzotto, R.F.
Materials Sci. Lab., Texas Instruments Inc., Dallas, TX.
J. Vac. Sci. and Technol. A (USA) Vol.2, No.2, Pt.1 597-8 April-June 1984
Proceedings of the 30th National Symposium of the American Vacuum Society
31 Oct.-4 Nov. 1983, Boston, MA.

The formation of SOI by the implantation of large doses of oxygen has been shown to be a commercially useful technique. The material is well understood and can be tailored to meet a specific application. ICs manufactured on buried oxide SOI have been shown to have properties that cannot be obtained with other materials. The abrupt oxide/silicon interfaces and the existence of the electric field shield layer are unexpected features that can be exploited. It has been demonstrated that CMOS circuits built on buried oxide are faster than the same circuits built on bulk single crystal. A three-dimensional material structure has been fabricated, but the lack of an interlevel connection technique has prevented device applications. Many believe that the long implant times required will keep this technology from being used in mass production. This is probably not true. There are implantation machines available now that are capable of producing 10 mA of oxygen at 80 keV (Hitachi) or 6 mA at 150 keV (Nova). NTT is developing the technology for a 100-mA 150-keV implantation machine. When these instruments become available, implant times will be only a few minutes per wafer. *IN*

436). Silicon on Insulator by Ion Implantation: A Dream or a Reality?
Pinizzotto, R.F.
Ultrastructure Inc., Richardson, TX.
Nucl. Instrum. & Methods Phys. Res. Sect. B (Netherlands), Vol. B7-8, Pt. 1, 261-4, March 1985
Proceedings of the Fourth International Conference on Ion Beam Modification of Materials, 16-20 July 1984, Ithaca, NY.

One method of producing a silicon-on-oxide structure is to implant a sufficient dose of oxygen into a conventional silicon substrate to synthesize a layer of SiO_2 just below the surface. If the proper implant conditions are maintained, the top silicon layer will be a single crystal. The required doses are large, but the use of commercially available medium current implanters can reduce the time to 25 minutes per wafer. This adds about $10 per chip in process-related costs. A very large implanter (100-mA analyzed beam) may not be the best approach for scaling up the process. The power in the beam and the power required for operation of the machine are both enormous. A more conservative approach of using multiple medium current implanters may prove to be more economical in the long run. *IN*

437). Self-Aligned Oxygen-Implanted SOI (SALOX SOI) Technology.
Tzeng, J. C.; Baerg, W.; Ting, C.; Siu, B.
Intel Corp, Santa Clara, CA
IEEE Transactions on Electron Devices, Vol. ED-33, No. 11, 44th Annual Device Res. Conf., Amherst, MA, June 23-25, 1986, 1841-1842 *EI*

438). Synthesis of Silicon Dioxide by Ion Implantation.
Wilson, I.H.
Dept. of Electronic and Electrical Engng., Univ. of Surrey, Guildford, England.
Nucl. Instrum. and Methods Phys. Res. Sect. B (Netherlands), Vol. 229, No. 2-3, 331-43, Feb. 1984.
Proceedings of the 2nd International Conference on Radiation Effects in Insulators, 30 May-3 June 1983, Albuquerque, NM.

The first pioneering and primitive attempts at synthesis of SiO_2 by implantation of oxygen into single-crystal silicon were in the late 1960s. The early layers, assessed mainly by infrared absorption and electrical measurements, were poor in quality. The prognosis for their use in microelectronics was pessimistic. Undeterred by this, a second wave of experimenters continued to study these layers and Rutherford backscattering analysis (RBS) was brought into use. Lately, buried oxide layers have been used to create silicon-on-insulator structures for high-speed CMOS (Complementary Metal-Oxide-Semiconductor (transistors)) integrated circuits. Progress has been rapid in the last six years, and results from analysis of buried layers by RBS, TEM, SIMS, AES, and XPS enable optimization of implant and annealing procedures for fabrication of device structures. However, many questions remain unanswered with regard to the microstructure of the various layers, particularly the near surface regions. Mass transport during implantation and annealing is not fully understood. Recent results in the areas of radiation damage and the behaviour of oxygen in silicon and SiO_2 shed light into some of these areas. *IN*

439). High Quality Si-on-SiO_2 Films by Large Dose Oxygen Implantation and Lamp Annealing.
Celler, G.K.; Hemmnent, P.L.F.; West, K.W.; Gibson, J.M.
AT&T Bell Labs., Murray Hill, NJ.
Appl. Phys. Lett. (USA), Vol.48, No.8, 532-4, 24 Feb. 1986

Ion-beam synthesis of a buried SiO_2 layer is an attractive silicon-on-insulator technology for high-speed complementary metal-oxide-semiconductor circuits and radiation-hardened devices. The authors demonstrate here a new annealing procedure at 1405°C that produces silicon films of excellent quality, essentially free of oxygen precipitates and with sharp interfaces between the Si and the SiO_2. Buried oxide layers have been formed in Si (100) wafers by implanting 400-keV molecular oxygen at 500°C to a dose of $1.8 \times 10^{18} cm^{-2}$. Annealing was performed by radiative heating of the back side of each sample to the melt temperature of silicon, T_M=1412°C, so that the buried oxide structure was at 1405°C. The temperature control relies entirely on the change in optical properties of silicon upon melting. This ensures, without any external feedback, that the surface exposed to the photon flux will remain at T_M. *IN*

440). Improvement of Crystalline Quality of the Surface Layer in Buried Implanted Oxide Structures by Silicon Implantation.
Das, K.; McClelland, S.; Butcher, J.B.
Microelectronics Centre, Middlesex Polytech., London, England
Electron. Lett. (GB), Vol.20, No.13, 526-7, 21 June 1984

An improvement of the crystalline quality of the surface layer in buried implanted oxide structures in silicon has been achieved by silicon ion implantation and subsequent 570°C anneal treatment. *IN*

441). Silicon-On-Insulator Structures Using High Dose Oxygen Implantation to Form Buried Oxide Films.
Das, K.; Shorthouse, G.; Butcher, J.; Anand, K.V.
Univ. of Kent, Canterbury, England;
Microelectron. J. (GB), Vol.14, No.6, 88-107, Nov.-Dec. 1983

The feasibility of growing epitaxial layers of silicon-on-silicon substrates with a buried oxide layer formed by the implantation of oxygen ions has been studied. Buried implanted oxide layers have been formed by high-dose implantation of oxygen ions in silicon. The effect of dose at a given energy for a given peak concentration on the distribution profile of oxygen has been studied. An approximately gaussian distribution is observed at doses contributing less than the stoichiometric requirement of oxygen for the formation of silicon dioxide. A saturation in the peak oxygen concentration is reached when the stoichiometric requirement is exceeded. A consequent reduction in the interface damage is also observed. Other parameters being equal, at higher substrate temperatures the interface damage is decreased. It has been attempted to optimise conditions for a dose of $1.4 \times 10^{18} cm^{-2}$ at 200 keV which provided the stoichiometric concentration only at the peak of the distribution. The epitaxial layers deposited on substrates maintained at approximately 550°C during implantation have a crystalline quality comparable to those of layers on untreated substrates. Fabricated p-n junction diodes have low leakage currents and high breakdown voltages. The minority carrier lifetime is comparable to that in diodes processed similarly but without an implanted oxide layer. *IN*

• 442). Dependence of Silicon-on-Insulator Transistor Parameters on Oxygen Implantation Temperature.
Davis, J.R.; Taylor, M.R.; Spiller, G.D.T.; Skevington, P.J.; Hemment, P.L.F.
British Telecom Res. Labs., Martlesham Heath, Ipswich, England
Appl. Phys. Lett. (USA), Vol.48, No.19, 1279-81, 12 May 1986

Silicon-on-insulator films have been formed by high-dose oxygen implantation. Thermal donors, resulting from the residual oxygen content of the single-crystal silicon region of the films, have been found to influence the electrical performance of transistors fabricated in them. The amount of oxygen in the active region of the silicon layer is strongly dependent on the oxygen implantation temperature. As the temperature is decreased below 500°C, an increasing thickness of oxygen-rich polycrystalline silicon is formed between the single-crystal region and the buried oxide, causing the oxygen concentration in the single-crystal region (and hence the thermal donor activity) to fall. As well as providing thermal donors, the residual oxygen also causes a lattice strain which increases the electron mobility.

443). Oxygen Implanter for SIMOX.
Guerra, M.; Benveniste, V.; Ryding, G.; Douglas-Hamilton, D.H.; Reed, M., Gagne, G.; Armstrong, A.; Mack, M.
Ion Beam Syst. Div., Eaton Corp., Beverly, MA.
Nucl. Instrum. & Methods Phys. Res. Sect. B (Netherlands) Vol.B6, No.1-2 63-9, Jan. 1985
Proceedings of the Fifth International Conference on Ion Implantation Equipment and Techniques, 23-27 July 1984, Jeffersonville, VT.

Interest in silicon-on-insulator (SOI) technology has led to the development of several alternatives to silicon on sapphire. One of the most promising techniques makes use of an ion implanter to form a buried oxide layer directly in the silicon substrate. To have useful single-crystalline silicon on top of the oxide layer, it is necessary to do the implant at high wafer temperatures and rely on solid phase epitaxy to maintain surface structure. A high-current, 160-keV, Nova ion implanter has been adapted to provide the ability to perform oxygen implants at elevated temperatures. The operator is free to choose any temperature in the range between 400°C and 600°C. The system then preheats the wafers to the selected temperature before the implant begins. A novel technique for providing both heating and cooling capability to the end station is employed. An infrared signal from the wafers is monitored by a room temperature lead salt detector. This signal is then used by a servo-loop to control the heating of the end station and to maintain the wafer temperature to within ±20°C during the implant. High doses of the type necessary to form a silicon dioxide buried layer require long-lived, high-current oxygen sources. An oxygen source has been specially developed, which provides as much as 10 mA of ion current. Special thermal barriers have been employed to protect the apparatus from extreme temperatures and to make the heating sequence more efficient and more rapid. Every effort has been made to avoid contamination of the implant. The implanter has been used to do a high-current oxygen implant with a dose of $1.25 \times 10^{18}/cm^2$, at a temperature of 570°C. Preliminary analysis of the results is very promising. *IN*

• 444). Formation of Buried Insulating Layers in Silicon by the Implantation of High Doses Of Oxygen.
Hemment, P.L.F.; Maydell-Ondrusz, E.; Stephens, K.G.; Butcher, J.; Ioannou, D.; Alderman, J.
Dept. of Electronic and Electrical Engng., Univ. of Surrey, Guildford, England.
Nucl. Instrum. and Methods Phys. Res. (Netherlands), Vol.209-210, Pt.1, 157-64, 1/15 May 1983, Proceedings of the Third International Conference on Ion Beam Modification of Materials, 6-10 Sept. 1982, Grenoble, France.

Silicon wafers have been implanted with 200-keV oxygen to doses of up to $2.4 \times 10^{18} O^+/cm^2$ at implantation temperatures of 325°C to 600°C. Rutherford backscattering and SIMS show the oxygen depth distribution is insensitive to the implantation temperature but is modified by subsequent high-temperature processing. Multiple laser irradiations produced a single-crystal layer at the surface by LPE regrowth but better crystallinity is observed in samples which have been furnace annealed, when a layer of 1000 Å thickness is formed which is denuded of oxygen. Preferred conditions to form a silicon-on-insulator structure (SOI) suitable for VLSI device technology are an

implantation temperature 400 to 500°C followed by furnace annealing at 1150°C for 2 to 4 h with an SiO_2 cap. *IN*

445). Regrowth of Amorphous Layers in Silicon-on-Insulator Structures Formed by the Implantation of Oxygen.
Hemment, P.L.F.; Maydell-Ondrusz, E.A.; Stevens, K.G.; Scovell, P.D.
Dept. of Electronic and Electrical Engng., Univ. of Surrey, Guildford, UK
Electron. Lett. (GB), Vol.19, No.13, 483-5, 23 June 1983

Synthesized silicon-on-insulator structures have been formed and implanted with $1 \times 10^{16} As^{+}/cm^{-2}$ at 40 keV. The regrowth kinetics of the amorphised layer, which also contains lattice defects and excess oxygen, has been studied by Rutherford backscattering. The regrowth of the layer occurs at a mean rate of 13 Å min^{-1} at 500°C with an activation energy of 2.7 ± 0.2 eV. This experiment further demonstrates the suitability of these synthesized structures as a direct replacement for bulk silicon in VLSI technology. *IN*

446). Silicon on Insulator Structures Formed by the Implantation of High Doses of Reactive Ions.
Hemment, P.L.F.; Peart, R.F.; Yao, M.F.; Stephens, K.G.; Arrowsmith, R.P.; Chater, R.J.; Kilner, J.A.
Dept. of Electron. & Electr. Eng., Surrey Univ., Guildford, England
Nucl. Instrum. & Methods Phys. Res. Sect. B (Netherlands), Vol.B6, No.1-2, 292-7, Jan. 1985
Proceedings of the Fifth International Conference on Ion Implantation Equipment and Techniques, 23-27 July 1984, Jeffersonville, VT.

Silicon-on-insulator structures have been formed by implanting O^{+} and N^{+} ions into (100) silicon. The structures have been evaluated by RBS and SIMS techniques. In oxygen-implanted substrates, the thickness and crystal quality of the surface layer is found to be insensitive to the ion energy. The thickness increases with anneal temperature over the range 1100°C to 1200°C and has a maximum value when the substrate temperature during implantation is 500°C. Nitrogen-implanted wafers have a thicker single-crystal layer with very abrupt Si-Si_3N_4 interface.

• 447). Lateral Dopant Diffusion in Implanted Buried-Oxide Structures.
Kamins, T.I.; Chiang, S.Y.
Hewlett-Packard Labs., Palo Alto, CA.
Appl. Phys. Lett. (USA), Vol.47, No.11, 1197-9, 1 Dec. 1985

During fabrication of short-channel transistors in silicon films above implanted buried oxides, the possibility of rapid lateral dopant diffusion in the damaged region near the bottom of the silicon layer is of concern. To investigate the possibility of such enhanced lateral diffusion, arsenic, phosphorus, and boron were diffused into silicon films on buried oxides. No excess lateral diffusion was observed even for the phosphorus diffusion, which penetrated through the thickness of the film in a fraction of the diffusion time. *IN*

448). Silicon-on-Insulator by Oxygen Ion Implantation.
Lam, H.W.; Pinizzotto, R.F.
Texas Instruments Inc., Dallas, TX.
J. Cryst. Growth (Netherlands), Vol.63, No.3, 554-8, Oct. 1983

A silicon-on-insulator SOI material structure can be produced by the formation of a buried oxide layer beneath the surface of a silicon wafer by the implantation of oxygen ions. The typical fluence required is on the order of $1.3 \times 10^{18} cm^{-2}$ of molecular oxygen at 300 keV. A 0.5-μm thick oxide layer is formed buried beneath a 0.12-μm thick layer of silicon. The top silicon layer is recrystallized by a high-temperature anneal after the implantation. Large-scale integrated circuits with excellent performance have been fabricated in epitaxial layers grown on this material. *IN*

449). High-Temperature Annealing of Implanted Buried Oxide in Silicon.
Mogro-Campero, A.; Love, R.P.; Lewis, N.; Hall, E.L.; McConnell, M.D.
Gen. Electr. Res. & Dev. Center, Schenectady, NY.
J. Appl. Phys. (USA), Vol.60, No.6, 2103-5, 15 Sept. 1986

A silicon-on-insulator structure was formed by implanting 2×10^{18} oxygen ions cm^{-2} into crystalline silicon at 150 keV. A systematic investigation of the effect of annealing temperature was carried out by annealing for 6 h at temperatures of 1150, 1200, 1250, and 1295°C. The microstructure and oxygen-concentration profile were investigated by using cross-sectional transmission-electron microscopy and Auger analysis. Changes were observed to occur throughout this annealing-temperature regime. After the highest annealing temperature, a single-crystal top silicon-layer of 150 nm with 4×10^9 dislocations cm^{-2} and no oxide precipitates was obtained. The 500 nm of buried oxide has very sharp interfaces, and contains crystalline-silicon inclusions near the interface with the substrate silicon. *IN*

450). Silicon-on-Insulator by Oxygen Implantation With a Stationary Beam.
Mogro-Campero, A.; Love, R.P.; Lewis, N.; Hall, E.L.
Gen. Electr. Res. & Dev. Center, Schenectady, NY.
Appl. Phys. Lett. (USA), Vol.46, No.9, 862-4, 1 May 1985

A single-crystal silicon layer on top of a buried oxygen has been achieved by implanting oxygen ions of 180 keV into a silicon substrate. A stationary beam and wafer scanning were used, with a dose of $2.4 \times 10^{18} cm^{-2}$. Similar structures produced by ion-beam scanning have been reported previously where scanning rates are sufficiently high to maintain a constant temperature profile during the implantation process. In high-current implanters, a stationary beam is often used, and the wafer is scanned instead. The slower scanning rates in the latter process can result in severe temperature cycling during implantation. This was the case in the present investigation. Nevertheless, as determined by transmission electron microscopy, the as-implanted material in this work is similar to that reported when ion-beam scanning is used. *IN*

451). An Isolation Technique Using A Buried Silicon Dioxide Layer Formed By Oxygen-Ion Implantation-SIMOX.
Ohwada, K.; Izumi, K.; Hayashi, T.
Nishizawa, J. (Editor)
Semiconductor Technologies. 1982, 25-35, 1981
North-Holland, Amsterdam, Netherlands

A description is given of a new isolation technique called SIMOX which uses buried SiO_2 formed by oxygen implantation. A homogeneous buried SiO_2 layer is formed by oxygen implantation, and with an extremely high dose, the interface between the surface Si and the buried oxide layer becomes very sharp and the interface charge density is reduced to the value of $6.9 \times 10^{10} cm^{-2}$. For a CMOS/SIMOX ring oscillator with an effective channel length of 3.1 μm, the propagation delay time and the dissipation power are 0.83 ns and 0.33 mW, respectively. Submicron buried-channel MOSFETs show much smaller threshold voltage shifts than conventional ones. With a ring-oscillator composed of 1-μm channel, the buried-channel MOSFETs show a minimum delay time of 95 ps and a power delay product of 310 fJ. *IN*

452). The Top Silicon Layer of SOI Formed by Oxygen Ion Implantation.
Pinizzotto, R.F.; Vandrager, B.L.; Matteson, S.; Lam, H.W.; Malhi, S.D.S.; Hamdi, A.H.; McDaniel, F.D.
Central Res. Labs., Texas Instruments Inc., Dallas, TX.
IEEE Trans. Nucl. Sci. (USA), Vol.NS-30, No.2, 1718-21, April 1983
1982 IEEE Conference on the Application of Accelerators in Research and Industry, 8-10 Nov. 1982, Denton, TX.

High-dose oxygen ion implantation has been used to form a buried oxide layer in Czochralski-grown silicon. Wafers were implanted with 300-keV O_2^+ to a total dose of $1.32 \times 10^{18} ions\ cm^{-2}$. A 0.5-$\mu$m thick SiO_2 layer is formed beneath a 0.17-μm thick top Si layer. Epitaxial films were grown on both annealed and unannealed wafers. Samples were subsequently annealed at 1150°C for times from 10 to 240 minutes in either Ar or N_2. The highest quality epitaxial layers were obtained with substrates that were annealed after implantation, but prior to epitaxial growth for 2 h at 1150°C followed by 4 h at 1150°C after epitaxial growth. RBS channeling shows that the top 300 nm of these films have (110) channel backscattering yields lower than any SOI produced to date. The buried oxide plus epitaxial process is a leading candidate for VLSI applications. *IN*

453). Some Recent Developments in Industrial Ion Implanters.
Ryding, G.
Div. of Eaton Corp., Ion Beam Syst., Beverly, MA.
Appleton, B.R.; Eisen, F.H.; Sigmon, T.W. (Editors)
Ion Beam Processes in Advanced Electronic Materials and Device Technology
367-79, 1985, 15-18 April 1985, San Francisco, CA.
Mater. Res. Soc., Pittsburgh, PA.

Ion implantation is now a dominant technology for semiconductor doping. The author surveys some of the equipment developed at Eaton Corporation in response to the proliferation of ion implanted devices. Developments in both high-current (approximately 10-mA) and medium-current (approximately 1-mA) implanters is discussed. The evolution of dedicated equipment for the production of buried oxide layers (silicon-on-insulator technology) is also reviewed. *IN*

454). High-Precision MOS Current Mirror.
Akiya, M.; Nakashima, S.
NTT Public Corp., Kanagawa, Japan
IEE Proc. I (GB), Vol.131, No.5, 170-5, Oct. 1984

Matching accuracies of current mirrors using SIMOX technology are discussed. The variation in matching errors has been both qualitatively and quantitatively analysed for MOS current mirrors. Matching errors at low operating currents are dominated by variations in threshold voltage and are inversely proportional to the drain current. In high-current operations, however, they are not dependent on drain current and are dominated by variations in channel length and width. Using 10-μm channel-length devices, matching error less than 0.6% with 100-μA drain current is obtained without any compensation circuits. MOS current mirrors have been found to present greater advantages for low-current operation, such as higher matching accuracy and a smaller pattern area, than similar bipolar current mirrors. *IN*

455). Silicon on Insulator by High Dose Implantation.
Hemment, P.L.F.
Dept. of Electron. & Electr. Eng., Surrey Univ., Guildford, England
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 41-51, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Silicon-on-insulator structures consisting of a buried dielectric, formed by the implantation of high doses of oxygen ions, have been shown to be suitable substrates for LSI circuits. The substrates are compatible with present silicon processing technologies and are confidently expected to be suitable for VLSI circuits. The microstructure and physical properties of this SOI material are described and the dependence of these characteristics upon the implantation conditions and subsequent thermal processing is discussed. With this information, it is then possible to outline the specification for a high-current oxygen implanter. *IN*

456). Optimized Conditions for the Formation of Buried Insulating Layers in Si by High Dose Implantation of Oxygen.
Holland, O.W.; Fathy, D.; Narayan, J.; Sjoreen, T.P.; Wilson, S.R.
Solid State Div., Oak Ridge Nat. Lab., TN.
J. Non-Cryst. Solids (Netherlands), Vol. 71, No. 1-3, 163-70, May 1985
Effects of Modes of Formation on the Structure of Glass. Proceedings of an International Conference, 9-12 July 1984, Nashville, TN.

Results are presented detailing the dependence of the residual damage on substrate temperature and dose for high-dose implantation of oxygen in Si. It has been previously demonstrated that a buried oxide layer can be formed by this method. However, the usefulness of this silicon-on-insulator (SOI) structure has been limited by the considerable damage which accumulates in the crystal overlayer during irradiation. Much of the damage remains even after high-temperature annealing. It is shown that the quality of the crystalline layer depends critically on the implant conditions. The preservation of the crystal quality of this layer by implanting at high temperatures to prevent defect clustering competes with the adverse effects caused by rapid diffusion of oxygen into this region. This leads to a rather narrow range of temperature over which optimization occurs. Rutherford backscattering/channeling spectroscopy and cross-sectional, transmission electron microscopy were used for analyzing the samples and for understanding the phenomena of formation of buried insulating layers. *IN*

457). Model Investigations of the Oxidation of Silicon by High Dose Implantation.

Jager, H.U.
Zentralinst. fur Kernforschung, Dresden, Germany
Deutsche Phys. Gesellschaft
Nucl. Instrum. & Methods Phys. Res. Sect. B (Netherlands) Vol.B15, No.1-6
748-51, April 1986

Using a model which takes into account changes in the ion range, target widening, surface sputtering, and internal oxidation due to unbonded oxygen, the depth profiles obtained after high-dose oxygen implantation into silicon have been calculated for a broad range of ion energies and implanted doses. Some general trends in the theoretical oxygen distributions are discussed with regard to recent investigations on the formation of silicon-on-insulator structures. *IN*

458). High-Voltage CMOS SIMOX Technology and Its Application to a BSH-LSI.
Nakashima, S.; Maeda, Y.; Akiya, M.
NTT Public Corp., Kanagawa, Japan
IEEE Trans. Electron Devices (USA) Vol.ED-33, No.1, 126-32, Jan. 1986

The authors describe high-voltage CMOS separation by implanted oxygen (SIMOX) technology and its application to a BSH-LSI that provides the basic functions of battery feed, supervisory, and hybrid for subscriber line interface circuits. This technology is characterized by the existence of an electric-field-shielding (EFS) layer formed between the buried SiO_2 and the surface Si layer by oxygen implantation. The density of localized states at the Fermi level of the EFS layer is estimated to be about $1 \times 10^{19} cm^{-3} eV^{-1}$ using the Cohen-Fritzsche-Ovshinsky model. The EFS layer reduces the substrate voltage dependence of the threshold voltage and increases the drain-to-source breakdown voltage for 180 V. Compared with a conventional bipolar BSH-LSI, the chip size and the dissipation power of the LSI are reduced by approximately one-third and one-half, respectively. *IN*

459). An Auger Electron Spectroscopy (AES) Investigation Into the Effect of Annealing on the Phase Distribution of Ion Implanted Oxygen in Silicon.
Tuppen, C.G.; Davies, G.J.; Taylor, M.R.; Heckingbottom, R.
British Telecom Res. Labs., Ipswich, England
Baglin, J.E.E.; Campbell, D.R.; Chu, W.K. (Editors)
Thin Films and Interfaces II. Proceedings of the Symposium, 537-42, 1984
14-18 Nov. 1983, Boston, MA.
North-Holland, New York.

Buried oxide layers, formed by high-dose ion implantation have been examined using Auger depth profiling. The phase distribution of oxygen in the wings of the implant profile and effects of high-temperature annealing have been investigated. Ion-beam-induced cascade mixing, which occurs during sputter etching, limits the minimum detectable size of SiO_2 precipitates. However, it is possible to minimise this effect by reducing the ion-beam energy. At very small precipitate sizes (<100 Å) silicon atoms at the edge of the precipitate particles will make a major contribution to the Si KLL Auger spectrum. A previously reported theoretical model has been expanded to take account of this phenomenon. *IN*

• 460). EPR of Defects in Silicon-on-Insulator Structures Formed by Ion Implantation. I. Oxygen$^+$ Implantation.
Barklie, R. C.; Hobbs, A.; Hemment, P. L. F.; Reeson, K.
Dep. Phys., Trinity Coll., Dublin, Ireland
J. Phys. C: Solid State Phys., Vol. 19, No. 32, 6417-32, 1986

EPR measurements at X band and room temperature were made of defects produced by implanting (100) and (111) Si wafers with doses $>10^{18}O^+$ cm^{-2} using 300-keV O^+ and 400 keV O_2^+ and an implantation temperature of 500 to 600°C. These doses are sufficient to form a buried SiO_2 layer. The main features of the EPR spectra are attributed to three types of defect, with (1) g = 2.0003(3), (2) g = 2.0013(2), g = 2.0082(2) with the axis parallel to any [111]-type direction and (3) g = 2.0054(3). The defects are: (1) E1′ centers in the amorphous SiO_2 layer, (2) P_{b0}-like centers primarily at Si/SiO_2 interfaces of SiO_2 precipitates, and (3) amorphous Si centers, possibly associated with O. The angular dependence of the P_{b0}-like center line width was measured, and is interpreted in terms of a spread in g-values. Annealing and etching studies were also made. *CA*

461). Nondestructive Analysis of Silicon-on-Insulator Wafers.
Bunker, S.N.; Sioshansi, P.; Sanfacon, M.M.; and Tobin, S.P.
Spire Corporation, Bedford, MA
Appl. Phys. Lett. Vol. 50, No.26, 1900-1902, 29 June 1987

Silicon-on-insulator structures have been fabricated using implantation of 160-keV oxygen ions at a dose of 1.9×10^{18} atoms/cm^2 with a wafer temperature of 500°C and no oxide cap. Both the as-implanted and annealed wafers were examined with optical reflectometry to determine the resultant interference pattern produced by the presence of the buried layer of SiO_2. The optical data are compared to the predictions of a calculation which simulated the geometry using a detailed multilayer optical model. Parameters of the model were adjusted to provide a best fit to the data. The optical prediction closely matches data from destructive measurements. It is demonstrated that the redistribution of oxygen due to annealing can be monitored with this technique.

• 462). High Resolution Transmission Electron Microscopy of Silicon-on-Insulator Formed by High Dose Oxygen Implantation.
Chang, P.H.; Mao, B.Y.
Mater. Sci. Lab., Texas Instrum., Dallas, TX
Appl. Phys. Lett., Vol. 50, No. 3, 152-4, 1987

The structure of Si-on-insulator formed by O implantation at 150 keV with a dose of $1.6 \times 10^{18} cm^{-2}$ was studied by high-resolution TEM. Polyhedral O precipitates were observed both in the top Si layer and in the substrate after 1150°C annealing. The O precipitates in the top Si layer coarsen at 1250°C, but no precipitate can be found in the substrate at this temperature. A layer of polycrystalline Si (polysilicon) exists near the top Si/buried oxide interface. Si crystals in the polysilicon layer also coarsen when the annealing temperature is changed from 1150 to 1250°C. At 1150°C, the buried oxide/substrate interface has many Si lamellas roughly parallel to the {100} wafer surface. The lamellar structure is broken up after 1250°C annealing and is replaced by island-like crystals which are strongly faceted on {100} planes. Defects are present in Si microcrystallites in both the polysilicon layer and the island-like particles. *CA*

463). Profiling of Inhomogeneous Carrier Transport Properties with the Influence of Temperature in Silicon-on-Insulator Films Formed by Oxygen Implantation.
Cristoloveanu, S.; Lee, J.H.; Pumfrey, J.; Davis, J.R.; Arrowsmith, R.P.; Hemment, P.L.F.
Lab. Phys. Composants Semicond., Inst. Natl. Polytech., Grenoble, France
J. Appl. Phys., Vol. 60, No. 9, 3199-203, 1986

The nonhomogeneous distribution of the carrier transport properties in Si-on-insulator thin films synthesized by O implantation is determined using gate-controlled p-type Hall devices. The conductivity, Hall effect, and capacitance were measured between 77 and 300 K as a function of the gate voltage and then differentiated to obtain depth profiles. The hole mobility is high and nearly constant in the top 100 nm of the film but drops rapidly in the region containing implantation-induced defects. The very good quality of the top layer, similar to that of bulk Si, is confirmed by the temperature behavior of both the mobility and the ionized impurity concentration at various depths in the film. Acoustic phonon scattering prevails above 120 K and Coulombian scattering below. A difference between the profile of the total number of holes and that of the mobile holes was observed at low temperatures and is explained in terms of long-range potential fluctuations. *CA*

464). Temperature Dependence and Non-Uniformity of Electrical Properties of SOI Films Obtained by Oxygen Implantation.
Cristoloveanu, S.; Wyncoll, J.; Spinelli,P.; Hemment, P.L.F.; Arrowsmith, R.P.
Lab. PCS, ENSERG, Grenoble, France
Physica B & C (Netherlands), Vol.129B+C, No.1-3, 249-54, March 1985
Proceedings of the 14th European Solid State Device Research Conference, Including Solid State Device Technology, 10-13 Sept. 1984, Lille, France

Spreading resistance and temperature-dependent van der Pauw measurements provide evidence of the non-homogeneity of resistivity, electron mobility, and scattering mechanism in silicon-on-insulator films obtained by oxygen implantation. The oxygen content of this material is also responsible for substantial thermal donor activity. Original results on MOS transistors, the channels of which are situated either at the front interface or near the buried oxide, illustrate the dissymmetry between these interfaces. *IN*

• 465). Thermal Donor and New Donor Generation in SOI Material Formed by Oxygen Implantation.
Cristoloveanu, S.; Pumfrey, J.; Scheid, E.; Hemment, P.L.F.; Arrowsmith, R.P.
LPCS, ENSERG, Grenoble, France
Electron. Lett. (GB), Vol.21, No.18, 802-4, 29 Aug. 1985

The oxygen content of silicon-on-insulator films, formed by oxygen implantation, is shown to be responsible for the generation of high-density free carriers: thermal donors at 450°C and new donors at 750°C. The variation of sheet resistance and spreading resistance profiles is measured after successive isochronal and isothermal anneals. The initial generation rate of new donors greatly exceeds that of thermal donors, suggesting a surface-states-related mechanism. *IN*

466). Application of the $^{16}O(d,\alpha)^{14}N$ Nuclear Reaction to Oxygen Depth Profiling in SIMOX Structures.
Dubus, M.; Margail, J.; Martin, P.
Lab. des Accelerateurs, CENG, Grenoble, France
Nucl. Instrum. & Methods Phys. Res. Sect. B (Netherlands) Vol. B15, No.1-6, 559-62, April 1986
Ion Beam Analysis. Proceedings of the Seventh International Conference 7-12 July 1985, Berlin, Germany

The high depth resolution $^{16}O(d,\alpha)^{14}N$ nuclear reaction is used to profile oxygen in SIMOX structures formed after high-dose (from $1\times10^{18}cm^{-2}$) implementation of oxygen into silicon at an energy of 20 keV. As the thickness of the buried silicon dioxide layers is large, the $^{16}O(d,p_0)$ peak interferes with the $^{16}O(d,\alpha)$ energy spectrum. The observation of the $^{16}O(d,p_1)$ peak allows one to deduce the expected p_0 peak which is then deducted from the energy spectrum. This numerical method has been successfully validated on thermal grown SiO_2 layers on Si and applied to SIMOX structures. *IN*

467). Behavior of Dopant Diffusion in a Silicon-on-Insulator Structure Formed by

High-Dose Oxygen Implantation.
Fahey, P.; Solmi, S.
Inst. LAMEL, Bologna, Italy
J. Appl. Phys., Vol. 60, No. 12, 4329-33, 1986

Diffusion of Sb and P in a Si-on-insulator (SOI) structure formed by heavy-dose O implantation was studied and compared to diffusion in normal bulk wafers. The nonequilibrium effects on diffusion during direct nitridation or nitridation of an SiO_2 layer are mitigated on the SOI structures, while under oxidizing conditions there are no large differences in diffusion behavior between bulk and SOI samples. Also, spatial extent of the low-concentration tail region of a P diffusion from $POCl_3$ is reduced in the SOI structure. *CA*

• 468). TEM, Microdiffraction and Electrical Studies of Buried SiO_2 Layers Formed by High Dose Oxygen Implantation.
Fathy, D.; Krivanek, O.L.; Carpenter, R.W.
Center for Solid State Sci., Arizona State Univ., Tempe, AZ.
Cullis, A.G.; Davidson, S.M.; Booker, G.R. (Editors)
Microscopy of Semiconducting Materials 1983. 3rd Oxford Conference, 479-84, 1983
21-23 March 1983, Oxford, England

A study has been made of the SiO_2 insulating layer in SOI (silicon-on-insulator) structures produced by high-energy oxygen implantation into Si. The SiO_2 layer and especially its two bounding Si-SiO_2 interfaces have been examined by high-resolution transmission electron microscopy (HREM) before and after annealing for two different implantation dose rates. The results indicate that the interface structure and oxide layer quality are 'dose-rate' dependent. For higher dose rates, less Si-SiO_2 intermixing is observed, the Si-SiO_2 interfaces are sharper, and there is less residual damage in the top Si overlayer. *IN*

• 469). Electrical Characterisation of Oxygen Implanted Silicon Substrates.
Foster, D.J.
Plessey Res. (Caswell) Ltd., Caswell, Towcester, England
Physica B & C (Netherlands), Vol.129 B&C, No.1-3, 171-5, March 1985
Proceedings of the 14th European Solid State Device Research Conference, Including Solid State Device Technology, 10-13 Sept. 1984, Lille, France

Results of an electrical assessment of CMOS SOI devices made in oxygen-implanted silicon substrates are presented. Devices were fabricated directly into the implanted silicon with electrical characteristics dependent on the material properties. Electrically active oxygen gave rise to unintentional island doping. Silicon crystallinity as assessed by mobility measurements was related to oxygen implant temperature. By restricting the oxygen implant temperature to the range of 460 to 510°C, excellent CMOS device performance was obtained. *IN*

470). Optimization of Oxygen-Implanted Silicon Substrates for CMOS Devices by Electrical Characterization.
Foster, D.J.; Butler, A.L.; Bolbot, P.H.; Alderman, J.C.
Plessey Res. Ltd., Caswell, Towcester, England
IEEE Trans. Electron Devices (USA), Vol.ED-33, No.3, 354-60, March 1986

The use of oxygen-implanted silicon substrates for CMOS SOI device technology has great potential for use in VLSI and radiation-hardened circuits. The electrical characterization of such substrates is described by reference to CMOS devices fabricated directly into them; no epitaxial silicon was grown. Electrical parameters were related to the oxygen-implantation conditions of dose and temperature. Thermally generated oxygen donors in the top silicon layer were identified as being responsible for threshold voltage shifts and resistivity changes that altered transistor characteristics. Suitable boron implants enabled electrical parameter control to be maintained. Full island-to-substrate electrical isolation was only achieved for oxygen doses greater than $1.6 \times 10^{18} B\ cm^{-2}$, a

larger dose from that required to create stoichiometric SiO_2. Channel mobilities and NMOS back-channel leakage currents were found to be dependent on oxygen implant temperature; as a result, a favorable implant window of 460 to 510°C was established to fabricate ring oscillators twice as fast as bulk silicon counterparts for the same power dissipation. *IN*

471). Influence of Oxygen Implantation Conditions on the Properties of a High-Temperature-Annealed Silicon-on-Insulator Material.
Golanski, A.; Perio, A.; Grob, J. J.; Stuck, R.; Maillet, S.; Clavelier, E.
Cent. Natl. Etud. Telecommun., Meylan, France
Appl. Phys. Lett., Vol. 49, No. 21, 1423-5, 1986

A Si-on-insulator (SOI) structure was formed by implanting 150-keV O^+ ions into a single-crystal, n-type Si. The substrate temperature during implantation, T_i, was regulated within the range 450 to 750°C. Implanted samples were subsequently annealed at 1300°C for 2 to 5 h and analyzed using TEM, RBS, the spreading resistance probe, and SIMS. The T_i during O implantation strongly influences the properties of the SOI structure after the high-temperature annealing; the residual O concentration within the Si surface layer depends on T_i and correlates with the carrier density, indicating the presence of O-related thermal donors. *CA*

472). Characterization of Device Grade SOI Structures Formed By Implantation of High Doses of Oxygen.
Hemment, P.L.F.; Maydell-Ondrusz, E.A.; Stephens, K.G.; Arrowsmith, R.P.; Glaccum, A.C.; Kilner, J.A.; Butcher, J.B.
Dept. of Electron. and Electr. Eng., Surrey Univ., Guildford, England;
Hubler, G.K.; Holland, O.W.; Clayton, C.R.; White, C.W. (Editors)
Ion Implantation and Ion Beam Processing of Materials. Proceedings of the Symposium, 281-6, 1984, 14-17 Nov. 1983, Boston, MA.
North-Holland, New York.

SOI structures have been formed in (100) silicon by implanting 400-keV molecular oxygen to a dose of 1.8×10^{18} O atoms cm^{-2}. These samples were annealed at 1150°C for 2 h with a SILOX cap. Oxygen depth profiles have been determined by SIMS, and wafers implanted at about 500°C have been characterized by studying the regrowth kinetics as drive-in and oxidation rate in the top silicon overlay. *IN*

473). Formation of Silicon on Insulator Structures by Ion Implantation.
Hemment, P.L.F.
Dept. of Electron. & Electr. Eng., Surrey Univ., Guildford, England
Proc. SPIE Int. Soc. Opt. Eng. (USA), Vol.530, 230-9, 1985
Advanced Applications of Ion Implantation, 23-25 Jan. 1985, Los Angeles, CA.

The synthesis of buried dielectric layers by the implantation of reactive ions (O^+, N^+) to form silicon-on-insulator substrates suitable for very-large-scale integration (VLSI) circuits is described. Silicon (100) wafers have been implanted with ions of energy 100 to 300 keV and doses in the range 0.25×10^{18} to $2.6 \times 10^{18} cm^{-2}$. These structures have been annealed at temperatures of up to 1200°C. The composition, microstructure, and electrical properties are reported and a comparison is made between substrates formed by O^+ and N^+ implantations. *IN*

474). Oxygen and Defect Distributions in Silicon on Insulator Structures Formed by High Dose O^+ Implantation Into Silicon.
Hemment, P.L.F.; Maydell-Ondrusz, E.; Stephens, K.G.; Arrowsmith, R.P.; Glaccum, A.E.; Kilner, J.A.; Wilson, M.C.; Booker, G.R.
Dept. of Electron. and Electr. Eng., Surrey Univ., Guildford, England;
Takagi, T. (Editor)
Proceedings of the International Ion Engineering Congress. The 7th

Symposium (1983 International) on Ion Sources and Ion Assisted Technology (ISIAT '83) and the 4th International Conference on Ion and Plasma Assisted Techniques (IPAT '83), 1855-60, Vol.3, 1983, 12-16 Sept. 1983, Kyoto, Japan
Int. Ion Eng. Congress, Kyoto, Japan

Synthesis of SiO_2 by ion implantation may become an important technology for the production of silicon-on-insulator (SOI) substrates which are suitable for VLSI circuit applications. Such structures may be fabricated by implantation of high doses ($> 10^{18}$ O cm^{-2}) of high-energy (>100-keV) oxygen ions into heated single-crystal silicon wafers. The authors report new results from experiments carried out as part of an 'on-going' collaborative project to characterise the implanted structures. Analysis was by Rutherford backscattering (RBS) and channelling of 1.5-meV He^+ ions together with SIMS using an Atomika Dida-II Spectrometer, Auger electron spectroscopy (AES), x-ray photospectroscopy, and sectional TEM. *IN*

475). Oxygen Distributions in Synthesized SiO_2 Layers Formed by High Dose O^+ Implantation Into Silicon.
Hemment, P.L.F.; Maydell-Ondrusz, E.; Stevens, K.G.; Kilner, J.A.; Butcher, J.
Dept. of Electronic and Electrical Engng., Univ. of Surrey, Guildford, England
Vacuum (GB), Vol.34, No.1-2, 203-8, Jan.-Feb. 1984
Proceedings of the 3rd International Conference on Low Energy Ion Beams
28-31 March 1983, Loughborough, England

Oxygen depth distributions have been determined in silicon-on-insulator (SOI) structures formed by implantation of 200-keV oxygen ions into (100) silicon wafers. The implanted layers have been studied by RBS, SIMS, and cross-sectional TEM, and a computer model has been developed which enables the evolution of the oxygen distribution to be followed. Processing conditions, to form SOI substrates for fabrication of VLSI devices in the top silicon layer, are implantation energy of 200 keV, dose $1.8 \times 10^{18} O\ cm^{-2}$ and implantation temperature 500°C. An anneal at 1150°C for 2 h is required to form a thin single-crystal layer, which is depleted of oxygen. The dielectric properties of the stoichiometric SiO_2 are improved by this thermal processing. *IN*

476). Precipitation of Oxygen in Single-Crystal Silicon Implanted with High Doses of Oxygen.
Hemment, P.L.F.; Maydell-Ondrusz, E.A.; Castle, J.E.; Paynter, R.;
Wilson, M.C.; Booker, R.G.; Kilner, J.A.; Arrowsmith, R.P.
Univ. of Surrey, Dept. of Electronic & Electrical Engineering, Guildford, United Kingdom
Thin Solid Films, Vol. 128, No. 1-2, June 14, 1985, 125-131

Oxygen and defect distributions in Si(100), implanted at 500°C with 400-keV molecular oxygen ions to achieve a maximum volume concentration of about 10^{22} O cm^{-3}, have been studied by transmission electron microscopy, secondary ion mass spectroscopy, and Auger and x-ray photoelectron spectroscopy. On annealing at 1150°C for 2 h, redistribution of the oxygen is observed with SiO_2 precipitates (platelets) nucleating on residual damage to form a simple two-phase (silicon and SiO_2) system. *EI*

477). The Microstructure of High Dose Oxygen Implanted Si and Its Dependence on Implantation Conditions.
Holland, O.W.; Fathy, D.; Sjoreen, T.P.; Narayan, J.; More, K.
Solid State Div., Oak Ridge Nat. Lab., TN.
Proc. SPIE Int. Soc. Opt. Eng. (USA), Vol.530, 255-61, 1985
Advanced Applications of Ion Implantation, 23-25 Jan. 1985, Los Angeles, CA.

The formation of a buried dielectric in single crystals of silicon by high-dose implantation of oxygen ions is investigated. The dependence of the microstructure on implantation conditions is determined. It is shown that the microstructure can be tailored by changing the implant conditions

to optimize its suitability for the silicon-on-insulator technology. Mechanisms responsible for the formation of the microstructure and the influence of implantation conditions are discussed. *IN*

• 478). Formation of Buried Oxide in Silicon by High-Dose Oxygen Implantation, and Application of This Technology to CMOS Devices.
Izumi, K.; Omura, Y.; Nakashima, S.
Atsugi Electr. Commun. Lab., NTT Public Corp., Kanagawa, Japan
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing Symposium
443-52, 14-17 Nov. 1983, Boston, MA
North-Holland, New York

SIMOX (Separation by Implanted Oxygen) technology has been developed for realization of oxygen-ion implanted SOI. The distribution of implanted oxygen was analyzed by Auger electron spectroscopy and Rutherford backscattering spectroscopy. The properties of the silicon oxide formed by oxygen-ion implantation were investigated by infrared spectra, capacitance-voltage characteristics, dielectric strength, and dielectric constants. The crystallinity of the top layer silicon and of the epitaxially grown silicon layer was determined by electron-beam diffraction. An electric-field-shielding effect was observed in the polycrystalline silicon region which was formed between the top layer silicon and the buried oxide. High-speed digital and high-voltage analogue CMOS LSIS, a 1-KB CMOS RAM, and a BSH LSI, were successfully fabricated using SIMOX technology. *IN*

479). SIMOX Technology and Its Application to CMOS LSIs.
Izumi, K.; Omura, Y.; Sakai, T.
Atsugi Electrical Communication Lab., NTT Public Corp., Kanagawa, Japan
J. Electron. Mater. (USA), Vol.12, No.5, 845-61, Sept. 1983

SIMOX technology has been developed for fabricating SOI-type devices. In this technology, buried silicon oxide is used for the vertical isolation of semiconductor devices. The buried oxide is formed by oxygen-ion implantation into silicon, followed by epitaxial growth of silicon onto the surface of the residual silicon above the buried oxide. The crystallinity of the residual silicon was investigated by electron-beam diffraction, while the implanted oxygen depth profile was analyzed by Rutherford backscattering spectroscopy. A 1-KB CMOS static RAM has been fabricated using polysilicon gate SIMOX technology with a 1.5-μm effective channel length. The chip-select access time of the RAM was 12 ns at 45-mW dissipation power. *IN*

480). Microstructure of Silicon Implanted With High Dose Oxygen Ions.
Jaussaud, C.; Stoemenos, J.; Margail, J.; Dupuy, M.; Blanchard, B.; Bruel, M.
Lab. d'Etudes et de Technol. de l'Inf., CEN, Grenoble, France;
Appl. Phys. Lett. (USA), Vol.46, No.11, 1064-6, 1 June 1985

Buried implanted oxide layers have been formed by high-dose implantation of oxygen ions ($3 \times 10^{18} ions\ cm^{-2}$) into (100) silicon wafers, at a constant temperature of 500°C. The implanted layers were studied by cross-sectional transmission electron microscopy and secondary ion mass spectroscopy. The defects at both the top Si/SiO_2 and the SiO_2/bulk Si interfaces are shown to be SiO_2 precipitates. The precipitates are unstable and can be eliminated by heat treatment, and a homogeneous top silicon layer with a low density of dislocations can be obtained. *IN*

481). Heavy Metal Gettering in Implanted Buried-Oxide Structures.
Kamins, T.I.; Chiang, S.Y.
Hewlett-Packard Lab., Palo Alto, CA
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 239-44, 1986

To investigate gettering of heavy metal impurities to the damaged regions surrounding an implanted buried oxide, the behavior of Cr and Cu on annealing was investigated. Cr tends to segregate to

the surface Si-SiO_2 interface, although a small fraction moves to the damaged regions surrounding the buried oxide. Cu segregates to the damaged regions more readily; in addition, a large fraction of the implanted Cu moves to a location several micrometers beneath the buried oxide layer. The buried oxide does not appear to stop the movement of the Cu. *CA*

482). Heavy Metal Gettering in Silicon-on-Insulator Structures Formed by Oxygen Implantation Into Silicon.
Kamins, T.I.; Chiang, S.Y.
Hewlett-Packard Labs., Palo Alto, CA.
J. Appl. Phys. (USA), Vol.58, No.7, 2559-63, 1 Oct. 1985

Gettering of chromium and copper metal impurities to the damaged regions surrounding an implanted buried oxide has been investigated. Cr tends to segregate to the surface Si-SiO_2 interface; only a small fraction moves to the damaged regions surrounding the buried oxide. Cu segregates to the damaged regions more readily; in addition, a large fraction of the implanted Cu moves to a location several micrometers beneath the buried oxide layer. The buried oxide does not appear to stop the movement of the Cu. *IN*

483). SIMS Analysis of Silicon on Insulator Structures Formed by High-Dose O^+ Implantation Into Silicon.
Kilner, J.A.; Littlewood, S.D.; Hemment, P.L.F.; Maydell-Ondrusz, E.; Stephens, K.G.
Dept. of Metall. and Materials SCI., Imperial Coll., London, England;
Nucl. Instrum. and Methods Phys. Res. (Netherlands), Vol.218, No.1-3, 573-8, 15 Dec. 1983, Proceedings of the Sixth International Conference on Ion Beam Analysis, 23-27 May 1983, Tempe, AZ.

Silicon-on-insulator (SOI) structures are promising candidates for the fabrication of VLSI circuits with very high packing densities. The preparation of such structures can now be achieved by high-dose implantation of reactive ion species such as oxygen to produce buried layers of SiO_2 in silicon. The authors report experiments to depth profile these layered structures by SIMS. SOI samples have been prepared by implanting (100) silicon wafers with 400-keV molecular oxygen ions at a dose of $1.8 \times 10^{18} O^+ cm^{-2}$. During the implantation, the wafers were maintained at temperatures between 325 and 600°C, using beam heating, which achieved in-situ annealing and ensured that the top silicon layer remained single crystal. Analysis was carried out on an Atomika Dida-II spectrometer using 10-keV Ar^+ ions with a low current density of less than 1 mA cm^{-2}. During analysis, negative secondary ions were monitored which provided a high-detection sensitivity for oxygen and revealed fine detail in the measured yields which reflected both the composition and structure of the samples. Depth distributions of the oxygen compare well with results obtained by other techniques, including Rutherford backscattering and sectional TEM. It has been shown that prolonged high-temperature annealing leads to diffusion of oxygen with the formation of a denuded layer of thickness of 1000 to 1500 Å which is of a suitable quality for successful fabrication of high-performance MOS devices. *IN*

484). SIMS and ^{18}O Tracer Studies of the Redistribution of Oxygen in Buried SiO_2 Layers Formed by High Dose Implantation.
Kilner, J.A.; Chater, R.J.; Hemment, P.L.F.; Peart, R.F.; Maydell-Ondrusz, E.A.; Taylor, M.R.; Arrowsmith, R.P.
Imperial Coll. of Science & Technology, Dept. of Metallurgy & Materials Science, London, United Kingdom
Nuclear Instruments & Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms, Vol. B7-8, Pt. 1, 293-298, Mar. 1985

The formation of buried SiO_2 layers by high-dose oxygen implantation has been monitored by the implantation of ^{18}O tracer atoms and subsequent analysis by negative ion SIMS. Exchange of ^{18}O

with matrix oxygen in the buried layer occurred for all experiments. Rapid redistribution of the implanted tracer trace to the edges of the SiO_2 layer was observed. The lower Si/SiO_2 interface appears to be a barrier to further redistribution of the tracer oxygen. *EI*

485). Effect of Annealing on the Structure of Buried Silica Layers Formed by Elevated Temperature High Dose Oxygen Implantation.
Krause, S.J.; Jung, C.O.; Wilson, S.R.; Lorigan, R.P.; Burnham, M.E.
Dep. Mech. Aerosp. Eng., Arizona State Univ., Tempe, AZ
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 257-62, 1986

O was implanted into Si wafers at high doses and elevated temperatures to form a buried SiO_2 layer for use in Si-on-insulator (SOI) structures. Substrate heater temperatures were varied (300, 400, 450 and 500°C) to determine the effect on the structure of the superfacial Si layer through a processing cycle of implantation, annealing, and epitaxial growth. Transmission electron microscopy was used to characterize the structure of the superfacial layer. The structure of the samples was examined after implantation, after annealing at 1150°C for 3 h, and after growth of the epitaxial Si layer. There was a marked effect on the structure of the superficial Si layer due to varying substrate heater temperature during implantation. The single-crystal structure of the superficial Si layer was preserved at implantation temperatures of 300 to 500°C. At the highest heater temperature, the superficial Si layer contained larger precipitates and fewer defects than did wafers implanted at lower temperatures. Annealing of the as-implanted wafers significantly reduced structural differences. All wafers had a region of large, amorphous 10- to 50-nm precipitates in the lower two-thirds of the superficial Si layer, while in the upper third of the layer there were a few threading dislocations. In wafers implanted at lower temperatures, the buried oxide grew at the top surface only. During epitaxial Si growth, the buried oxide layer thinned and the precipitate region above and below the oxide layer thickened for all wafers. There were no significant structural differences of the epitaxial Si layer for wafers with different implantation temperatures. The epitaxial layer was high-quality single-crystal Si and contained a few threading dislocations. Overall, structural differences in the epitaxial Si layer due to differences in implantation temperature were minimal. *CA*

486). Characteristics of MOSFETs Fabricated in Silicon-on-Insulator Material Formed by High-Dose Oxygen Ion Implantation.
Lam, H.W.; Pinizzotto, R.F.; Yuan, H.T.; Bellavance, D.W.
Central Res. Lab., Texas Instruments Inc., Dallas, TX.
Electron. Lett. (GB), Vol.17, No.10, 356-8, 14 May 1981

By implanting a dose of $6 \times 10^{17} cm^{-2}$ of $^{32}O_2^+$ at 300 keV into a silicon wafer, a buried oxide layer is formed. Crystallinity of the silicon layer above the buried oxide layer is maintained by applying a high (> 200°C) substrate temperature during the ion-implantation processes. A two-step anneal cycle is found to be adequate to form the insulating buried oxide layer and to repair the implantation damage in the silicon layer on top of the buried oxide. A surface electron mobility as high as 710 $cm^2/V \cdot s$ has been measured in n-channel MOSFETs fabricated in a 0.5-μm thick epitaxial layer grown on the buried oxide wafer. A minimum subthreshold current of about 10 pA per micron of channel width at V_{DS}=2 V has been measured. *IN*

487). Accurate Technique for CV Measurements on SOI Structures Excluding Parasitic Capacitance Effects.
Lee, J.-H.; Cristoloveanu, S.
Nat. Polytech. Inst. of Grenoble, France
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.9, 537-9, Sept. 1986

A simple method is proposed based on capacitance measurements between the various terminals and their interpretation according to an appropriate equivalent circuit. Typical results obtained for a mesa-isolated SIMOX capacitor are given. *IN*

• 488). Electron Spin Resonance Studies on Buried Oxide Silicon-on-Insulator.
Makino, T.; Takahashi, J.
Electr. Commun. Lab., NTT Public Corp., Atsugi 243-01, Japan
Appl. Phys. Lett., Vol. 50, No. 5, 267-9, 1987

ESR was used to study defects in high-dose O-ion-implanted Si substrates. By this implantation, a crystalline Si/buried SiO_2/crystalline Si structure was created. Two kinds of defect centers are found: one is assigned to the amorphous center, and the other, the P_{b0} center, which is observed at thermally grown SiO_2/(111) Si interfaces. The observed P_{b0} center apparently exists near precipitated SiO_2/crystalline Si interfaces, rather than crystalline Si/buried SiO_2 interfaces. When annealed at 1150°C, the spin density decreases due to O out-diffusion from the crystalline Si. *CA*

489). The Effects of Annealing Temperature on the Characteristics of Buried Oxide Silicon-on-Insulator.
Mao, B.-Y.; Chang, P.H.; Lam, H.W.; Shen, B.W.; Keenan, J.A.
Semicond. Process Des. Cent., Texas Instrum., Dallas, TX
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 251-6, 1986

The effects of post-implantation annealing on the properties of buried oxide Si-on-insulator (SOI) substrates at 1150 to 1300°C were studied. The crystallinity of the top Si layer was improved at higher annealing temperature. Lower thermal donor generation at 450°C was observed in SOI annealed at higher temperature. The improvement in microstructure and lower thermal donor generation were correlated to the lower O concentration in the top Si film. *CA*

490). Microstructure of High-Temperature Annealed Buried Oxide Silicon-on-Insulator.
Mao, B.-Y.; Chang, P.-H.; Lam, H.W.; Shen, B.W.; Keenan, J.A.
Semicond. Process & Design Center, Texas Instrum., Dallas, TX.
Appl. Phys. Lett. (USA), Vol.48, No.12, 794-6, 24 March 1986

The microstructure of buried oxide silicon-on-insulator (SOI) annealed in the temperature range of 1150 to 1300°C was examined. The microstructure of the buried oxide SOI was improved by increasing the annealing temperature. The minimum channeling yield of the top silicon layer in 1250°C annealed SOI measured by Rutherford backscattering and channeling analysis is 5% which is comparable to unprocessed bulk single-crystal material. This is further verified by the cross-sectional transmission electron microscopy observation of the precipitate-free top silicon layer with low dislocation density. The improvement in the microstructure is attributed to the dissolution of oxygen precipitates and oxygen outdiffusion during high-temperature annealing. *IN*

• 491). Changes of Electrical Properties of Implanted Buried Oxide in Silicon by High-Temperature Annealing.
Mogro-Campero, A.
Gen. Electr. Res. and Dev. Cent., Schenectady, NY
J. Appl. Phys., Vol. 61, No. 2, 639-42, 1987

Implantation of 150-keV O into Si to a dose of $2 \times 10^{18} cm^{-2}$ at 600°C resulted in a Si-on-insulator structure. Annealing was carried out at 1150, 1200, and 1250°C. The top Si layer was removed, and metal contacts were evaporated to form capacitors for capacitance-voltage and capacitance-time measurements. The values of all the electrical parameters measured changed with annealing temperature. Oxide charge and doping density in the underlying Si decrease with increasing annealing temperature. The capacitance relaxation time after pulsing into deep depletion and the carrier generation lifetime increase with increasing annealing temperature. Low values of doping density and high values of capacitance relaxation time are desirable for supporting high voltages across such a structure. *CA*

• 492). Electrical Characteristics of an Upper Interface on a Buried SiO_2 Layer Formed by

Oxygen Implantation.
Nakashima, S.; Ohwada, K.
Musashino Electrical Communication Lab., NTT Public Corp., Tokyo, Japan
Jpn. J. Appl. Phys. part 1 (Japan), Vol.22, No.7, 1119-24, July 1983

The electrical characteristics of an upper interface on a buried oxide layer formed by oxygen implantation in an Si wafer and subsequent thermal annealing were studied using an MOS diode and capacitance-voltage (C-V) measurements. The measured C-V curves strongly depended on the ion dose. The C-V curve was independent of the gate voltage for a dose of $1.2 \times 10^{18} cm^{-2}$, voltage-dependent for doses above $1.8 \times 10^{18} cm^{-2}$, and similar to those for thermal oxide for a dose of $2.4 \times 10^{18} cm^{-2}$. This strong dependence on the ion dose is considered to result from a change in the interface structure with increase in dose. In this change, the transition layer existing between the buried oxide and the upper Si layer at low doses, which shields the upper Si layer from external electric fields, disappears with increase in dose. *IN*

493). The Microstructure of Silicon-on-Insulator Structures Formed by High Dose Oxygen Ion Implantation.
Pinizzotto, R.F.; Vaandrager, B.L.; Lam, H.W.
Texas Instruments Inc., Dallas, TX.
Picraux, S.T.; Choyke, W.J. (Editors)
Metastable Materials Formation by Ion Implantation. Proceedings of the Materials Research Society Annual Meeting, 401-7, 1982, Nov. 1981, Boston, MA.
North-Holland, New York.

Cross-sectional and plane-view transmission electron microscopy and high-resolution scanning electron microscopy have been used to characterize the microstructure of silicon-on-insulator formed by high-dose oxygen ion implantation. The complete microstructure was observed to be composed of a series of distinct zones. The top silicon layer was (100) single crystal with a very low dislocation density. The second layer was a mixture of fine grained polysilicon and amorphous SiO_2. The third layer was pure SiO_2, followed by a second mixed layer. Finally, there was a layer of (100) silicon with an extremely high dislocation density. Some of the dislocations extended as far as 1 μm into the Si substrate. The relative widths of the layers were found to depend on the total ion fluence. The oxide layer did not occur for low doses and the two mixed layers merged into one zone. At high doses, the silicon-silicon dioxide interfaces are abrupt due to internal oxidation. *IN*

494). Influence of Substrate Heating and Thermal Annealing on the Surface Crystallinity in Single Si Crystals Implanted with High Doses of ^{16}O.
Sjoreen, T.P.; Holland, O.W.; Fathy, D.; More, K.; Davis, R.F.
Oak Ridge Natl. Lab., Solid State Div., Oak Ridge, TN
Nuclear Instruments & Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms, Vol. 10-11, Pt 1, May 15, 1985, Appl. of Accel. in Res. and Ind. '84, Proc. of the 8th Int. Conf., Denton, TX, Nov. 12-14, 1984, 574-579

The dependence of near-surface crystallinity on substrate heating during high-dose O^+ implantation into Si and post-implantation annealing was studied. It is shown that the damage morphology in the crystalline region above the SiO_2 layer is very sensitive to substrate temperature and that, under optimum implant conditions which minimize damage conditions in the near surface, annealing does not improve the near surface crystallinity. Rutherford backscattering/channeling spectroscopy and cross-sectional transmission electron microscopy were used to analyze the microstructure of the samples. *EI*

495). New Conditions for Synthesizing SOI Structures by High Dose Oxygen Implantation.
Stoemenos, J.; Jaussaud, C.; Brue, M.; Margail, J.
Lab. d'Electron. et de Technol. de l'Inf., CENG, Grenoble, France

J. Cryst. Growth (Netherlands), Vol. 73, No. 3, 456-50, Dec. 1985

J. Cryst. High doses ($1.5 \times 10^{18} ions\ cm^{-2}$) of oxygen ions were implanted at 200 keV into a silicon wafer kept at 700°C throughout the implantation. After annealing at 1150°C for 2 h, the top silicon layer contains dislocations with a density of about $5 \times 10^{8} cm^{-2}$ and a large density of SiO_2 precipitates. Annealing at 1300°C for 6 h dissolves all the precipitates and leads to a 310-nm thick silicon layer free of precipitates and with a dislocation density of about $10^{7} cm^{-2}$. The SiO_2 layer is 320 nm thick and the Si/SiO_2 interfaces are very sharp. *IN*

496). Nucleation and Growth of Oxide Precipitates in Silicon Implanted with Oxygen.
Stoemenos, J.; Margail, J.
Dept. of Phys., Aristotle Univ., Thessaloniki, Greece
Thin Solid Films (Switzerland), Vol.135, No.1, 115-27, 2 Jan. 1986
Sixth International Conference on 'Thin Films', 13-17 Aug. 1984, Stockholm, Sweden

Oxygen precipitates with polyhedral or tetragonal rod-like shapes have been observed in implanted silicon which has been exposed to a high-dose oxygen flux. The evolution and dissolution of these precipitates with annealing is discussed and a mechanism is proposed for their growth or shrinkage. A critical annealing temperature above which the individual precipitates become unstable is defined; in this process the role of the buried SiO_2 layer is enhanced and hence the process is irreversible. *IN*

497). The Effects of Different Implantation and Annealing Temperatures on the Structural and Chemical Properties of High Dose Oxygen-Ion-Implanted Silicon.
Tuppen, C.G.; Taylor, M.R.; Hemment, P.L.F.; Arrowsmith, R.P.
Br. Telecom Res. Lab., Ipswich/Suffolk, United Kingdom
Thin Solid Films, Vol. 131, No. 3-4, 233-44, 1985

Substrates implanted with a high dose of O ions were prepared at high ($T_i = 500°C$) and low ($T_i = 400°C$) implantation temperatures. The implanted material was then subjected to high-temperature anneals in the range $1000 < T_a < 1200°C$. Physical and chemical characterization of the material was achieved using a unique combination of cross-sectional TEM and Auger depth profiling. The structure and composition of the top Si layer (electrically isolated by a buried oxide) control the eventual device performance and were highly dependent on the implantation temperature. At an implantation temperature of 400°C, a layer of amorphous Si of very high O content is formed at the top Si/buried oxide interface. During annealing, this layer became isolated from the top single crystal by a thin band of oxide and did not recrystallize epitaxially, but formed a region of polycrystalline Si. The effect of different annealing conditions on this structure is described, and a simple transport model is used to explain the observed O migration. *CA*

498). Amorphous and Crystalline Oxide Precipitates in Oxygen Implanted Silicon.
Van Ommen, A.H.; Koek, B.H.; Viegers, M.P.A.
Philips Res. Labs., Eindhoven, Netherlands
Appl. Phys. Lett. (USA), Vol.49, No.11, 628-30, 15 Sept. 1986

The authors studied precipitation of oxygen in the region below the buried oxide of a silicon-on-insulator structure formed by high-dose implantation of oxygen. Underneath the oxide layer there is first a region containing amorphous precipitates, spherical in shape. At greater depth, platelike precipitates of the monoclinic silica phase coesite are observed on (113) silicon planes. The lower interface of the buried oxide is very rough compared to the upper interface. The morphology of the implanted structure is attributed to intrinsic point defects. In particular, it is proposed that a high concentration of self-interstitials occurs below the oxide as soon as it becomes a continuous layer. This leads to a large reduction of the oxidation rate in this region. Oxidation then only occurs above the buried oxide, reducing the thickness of the superficial silicon film. *IN*

499). Characterization of Buried SiO_2 Layers Formed by Ion Implantation of Oxygen.

Wilson, S.R.; Fathy, D.
Semiconductor Res. and Dev. Labs., Motorola Inc., Phoenix, AZ.
J. Electron. Mater. (USA), Vol.13, No.1, 127-46, Jan. 1984

Oxygen has been ion implanted (200 keV) into silicon at doses ranging from $2\times10^{17}cm^2$ to $2\times10^{18}cm^2$. The peak oxygen concentration occurs at a depth of 0.5 μm. These doses produce peak oxygen concentrations which are below and above the concentrations necessary to form stoichiometric SiO_2. If the oxygen concentration exceeds stoichiometry, a buried SiO_2 layer is formed with a thin superficial silicon layer on the surface. This superficial silicon layer has been used as a seed for growing single-crystal silicon epi. The resulting silicon-on-insulator (SOI) structure has been characterized by Rutherford backscattering, cross-sectional TEM, AES, optical microscopy, spreading resistance probe, Hall effect, and infrared transmission measurements. The effects of dose, substrate temperature during the implant, and subsequent anneal conditions have been examined. *IN*

500). Temperature Dependence of Hall Mobility and Electrical Conductivity in SIMOX Films.
Wyncoll, J.; Kang, K.N.; Cristoloveanu, S.; Hemment, P.L.F.; Arrowsmith, R.P.
Inst. of Nat. Polytech. de Grenoble, Enserg, Grenoble, France
Electron. Lett. (GB) Vol.20, No.12, 845-6, 7 June 1984

Transport data obtained on SIMOX films between 77 and 300 K are qualitatively different from those derived for bulk silicon. Results suggest a strong nonuniformity of carrier mobility: the uppermost part of the SIMOX layer is of comparable quality to bulk Si, but near the buried oxide there is a degradation, confirmed by prevailing Coulombian scattering even at 300 K. *IN*

501). Compatible High And Low Voltage CMOS Devices Using SIMOX Technology.
Akiya, M.; Nakashima, S.; Kato, K.
Musashino Electrical Communication Lab., Tokyo, Japan.
Jpn. J. Appl. Phys. Suppl. (Japan), 85-8, 1982.

New types of high- and low-voltage CMOS buried channel devices are described, which are applied to a current mirror and an operational amplifier using SIMOX technology. In the MOS current mirrors, a 0.5% matching error rate was obtained in a 10-μA drain current without any compensation circuits. In the two-stage operational amplifier, an open loop voltage gain of 60 dB was obtained with a $\pm$5 V supply. *IN*

502). Substrate Bias Effect for C-MOS Operational Amplifier Using SIMOX Technology.
Akiya, M.; Kimura, T.
NTT Public Corp., Musashino, Tokyo, Japan
Electron. Lett. (GB), Vol.19, No.2, 36-7, 20 Jan. 1983

The substrate bias effect for SIMOX devices is described. By setting the substrate bias voltage to the accumulation mode in the bulk, the kink onset voltage for the n-channel MOSFET has been found to increase. Open-loop voltage gain for a C-MOS two-stage operational amplifier has been enhanced up to 65 dB. *IN*

503). A Wide Range Linear Variable Resistor By Buried Channel MOS/SIMOX.
Akiya, M.; Nakashima, S.; Kato, K.
Atsugi Electr. Commun. Lab., NTT Public Corp., Kanagawa, Japan.
IEEE J. Solid-State Circuits (USA) Vol. SC-19, No.4, 526-31, Aug. 1984

A low-distortion linear variable resistor using an offset gate buried-channel MOSFET fabricated by SIMOX technology is described. The offset gate structure on the insulating substrate provides 15 to 100 K-Ω drain-to-source resistance, and 2.5% total harmonic distortion at 100 K-Ω. *IN*

504). 1.25-μm Buried-Oxide SOI/CMOS Process for 16K/64K SRAMs.
Chen, C.-E.; Matloubian, M.; Mao, B.-Y.; Sundaresan, R.; Slawinski, C.; Lam, H. W.; Blake, T. G. W.; Hite, L. R.; Hester, R. K.
Texas Instruments Inc, Dallas, TX
IEEE Transactions on Electron Devices, Vol. ED-33, No. 11, 44th Annual Device Res. Conf., Amherst, MA, June 23-25, 1986, 1840-1841 *EI*

• 505). SOI-CMOS 4K SRAM Via Oxygen Implant.
Chen, C.-E.; Lam, H.W.; Malhi, S.D.S.; Mao, B.-Y.; Blake, T.G.W.; Hite, L.R.
Semiconductor Process & Design Center, Texas Instrum. Inc., Dallas, TX.
Semicond. Int. (USA), Vol. 8, No.7, 136-8, July 1985

This paper reports on the fabrication of SOI-CMOS 4K SRAM using the implanted buried oxide SOI technology with a minimum feature size of 2.5 μm. High-dose oxygen implantation is the leading SOI technology because it provides the best quality single-crystal silicon for device fabrication. But across-the-wafer uniformity of device parameters has not been addressed. The 4K SRAM has been fabricated using the high-dose oxygen implantation SOI technology with 2.5-μm design rules and a 500-Å thick gate oxide. The author discusses SOI device parameters with comparison to the bulk devices, ring oscillator data, and the SOI 4K SRAM circuit results. Buried oxide SOI device parameters, and their uniformities were found to be similar to those of their bulk counterparts. The 55 ns address access time of the SOI-CMOS 4K SRAM agreed well with the SPICE simulations. *IN*

506). SOI-CMOS 4K SRAM with High Dose Oxygen Implanted Substrate.

Chen, C.-E.; Blake, T.G.W.; Hite, L.R.; Malhi, S.D.S.; Mao, B.-Y.; Lam, H.W.
Texas Instrum. Inc., Dallas, TX.
International Electron Devices Meeting, Technical Digest, 702-5, 1984
9-12 Dec. 1984, San Francisco, CA, USA
IEEE, New York.

The fabrication of a SOI-CMOS 4K SRAM using the implanted buried oxide SOI technology with a minimum feature size of 2.5 μm is described. The 4K by 1 CMOS SRAM, using a 6-T cell which contained n-channel loads and p-channel driver and pass transistors, exhibited a power dissipation of 85 mW at a V_{dd} of 5 V and an address access time of 55 ns, which agreed with the SPICE simulations. Electrical parameters of the buried oxide SOI devices were compared to those of the bulk CMOS devices. Except for an approximately 10% degradation of the carrier mobility and the 'kink' effect due to the floating body node, the buried oxide SOI devices were indistinguishable from the bulk devices. The uniformity of the buried oxide SOI device parameters is emphasized. *IN*

507). High-Speed, Low-Power Buried-Oxide SOI CMOS Technology.
Colinge, J.-P.; Kamins, T.I.; Chiang, S.Y.; Liu, D.; Peng, S.;
Rissman, P.; Hashimoto, K.
Hewlett-Packard Lab, Palo Alto, CA
IEEE Transactions on Electron Devices, Vol.ED-33, No.11, Nov. 1986,
44th Annual Device Res. Conf., Amherst, MA, June 23-25, 1986, p. 1842 *EI*

508). High-Speed, Low-Power, Implanted-Buried-Oxide CMOS Circuits.
Colinge, J.-P.; Hashimoto, K.; Kamins, T.; Chiang, S.-Y.; Liu, E.-D.;
Peng, S.; Rissman, P.
Hewlett-Packard Labs., Palo Alto, CA.
IEEE Electron Device Lett. (USA), Vol.EDL-7, No.5, 279-81, May 1986

CMOS ring oscillators with channels less than 0.5 μm long were fabricated in implanted-buried-oxide silicon-on-insulator films using direct-write electron-beam lithography. Transistors with polysilicon gate lengths as short as 0.4 μm and effective channel lengths as short as 0.21 μm operate satisfactorily. Ring oscillators have delays per gate of 52 and 83 ps and power-delay products of 55 and 5 fJ for supply voltages of 5 and 3.3 V, respectively. *IN*

• 509). A Lateral COMFET Made in Thin Silicon-on-Insulator Film.
Colinge, J.-P.; Chiang, S.Y.
Hewlett-Packard Lab., Palo Alto, CA
IEEE Electron Device Lett., Vol. EDL-7(12), 697-9, 1986

Lateral conductivity-modulated FETs (COMFETs) were fabricated by using a Si-on-insulator CMOS (complementary MOS) process. High-speed low-voltage CMOS and medium-voltage COMFETs were thus produced on the same chips. The COMFETs have an 80-V blocking capability in both the forward and reverse modes. Turn-off times of a few micrometers were obtained, which is comparable to values obtained in bulk COMFETs. Due to the thinness of the Si film in which the devices are made, the linear current density is limited to $\sim 10\mu A/\mu$m.

510). Properties of Front and Buried Interfaces of Oxygen Implanted SOI Films
Deduced from MOS Device Characteristics.
Cristoloveanu, S.; Pumfrey, J.; Arrowsmith, R. P.; Brini, J.; Hemment, P. L. F.
ENSERG, Grenoble, France
Simonne, J. J.; Buxo, J. (Editors)
Insul. Films Semicond., Proc. Int. Conf. INFOS 85, Meeting Date 1985,
49-52, North-Holland: Amsterdam, Neth., 1986

The interface characteristics were studied of O ion-implanted Si on SiO_2 film structures in MOSFETs, capacitors, and Hall devices. The interface state densities, threshold voltages, carrier mobilities, and leakage currents were determined. Defect effects are still present even after annealing at 1150°C for 2 h. Improvements are obtained by implanting at high temperatures. Implantation allows control of the leakage currents. *CA*

511). Improved Subthreshold Characteristics of n-Channel SOI Transistors.
David, J.R.; Glaccum, A.E.; Reeson, K.; Hemment, P.L.F.
British Telecom Research Lab, Ipswich, England
IEEE Electron Device Letters, Vol.EDL-7, No.10, 570-572, 10 Oct. 1986

It has been found that certain n-channel MOSFETs fabricated on silicon-on-insulator (SOI) substrates formed by oxygen implantation can have log (I_d):V_g, characteristics with very steep slopes in the subthreshold region. In contradiction to normal models for short-channel transistors on bulk silicon, the slope becomes steeper for shorter gate lengths or higher drain voltages. The effect is shown to be related to the kink in the output characteristics of transistors with floating islands. *EI*

• 512). Transient Radiation Effects in SOI Memories.
Davis, G.E.; Hite, L.R.; Blake, T.G.W.; Chen, C.-E.; Lam, H.W.; DeMoyer, R., Jr.
U.S. Naval Res. Lab., Washington, DC.
IEEE Trans. Nucl. Sci. (USA), Vol.NS-32, No.6, 4432-7, Dec. 1985
1985 Annual Conference on Nuclear and Space Radiation Effects, 21-24 July 1985, Monterey, CA.

Measurements of transient radiation effects on SOI discrete devices and an LSI memory are discussed. A commercially processed LSI SOI memory, a 4K×1 SRAM on SIMOX, was tested for single event upset (SEU) and transient ionizing radiation effects as a function of bias conditions and dose rate. The SEU error rate was between 1.5 and 2.5×10^{-8} errors/bit-day for the 10% worst-case orbit model. The output-voltage logic upset level was greater than 1.6×10^{10} rad(Si)/s for V_{cc} supply voltage variations of −10% and +20% with V_{sub} at −10 V. For the discrete devices and memory, the measured transient photocurrents were larger than the calculated volumetric photocurrent generated in the active device region. This increased transient response is postulated to be due to the gain of the parasitic phototransistor of the dielectrically isolated MOS device. *IN*

513). Electrical Characterisation of Oxygen Implanted Silicon Substrates (for CMOS SOI Devices).
Foster, D.J.; Butler, A.L.; Bolbot, P.H.
Plessey Res. Ltd., Caswell, Towcester, England
International Electron Devices Meeting, Technical Digest, 804-7, 1984
9-12 Dec. 1984, San Francisco, CA.
IEEE, New York.

Results of an electrical assessment of CMOS SOI devices employing oxygen-implanted silicon substrates are presented. Devices were fabricated directly into the implanted silicon with electrical characteristics dependent on the material properties. Electrically active oxygen gave rise to unintentional island doping. Silicon crystallinity as assessed by mobility measurements was related to oxygen implant temperature. By restricting the oxygen implant temperature to the range 460 to 510°C, excellent CMOS device performance was obtained. *IN*

514). Vertical N-P-N Bipolar Transistors Fabricated on Buried Oxide SOI.
Greeneich, E.W.; Reuss, R.H.
Dept. of Electrical and Computer Engng., Arizona State Univ., Tempe, AZ.
IEEE Electron Device Lett. (USA), Vol.EDL-5, No.3, 91-3, March 1984

Vertical n-p-n bipolar transistors have been fabricated in silicon-on-insulator (SOI) films prepared by buried oxide implantation. Electrical device characteristics are shown to be comparable to those

obtained on devices fabricated in bulk silicon, indicating no significant degradation owing to the buried layer. Dielectric isolation in excess of $10^{11}\Omega \cdot cm$ and $= 3 \times 10^{6} V/cm$ is measured. *IN*

515). Characteristics of Submicrometer CMOS Transistors in Implanted-Buried-Oxide SOI Films.
Hashimoto, K.; Kamins, T.I.; Cham, K.M.; Chiang, S.Y.
Hewlett Packard Labs., Palo Alto, CA.
International Electron Devices Meeting, Technical Digest, 672-5, 1985
1-4 Dec. 1985, Washington, DC.
IEEE, New York.

Characteristics of submicrometer MOS transistors on SOI films have been studied. The SOI films were formed by implantation of a buried oxide layer followed by epitaxial growth of additional silicon. MOS transistors were fabricated using a process compatible with a submicrometer bulk CMOS process. The final SOI thicknesses were designed to be 220 and 520 nm after device fabrication; the thickness of the implanted buried oxide was 400 nm. Satisfactory characteristics were obtained for CMOS transistors as short as 0.6 μm. Abnormal impurity diffusion did not occur in these implanted-buried-oxide SOI films. Small-geometry effects, such as threshold-voltage shift, were less severe in the thin SOI films than in bulk wafers. The authors show that this technology offers significant potential for submicrometer CMOS in addition to the other advantages of SOI technology. *IN*

516). A CMOS/SIMOX Frequency Synthesizer IC.
Ishikawa, M.; Sano, E.; Habuka, T.; Izumi, K.; Kimura, T.
Musashino Electrical Communication Lab., NTT Public Corp., Musashino, Japan.
Trans. Inst. Electron. and Commun. Eng. Jpn. Part C (Japan), Vol. J66c, No.7, 497-504, July 1983.

A high-speed CMOS/SIMOX PLL-IC with a built-in prescaler has been developed to obtain a low power and smaller size frequency synthesizer. The PLL-IC consists of a prescaler, a programmable counter, and a phase frequency comparator. The chip is fabricated with 2-μm-rule CMOS/SIMOX technology. In this technology, silicon islands are isolated by implanted silicon dioxide layers, which obtain high-performance MOS devices with reduction of parasitic capacitance. The die area with about 400 gates is 1.2 by 0.63 mm^2. The fabricated PLL-IC achieves a maximum operating frequency of 420 MHz at power dissipation of 65 mW. *IN*

517). Completely Isolated CMOS ICs Fabricated by Oxygen Ion Implantation Technique Called 'SIMOX'.
Izumi, K.; Doken, M.; Yamamoto, E.; Irita, Y.
Res. and Dev. Bureau, NTT Public Corp., Musashino, Japan
Trans. Inst. Electron. and Commun. Eng. Jpn. Sect. E (Japan), Vol. E62 No. 12, 921-2, Dec. 1979

CMOS ICs were fabricated utilizing buried SiO_2 layers formed by oxygen-ion ($^{16}O^{+}$) implantation into silicon for the purpose of device isolation (this technology is referred to as 'separation by implanted oxygen' (SIMOX)). Fabrication of devices having this structure requires formation of buried SiO_2 layers having good properties for application to device isolation and growth of epitaxial single-crystal silicon on the buried SiO_2 layers. A transition layer, which is the silicon region above the buried SiO_2 layer, is required to grow epitaxial silicon and oxygen ions were implanted into the silicon substrate with an implantation energy of 150 keV and a dose of $1.2 \times 10^{18} ions/cm^2$. *IN*

518). SIMOX Technology for CMOS LSIs.
Izumi, K.; Omura, Y.; Ishikawa, M.; Sano, E.
Musashino Electrical Communication Lab., NTT Public Corp., Tokyo, Japan
1982 Symposium on VLSI Technology, Digest of Papers, 10-11, 1982

1-3 Sept. 1982, Oiso, Japan
IEEE, New York.

SIMOX technology (separation by implanted oxygen) has been proposed to fabricate CMOS devices. In this technology silicon islands are completely surrounded by the buried and thermally-grown SiO_2 layers, which realize high-performance CMOS devices with a simple fabrication process due to the good mono-crystalline state of the active region, reduction of parasitic capacitance, and effective structure free from auto-doping and latch-up. In this work, the application of SIMOX to CMOS LSIs was successfully carried out using LOCOS, double metal layer, and polysilicon. *IN*

• 519). Device Application of SIMOX (Separation by IMplanted OXygen) Structure.
Kajiyama, K.; Izumi, K.; Nakashima, S.
Electr. Commun. Labs., NTT Public Corp., Kanagawa, Japan.
Furukawa, S. (Editor).
Silicon-on-Insulator: Its Technology and Applications.
US-Japan Seminar on 'Solid Phase Epitaxy and Interface Kinetics', 283-94
20-24 June 1983 Oiso, Japan.
Reidel, Dordrecht, Netherlands.

SIMOX/SOI is produced by high-dose (approximately $1 \times 10^{18}/cm^2$) and high-energy (approximately 100-keV) oxygen implantation, forming a buried oxide layer and reserving the surface single-crystalline Si layer. Annealing improves surface Si crystallinity and buried Si-O bonding. Epitaxial growth adds necessary Si thickness and improves crystallinity further. Using SIMOX, a 1 KB CMOS static RAM and a 400-gate PLL IC have been successfully fabricated. They proved to have good electrical characteristics and stable operation. SIMOX is good for VLSIs, because the fabrication process is reproducible and circuit design is flexible. A high-current implanter is desired. *IN*

520). The j-MOS Transistors Fabricated in Oxygen-Implanted Silicon-on-Insulator.
MacIver, B.; Jain, K.
Electron. Dep., Gen. Mot. Res. Lab., Warren, MI
IEEE Trans. Electron Devices, Vol. ED-33, No. 12, 1953-5, 1986

The j-MOS (junction MOS) transistor reported earlier was fabricated in a Si-on-insulator (SOI) structure prepared by O ion implantation. Significant improvements in the drain breakdown voltage and off-state leakage current are attributed to a contoured gate oxide and to the quality of the SOI structure, respectively. The electron mobility in the channel Si is 910 $cm^2/V\text{-}s$ and the minority-carrier lifetime is 3 μs. The j-MOS transistor in SOI shows promise for controlling moderate power loads, particularly in dielectrically isolated power integrated circuit applications. *CA*

521). Total Dose Characterizations of CMOS Devices in Oxygen Implanted Silicon-on-Insulator.
Mao, B.-Y.; Chen, C. E.; Matloubian, M.; Hite, L. R.; Pollack, G.;
Hughes, H. L.; Maley, K.
Semicond. Process and Design Cent., Texas Instrum., Dallas, TX
IEEE Trans. Nucl. Sci., Vol. NS-33, No. 6, Pt. 1, 1702-5, 1986

The total dose characteristics of CMOS devices fabricated in O-implanted buried oxide Si-on-insulator (SOI) substrates with different post-implant annealing processes were studied. The threshold voltage shift, subthreshold slope degradation, and mobility degradation of front channel SOI/CMOS devices are the same as those of bulk devices processed identically. Negative substrate bias lowers the threshold voltage shift of back channel SOI transistors, while not affecting the front channel characteristics. Under present processing conditions, the radiation characteristics of front channel devices are independent of the post-O-implant annealing temperature. O precipitates at the Si/buried oxide interface enhance interface state generation of the back channel devices during irradiation. *CA*

522). Electric-Field-Shielding Layers Formed by Oxygen Implantation into Silicon.
Nakashima, S.; Akiya, M.; Kato, K.
NTT Public Corp., Kanagawa, Japan
Electron. Lett. (GB), Vol.19, No.15, 568-10, 21 July 1983

The electric-field-shielding effect was found in a layer consisting of a mixture of polycrystalline silicon and silicon oxide formed by oxygen ion implantation. The layer was formed between the buried SiO_2 and the upper Si layer, which improved characteristics for MOSFETs fabricated using SIMOX (separation by implanted oxygen) technology. By forming this layer, the threshold voltages for the MOSFETs were almost independent of substrate bias. Drain-to-source breakdown voltages for the p-MOSFETs and n-MOSFETs were raised to 250 V and 180 V, respectively. *IN*

523). Subscriber Line Interface Circuit LSI Fabricated Using High-Voltage CMOS/SIMOX Technology.
Nakashima, S.; Maeda, Y.
NTT Public Corp., Kanagawa, Japan
Electron. Lett. (GB), Vol.19, No.25-26, 1095-7, 8 Dec. 1983

High-voltage buried-channel CMOS/SIMOX technology which is characterised with the existence of an electric-field-shielding layer formed by oxygen implantation was applied to fabricate a BSH-LSI for a subscriber line interface circuit providing three functions of battery feed, supervision and hybrid. In this CMOS BSH-LSI, a high-breakdown voltage of higher than 60 V and a low-breakdown voltage of 15 V were fabricated by the same process. This BSH/LSI showed a high level of performance during operation. The chip size and dissipation power of the BSH-LSI were reduced to approximately one-third and one-half, respectively, compared with a conventional BSH-LSI fabricated with bipolar technology. *IN*

524). Radiation-Hardened N-Channel MOSFET Achieved by a Combination of Polysilicon Sidewall and SIMOX Technology.
Ohno, T.; Izumi, K.; Shimaya, M.; Shiono, N.
NTT Electr. Commun. Labs., Kanagawa, Japan
Electron. Lett. (GB), Vol.22, No.10, 559-60, 8 May 1986

A radiation-hardened n-channel MOSFET has been developed by a combination of a polysilicon sidewall and SIMOX technology. The MOSFET is laterally isolated by multilayers of sidewall SiO_2, sidewall polysilicon and field SiO_2. It is vertically isolated by multilayers of highly oxygen-doped polysilicon and buried oxide. By using this isolation structure and a thin gate oxide, an increase in leakage currents and a threshold voltage shift were suppressed to less than 1.5 orders of magnitude and 0.08 V, respectively, after 10^6 rad(Si) irradiation. *IN*

525). A 4KB CMOS/SIMOX SRAM.
Omura, Y.; Nakashima, S.; Izumi, K.
Atsugi Electr. Commun. Lab., NTT Public Corp., Kanagawa, Japan
1985 Symposium on VLSI Technology, Digest of Technical Papers, 24-5, 1985
14-16 May 1985, Kobe, Japan
Bus. Center Acad. Soc. Japan, Tokyo, Japan

In recent years, many kinds of CMOS LSIs using the silicon-on-insulator (SOI) technology have been developed. Among them, SIMOX (Separation by IMplanted OXygen) technology has proved to be one of the technologies which lends itself to LSIs. In SIMOX technology, however, the implantation time was too long to be practical. To improve the situation, a modified oxygen implanter with a microwave ion source was used for the formation of SIMOX substrates. A 4-KB CMOS/SIMOX SRAM has been fabricated with high-level performance using these substrates. *IN*

526). Hydrogenation by Ion Implantation for Scaled SOI/PMOS Transistors.
Singh, H.J.; Saraswat, K.C.; Shott, J.D.; McVittie, J.P.; Meindl, J.D.

Integrated Circuits Lab., Stanford Univ., CA.
IEEE Electron Device Lett. (USA), Vol. EDL-6, No. 3, 139-41, March 1985

Hydrogenation by ion implantation has been investigated as a promising technique for VLSI/SOI and has been correlated with the resultant characteristics of silicon-on-insulator (SOI) PMOS transistors fabricated in polycrystalline silicon. It is found that SOI/PMOS on currents increase by one order of magnitude and off currents decrease by two orders of magnitude; that hydrogenation improves weak-inversion slopes by nearly an order of magnitude; and that channel-length scaling does not adversely affect leakage currents in SOI/PMOS devices in hydrogenated fine grain polysilicon down to a channel length of 2 μm on the mask, whereas devices in laser recrystallized polysilicon do show a degradation. *IN*

527). EPR of Defects in Silicon-on-Insulator Structures.
Barklie, R. C.; Hobbs, A.; Hemment, P. L. F.
Phys. Dep., Trinity Coll., Dublin, Ireland
Radiat. Eff., Vol. 99, No. 1-4, 83-7, 1986

EPR measurements were made on Si-on-SiO_2 and Si-on-Si_3N_4 structures produced by ion implantation. In the former type of structure, the EPR spectra are ascribed to the O vacancy center E1′ in the SiO_2, the defect P_{b0} at the Si/SiO_2 interface, and the amorphous Si center in the bulk Si. A single line of width $\Delta B_{pp} = 0.84(2)$ mT and an isotropic g = 2.0039(2) were found in the latter structure. The single line is attributed to Si dangling bonds in the Si_3N_4. The annealing behavior of these defects both in air and N was measured. *CA*

528). Nitrogen Implantation at High Doses in Monocrystalline Silicon: Doses and Annealing Conditions for Obtaining a Buried Homogeneous Insulating Layer.
Bourguet, P.; Dupart, J.M.
Lab. De Microelectronique, Ecole Superieure d'Electricite, Cesson, Sevigne, France
Rev. Phys. Appl. (France), Vol.15, No.3, 647-52, March 1980

Measurements show that to obtain an insulating layer, it is necessary to implant doses over a critical value according to the energy; it is also necessary to achieve minimal annealing conditions. IR spectroscopy confirms that the implanted layer evolves to a crystalline form of Si_3N_4. The crystallinity state of the superficial silicon layer over buried Si_3N_4 may give good epitaxy for silicon-on-insulator technology. *IN*

• 529). Microstructural Characterization of Nitrogen-Implanted Silicon-on-Insulator.
Chang, P. H.; Slawinski, C.; Mao, B. Y.; Lam, H. W.
Cent. Res. Lab., Texas Instrum., Inc., Dallas, TX
J. Appl. Phys., Vol. 61, No. 1, 166-74, 1987

The effects of implant dose and post-implant annealing treatment on the microstructure of N-implanted Si-on-insulator were studied by using cross-sectional transmission electron microscopy techniques. In the lower dose case ($0.75 \times 10^{18}/cm^2$), an amorphous Si layer forms after implantation. Annealing at 1200°C or higher results in a buried polycrystalline α-Si_3N_4 layer containing many randomly oriented Si particles. Higher dose implantation results in an amorphous Si-nitride layer. A porous layer also forms in the middle of the amorphous layer if the implant dose is $\geq 1.2 \times 10^{18}/cm^2$. The crystallization of the amorphous layer in the higher dose cases happens in two steps. In the first step, nucleation and growth of α-Si_3N_4 grains occur in the amorphous nitride region to form a spherulitic polycrystalline structure. The second step is the cellular growth of the spherulitic nitride grains into the crystalline Si regions. Si particles are trapped at the cell walls as the cellular reaction advances. These particles are conglomerated and spherodized but retain the same orientation as the substrate Si at higher temperatures. The quality of the top Si film is excellent after annealing at $\geq$1200°C, irrespective of the implant dose. *CA*

530). Microstructure and Electrical Properties of Buried Silicon Nitride Layers in Silicon Formed by Ion Implantation.
Fung, C.D.; Liao, J.L.; Elsayed, K.R.; and Kopanski, J.J.
Dept. of Electrical Engineering and Applied Physics, Case Western Reserve Univ., Cleveland, OH
Proceedings of the Symposium on Silicon Nitride Thin Insulating Films
p. 403, 1983

The formation of a buried insulating layer in silicon by ion implantation has a potential to achieve silicon-on-insulator structure. This can be used as an isolation method in very-large-scale integrations. The present paper reports implantation of N_2^+ and N^+ ions at 100 and 174 keV, respectively,

followed by thermal anneal to form buried silicon nitride in silicon. Studies include the nitrogen distribution, the microstructure, and the electrical properties pertaining to the silicon/silicon nitride/silicon structure. The results indicate that as the ion dose approaches the required value for obtaining stoichiometric silicon nitride (approximately 0.25 and $1 \times 10^{18}\text{cm}^{-2}$ for N_2^+ and N^+ ions, respectively, in this case), a continuous nitride film with good insulating property is formed. Measurements resulting from transmission electron spectroscopy and from depth profiles by Auger electron spectroscopy suggest, at higher doses, a possible nitrogen gas phase formation. *IN*

• 531). High Quality Silicon on Insulator Structures Formed by the Thermal Redistribution of Implanted Nitrogen.
Hemment, P.L.F.; Peart, R.F.; Yao, M.F.; Stephens, K.G.; Chater, R.J.; Kilner, J.A.; Meekison, D.; Booker, G.R.; Arrowsmith, R.P.
Dept. of Electron. & Electr. Eng., Surrey Univ., Guildford, England;
Appl. Phys. Lett. (USA), Vol.46, No.10, 952-4, 15 May 1985

Silicon wafers have been implanted with 200-keV $^{14}N^+$ ions to doses between 0.25 and $1.4 \times 10^{18} N^+ cm^{-2}$ at a temperature of 500°C and have been annealed at 1200°C for 2 and 8 h. Rapid redistribution of the implanted nitrogen occurs, against the macroscopic concentration gradient, in samples implanted with doses below that required to directly synthesize stoichiometric Si_3N_4. This leads to the formation of a continuous buried layer of either amorphous or polycrystalline Si_3N_4. The surface layer is high-quality single-crystal silicon (χ_{min}=0.043) containing no polycrystalline material nor precipitates. The Si-Si_3N_4 interfaces are extremely abrupt but with an irregularity of approximately 100 and approximately 50 Å at the upper and lower interfaces, respectively. *IN*

• 532). EPR of Defects in Silicon-on-Insulator Structures Formed by Ion Implantation. II. Nitrogen$^+$ Implantation.
Hobbs, A.; Barklie, R. C.; Hemment, P. L. F.; Reeson, K.
Dep. Phys., Trinity Coll., Dublin, Ireland
J. Phys. C: Solid State Phys., Vol. 19, No. 32, 6433-9, 1986

EPR spectra were measured for defects produced by implanting a (100) Si wafer with a dose of $0.75 \times 10^{18} cm^{-2}$ 200-keV N^- ions at ~520°C. A single nearly isotropic line with $g = 2.0039 \pm 0.0002$ and peak-to-peak linewidth 0.80 ± 0.04 mT is observed. It is attributed almost entirely to Si dangling bonds which lie mainly within a buried amorphous layer, 0.21 μm thick, which is rich in N. The defect concentration, initially $\sim 4.5 \times 10^{14} cm^{-2}$ was measured as a function of etching time and annealing temperature. *CA*

533). SIMS Analysis of Buried Silicon Nitride Layers Formed by High Dose Implantation of ^{14}N and ^{15}N.
Kilner, J.A.; Chater, R.J.; Hemment, P.L.F.; Peart, R.F.; Reeson, K.J.; Arrowsmith, R.P.; Davis, J.R.
Dept. of Metall. & Mater. Sci., Imperial Coll., London, England;
Nucl. Instrum. & Methods Phys. Res. Sect. B (Netherlands) Vol.B15, No.1-6 214-17, April 1986
Ion Beam Analysis. Proceedings of the Seventh International Conference 7-12 July 1985, Berlin, Germany

In order to obtain more information about the formation of buried layers of insulating material, the authors have undertaken a series of experiments in which they added incremental doses of the stable isotope, ^{15}N, as a tracer, during the ion-beam synthesis of the buried Si_3N_4 layers. The atomic processes causing tracer redistribution are discussed with particular reference to those occurring during post implant annealing. *IN*

534). Nitrogen Ion Implantation in Silicon: Structure of the Subsurface Region.
Liliental, Z.; Carpenter, R.W.; Fathy, D.; Kelly, J.C.

Arizona State University, Tempe, AZ.
Baglin, J.E.E.; Campbell, D.R.; Chu, W.K. (Editors)
Thin Films and Interfaces II. Proceedings of the Symposium, 525-530, 1984.
14-18 Nov. 1983, Boston, MA.
North-Holland, NY.

Subsurface dielectric layers in silicon formed by oxygen ion implantation have been the subject of various investigations as an attractive alternative to building devices and integrated circuits on insulating substrates. More recently, the methods of high-resolution analytical electron microscopy (HRAEM) have been applied to the analysis of these buried dielectric layers with significant results. When oxygen is implanted into silicon, the interface between the amorphous oxide and the silicon is sharp on an atomic scale, but islands of silicon exist in the oxide for some distance from the interface. The effect is ion-implantation-condition-dependent. Dielectric layers formed by nitrogen ion implantations are expected to be similar to those formed by oxygen implantation, but offer advantages from the materials science viewpoint in terms of thermodynamic stability and mechanical strength. In this paper we report observations of the structure of silicon after two different implantation conditions which are the first part of an investigation to determine the effect of implantation variables on microstructure. *IN*

535). Microstructure of Silicon-on-Insulator Structures Produced by High Dose Nitrogen Implantation of Silicon.
Meekison, C. D.; Booker, G. R.; Reeson, K. J.; Hemment, P. L. F.;
Chater, R. J.; Kilner, J. A.; Davis, J. R.
Dep. Metall. Sci. Mater., Univ. Oxford, Oxford, United Kingdom
Vacuum, Vol. 36, No. 11-12, 925-8, 1986

The (100)Si wafers were implanted with 200-keV N^+ to doses 0.25 to 1.4 $\times 10^{18} cm^{-2}$, at 500 $\pm 10°C$. The microstructure in the as-implanted state and after annealing at 1200°C for 2 h was investigated by TEM. In the unannealed sample implanted to a dose of $0.25 \times 10^{18} cm^{-2}$, cross-sectional TEM indicated an amorphous layer close to the peak of the N distribution as shown by SIMS. Damaged Si layers were present above and below the amorphous layer. A dose of $1.4 \times 10^{18} cm^{-2}$ produced a thicker amorphous region containing bubbles. Annealed samples, implanted with doses of 1.0 and $1.4 \times 10^{18} cm^{-2}$ were examined and compared with earlier observations at doses of 0.25 and $0.75 \times 10^{18} cm^{-2}$. A dose of $1.0 \times 10^{18} cm^{-2}$ produced a well-defined α-Si_3N_4 layer showing a sublayer structure, and containing small Si islands. A dose of $1.4 \times 10^{18} cm^{-2}$ gave a more complex layer structure, including α-Si_3N_4 free from Si islands, and bubbles. Some threading dislocations (10^8 to $10^9/cm^2$) were present in the Si overlayer. *CA*

536). Vertical Bipolar Transistors on Buried Silicon Nitride Layers.
Munzel, H.; Albert, G.; Strack, H.
Solid State Electronics Lab., Tech. Univ. of Darmstadt, Darmstadt, Germany
IEEE Electron Device Lett. (USA), Vol.EDL-5, No.7, 283-5, July 1984

The authors report on the integration of vertically operating n-p-n bipolar transistors with base widths of about 1 μm in silicon-on-insulator (SOI) structures. Nitrogen ion implantation at substrate temperatures of 550°C and subsequent $SiCl_4$ epitaxy provide SOI films with excellent crystalline quality. Conventional bipolar diffusion processes have been used to fabricate diodes and vertical bipolar transistor alloys on isolated epitaxial layers. The leakage current of SOI diodes exceeds the value for bulk devices by only a factor of 2. The transistors exhibit emitter current gains of up to 100 and emitter-collector breakdown voltages of up to 35 V. *IN*

537). Formation of Silicon-on-Insulator Structures by Implanted Nitrogen.
Nesbit, L.; Stiffler, S.; Slusser, G.; Vinton, H.
IBM Gen. Technol. Div., Essex Junction, VT.
J. Electrochem. Soc. (USA), Vol.132, No.11, 2713-21, Nov. 1985

The formation of a buried Si_3N_4 by high-dose nitrogen ion implantation to form a silicon-on-insulator (SOI) structure is studied by transmission electron microscopy (TEM) and by secondary ion mass spectroscopy (SIMS). Silicon wafers are implanted with a dose of $7.5 \times 10^{17} N^+ ion/cm^2$ at an energy of 160 keV at wafer temperatures of 400, 500, and 600°C. The wafers are subsequently annealed at 1200°C for 2 h to form the buried silicon nitride layer. Both the as-implanted and postannealed microstructures are examined as a function of the implant temperature by TEM cross-sectional analysis. The microstructures of implanted wafers annealed for intermediate times are also examined to elucidate the development of the final microstructure. The as-implanted nitrogen profile and its redistribution during subsequent annealing at 1200°C are studied by SIMS. *IN*

538). Microstructure of Silicon Implanted with High Doses of Nitrogen and Oxygen.
Nesbit, L.; Slusser, G.; Frenette, R.; Halbach, R.
Div. of Gen. Technol., IBM, Essex Junction, VT.
J. Electrochem. Soc. (USA), Vol.133, No.6, 1186-90, June 1986

Silicon-on-insulator (SOI) structures are formed by implanting a high dose of nitrogen ions in combination with various doses of oxygen ions. A constant nitrogen dose of $7.5 \times 10^{17} N^+ ions/cm^2$ is implanted into all of the wafers in combination with additional oxygen doses of zero (0), 1×10^{16}, 1×10^{17}, or $1 \times 10^{18} O^+ ions/cm^2$. All implants are done at 160 keV at a wafer temperature of 500°C. The implanted silicon wafers are subsequently annealed at 1200°C. The resulting microstructures are monitored by transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), and by spreading resistance. Both the as-implanted and annealed microstructures are found to be dependent upon the relative oxygen to nitrogen doses. The spreading resistance of the buried silicon nitride layer increases with increasing oxygen dose up to a dose of $1 \times 10^{17} O^+ ions/cm^2$. *IN*

• 539). Transmission Electron Microscopy and Auger Electron Spectroscopy of Silicon-on-Insulator Structures Prepared by High-Dose Implantation of Nitrogen.
Petruzzello, J.; McGee, T.F.; Frommer, M.H.; Rumennik, V.; Walters, P.A.
Chou, C.J.
Philips Labs., Briarcliff Manor, NY.
J. Appl. Phys. (USA), Vol.58, No.12, 4605-13, 15 Dec. 1985

The effects of substrate temperature and ion dose on silicon-on-insulator structures prepared by nitrogen implantation were characterized by transmission electron microscopy and Auger electron spectroscopy. Substrate temperatures below 200°C during implantation result in amorphous surface layers that become polycrystalline after annealing. Implantation above 800°C leaves the surface single crystalline containing a high density of defects. The majority of these defects are removed after annealing. High nitrogen doses ($1.6 \times 10^{18} cm^{-2}$ at 150 keV) resulted in two nitride layers separated by a porous region. This porous region may be attributed to the creation of N_2 gas. A continuous nitride layer, without a porous region, was formed using a nitrogen dose of $9.4 \times 10^{17} cm^{-2}$. When a nitrogen dose of $4 \times 10^{17} cm^{-2}$ is used, however, it results in a two-phase layer containing amorphous nitride and Si crystallites. *IN*

540). Formation of SOI-Structures by High Dose Nitrogen Implantation and Flash Lamp Annealing.
Skorupa, W.; Kreissig, U.; Hensel, E.; Wollschlager, K.; Hoffmann, W.;
Pham, M.T.; Bartsch, H.
Central Inst. for Nucl. Res., Dresden, Germany
Hennig, K.; Heinig, K.-H.; Jager, H.-U.; Klabes, R.; Wieser, E. (Editors)
Energy Pulse Modification of Semiconductors and Related Materials.
Proceedings of the Conference, 392-6, Vol.2, 1985
25-28 Sept. 1984, Dresden, Germany
Akad. Wissenschaften DDR, Dresden, Germany

At present, different methods are under investigation to realize new SOI-structures for modern VLSI-systems. One of the most promising methods is high-dose oxygen or nitrogen implantation into silicon to produce buried insulating layers. Recently, the authors found that target heating during implantation and post-annealing at high temperatures are the crucial steps to produce monocrystalline top layers and Si_3N_4 with a high resistivity. Hitherto, only furnace annealing has been used to complete compound formation of the buried layer and to anneal radiation damage of the whole structure. The authors now report the application of flash lamp annealing to solve these problems because short-time annealing methods are of increasing importance for modern semiconductor technologies. *IN*

541). Increased Carrier Lifetimes in Epitaxial Silicon Layers on Buried Silicon Nitride Produced by Ion Implantation.
Skorupa, W.; Kreissig, U.; Hensel, E.; Bartsch, H.
Central Inst. for Nuclear Res., Dresden, Germany
Electron. Lett. (GB), Vol.20, No.10, 426-7, 10 May 1984

Carrier lifetimes were measured in epitaxial silicon layers deposited on buried silicon nitride produced by high-dose nitrogen implantation at 330 keV. The values were in the range 20 to 200 μs. The results are remarkable taking into account the high density of crystal defects in the epitaxial layers. Comparing with other SOI technologies the measured lifetimes are higher by 1 to 2 orders of magnitude. *IN*

542). Mechanism of Carrier Lifetime Increase in Ion Beam Synthesised SOI Structures.
Skorupa, W.; Oertel, H.; Bartsch, H.
Central Inst. of Nucl. Res., Dresden, Germany
Electron. Lett. (GB), Vol.22, No.20, 1062-4, 25 Sept. 1986

Carrier lifetimes were measured in epitaxial silicon layers which were deposited on silicon wafers implanted with different nitrogen doses at 330 keV. At doses greater than $10^{16} cm^{-2}$, the lifetime was more than one order of magnitude higher on the implanted part of the wafers (approximately 300 μs). The mechanism responsible for this effect is connected with the gettering efficiency for heavy metals of a precipitation-rich dislocation network in the implanted silicon. *IN*

543). The Physical and Electrical Properties of Buried Nitride SOI Structures Synthesized by Nitrogen Ion Implantation.
Slawinski, C.; Mao, B. Y.; Chang, P. H.; Lam, H. W.; Keenan, J. A.
Semicond. Process Des. Cent., Texas Instrm., Inc., Dallas, TX
Mater. Res. Soc. Symp. Proc., 53(Semicond. Insul. Thin Film Transistor Technol.), 269-80, 1986

Buried nitride Si-on-insulator (SOI) structures were fabricated by using the N ion-implantation technique. The crystallinity of the top Si film was exceptionally good. The mininum channeling yield, χ_{min}, was > 3%. This is comparable to the value observed for single-crystal Si. The buried insulator formed during the anneals was polycrystalline α-Si_3N_4 with numerous Si inclusions. This nitride, however, remains amorphous in regions at the center of the implant where the Ni concentration exceeds the center of the implant where the Ni concentration exceeds the stoichiometric level of Si_3N_4. N donor formation in the top Si was also observed. *CA*

544). Comparison of Pulsed Laser and Furnace Annealing of Nitrogen Implanted Silicon.
Smith, III, T.P.; Stiles, P.J.; Augustyniak, W.M.; Brown, W.L.; Jacobson, D.C.; Kant, R.A.
Brown University, Providence, RI.
Fan, J.C.C.; Johnson, N.M. (Editors)
Energy Beam-Solid Interactions and Transient Thermal Processing, Proceedings of

the Symposium, 453-458, 1984.
14-17 Nov. 1983, Boston, MA.
North-Holland, NY. *IN*

545). CMOS on Buried Nitride > A VLSI SOI Technology.
Zimmer, G.; Vogt, H.
Univ. of Dortmund, Dortmund, Germany
IEEE Trans. Electron Devices (USA), Vol.ED-30, No.11, 1515-20, Nov. 1983

A CMOS technology in silicon-on-insulator (SOI) for VLSI applications is presented. The insulator is a buried silicon nitride formed by nitrogen implantation and annealing. The CMOS devices are fabricated in the superficial monocrystalline silicon layer without an epitaxial process. 1-μm PMOS and 2-μm NMOS transistors have been realized, which have been used to build inverters, ring oscillators, and other circuits. With 40-nm gate oxide, the transistors withstand gate and drain voltages of 10 V. Mobilities, subthreshold behavior, and leakage currents are nearly the same as in bulk-CMOS devices. Ring-oscillator measurements yield inverter delay times of 230 ps and power delay products of 14 fJ. *IN*

546). Silicon on Insulator. SOS – A Suitable SOI-Technique for CMOS.
Astrand, B.; Hammarfors, H.
Eltek. Aktuell Elektron. (Sweden), No. 14, 87-90, Sept. 1984

SOS/silicon on sapphire is the only silicon-on-insulator technique in production today. ASEA-HAFO produce CMOS-circuits in SOS-technology. The main advantages are: speed, packing density, simpler manufacture, radiation hardness, and temperature tolerance. *IN*

• 547). Silicon on Sapphire in France. A Review of the Physico-Chemical and Electrical Properties.
Cristoloveanu, S.; Ghibaudo, G.; Kamarinos, G.
Lab. de Phys. des Composants a Semiconducteurs, Enserg, Grenoble, France
Rev. Phys. Appl. (France), Vol.19, No.2, 161-85. Feb. 1984

The authors present an overview of investigations conducted in France for the assessment of thin Si films epitaxied on sapphire substrates. Techniques and relevant data concerning physico-chemical properties (e.g., defects, impurities, contamination, etc.) and electrical features (e.g., transport, recombination, trapping, etc.) in SOS are reviewed extensively. The key physical parameters are: (1) existence of a transition layer 100 to 150 Å thick, situated at the Si-Al_2O_3 interface, which is responsible for important leakage currents in MOS/SOS transistors; (2) film nonuniformity connected with an increasing profile of defects towards the Si-Al_2O_3 interface and resulting in a noticeable degradation of carrier mobility and lifetime; (3) lateral stress at the film-substrate interface, the effect of which is to modify both the band energy configuration and the transport parameters as compared to bulk Si; (4) autodoping; and (5) potential fluctuations. The consistency of different results derived from independent measurements performed on non-processed SOS films and on devices is emphasized. Finally, taking into account the great number of techniques and experimental conditions, the authors discuss their pertinence, precision, or limitations as well as their interest for the characterization of other silicon-on-insulator technologies. *IN*

548). Recent Advances in the Heteroepitaxial Silicon-on-Sapphire Technology.
Cullen, G.W.; Duffy, M.T.; Smeltzer, R.K.
RCA Labs., Princeton, NJ.
Bean, K.E.; Rozgonyi, G.A. (Editors)
VLSI Science and Technology-1984, Proceedings of the Second International Symposium on Very Large Scale Integration Science and Technology. Materials for High Speed/High Density Applications, 230-49, 6-11 May 1984, Cincinnati, OH.
Electrochem. Soc., Pennington, NJ.

In the heteroepitaxial silicon-on-sapphire technology, recent advances have been made in the areas of characterization, radiation-hardness, and solid-phase epitaxial regrowth. The application of UV reflectometry as a rapid and non-destructive quality control tool has had a dramatic impact on the reproducibility of the properties of heteroepitaxial silicon. Mainly through modification of device processing techniques, radiation-induced shifts in threshold voltages and back-channel leakage currents of CMOS/SOS transistors have been brought to acceptable levels. High-density high-performance logic and memory circuits can now be made for applications in which a high tolerance to radiation is required. Thinner silicon deposits ($= 0.3\mu m$) are needed for the fabrication of IC circuits with submicron features. It now appears that the crystalline perfection required will be achievable through application of the solid-phase epitaxial regrowth process. In light of these recent advances, it seems unlikely that silicon-on-sapphire will be replaced by alternative SOI technologies in the near future for applications in CMOS IC device structures. *IN*

• 549). Radiation-Hardened CMOS/SOI Development Status.

Davis, G.E.
Naval Res. Lab., Washington, DC.
Trans. Am. Nucl. Soc. (USA), Vol.49, 23-4, 1985
American Nuclear Society 1985 Annual Meeting
9-14 June 1985, Boston, MA.

Dielectrically isolated complementary metal-oxide semiconductor (CMOS) circuits should have a significant influence in the area of communication satellites and military systems that require radiation-hardened low-power circuits. The silicon-on-insulator (SOI) technologies are becoming increasingly important for these applications. The typical advantages of dielectrically isolated devices are (a) increased speed due to reduced parasites, (b) high packing density, (c) reduction in transient photocurrent, (d) elimination of radiation-induced latch-up, (e) reduction of soft-error/single-event upset rates and (f) innovative architectures for three-dimensional integration and the possibility of implementing complementary bipolar and CMOS circuitry. There are several SOI technologies that have applications for hardened circuits: silicon-on-sapphire (SOS) and the new, all-silicon-based, thin-film technologies such as zone-recrystallized SOI, full isolation by porous oxidized silicon (FIPOS), epitaxial lateral overgrowth (ELO), and silicon implanted oxide (SIMOX). These thin-film SOI technologies have tremendous potential for hardened very-large-scale integrated circuit applications by stacking devices, and by permitting substrate biasing. *IN*

550). The Current Status of Silicon-on-Sapphire and Other Heteroepitaxial Silicon-on-Insulator Technologies.
Golecki, I.
Microelectron. Res. & Dev. Center, Rockwell Int. Corp., Anaheim, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 1-23
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, Amsterdam.

The present understanding of the properties of thin ($\leq 0.6\mu m$) heteroepitaxial Si films grown on single-crystal bulk and thin-film insulators is reviewed. Three areas are covered: as-deposited Si films on bulk insulators, with particular emphasis on sapphire and cubic zirconia; post-growth processing methods to reduce the defect concentration and compressive strain in such Si films; and the growth and properties of monocrystalline insulating films on bulk Si and of Si on such films. The desired characteristics of the insulating material are given, and it is shown that the mismatch in thermal expansion coefficients between the insulator and Si dominates the properties of heteroepitaxial Si films. Present and future areas of application for Si-on-insulator technologies are briefly described, and directions for further studies are proposed. *IN*

• 551). Recent Advances in Hetero-Epitaxial Silicon-on-Insulator Technology. I.
Gupta, A.; Vasudev, P.K.
Hughes Aircraft Co., Newport Beach Res. Center, Newport Beach, CA.
Solid State Technol (USA), Vol. 26, No. 2, 104-9, Feb. 1983

Silicon-on-sapphire (SOS) has matured as the primary hetero-epitaxial silicon-on-insulator technology for fabricating integrated circuits. Recent advances in the growth, characterization, and processing of SOS material for commercial and military VLSI applications are reviewed. A major deficiency preventing the realization of the full potential of SOS technology has been the quality of the as-grown epitaxial Si film. Crystallinity, chemical impurities, and electrical properties of SOS films are evaluated by both destructive and non-destructive measurement techniques. Their advantages and limitations are analyzed. Material improvement processes, such as laser annealing, solid-phase epitaxial regrowth, and optimization of epitaxial growth conditions, are reviewed. Their impact on device performance and future potential is discussed. *IN*

• 552). Recent Advances in Hetero-Epitaxial Silicon-on-Insulator Technology. II.

Gupta, A.; Vasudev, P.K.
Hughes Aircraft Co., Newport Beach, CA.
Solid State Technol (USA), Vol. 26, No. 6, 129-34, June 1983

This paper, a discussion of material characterization methods, examines novel material improvement techniques, and presents some applications of the technology to digital and microwave circuits. The authors discuss Rutherford backscattering, secondary ion mass spectrometry, use of stress, electronic properties, recrystallisation, and laser annealing. *IN*

553). Simulation of Deep Depleted Silicon-on-Insulator MOS Transistor With Back Potential Control.
Balestra, F.; Brini, J.
Lab. De Phys. Des Composants A Semiconducteurs, Enserg, Grenoble, France
Rev. Phys. Appl. (France), Vol.19, No.11, 921-6, Nov. 1984

The authors consider SOI MOSFET structures of n- and p-type controlled by two gates. In the case of a lightly doped thin-film silicon, the two interfaces of the MOS transistor are strongly coupled. In order to study the action of the interface parameters on the threshold voltages, they carried out a numerical integration of Poisson's equation. They obtain the potential profile and the corresponding electron and hole densities, as a function of the applied front (V_{G1} and back (V_{G2}) gate voltages. They also deduce the $I_d(V_{G1}, V_{G2})$ characteristics in the case of low drain voltage. The simulated $I_d(V_{G2})$ characteristics are compared with the $I_D(V_{G2})$ characteristics obtained with CMOS/SOS transistors. The sapphire of these devices has been locally thinned down to control the back surface potential by using a back gate. This comparison gives direct measures of the fast state density and the fixed charge at the back interface. *IN*

554). Charge Collection in CMOS/SOS Structures.
Campbell, A.B.; Knudson, A.R.; Stapor, W.J.; Shapiro, P.;
Diehl-Nagle, S.E.; Hauser, J.
US Naval Research Lab, Washington, DC
IEEE Transactions on Nuclear Science, Vol. NS-32, No. 6, Dec. 1985, 1985
Annual Conf. on Nucl. and Space Radiat. Eff., Monterey, CA, July 22-24, 1985, 4128-4132

Charge-collection measurements in CMOS/SOS test structures have shown that, even for highly ionizing ion tracks, the fraction of the charge collected at a node is about equal to what is expected from the amount deposited in the silicon layer and that no charge is collected from the sapphire substrate. *EI*

555). CMOS/SOS High Soft-Error Threshold Memory Cell.
Hsueh, F.-L.; Napoli, L.S.
RCA Lab, Princeton, NJ
IEEE Transactions on Nuclear Science, Vol. NS-32, No. 6, Dec. 1985, 1985
Annual Conf. on Nucl. and Space Radiat. Eff., Monterey, CA, July 22-24, 1985, 4155-4158

The five-transistor (5T) CMOS/SOS memory cell has been widely used in RCA's radiation hardness products. The p-channel devices in the memory cell are protected from the cosmic ray hit by the buried contact diodes. However, there is no protection for the n-channel devices. A configuration referred to as seven-transistor CMOS/SOS memory cell which is modified from the 5T memory cell layout by inserting a depletion-mode NMOS transistor in the feedback path of enhancement NMOS drain node has been proposed. Simulations show that this configuration increases the single-event-upset critical charge by a factor of 25 at $V_{dd} = 5$ V. The increase in silicon area is only 10%. *EI*

556). J-MOS: A Versatile Power Field-Effect Transistor.
MacIver, B.A.; Jain, K.C.
General Motors Res. Labs., Warren, MI.
IEEE Electron Device Lett. (USA), Vol.EDL-5, No.5, 154-6, May 1984

A field-effect transistor structure that is attractive for power control applications is proposed and demonstrated. It combines MOSFET structural features and junction FET function in a simple, self-aligned structure that is referred to as J-MOS. Lateral J-MOS transistors were fabricated in

silicon-on-sapphire (SOS) with on-resistance as low as 2.5 Ω in 1 cm of channel width. This result suggests that a vertical version of J-MOS can be fabricated in silicon-on-buried-insulator with a specific on-resistance > $1\mu m\ \Omega - cm^2$, approximately a factor-of-two improvement over current power FET technology. *IN*

557). Monolithic Capacitor-Coupled Gate Input High Voltage SOS/CMOS Driver Array.
Sakuma, H.; Hirata, K.
NEC Corp., Kawasaki, Japan.
Proceedings of the 1984 Custom Integrated Circuits Conference, 564-8
21-23 May 1984, Rochester, NY.
IEEE, New York.

A high-voltage CMOS pulse generator array with high-voltage gate-coupling capacitors, suitable for display driver use, was experimentally integrated on one chip by using high-voltage SOS/MOS technology. This array succeeded in generating 700- to 2.5-MHz, 30- to 40-mA output currents, 150-V pulses with extremely low operation power. It can charge or discharge a 25-pF capacitor load within 160-ns rise or fall time, or a 2220-pF load within 10-μs rise or fall time, at 150 V. It never dissipates power at quiescent state and dissipates only 0.96-mW/inverter under 150-V, 10-kHz no-load operating conditions. A proposed high-voltage SOS/MOS transistor structure, which is applicable to thin-layer SOI substrate (such as laser or electron-beam-annealed SOI, Si/spinel/Si substrate, SIMOX), is also discussed. *IN*

558). CMOS/SOS VLSI Technology.
Sato, T.; Iwamura, J.; Tango, H.; Doi, K.
Toshiba Corp., Kawasaki, Japan
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 25-34
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

CMOS is considered as a prospective technology in the VLSI era because of its low power consumption and high driving capability. Ordinary bulk silicon CMOS devices are inferior to SOS CMOS devices in chip area, operation speed, and latch-up problems due to the need for isolation wells. SOS is a good partner of the CMOS circuits owing to the simple and perfect isolation. SOS technology, however, has the problem of high wafer cost. Consequently, SOS technology is best applied to high-performance logic devices. Latest results of 8K-gate CMOS/SOS gate arrays and 16 by 10 bit multipliers show 0.87-ns 2-NAND gate delay and 27-ns multiplication time, respectively, which compare with ECL devices. Application of SOS devices down to 1 μm is also promising for very high speed operation. A 78-ps gate delay is achieved by double solid phase epitaxy and 1-μm technology. *IN*

559). MOS Integrated Circuits Fabricated on Multilayer Heteroepitaxial Silicon-Insulator Structures for Applications to 3-D Integrated Circuits.
Sugiura, S.; Yoshida, T.; Kaneko, Y.; Shono, K.; Dumin, D.J.
Dept. of Electr. Eng., Sophia Univ., Tokyo, Japan
IEEE Trans. Electron Devices (USA), Vol.ED-32, No.11, 2307-13, Nov. 1986

Multiple layers of single-crystal and boron phosphide have been grown on silicon-on-sapphire substrates. Up to four layers have been grown on silicon and two layers on silicon-on-sapphire. The quality of the silicon layers was confirmed by fabricating PMOS integrated circuits on the top silicon layer in all of these structures. The integrated circuits contained individual transistors, p-n diodes, inverters, flip-flops, and ring oscillators. All circuits successfully operated on all of the layers tested. The transistor mobilities tended to drop as more layers were added to the structure. The delay time of the ring oscillators rose as the number of layers increased, reflecting the drop in transistor mobilities. By fabricating circuits on the various layers, the quality of the individual

layers has been shown to be sufficiently high to consider this material combination as a possible candidate for 3-D integrated circuits. The boron phosphide was used not only as an insulator but also for the fabrication of vertical resistors and p-n junctions. *IN*

• 560). Characterization of CMOS Devices in 0.5-1 μm Silicon-on-Sapphire Films Modified by Solid Phase Epitaxy and Regrowth (SPEAR).
Vasudev, P.K.; Mayer, D.C.
Hughes Res. Lab., Malibu, CA.
Lam, H.W.; Thompson, M.J. (Editors)
Comparison of Thin Film Transistor and SOI Technologies Symposium, 35-9, 1984
26-28 Feb. 1984, Albuquerque, NM.
North-Holland, New York.

Complementary metal-oxide-semiconductor (CMOS) devices and circuits with minimum feature sizes of about 1 μm were fabricated in 0.5-μm thick epitaxial silicon-on-sapphire (SOS) films. The films were modified by ion implantation and subsequent solid phase recrystallization processes which reduced the total microtwin concentrations in the Si layers by more than a hundredfold, while increasing electron and hole channel mobilities between 40 to 50%. Leakage currents were reduced by over 2 orders of magnitude, while drive currents and subthreshold slopes showed significant improvements over as-grown SOS films. Propagation delays of less than 80 ps were obtained for CMOS/SOS inverters with $L_{eff} = 0.6\mu$m. *IN*

561). Simulation of Deep Depleted SOI MOSFETs With Back Potential Control.
Balestra, F.; Brini, J.; Gentil, P.
Lab. de Phys. des Composants a Semiconducteurs, ENSERG, Grenoble, France
Physica B & C (Netherlands), Vol.129B+C, No.1-3, 296-300, March 1985
Proceedings of the 14th European Solid State Device Research Conference, Including Solid State Device Technology, 10-13, Sept. 1984, Lille, France

The authors consider SOI MOSFET structures of n- and p-types for which a control of the back potential of the epi layer is obtained by using a back gate. The action of the interface parameters on the back and front threshold voltages is analysed in the case of a strong coupling between the front and back interface (lightly doped epi layer). This analysis is carried out by a numerical simulation of Poisson's equation throughout the structure. They thus obtain the potential profile and the electron and hole densities, as a function of front (V_{G1}) and back (V_{G2}) gate voltages. They also deduce the $I_d(V_{G1}, V_{G2})$ characteristics in the case of low drain voltage. Experimental material is given by CMOS/SOS transistors, the sapphire substrate of which has been locally thinned down. Comparison of the experimental $I_d(V_{G2})$ characteristics with the simulated characteristics allows the authors to determine directly the fast state density and the fixed charge at the back interface. *IN*

562). Analysis of Electrical Transport Properties Of Silicon on Insulator. Use of Thermoelectric Power.
Ghibaudo, G.; Kamarinos, G.
Lab. de Phys. des Composants a Semiconducteurs, Enser, Grenoble, France
Rev. Phys. Appl. (France), Vol.17, No.3, 133-43, March 1982

The use of the thermoelectric power (TEP) for the study of the transport properties of inhomogeneous semiconductors is proposed. Silicon-on-sapphire (SOS) of n-type is considered as a reference and as a test material. A theoretical study of the electrical conductivity, the Hall effect, and the TEP of such samples is presented; the variations of the mobilities and the densities of free carriers with temperature in the different parts of the inhomogeneous samples are taken into account. A model concerning semiconductors which can be considered as two-layer materials is established. Using this theoretical model, a detailed comparison between the Hall effect and the TEP is performed. The measurements of TEP are much more sensitive to transport inhomogeneities than Hall effect measurements. In the case of SOS, the study of the sensitivity of the TEP (S) and the electrical conductivity (σ) versus the variations of the transport parameters, show that the combined measurements of σ and s can be sufficient for a satisfactory and efficient characterization of this material, the main problem of which is, precisely, its epitaxial inhomogeneity. Experimental results performed on phosphorus-doped SOS films are presented and analysed. The thickness of the films is about 0.7 μm; they are studied between 77 K and 360 K. The analysis of (σ,T) and (S,T) characteristics leads to the transport parameters as well as to the law of their variations. The SOS samples are represented by the main n-type part and a degenerate, n^+ type, thin layer; the thickness of the n^+ type transition (Si-Al_2O_3) layer is estimated to be about 150 Å. The transition layer is either an overdoped and highly disturbed region or a strongly accumulated layer. *IN*

563). The Numerical Simulation of Silicon-on-Insulator MOS Devices.
Mole, P.J.
GEC Res. Ltd., Hirst Res. Centre, Wembley, England
Board, K.; Owen, D.R.J. (Editors)
Simulation of Semiconductor Devices and Processes. Vol.2., Proceedings of the Second International Conference, 434-48, 1986
21-23 July 1986, Swansea, Wales
Pineridge Press, Swansea, Wales

The differences between MOSFETs fabricated in a silicon-on-insulator (SOI) and in a bulk silicon technology are discussed along with examples of applications of simulation techniques to SOI devices. These examples include the calculation of the magnitude of the parasitic capacitances which become important in low-capacitance SOI technology, calculation of the influence of the edges of a device on its behaviour, calculation of the threshold voltage of an SOI device, and calculation of the 'substrate' potential in an SOI device using two-dimensional simulation. For most of the examples, silicon-on-sapphire (SOS) technology has been chosen to illustrate the methods used. *IN*

308). Recrystallization of Silicon Film on Insulating Layers Using a Laser Beam Split by a Birefringent Plate.
Aizaki, N.

309). Recrystallization of SOI Structures by Split Laser Beam.
Aizaki, N.

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266). High Speed CMOS Devices Fabrication on Laser-Recrystallized Polycrystalline Silicon Island.
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Akiya, M.; Nakashima, S.

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Akiya, M.; Nakashima, S.; Kato, K.

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Asano, T.; Kuriyama, Y.; Ishiwara, H.

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Astrand, B.; Hammarfors, H.

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Atwater, H.A.; Smith, H.I.; Thompson, C.V.; Geis, M.W.

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Auberton-Herve, A.J.; Joly, J.P.; Hode, J.M.; Castagna, J.C.

268). Device Performances of a Submicron SOI Technology.
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• 63). A Seeded-Channel Silicon-on-Insulator (SOI) MOS Technology.
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64). Deep Depleted SOI MOSFETs With Back Potential Control: A Numerical Simulation.
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Balestra, F.; Brini, J.; Gentil, P.

348). Annealing of Ion-Implanted Silicon-on-Insulator Films Using a Scanned Graphite Strip Heater.
Banerjee, S.K.; Lee, B.; Baker, J.E.; Reed, D.A.; Streetman, B.G.

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Barklie, R. C.; Hobbs, A.; Hemment, P. L. F.

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Biegelsen, D.K.; Hawkins, W.G.; Fennell, L.E.; Johnson, N.M.; Moyer, M.D.

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Bleil, C.E.; Troxell, J.R.

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Bourguet, P.; Dupart, J.M.

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Burnham, M.E.; Wilson, S.R.

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Celler, G.K.; Hemment, P.L.F.; West, K.W.; Gibson, J.M.

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Chang, C.Y.; Fang, Y.K.; Wu, B.S.; Chen, R.M.

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Chantre, A.; Ronzani, D.; Vu, D.P.

66). Radiation Effects in Semiconductors: Technologies for Hardened Integrated Circuits.
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152). SOI Edge Parasitics and Their Couplings.
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Chen, C.-E.; Blake, T.G.W.; Hite, L.R.; Malhi, S.D.S.; Mao, B.-Y.; Lam, H.W.

• 505). SOI-CMOS 4K SRAM Via Oxygen Implant.
Chen, C.-E.; Lam, H.W.; Malhi, S.D.S.; Mao, B.-Y.; Blake, T.G.W.; Hite, L.R.

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11. ABSTRACT (*A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here*)

This bibliography of silicon-on-insulator SOI technology was compiled from a literature search of three data bases: INSPEC, Engineering Index, and Chemical Abstracts. The bibliography has been categorized according to the technique used to produce the SOI substrate. It includes the abstracts for most of the papers. It can either be used to obtain a quick evaluation of the "state of the art" in a particular SOI technique, or as a guide for further in-depth study.

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