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CMOS/SOS Test Patterns for Process Evaluation and Control: Annual Report, March 1 to November 1, 1978

Loren W. Linholm

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, D.C. 20234

January 1979

Prepared for
U.S. Air Force
Air Force Avionics Laboratory
Wright Patternson AFB, Ohio 45433

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U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, *Secretary*

Jordan J. Baruch, *Assistant Secretary for Science and Technology*

NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

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ANNUAL REPORT

March 1 to November 1, 1978

Loren W. Linholm

Executive Summary:

The National Bureau of Standards in collaboration with the Jet Propulsion Laboratory, Pasadena, CA and RCA, Somerville, NJ, has designed a CMOS/SOS test pattern, NBS-16, and the necessary measurement techniques. RCA is required to process one test pattern wafer with each CMOS/SOS wafer lot being fabricated for the radiation-hardened microprocessor chip set. Each test pattern wafer is to be tested at NBS and JPL and recommendations for improvements made to the Air Force Avionics Laboratory (AFAL), the Air Force Materials Laboratory (AFML), and RCA. A second-generation test pattern will be designed later based on information and experience obtained from the first. To date, the NBS-16 test pattern has been designed, a pattern generator tape has been delivered to RCA, and the testing hardware and software has been developed. A simple test pattern, NBS-21, has been designed and fabricated to verify the compatibility of NBS layout programs with the RCA pattern generator and also to electrically determine linewidth variations across a pattern. NBS-16 test wafers are being fabricated at RCA. A program schedule (AFSC form 103) can be found in Appendix A.

Objective:

The objective of this program is to develop process assessment methods which can be used by an independent source to evaluate the electrical performance, radiation tolerance, and yield potential of LSI circuits fabricated with a radiation-hardened silicon gate CMOS/SOS process.

Approach:

In collaboration with JPL and RCA, NBS has designed a CMOS/SOS test pattern, NBS-16, and developed the required measurement techniques. Under AFAL contract, RCA is processing one wafer on NBS-16 with each CMOS/SOS wafer lot. Each wafer will be tested by NBS and JPL. Recommendations for improvements will be made to AFAL, AFML, and RCA based on the analysis of test results. By July 1979, a second-generation test pattern will be designed incorporating the information and experience gained from the first.

NBS-16 Test Pattern Design:

Prior to the design of NBS-16, a meeting was held with RCA personnel to carefully review the RCA radiation hardened silicon gate CMOS/SOS process and topological design rules. RCA uses a seven-level mask set for their radiation-hardened process. This process has nine photolithography steps (see table 1). Two of the masks are used twice. In the standard RCA process the N-I mask is used for the N- and P+ implants and P-I mask is used for the P- and N+ implants. A list of the topological design rules and tolerances can be found elsewhere.[1] For optimum flexibility, the test pattern mask set is nine levels. This allows for N+ into N- and P+ into P- implants. It does not require any additional processing and is fully compatible with RCA production process. The function of each mask level is described in table 1. The working photomasks were fabricated by a computer-controlled pattern generator at RCA.

Pattern Generator Software Verification:

Prior to fabrication of the NBS-16 photomasking, a simple one-level test pattern, NBS-21, was designed at NBS to check the compatibility of the

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[1]Design Rules, Silicon-Gate CMOS/SOS RCA Solid State Technology Center, April 15, 1978.

Table 1

Photomask Level Functions

Process Sequence	Function	Mask Designator	RCA level No.
1.	Island Definition	ISD	8
2.	N- Implant	N-I	(9)
3.	P- Implant	P-I	(4)
4.	Poly Definition	PLY	3
5.	N+ Implant	N+	4
6.	P+ Implant	P+	9
7.	Contact	CNT	5
8.	Metal Definition	MET	6
9.	Passivation	PRO	7

NBS layout programs with the RCA pattern generator. An NBS-21 tape which could be read by the pattern generator was sent to RCA and a satisfactory reticle was produced.

NBS-16 Description:

NBS-16 is a square test pattern 250 mils (6.35 mm) on a side. It was designed in English units in order to be compatible with RCA photomask fabrication. It is divided into seven basic areas as shown in figure 1. Each area can be physically separated, if desired. The functions of each area are listed in table 2. A computer-generated plot of the actual layout is shown in figure 2.

NBS-16 is being fabricated on 3-in. (76.2-mm) diameter sapphire wafers. Approximately 94 sites are available. An RCA TCS-121 test pattern is being placed in two of the available sites. This pattern is an internal RCA test pattern and contains structures such as a ring oscillator circuit not found on NBS-16. A detailed description of each structure in the NBS areas of NBS-16 is provided in Appendix B.

Table 2

Device Types on NBS-16

	Area	Types of Devices
I.	Process Parametric Device Pattern (NBS)	MOSFETS, cross-bridge sheet resistors, contact resistors, capacitors, RCA Gate Universal Array Cells.
II.	Physical Analysis Pattern (NBS)	Level designators, alignment marks, ion beam areas, surface profilometer, etch structure.
III.	Random Fault Structure I (NBS)	MOSFET arrays.
IV.	Random Fault Structure II (NBS)	Capacitor arrays.
V.	Process Parametric Device (JPL)	MOSFETS, capacitors, resistors.
VI.	Oxide Breakdown Pattern (JPL)	Capacitor array, P- substrate.
VII.	Oxide Breakdown Pattern (JPL)	Capacitor array, N- substrate.

NBS-16 Evaluation:

The NBS portions of NBS-16 are to be evaluated at NBS. Baseline electrical parameters from the Process Parametric Device Pattern will be measured. Where appropriate, statistical averages and wafer maps will be produced. Random Fault Structure I will be analyzed to determine the suitability of using a logic type MOSFET array as a test structure for detection of random faults and to determine the fault density of minimum geometry MOSFET structures. Random Fault Structure II will be used to determine the density of faults in the gate oxide.

The degree of overetch and surface topography will be determined from the Physical Analysis Pattern at specific chip sites. Information obtained from these measurements will be sent to AFAL, AFML, and RCA on a monthly basis. When a wafer has been completely tested at NBS, it will be sent to JPL for further evaluation.

Cross-Bridge Sheet-Resistor Array, NBS-21:

NBS-21 is a one-level pattern consisting of an 8 by 15 array of identical metal cross-bridge sheet resistors. A computer-generated plot of the actual chip layout is seen in figure 3. A working photomask was made from a reticle of this pattern produced by Harry Diamond Laboratories, Adelphi, MD. Wafers were made at NBS.

Initial evaluation of the NBS-21 array indicates that periodic intrachip variations in linewidth occur and can be measured. Figure 4 illustrates a map of the intrachip linewidth variations.

The linewidth of each of the cross-bridge sheet resistors on a wafer was measured. There are 120 resistors per chip and 53 chips on a wafer. A map of linewidth variations was obtained for each of the 53 chips. Figure 4 is a point-by-point average of the 53 chip maps. The standard deviation of each point of the map was about $\pm$ 1 percent.

It is believed that the intrachip variation in linewidth is a function of the resolution of the lens in the step and repeat camera used in fabricating the 1X photomasks. After the periodic intrachip variation in linewidth is known, chip-to-chip and wafer-to-wafer variations in linewidth can be determined. These are believed to be caused by variables in the photolithographic processing. If specific variables in the photolithography can be identified by this type of structure, it will be included on the second-generation test pattern. Further work is being performed to increase our data base and to measure periodic or random chip-to-chip and wafer-to-wafer variations.

Acknowledgment

The author would like to acknowledge the technical contributions made by Martin G. Buehler, the computer-aided layout and design efforts of Dwight A. Maxwell, the assistance in software development from Richard L. Mattis, and the wafer testing performed by Melvin R. Doggett.

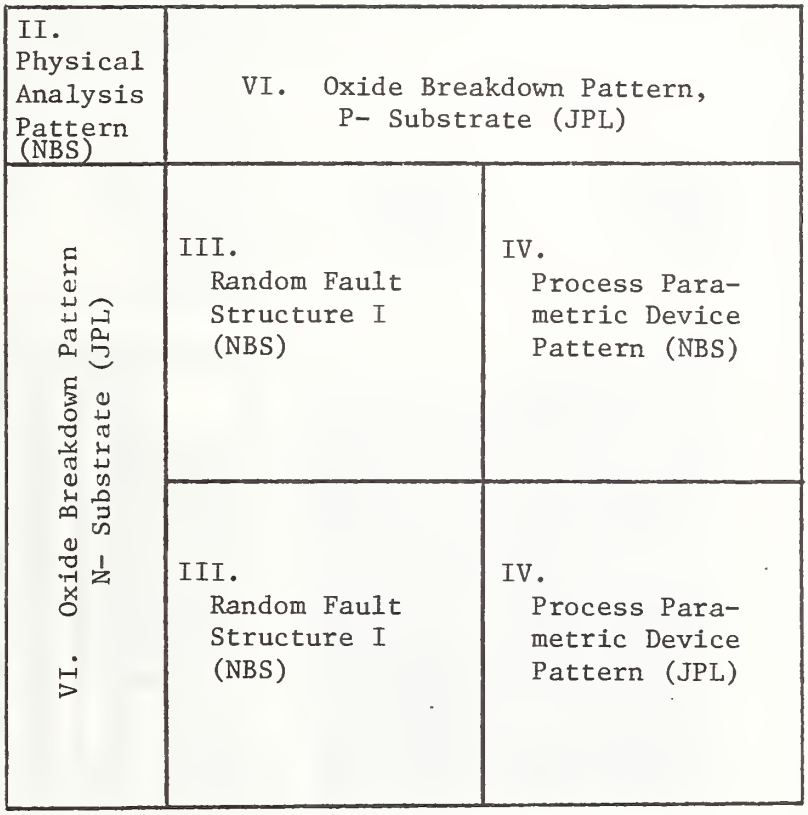


Figure 1. NBS-16 test pattern.

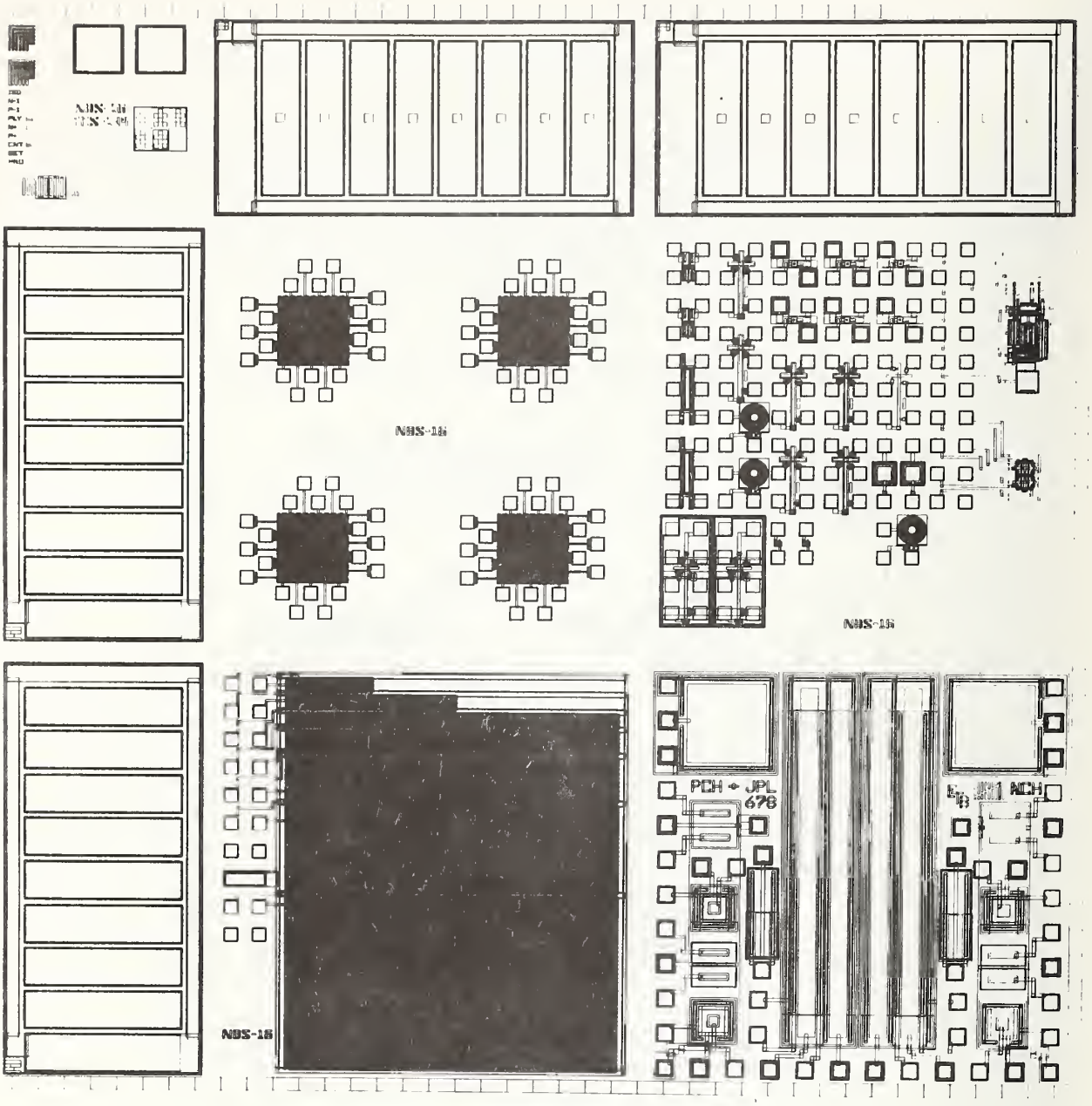


Figure 2. Computer plot of NBS-16.

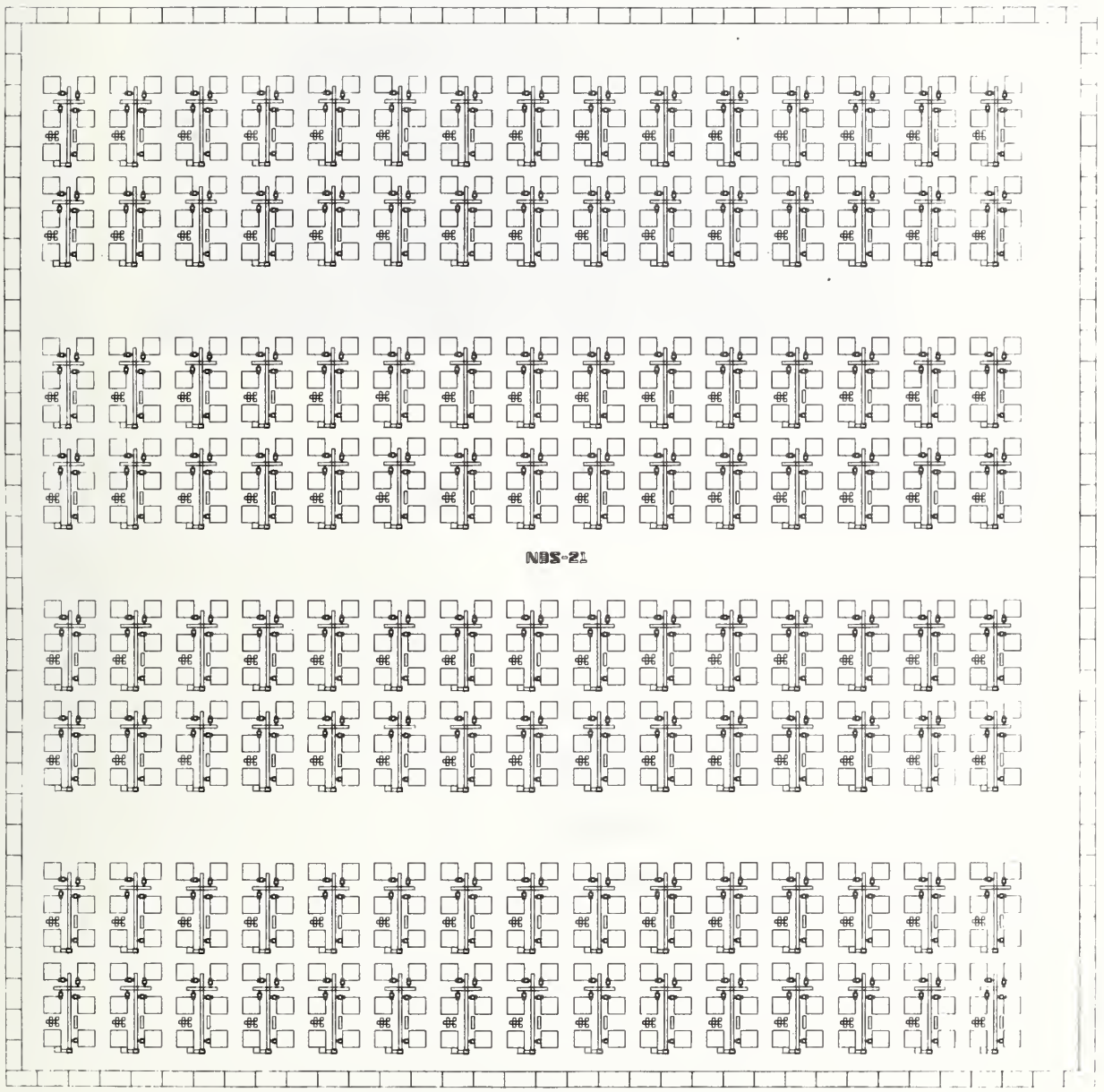


Figure 3. Computer-generated plot of NBS-21.

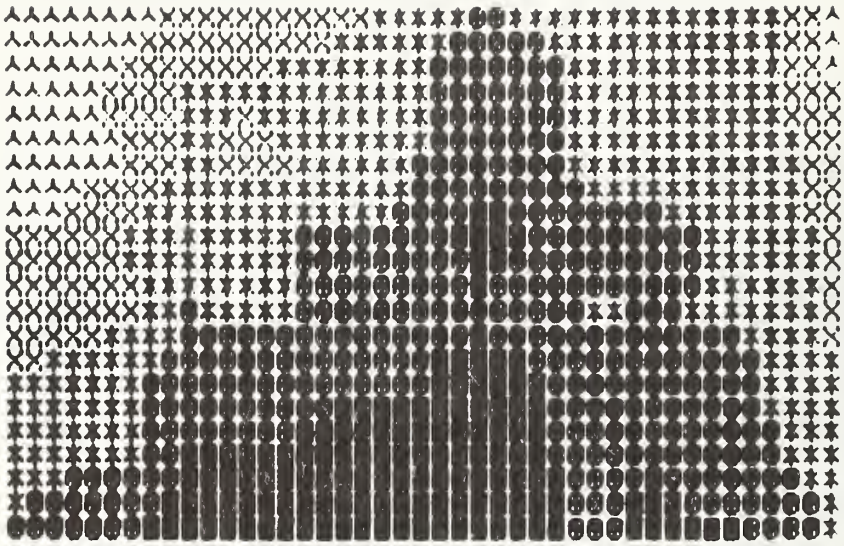
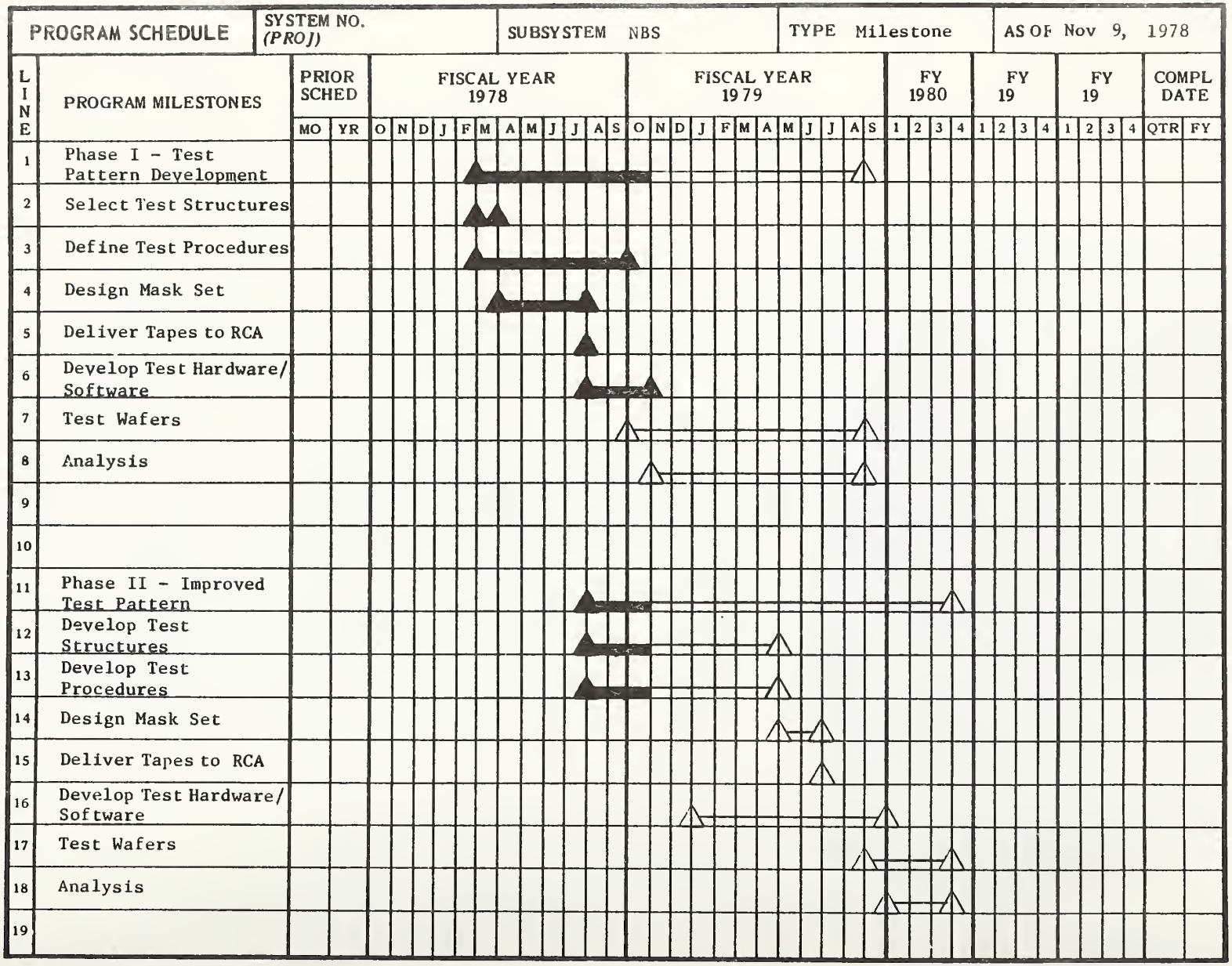


Figure 4. Intrachip linewidth variations.

Appendix A

Program Schedule

(AFSC Form 103)



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AFSC-ANDREWS AFB MD 1977

PROGRAM SCHEDULE	SYSTEM NO. *(PROJ)*	SUBSYSTEM NBS	TYPE Milestone	AS OF Nov 9, 1978

LINE	PROGRAM MILESTONES	PRIOR SCHED		FISCAL YEAR 1978												FISCAL YEAR 1979												FY 1980				FY 19				FY 19				COMPL DATE	
		MO	YR	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	1	2	3	4	1	2	3	4	1	2	3	4	QTR	FY
1	Monthly Status Letters																																								
2	Technical Report (Draft)															▲												△													
3	Technical Report (Final)																	△										△													
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Appendix B

CMOS/SOS Test Pattern for Process Evaluation and Control: NBS-16

CMOS/SOS Test Pattern For Process Evaluation and Control: NBS-16

Introduction: This report describes the structures designed by NBS and included on the NBS-16 test pattern. NBS-16 is illustrated in Figure B-1.

This report contains a number of figures produced on a computer-controlled plotter. Figure B-2 is a key for identifying the individual levels. Many structures require a change in only the level position of the implant mask to form a new device (e.g., P-channel MOSFET vs. N-channel MOSFET). Only one figure has been included in this report for each basic structure. Similar structures, varying only in the level of the implant mask, are grouped in this listing. The figures show, in each case, the levels associated with the first structure of the group.

A description of the method used to measure the MOSFET electrical parameters is found elsewhere [B-1].

I. Process Parametric Pattern

Purpose: The process parametric portion of NBS-16 contains structures necessary to evaluate baseline electrical parameters.

Description: The process parametric pattern is laid out in 2 by N columns of probe pads. The pattern is a square approximately 100 mil (2.54 mm) on a side. Six columns containing 28 structures are present. The pattern can be probed automatically by a 2 by 10 probe card and computer tester.

Drawing: Figure B-3. (The structure number appears in the upper left probe pad of each structure.)

List of Structures

1. P-channel four-terminal MOSFET
2. N-channel four-terminal MOSFET
   a. Description: This device is a conventional MOSFET with electrical contacts to gate, source, drain, and body. The gate dimensions are 2.5 by 0.3 mil (0.064 by 0.0076 mm).
   b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 1.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor K', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
   c. Drawing: Figure B-4.
3. N-channel MOSFET
4. P-channel MOSFET
   a. Description: This device is a five-terminal MOSFET with electrical contacts to gate, source, and drain, and two contacts to the body. The device is much larger than Devices 1 and 2 but has approximately the same length-to-width ratio. The gate dimensions are 9.0 by 1.0 mil (2.3 by 0.025 mm).
   b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 1.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction

factor K', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.

c. Drawing: Figure B-5.

The fifth electrical contact to the body region is made via an implanted region of opposite dopant concentration to the body. This may be useful in evaluating the back channel leakage characteristics of the device.

5. N-channel closed geometry MOSFET
6. P-channel closed geometry MOSFET
   a. Description: This device is a four-terminal MOSFET with electrical connection to gate, source, drain, and body. It is a circular device with the source completely surrounded by the gate channel and the gate channel surrounded by the drain. The gate channel is "edgeless"; it has a length of 0.3 mil (0.0076 mm).
   b. Parameters determined; Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 1.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor K', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
   c. Drawing: Figure B-6.
7. P- cross-bridge sheet resistor
8. N- cross-bridge sheet resistor
9. P+ cross-bridge sheet resistor
10. N+ cross-bridge sheet resistor
11. P+ doped poly cross-bridge sheet resistor
12. N+ doped poly cross-bridge sheet resistor
13. Metal cross-bridge sheet resistor
    a. Description: The cross-bridge sheet resistor is a combination of a van der Pauw sheet resistor and a bridge resistor [B-2]. The design linewidth is 0.6 mil (0.015 mm).
    b. Parameters measured: Sheet resistance and linewidth of the conducting layer.
    c. Drawing: Figure B-7.

14. P- gated cross-bridge sheet resistor
15. N- gated cross-bridge sheet resistor
    a. Description: The gated cross-bridge sheet resistor is similar in geometry to device 7 except that the resistor is junction isolated in an epi island. The resistor is defined by a poly silicon gate which is a mask for a further heavy channel stop implant. Electrical contact is made to the resistor (or channel region), the poly gate, and the channel stop.
    b. Parameters measured: Sheet resistance and linewidth of the channel region with the gate grounded.
    c. Drawing: Figure B-8.
16. Metal to P- contact resistor
17. Metal to N- contact resistor
18. Metal to P+ contact resistor
19. Metal to N+ contact resistor
20. Metal to P+ doped poly contact resistor
21. Metal to N+ doped poly contact resistor
    a. Description: The contact resistor is used to measure the electrical resistance between the metal level and a resistive layer [B-3]. The size of the contact opening is a square 0.4 mil (0.010 mm) on a side. This is the same size contact opening used on the cross-bridge sheet resistor.
    b. Parameters measured: Contact resistance.
    c. Drawing: Figure B-9.
22. P-type MOS capacitor
23. N-type MOS capacitor
    a. Description: This structure is a poly-oxide-epi capacitor with an area of 10.24 mil^2 (6.61×10^{-3} mm^2) and with an electrical guard ring.
    b. Parameters measured: Capacitance per unit area and possibly capacitance vs. voltage characteristics.
    c. Drawing: Figure B-10.

24. Closed geometry gated diode

    a. Description: This device is similar to the closed geometry MOSFET (device No. 5) except that the gate is extended beyond the drain region and off the epi island. The electrical connection to the drain has been removed leaving electrical connection to the source, body, and gate.

    b. Parameters measured: Leakage current caused by bulk and surface carrier generation.

    c. Drawing: Figure B-11.

25. N-channel two-terminal MOSFET

26. P-channel two-terminal MOSFET

    a. Description: This structure is a two-terminal MOSFET with the gate permanently connected to the drain. It is used as the internal cell in the Random Fault Structure I MOSFET arrays. It is included here to permit electrical access to a single cell.

    b. Parameters measured: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 1.0 μA, and source-to-drain leakage current at 10.0 V.

    c. Drawing: Figure B-12.

27. Internal cell from RCA Gate Universal Array (GUA)

    a. Description: This is an internal cell from the RCA GUA family and has been included to provide electrical access to an individual structure used frequently in the RCA GUAs. The cell consists of two P-channel MOSFETs and two N-channel MOSFETs [B-4].

    b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 1.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor K', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.

    c. Drawing: Figure B-13.

28. Input/Output cell with input protection from RCA GUA

    a. Description: This is an input/output cell consisting of a P-channel and N-channel MOSFET, two diodes, and a

resistor [4]. The diodes and resistor are arranged so they can be included in input structures or omitted in output structures. The device on NBS-16 has no components internally connected. Each device is connected to a probe pad for electrical access.

b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 1.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor K', calculated threshold voltage, and the standard error of estimate of the two calculated parameters. PN junction characteristics.

c. Drawing: Figure B-14.

II. Physical Analysis Pattern

Purpose: The physical analysis portion of NBS-16 contains structures which are intended for physical, visual, or beam analysis. No electrical testing is performed with these structures.

Description: The physical analysis pattern is a square approximately 50 mil (1.27 mm) on a side located in the upper left corner of NBS-16. Mask alignment marks and level designators are also included in this pattern.

Drawing: Figure B-15. (The structure number appears to the left of each structure.)

List of structures

29. Light-Field RCA alignment marks (Figure B-16)
30. Dark-Field RCA alignment marks (Figure B-17)
31. Mask level designators and critical dimension structures
    a. Description: This structure contains mask level designators and critical dimension structures on each level. The critical dimension structure consists of a pair of minimum width 2.0-mil (0.051-mm) long parallel lines separated by the width of one line.

b. Parameters measured: Linewidth of critical dimensions on the working photomasks.

c. Drawing: Figure B-18.

32. Overetch structure

a. Description: This structure contains checker board elements which can be inspected visually to determine over-etching or underetching for epi definition; poly-over-epi definition, metal-over-epi definition, contact window over epi definition, and contact-window-over-poly definition.

b. Parameters measured: The degree of over-etching or under-etching of critical levels.

c. Drawing: Figure B-19.

33. P- SIMS area

34. N- SIMS area

a. Description: This structure is a square 10.0 mil (0.0254 mm) on a side which can be analyzed by secondary ion mass spectroscopy.

b. Parameters measured: Impurity atom concentration.

c. Drawing: Figure B-20.

35. Surface profilometer

a. Description: This structure is a series of parallel 4.0 mil (0.10 mm) long stripes of metal, oxide, epi, and poly and is intended for use with a surface-profile-type instrument.

b. Parameters measured: The step height of epi, poly, metal, and contact window on sapphire and the step height of poly, contact window, and metal on epi.

c. Drawing: Figure B-21.

36. NBS Designator "NBS-16" (Figures B-22 and B-23)

37. NBS Designator "NBS-16" (Figure 24)

III. Random Fault Structure I

Purpose: The purpose of this structure is to test the feasibility of using a logic type array to determine the random fault density of a MOSFET array and determine the location and nature of any faults detected. The spatial integrity of important parameters will also be determined.

Description: This structure consists of two 10 by 10 arrays of P-channel MOSFETs and two 10 by 10 arrays of N-channel MOSFETs. The arrays are within a 100-mil (2.54-mm) square. The devices are interconnected such that the drains and gates are common. They are arranged in rows and columns similar to a diode matrix with source connections to columns and the gate and drain connections to rows. Each device is electrically isolated from its neighbor and can be individually tested by addressing the appropriate row and column probe pads.

Parameters measured: For each MOSFET in the array, threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 1.0 μA, source-to-drain leakage current at 10.0 V, and fault location (e.g., the location of a MOSFET not having reasonable electrical parameters). Based on the nature of detected faults (shorts or opens) and location, information regarding the quality of the metal step coverage, metal bridging and other shorts or opens in the metal level can be determined.

Drawing: Figure B-25.

IV. Random Fault Structure II

Purpose: The purpose of this structure is to determine the fault density of gate oxide dielectric breakdown primarily at the epi island edge.

Description: This structure contains an array of capacitors and is used to detect metal-to-poly, poly-to-epi, and metal-to-epi leakage caused by photolithography-induced defects or dielectric

breakdown of the gate or field oxide. The array consists of 6,021 capacitors connected in electrically parallel groups of 57, 114, 225, 375, 750, 1500, and 3000. The array is in a 100-mil (2.54-mm) square and can be probed by a 2 by 10 probe card.

Parameters measured: Metal-to-poly, poly-to-epi, and metal-to-epi leakage current as a function of array size.

Drawing: Figure B-26.

References

B-1. Penny, W. M. and Lau, L., Editors, *MOS Integrated Circuits*, pp. 126-129, (van Nostrand Co, New York, 1972).

B-2. Buehler, M. G., Grant, S. D., and Thurber, W. R., Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers, *J. Electrochem. Soc.* 125, 650-654 (1978).

B-3. Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Pattern NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon, NBS Special Publication 400-22 (June 1976).

B-4. Skorup, Gordon E., SOS COS/MOS Universal Array User's Manual, Solid State Technology Center, Somerville, NJ, (May 1977).

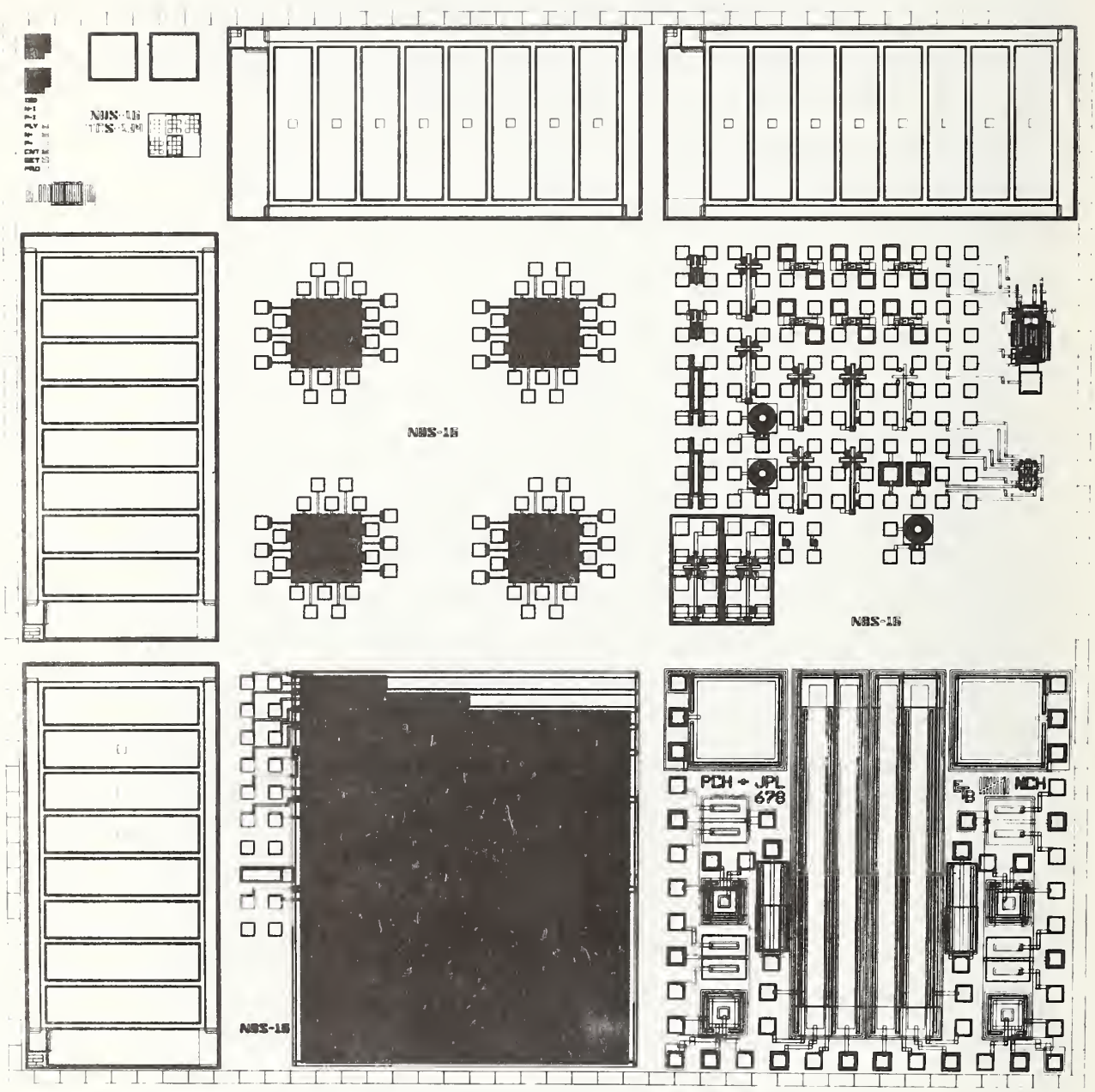


Figure B-1. NBS-16 test pattern.

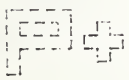
	Process Sequence	Function
	1.	Island Definition
	2.	N- Implant
	3.	P- Implant
	4.	Poly Definition
	5.	N+ Implant
	6.	P+ Implant
	7.	Contact
	8.	Metal Definition
	9.	Passivation

Figure B-2. Level identification key.

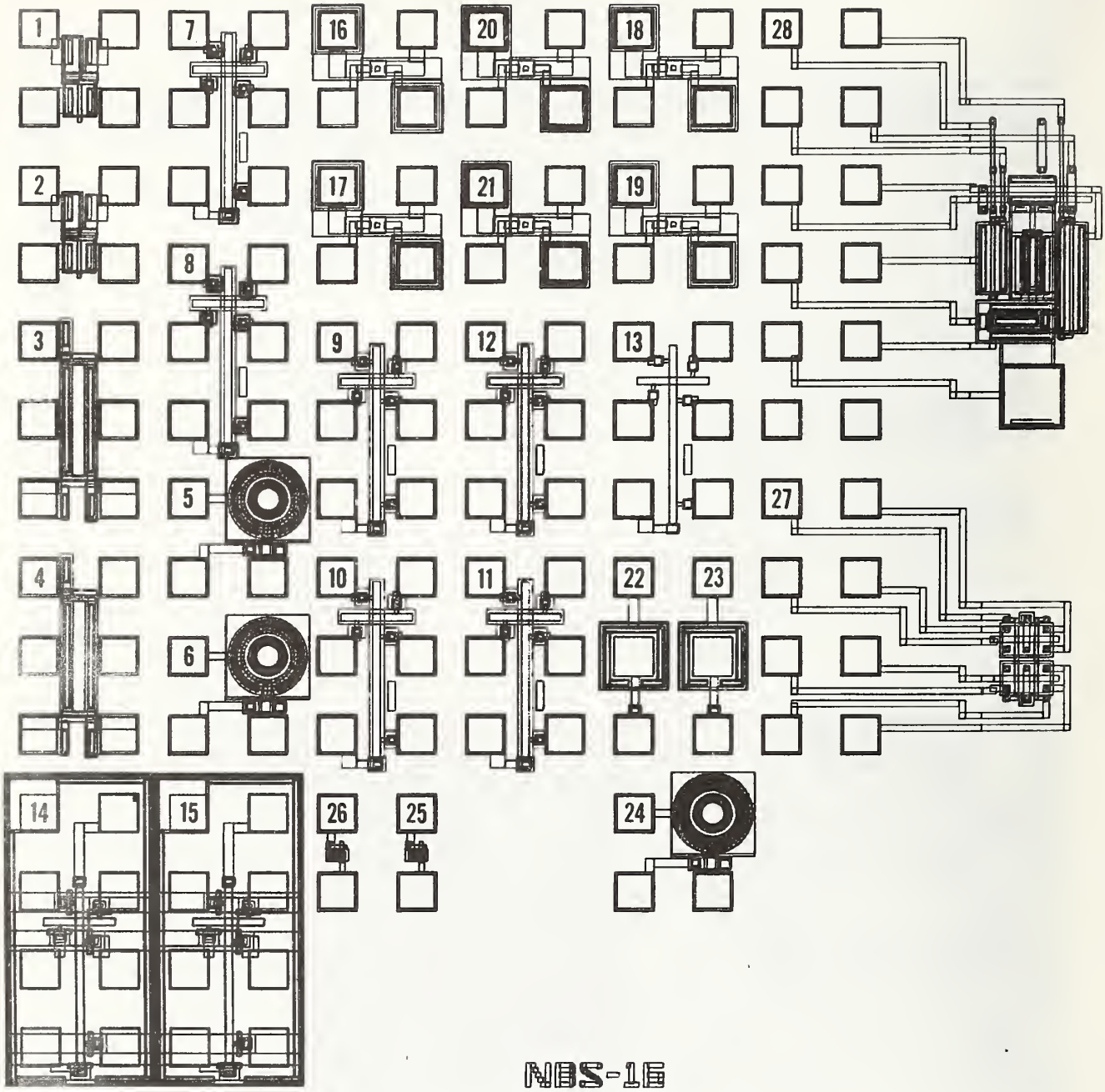


Figure B-3. NBS-16 process parametric pattern.

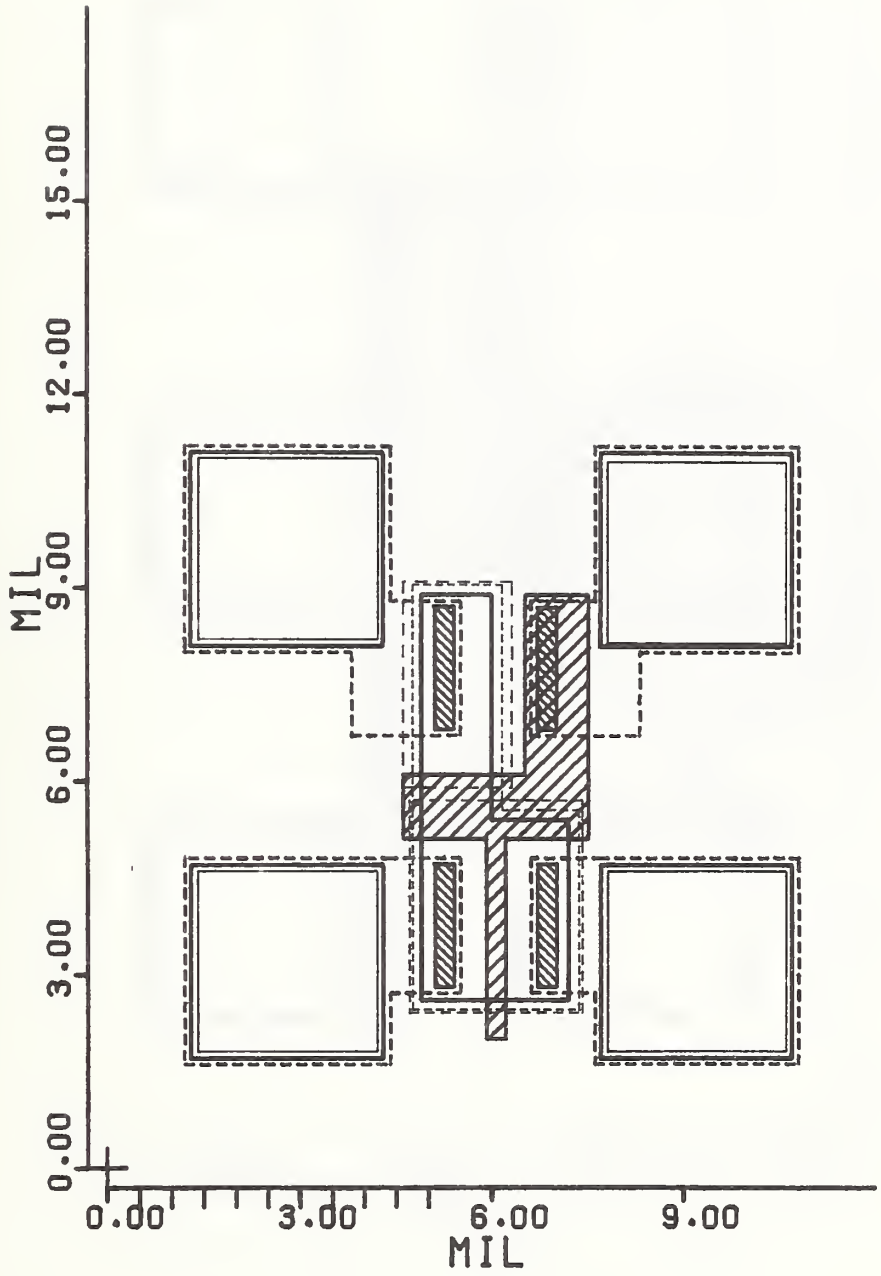


Figure B-4. Four-terminal MOSFET.

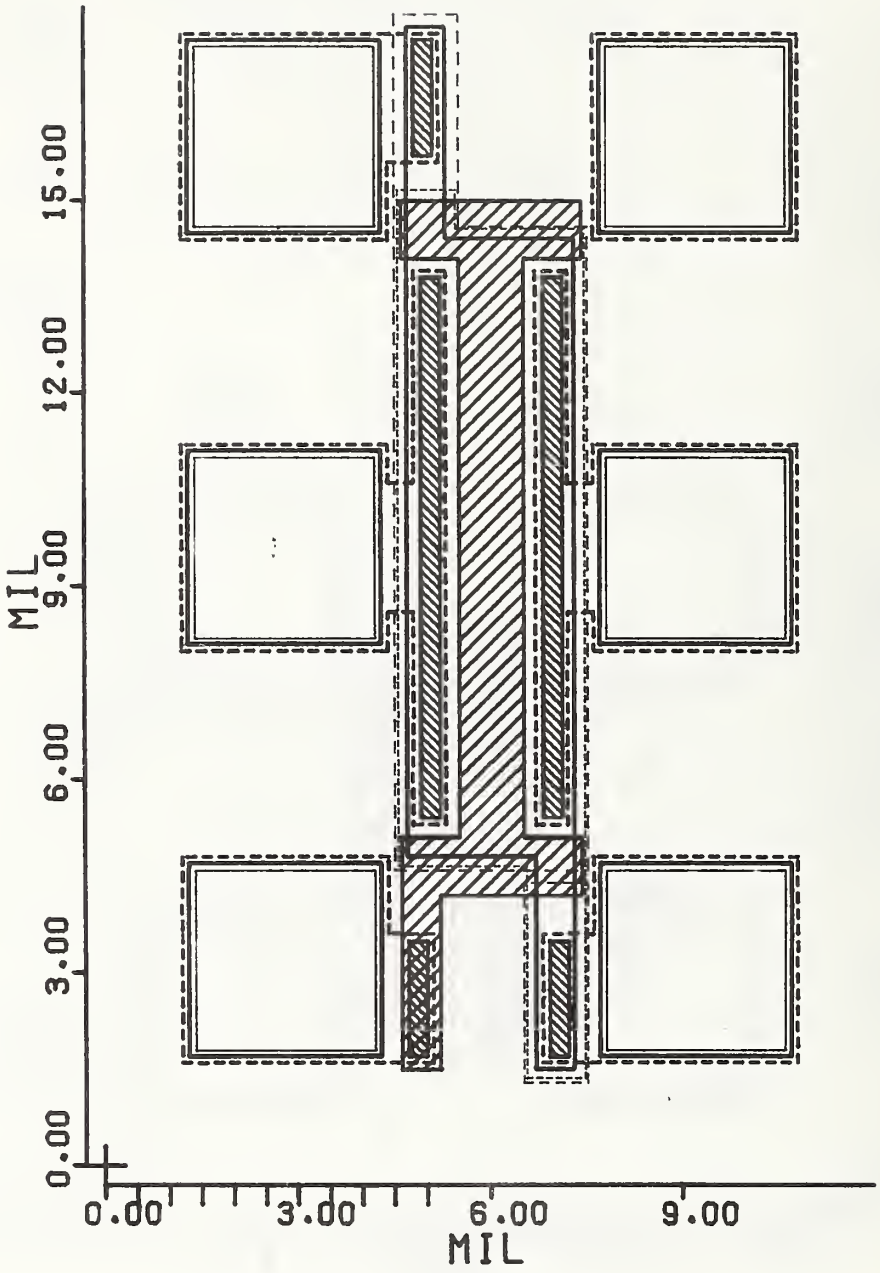


Figure B-5. MOSFET.

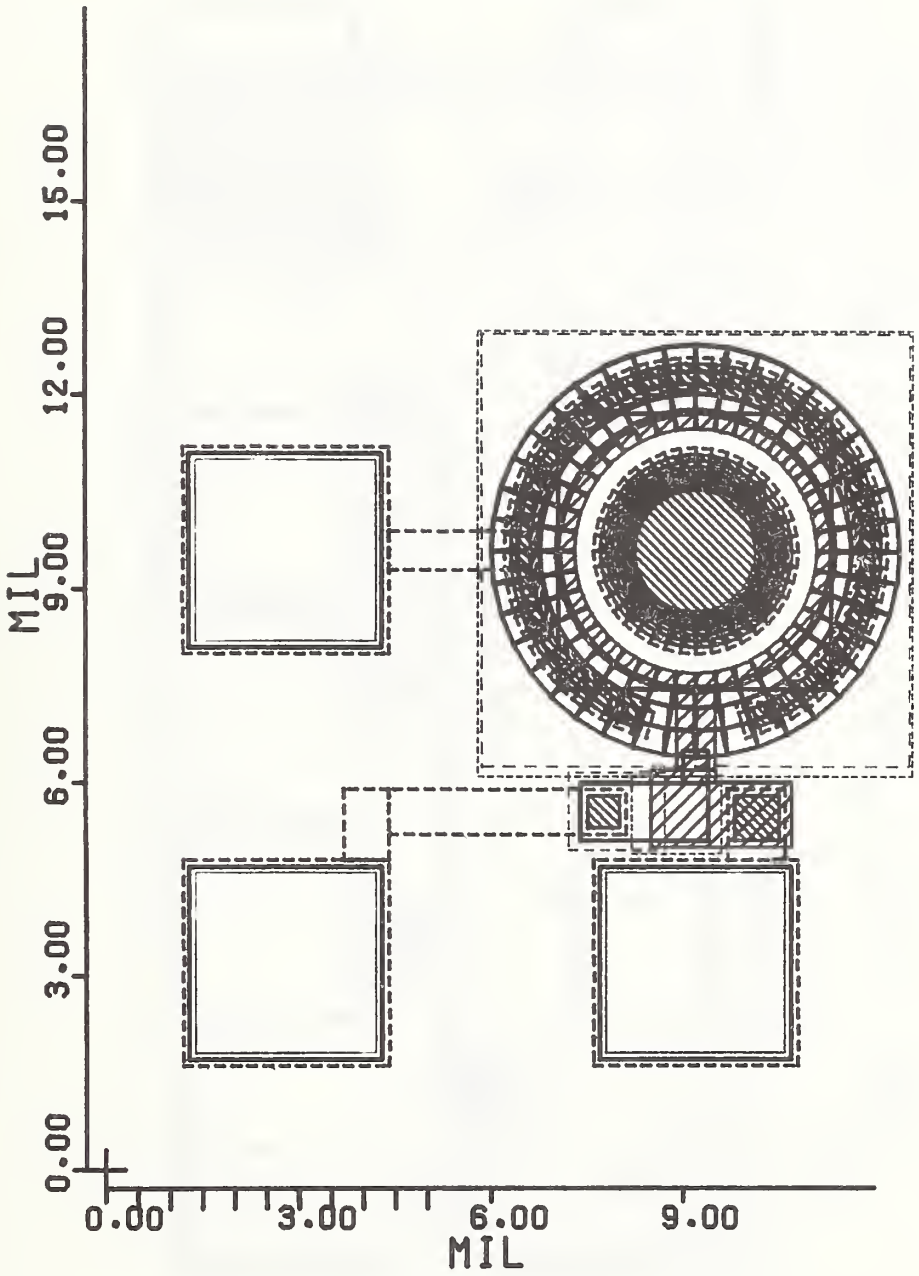


Figure B-6. Closed geometry MOSFET.

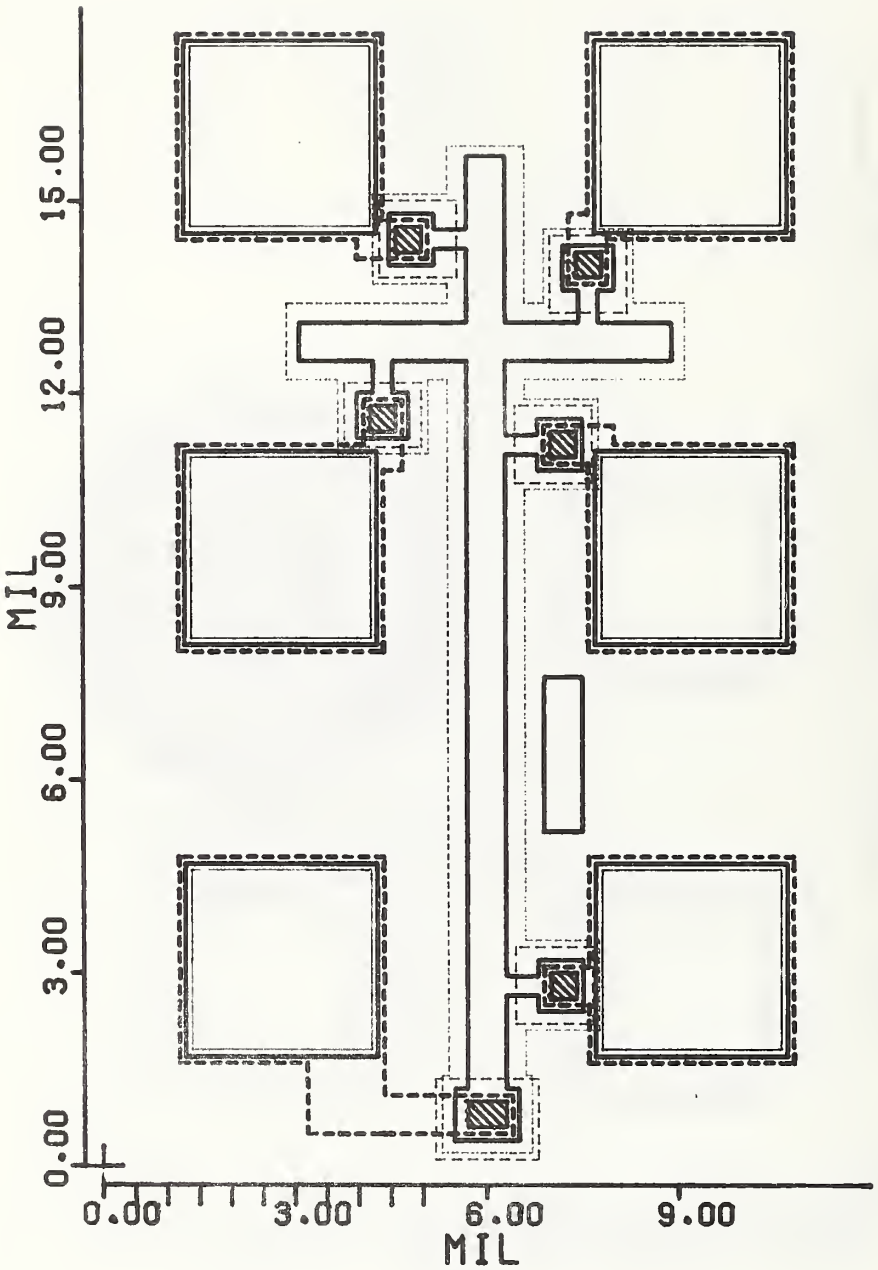


Figure B-7. Cross-bridge sheet resistor.

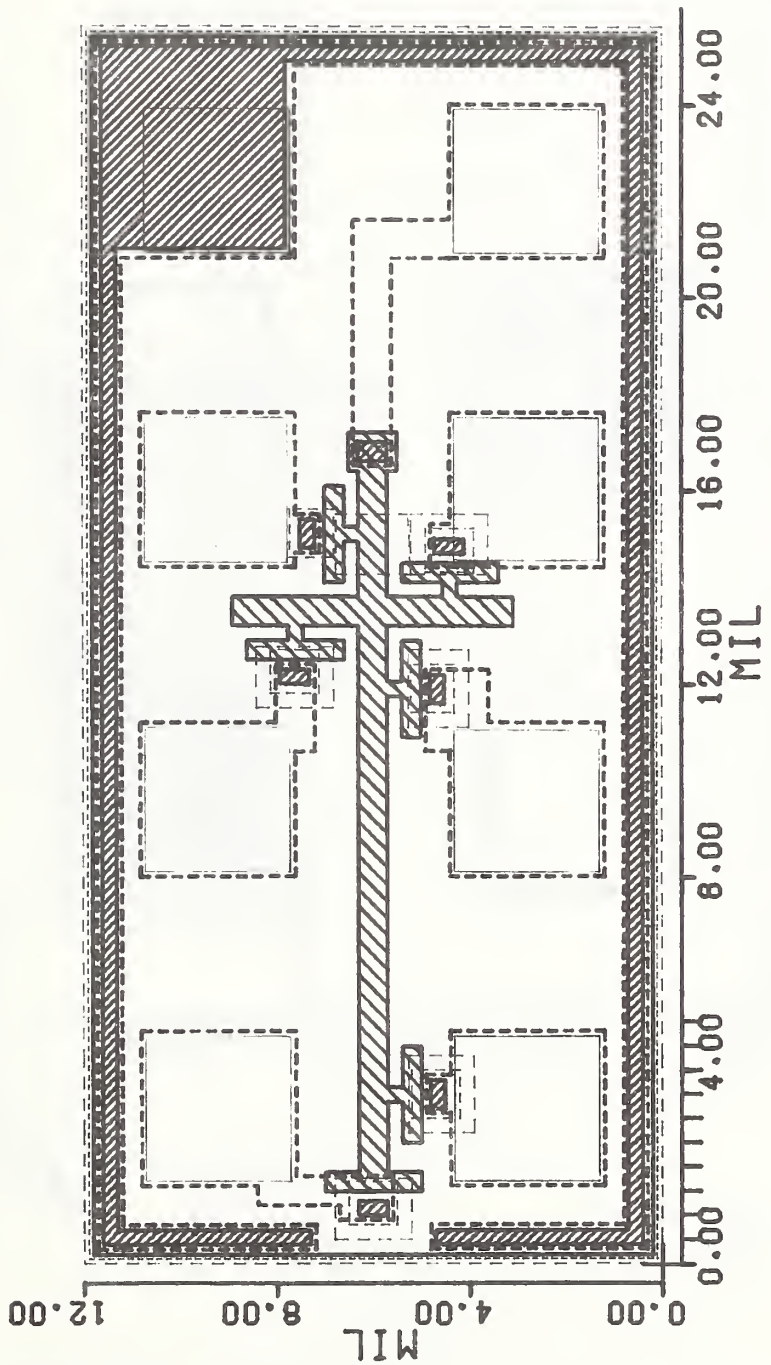


Figure B-8. Gated cross-bridge sheet resistor.

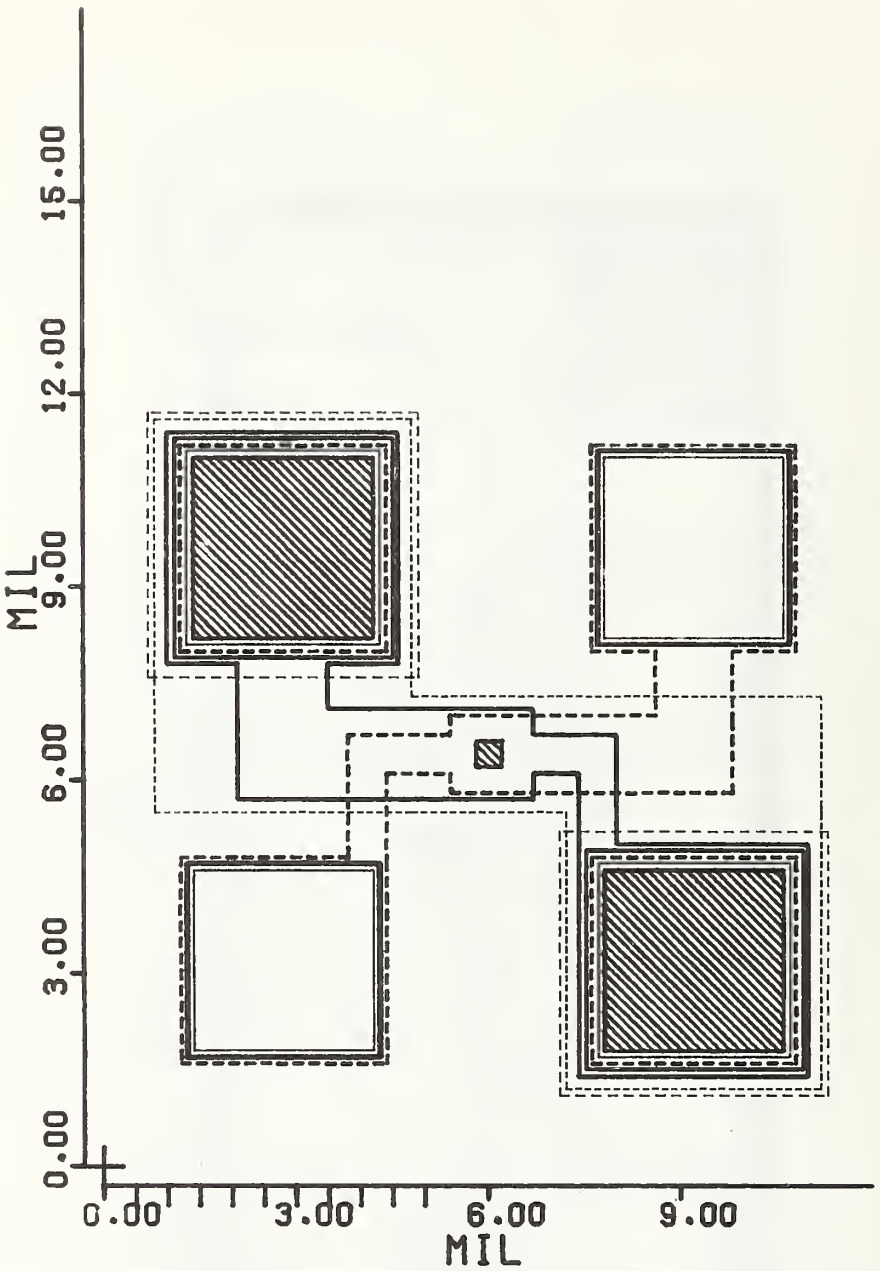


Figure B-9. Contact resistor.

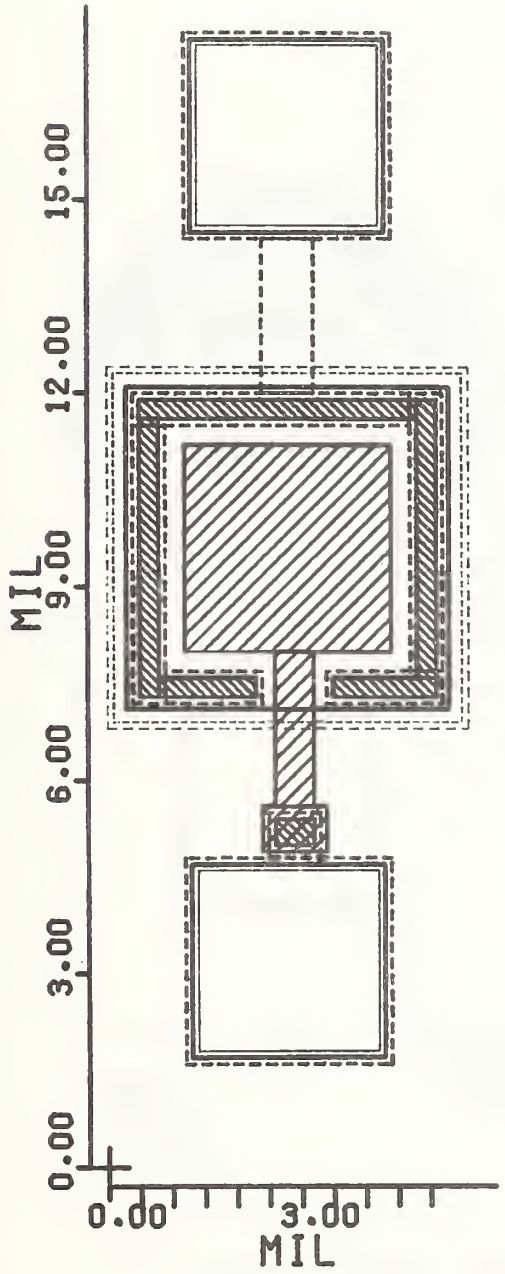


Figure B-10. MOS capacitor.

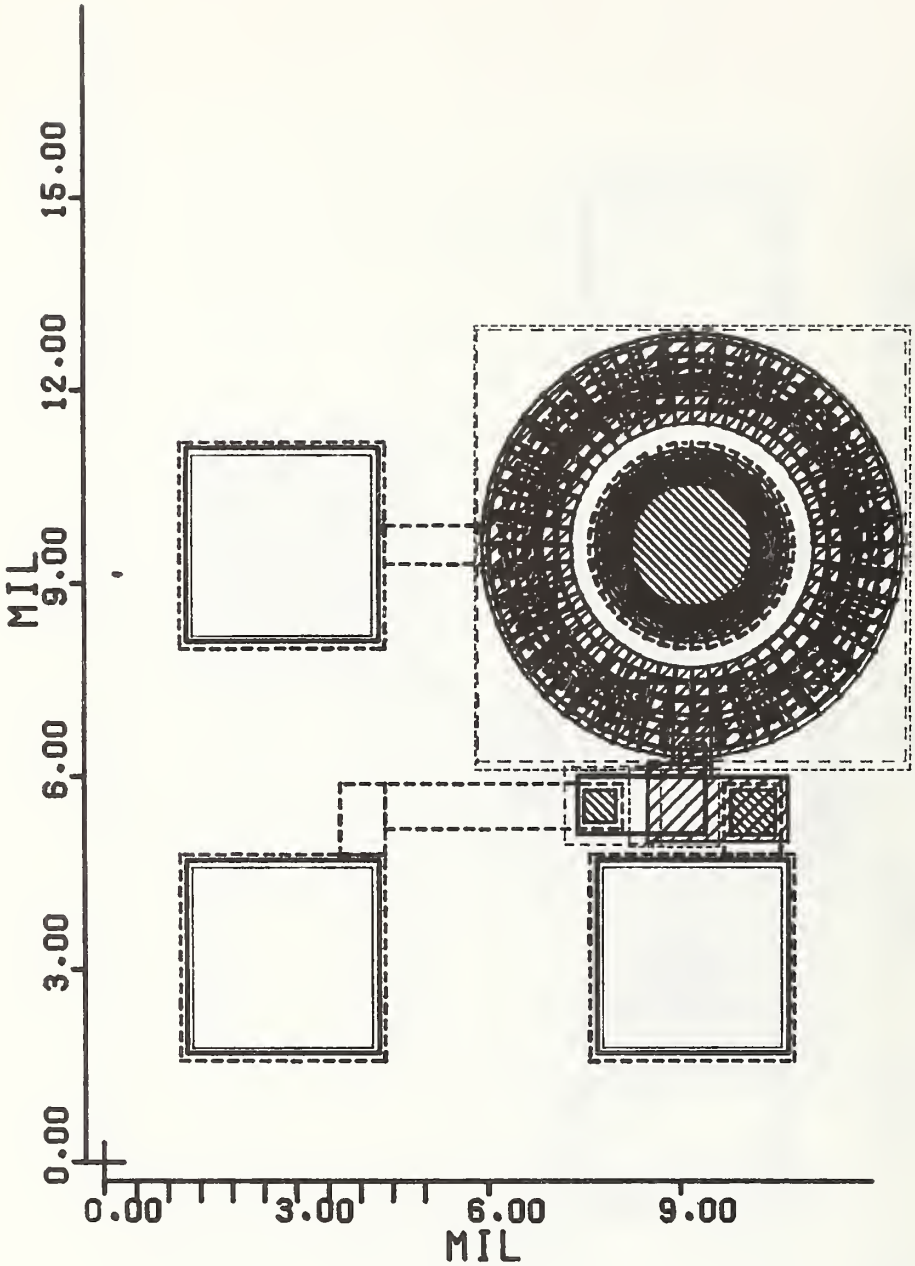


Figure B-11. Closed geometry gated diode.

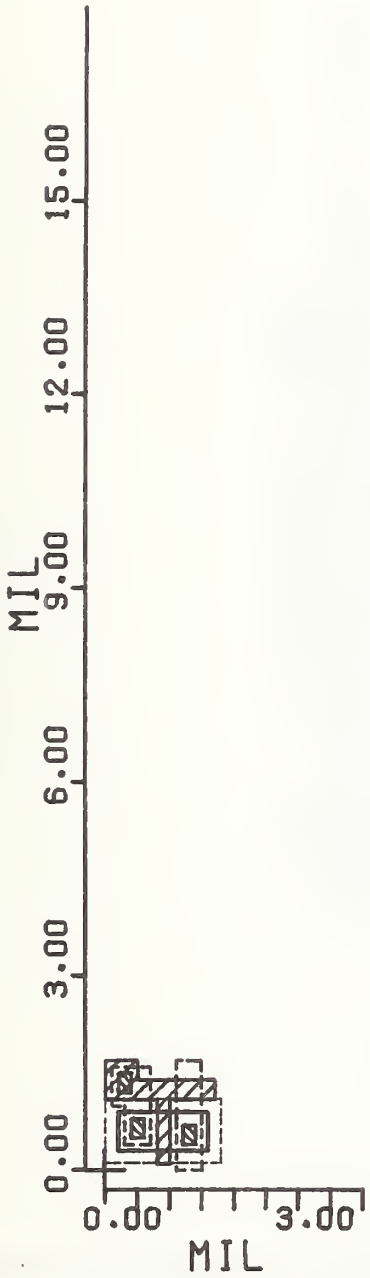


Figure B-12. Two-terminal MOSFET.

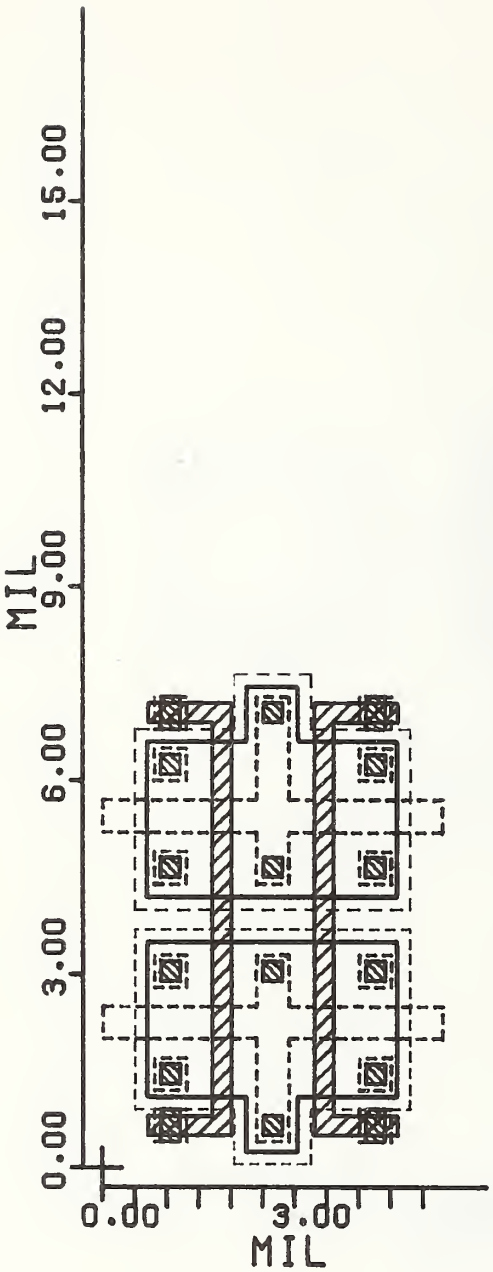


Figure B-13. Internal cell from RCA Gate Universal Array.

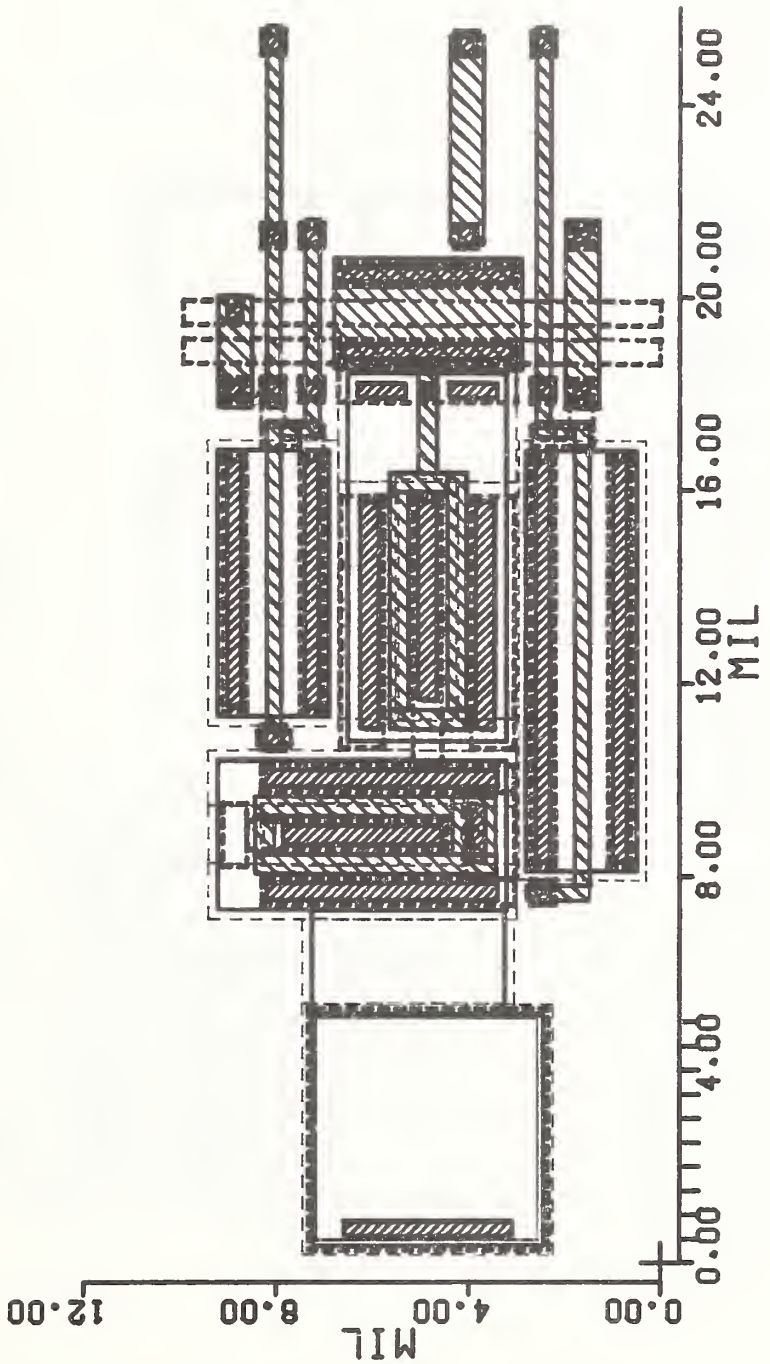


Figure B-14. Input/output cell with input protection from RCA GUA.

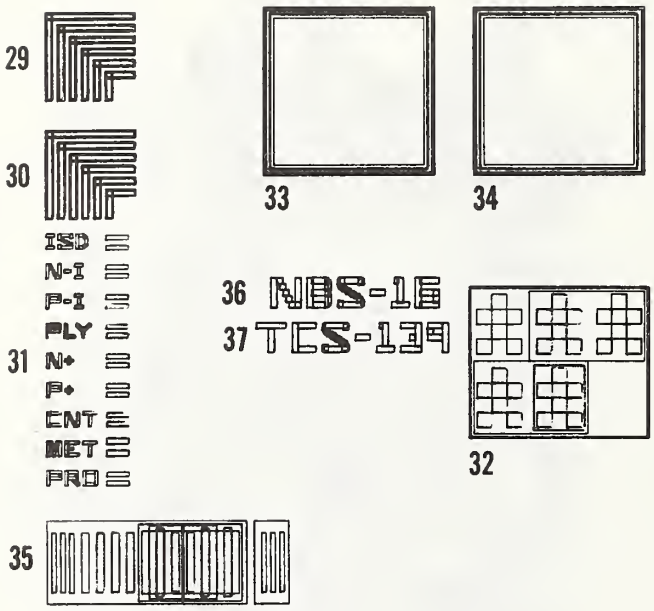


Figure B-15. NBS-16 physical analysis pattern.

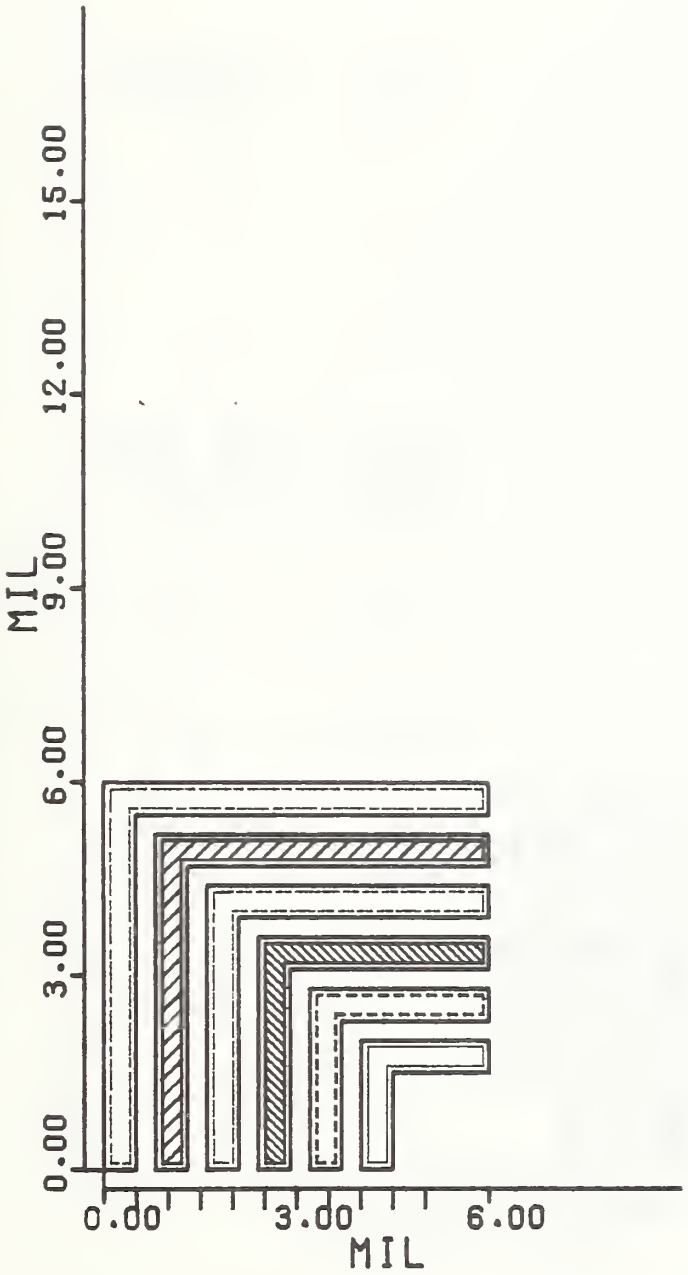


Figure B-16. Light-field RCA alignment marks.

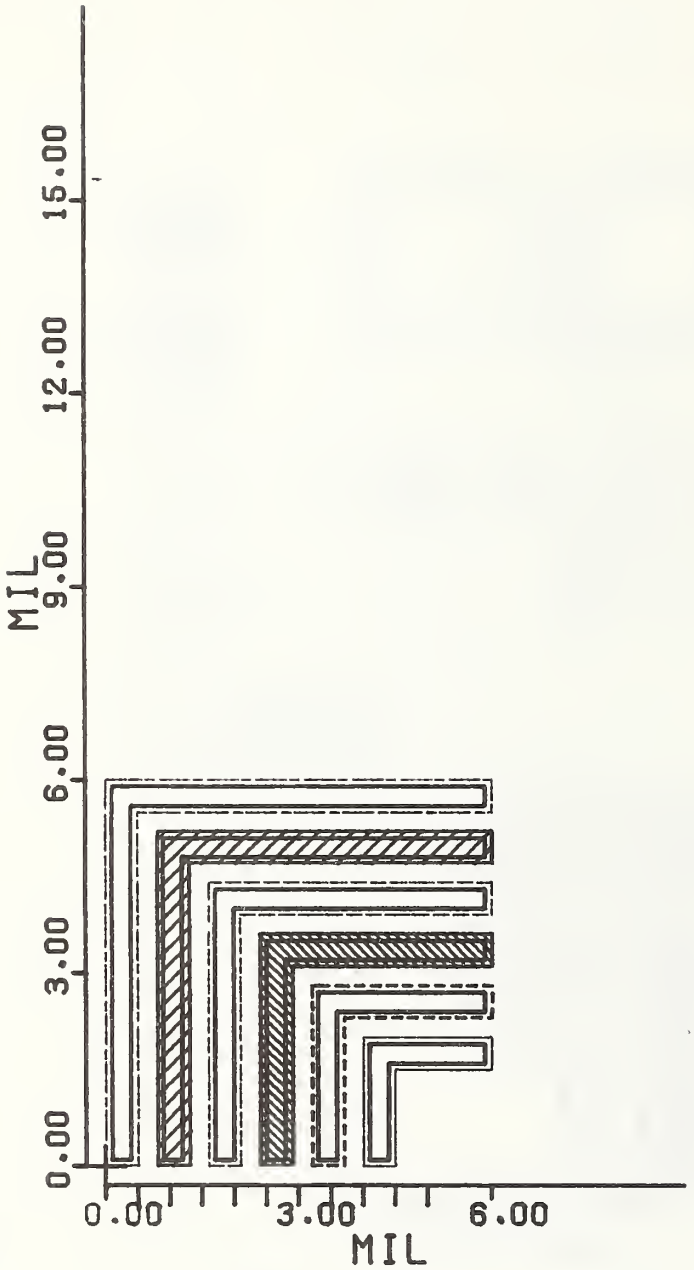


Figure B-17. Dark-field RCA alignment marks.

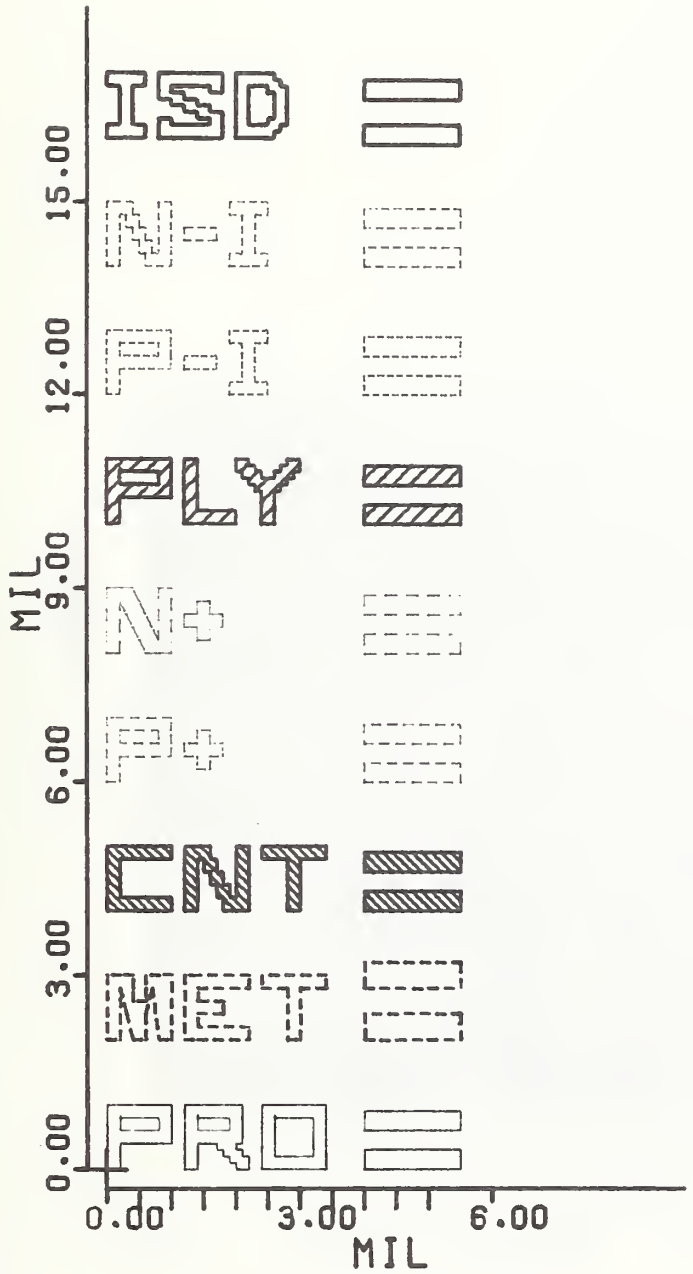


Figure B-18. Mask level designators and critical dimension structures.

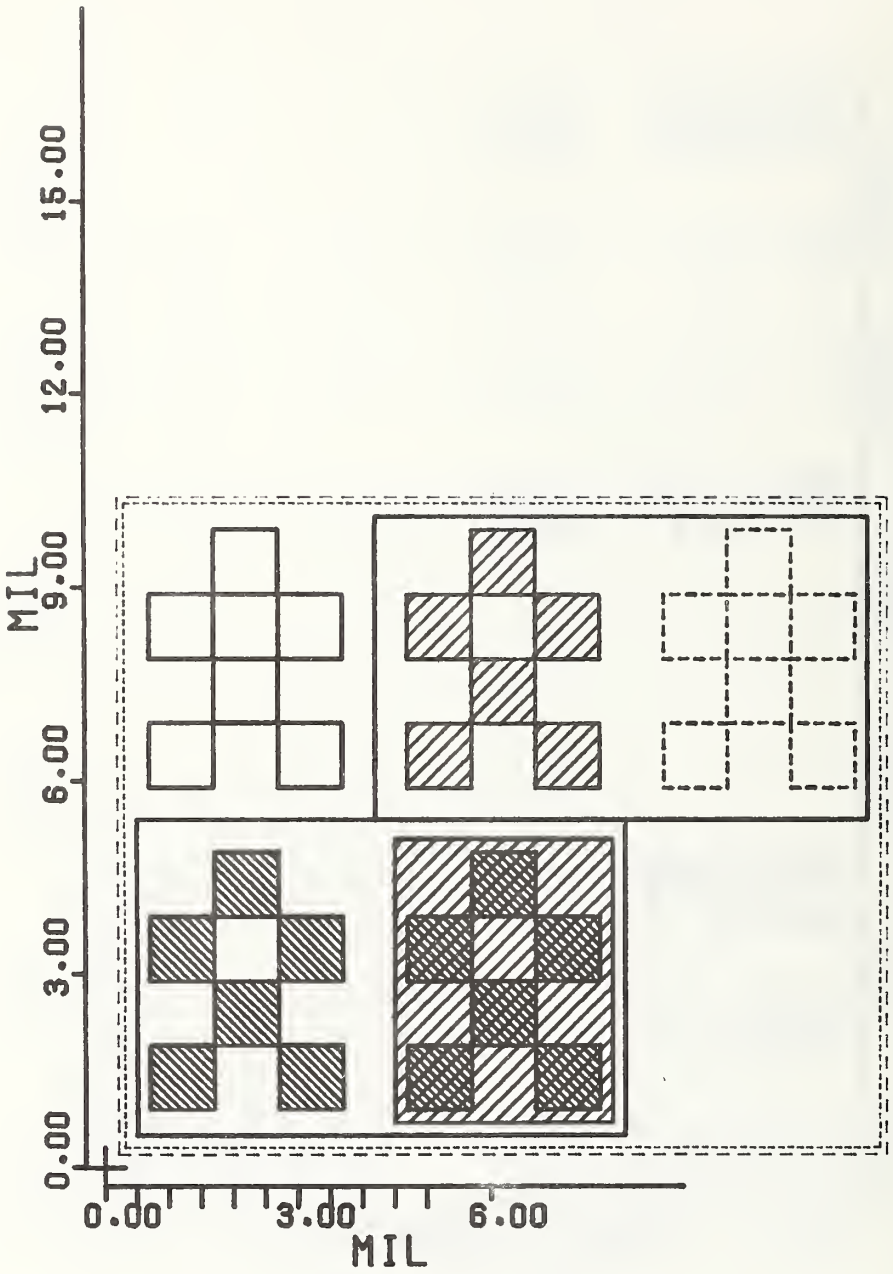


Figure B-19. Overetch structure.

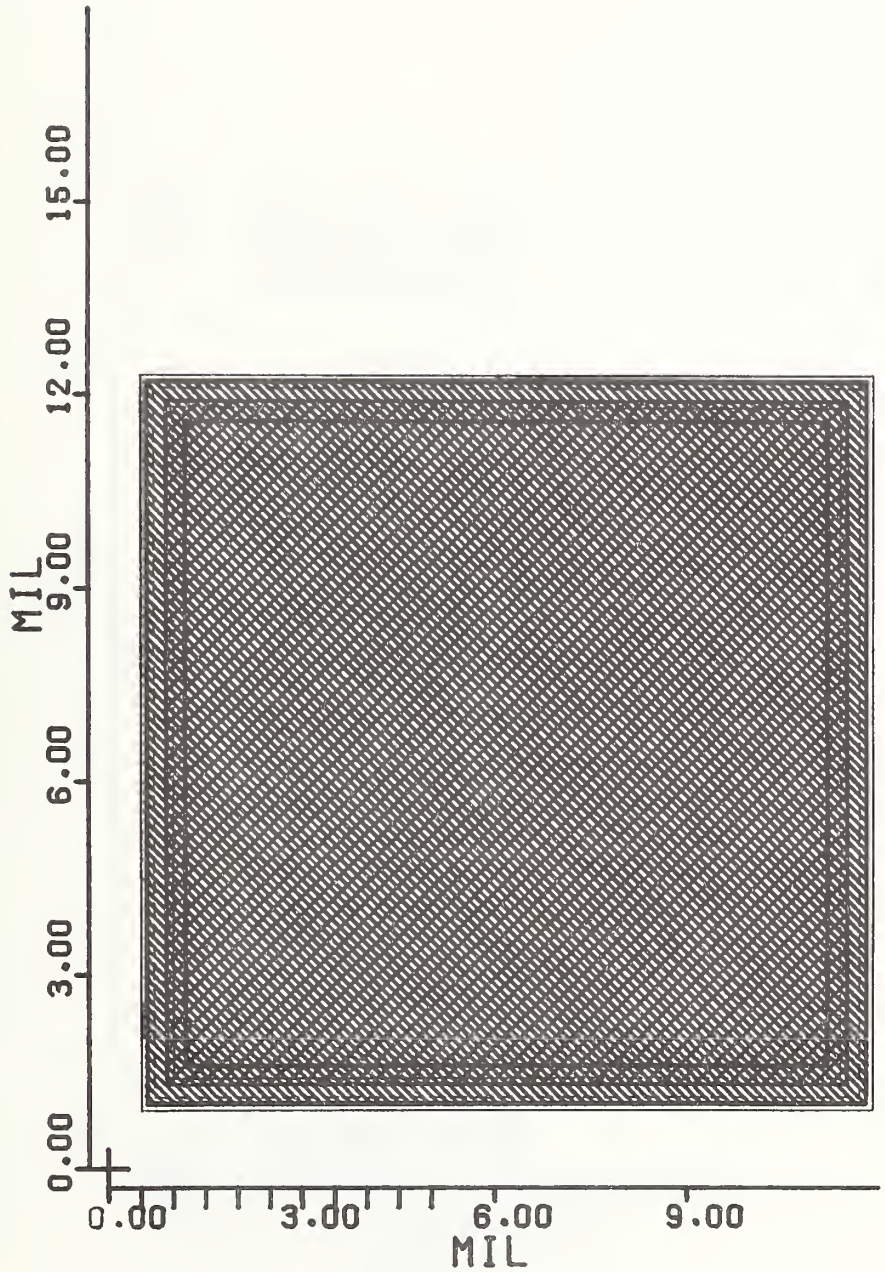


Figure B-20. SIMS area.

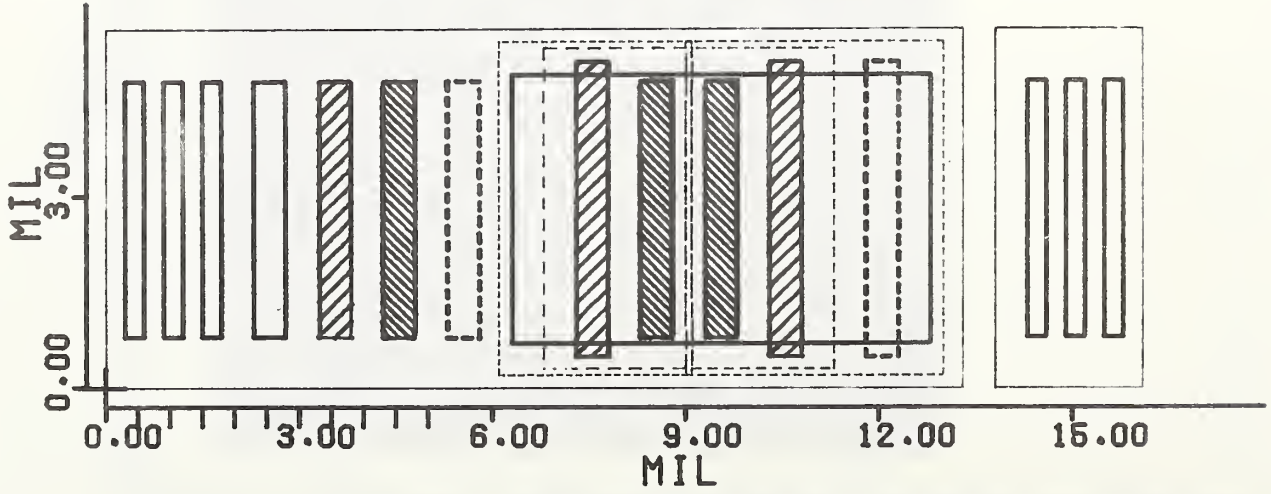


Figure B-21. Surface profilometer.

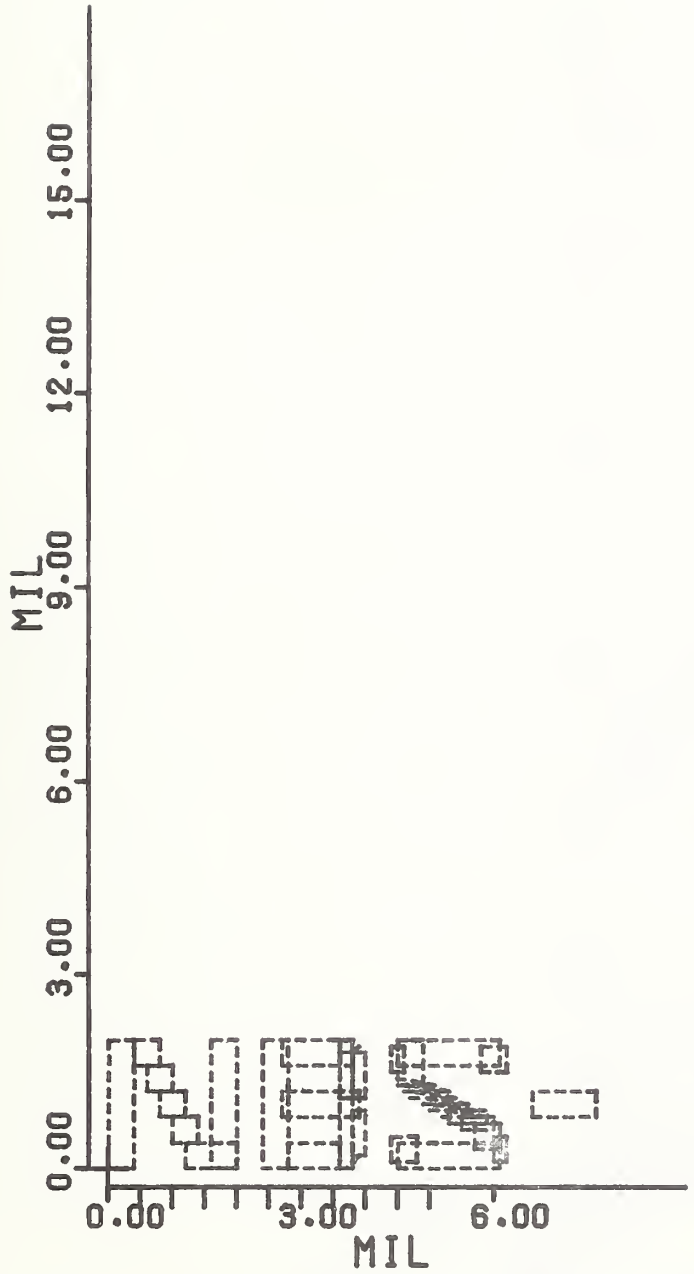


Figure B-22. Designator NBS- .

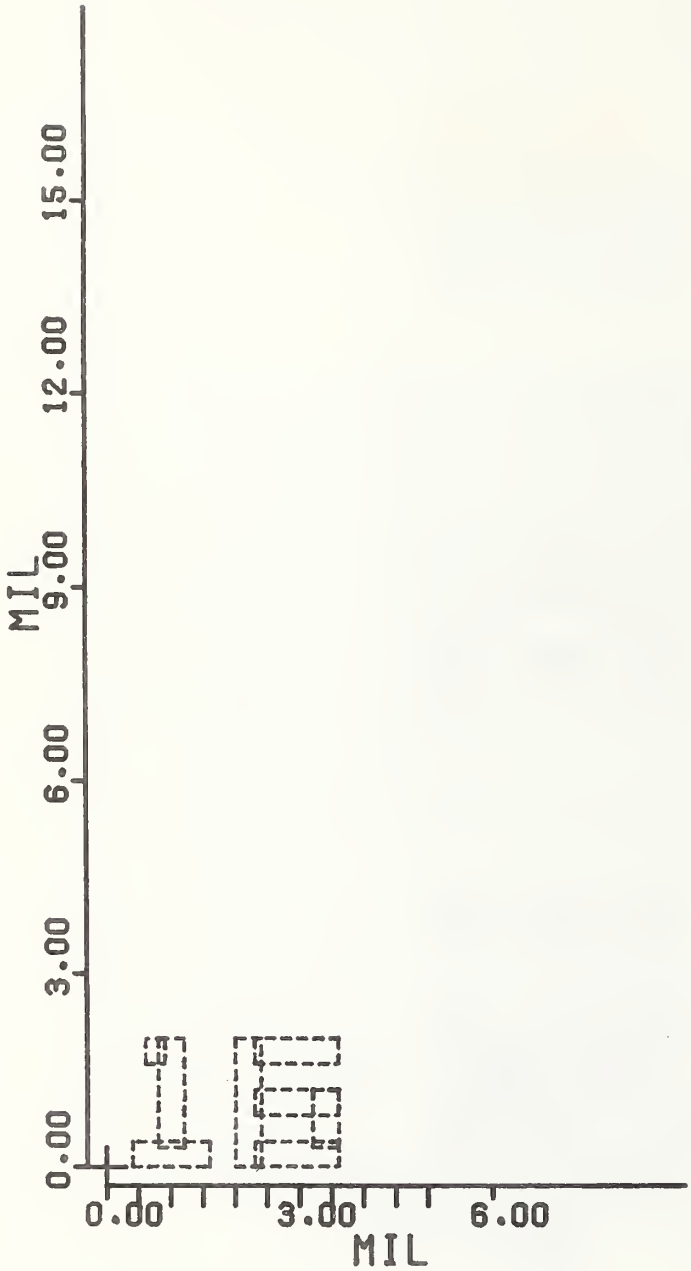


Figure B-23. Designator 16.

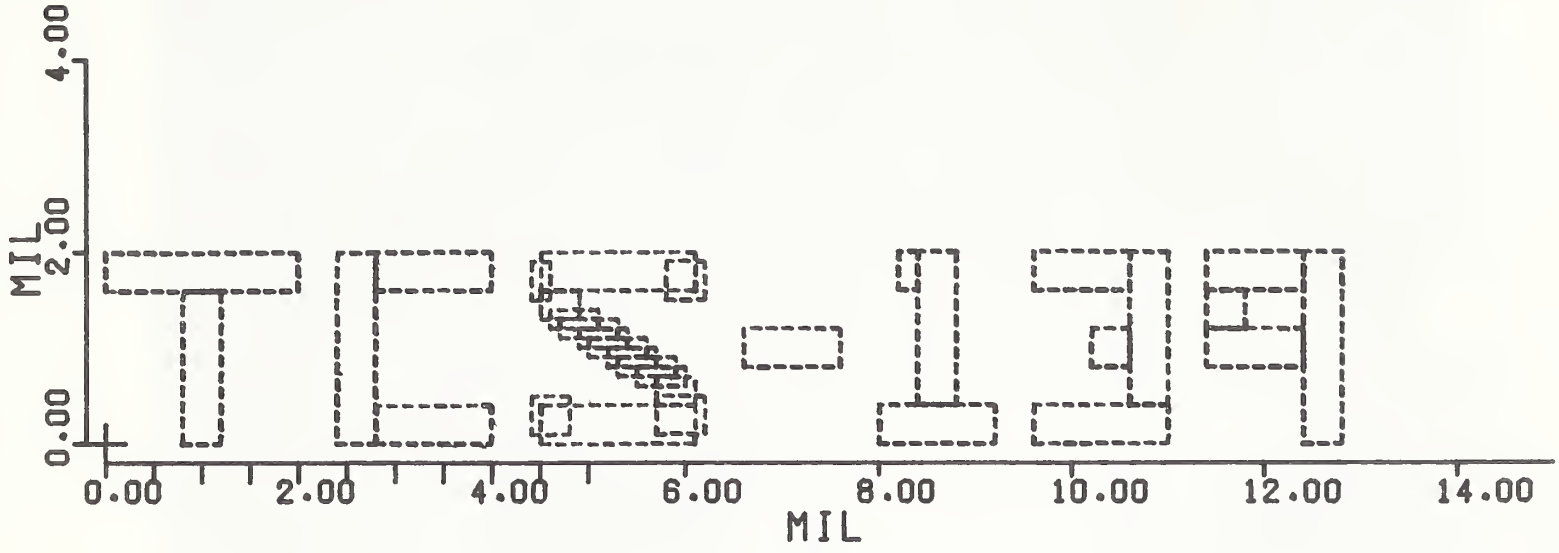


Figure B-24. Designator TCS-139.

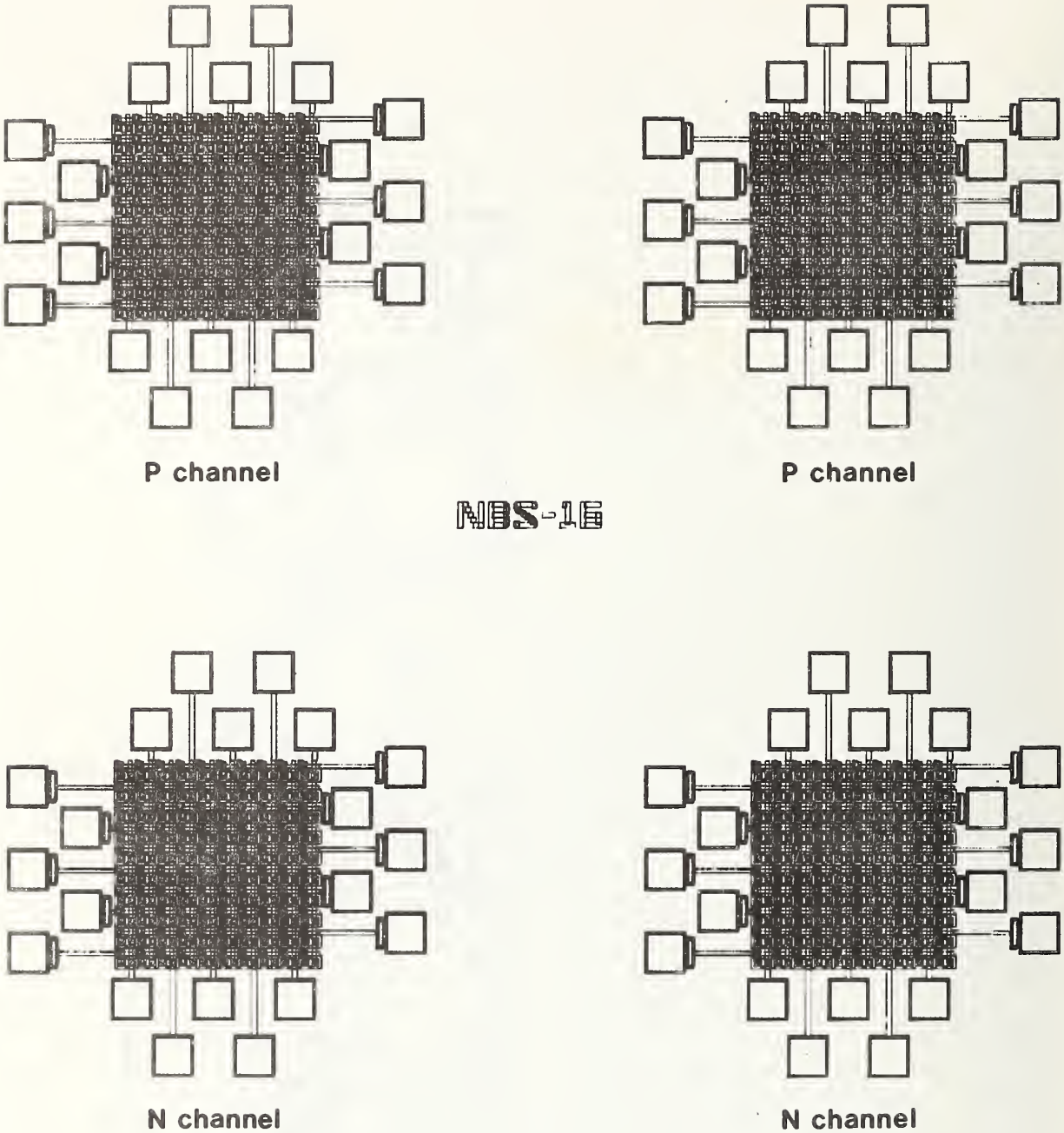


Figure B-25. NBS-16 random fault structure I.

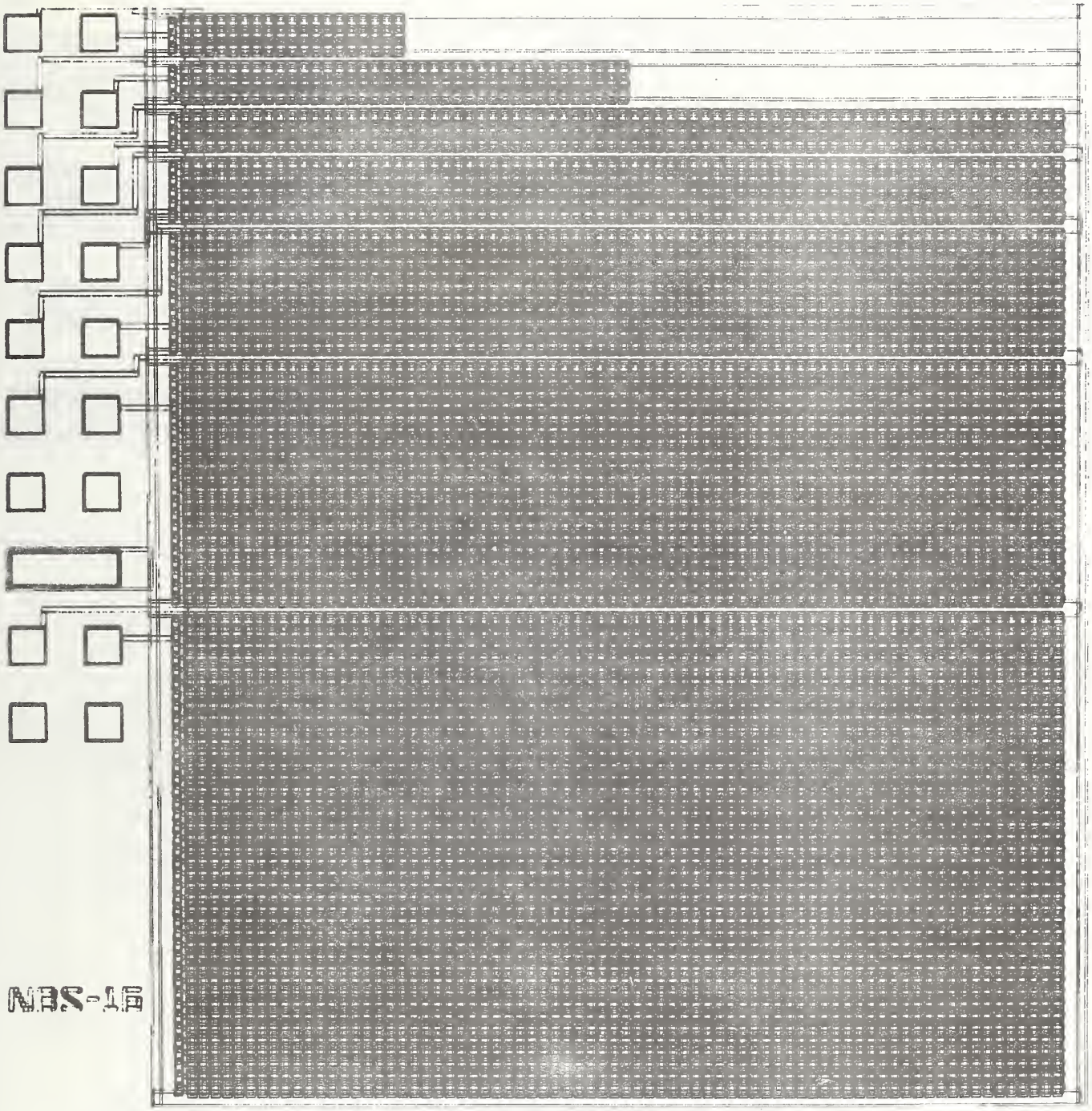


Figure B-26. NBS-16 random fault structure II.

NBS-114A (REV. 9-78)

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

The National Bureau of Standards in collaboration with the Jet Propulsion Laboratory, Pasadena, CA and RCA, Somerville, NJ, has designed a CMOS/SOS test pattern, NBS-16, and the necessary measurement techniques. RCA is required to process one test pattern wafer with each CMOS/SOS wafer lot being fabricated for the radiation hardened microprocessor chip set. Each test pattern is to be tested at NBS and JPL and recommendations for improvements made to the Air Force Avionics Laboratory (AFAL), the Air Force Materials Laboratory (AFML), and RCA. A second generation test pattern will be designed later based on information and experience obtained from the first. To date, the NBS-16 test pattern has been designed, a pattern generator tape has been delivered to RCA, and the testing hardware and software has been developed. A program schedule and a description and illustration of each test structure are found in the appendices.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

CMOS/SOS; process control; process metrology; silicon gate; test patterns; test structures.

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