NIST

National Institute of Standards and Technology

Technology Administration

U.S. Department of Commerce

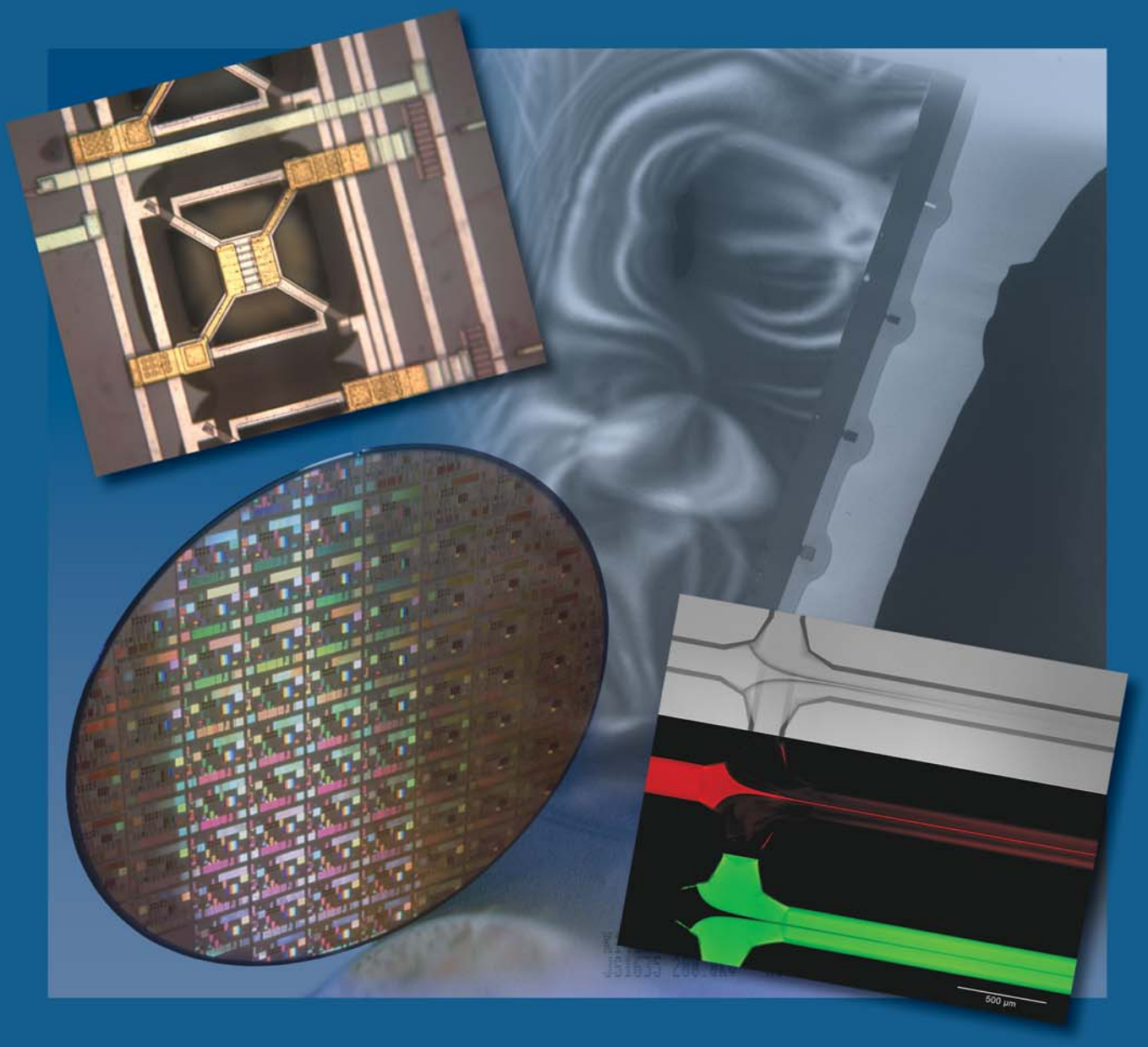
NISTIR 7181

January 2005

Electronics and Electrical Engineering Laboratory

Semiconductor Electronics Division

Programs, Activities, and Accomplishments



The Electronics and Electrical Engineering Laboratory

One of NIST's seven Measurement and Standards Laboratories, EEEL conducts research, provides measurement services, and helps set standards in support of: the fundamental electronic technologies of semiconductors, magnetics, and superconductors; information and communications technologies, such as fiber optics, photonics, microwaves, electronic displays, and electronics manufacturing supply chain collaboration; forensics and security measurement instrumentation; fundamental and practical physical standards and measurement services for electrical quantities; maintaining the quality and integrity of electrical power systems; and the development of nanoscale and microelectromechanical devices. EEEL provides support to law enforcement, corrections, and criminal justice agencies, including homeland security.

EEEL consists of four programmatic divisions and two matrix-managed offices:

Semiconductor Electronics Division

Optoelectronics Division

Quantum Electrical Metrology Division

Electromagnetics Division

Office of Microelectronics Programs

Office of Law Enforcement Standards

This document describes the technical programs of the Semiconductor Electronics Division. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220, On the Web: www.eeel.nist.gov

Cover caption: (clockwise from lower left) an IBM 200 mm EDRAM Wafer (photo by Tom Way, courtesy of International Business Machines Corporation, unauthorized use not permitted); a CMOS microhotplate-based conductance-type gas sensor; an HRTEM cross section of a structure, showing four of the six reference features, optimized for calibration to the structure's silicon lattice; and fluorescence images of a microfluidic device.

Electronics and Electrical Engineering Laboratory

Semiconductor Electronics Division

Programs, Activities, and Accomplishments

NISTIR 7181

January 2005

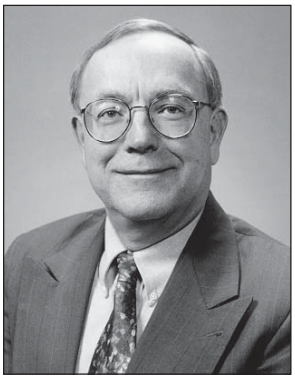
U.S. DEPARTMENT OF COMMERCE
Donald L. Evans, Secretary

Technology Administration
Phillip J. Bond, Under Secretary for Technology

National Institute of Standards and Technology
Hratch G. Semerjian, Acting Director

Any mention of commercial products is for information only; it does not imply recommendation or endorsement by the National Institute of Standards and Technology nor does it imply that the products mentioned are necessarily the best available for the purpose.

Contents



David G. Seiler,
Division Chief

"Industry views SED's contributions as unique and essential to efficiently providing measurement techniques and standards."

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

Welcome

The Semiconductor Electronics Division (SED) provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness. It provides necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary mission of the Division is to provide the measurement infrastructure to U.S. industry for mainstream silicon CMOS (complementary metal-oxide semiconductor) technology. The Division's programs also respond to industry measurement needs related to MicroElectroMechanical Systems (MEMS), power electronics, and various sub-areas of nanotechnology including nanoelectronics, nanocharacterization, nanobiotechnology, and plastic electronics.

The Division has extensive interactions with individual companies, industry organizations, and professional societies; these activities enable the development of a research agenda responsive to the needs of industry. Active participation in industry roadmapping, such as the Semiconductor Industry Association's International Technology Roadmap for Semiconductors, and standards activities, such as committee work for the American Society for Testing and Materials, is practiced by the Division to prioritize and establish programs with the highest potential impact. The Division widely disseminates the results of its research, especially in the areas of standardized test methods and Standard Reference Materials (SRMs), through a variety of channels: publications, software, conferences and workshops, and participation in standards organizations and consortia. The Division also actively seeks industrial, academic, and non-profit research partners to work with collaboratively on projects of mutual benefit.

The Division, with a staff of about 80 including full-time and part-time employees as well as guest researchers, post-doctoral associates, and contractors, is based in Gaithersburg, Maryland. The Division is one of four divisions within the Electronics and Electrical Engineering Laboratory at NIST. The Division's technical activities are organized into three groups: the Enabling Devices and ICs Group, the CMOS and Novel Devices Group, and the Electronic Information Group. The Division assists industry by providing tools such as SRMs, test chips, standard reference data, and software that support the needed measurement infrastructure. Division personnel visit industrial sites, host a variety of visitors, and make available tutorial material on an as-needed basis. We also are active in conference and workshop activities that directly benefit the industry.

A broad array of activities that serve the semiconductor industry is currently underway in the Division. The staff of the SED addresses projects ranging from materials qualification to test structures for integrated circuits. Some of these projects are supported by the NIST National Semiconductor Metrology Program (NSMP), which is managed by the Electronics and Electrical Engineering Laboratory's Office of Microelectronics Programs. For more information on the NSMP, please visit their Web site at www.eeel.nist.gov/omp.

The Division, in cooperation with the National Research Council (NRC), offers competitive awards for post-doctoral research for U.S. citizens in a variety of technical fields related to the semiconductor electronics industry. For additional details, including field descriptions and qualification guidelines, please see page 42.

The technical programs, their goals, technical strategies, activities, and accomplishments described here for each Division project clearly demonstrate the impact of the SED's leadership and effective service as it continues to respond to the needs of industry and to contribute to the scientific and engineering communities.

Please take an opportunity to visit our Division website at www.eeel.nist.gov/812/. In addition to providing further details on our Division and up-to-date project information, our website has interactive tutorials on the Hall effect (www.eeel.nist.gov/812/hall.html) and MEMS standard test structures based on e-standards (www.eeel.nist.gov/812/test-structures/). Please also be sure visit the Systems Integration for Manufacturing Applications website (www.nist.gov/sima) on product data exchange standards.

Thank you for your interest in our Division and its technical programs! I welcome your comments and suggestions. Feel free to e-mail me at david.seiler@nist.gov.

David G. Seiler
Division Chief

Semiconductor Electronics Division Staff

For additional information, contact:

Division/Office Telephone: 301-975-2054
Division/Office Facsimile: 301-975-6021
On the Web: www.eeel.nist.gov/812/

Mission

"The nature of the vision's purpose is not only to achieve a meaningful strategic or company goal, but also to build a dedicated community…"

Jay A. Conger, The Brave New World of Leadership Training, IEEE Eng. Mgmt. Review (1996)

The Semiconductor Electronics Division provides technical leadership to industry, government, and academia in research and development of the semiconductor measurement and software infrastructure needs essential to the silicon microelectronics industry, advanced semiconductor materials technologies, and advanced electronic devices based upon molecular or quantum structures.

Vision

The Semiconductor Electronics Division strives to be recognized as a dynamic, world-class resource for semiconductor measurements, data, models, software, and standards focused on enhancing U.S. technological competitiveness in the world market.

Values

The Semiconductor Electronics Division values its commitment to identify and meet crucial measurement technology needs. The Division values its collaboration with all segments of the semiconductor community. It strives for integrity, excellence, objectivity, responsiveness, and creativity, while maximizing and utilizing the potential of its employees.

Goals

The Division will:

- Aggressively pursue and achieve select metrology needs as identified in the International Technology Roadmap for Semiconductors for mainstream silicon.
- Develop new and improved process-monitoring tools, methodologies, and data for the more efficient manufacture of silicon and compound-semiconductor devices.
- Support novel research that has high potential for providing breakthroughs in materials, process, devices, and measurement technologies for the semiconductor industry.

Semiconductors: Backbone of the Electronic/Digital Revolution

For the past 20 years, the personal computer reigned supreme as the driver of semiconductor industry growth. But new leadership is emerging. The communications revolution, perhaps the defining social and economic transition of our time, is fueled by the ever smaller, ever cheaper, ever faster invention of the chip industry. The explosive demands of the wireless, broadband Internet and optical networking industries have crowned the communications chip as the dominant end market for semiconductors.

- Information technology (IT) continues to be the primary driver of the U.S. economy, and U.S. semiconductor companies are leading the charge. American chipmakers now supply nearly half of the world's chips.
- U.S. chipmakers add more value to the national economy than any other industry.
- For 50 years, the semiconductor industry has provided the bricks and mortar that built the modern world. The exciting expansion in semiconductor applications means our job has only just begun and that our industry's greatest growth lies ahead.
- Personal communications devices will become so functional as to be indispensable, cars will be safer and more fuel-efficient, the quality of education will improve, chips implanted in our bodies will tell our doctor we're sick before we register symptoms. Eventually silicon and biology will converge, and the biocomputer will seem no more novel than today's laptop. As *Forbes ASAP* Editor Michael Malone has noted, "the microprocessor is the defining invention of the electronic age, the inventor of inventions."

- adapted from the Semiconductor Industry Association (SIA) 2001 Annual Report, pp. 2–5.

"This year the semiconductor industry will manufacture about 60 million transistors for every man, woman and child on earth. By 2008, chipmakers will be producing 1 billion transistors or more per year. Transistors improve our lives in countless ways—they make cars safer and more fuel-efficient, they enable personal communication devices, they promote medical breakthroughs and they improve the quality of education."

Building Blocks for Innovation, SIA Annual Report 2002, p. 17

Semiconductors, transistors, and their applications represent one of the greatest scientific and technological breakthroughs of the twentieth century. Consider their far reaching influence on our society in general and our daily lives. Can you imagine life without them? Semiconductors are pervasive in the microelectronic components used in computers, entertainment equipment, automotive electronics, medical instrumentation, telecommunications, space technology, television, radio, cell phones, and many other information technologies. Every hospital, school, factory, car, airplane, office, bank, and household contains transistors, microprocessors, and other semiconductor devices.

These breakthroughs are possible because of the miniaturization of the transistor dimensions, which allows the construction of compact systems with tremendous computing power and memory. Miniaturization, in turn, is possible because of the perfection of fabrication techniques that allow the *integration* of circuits and thus the production of chips containing millions of elements per square centimeter. The foundation stone of this complex technology is silicon. Meeting the demands for these large-scale, complex, integrated circuits (ICs) continues to require technological advances in materials, processing, circuit design, characterization, testing, and standards.

The semiconductor electronics industry is outstripping the measurement capability needed for maintaining and improving U.S. international competitiveness. Important factors affected include product performance, price, quality, compatibility, and time to market. The Semiconductor Electronics Division provides the measurement capability needed to support the efforts of U.S. industry to improve its competitiveness. In order to support this effort, the Division also engages in technology development and fundamental research, making the findings available to industry.

The Division focuses the largest part of its resources on the development and delivery of measurement capability for two principal reasons: measurement capability has a very high impact on U.S. industry because it helps manufacturers address many of the challenges they face in realizing competitive products in the marketplace, and NIST is the official lead U.S. Government agency for measurements.

The Division focuses on developing measurement capability that is beyond the reach of the broad range of individual companies. Companies seek NIST's help for several reasons:

"Another success occurred in the development of standards for measuring the shrinking line widths that characterize semiconductor products. Because industry alone cannot develop these new standards of measurement, the National Institute of Standards and Technology (NIST) is overseeing the process."

SIA Annual Report 2004, p. 30.

- The companies need NIST's special technical capability for measurement development.
- The companies need NIST's acknowledged impartiality for diagnosing a measurement problem affecting the industry broadly or for achieving adoption of a solution across the industry.
- The companies cannot develop the measurement capability needed by the industry broadly because they cannot individually capture the returns of the cost of development.
- Industry's quality standards require that key measurements be traceable to the national measurement reference standards that NIST maintains. This is a requirement of growing importance in export markets.

The Division continues to interact and collaborate with a wide variety of companies, consortia [such as International Semiconductor Manufacturing Technology (ISMT), Semiconductor Equipment and Materials International (SEMI), and the Semiconductor Research Corporation (SRC)], academia, and other government labs to accomplish its mission. Specific details are given in the project descriptions that follow. Work in the Division results in extensive outputs or deliverables that cover knowledge and improvements in physical understanding, test methods and measurements, Standard Reference Materials (SRMs), Standard Reference Data (SRD) sets, standards, test structures and test chips, software, measurement accuracy and traceability, publications and reports, patents and Cooperative Research and Development Agreements (CRADAs), round robins, data and models, talks and short courses, company visits, conferences and workshops, consortia participation, and various activities and leadership roles on committees and working groups.

Division staff serve the semiconductor community in leadership roles on standards committees such as American Society for Testing and Materials (ASTM) and Electronic Industries Alliance (EIA) / Joint Electron Device Engineering Council (JEDEC), societies such as IEEE, ECS, and APS, and numerous semiconductor conferences/workshops. Many test methods and standards have been developed and written over the years by NIST staff for ASTM and EIA/JEDEC, including ones for resistivity, oxygen in silicon, thin dielectrics, electromigration, and device characterization. Staff serve on various Technical Working Groups to help put together the International Technology Roadmap for Semiconductors (ITRS). These groups are Process Integration, Devices, and Structures; Assembly and Packaging; Lithography; Interconnect; Front End Processes; and RF and Analog Mixed Signal. The ITRS provides targets for equipment, material, and software suppliers; provides targets for researchers; and serves as a common reference for the semiconductor industry.

The Division also has impacted the semiconductor community by producing a number of SRMs. To date, over 2,800 SRMs have been sold and distributed for resistivity, oxygen in silicon, and optical thickness by ellipsometry. Hundreds of companies throughout the world have purchased these SRMs to maintain and improve their measurement capabilities.

For the future, the Division has identified nanotechnology and its various sub-areas, including nanoelectronics, nanocharacterization, nanobiotechnology, and plastic electronics, as emerging areas of research to address.

> "The semiconductor industry is rapidly reaching a point in its evolution where its ability to build smaller nodes will encounter serious difficulties in the form of quantum effects and atomic level statistical fluctuations … nanotechnology will both help keep CMOS scaling on track *and* enable new materials/technology platforms that satisfy market needs better than CMOS … as current lithography methods reach their limit, the tools used in the development, manufacture, and testing of CMOS will increasingly be based on nanotechnology."
>
> *- from L. Gasman, "Why Nanotechnology Is So Important for the Semiconductor Industry," NanoMarkets White Paper, p. 2.*

Semiconductor Electronics Division Organization

Division Office (812.00)

2054 SEILER, David G., Chief
2054 GUARIGLIA, Lori A., Secretary
4514 COOK, Sharon W., AO
2079 BENNETT, Herbert S., NIST Fellow
2097 HARMAN, George G., Scientist Emeritus
2050 SECULA, Erik M., Editor

Enabling Devices and ICs Group (812.05)

2068 BLACKBURN, David L. (GL)
2052 WILKES, Jane, Secretary

Electrical Test Structure Metrology

2072 CRESSWELL, Michael W. (PL)
5026 ALLEN, Richard A.
8193 MURABITO, Christine E.
2234 SCHAFFT, Harry A. (CNR)
2182 YARIMBIYIK, Emre (GR)

Metrology for System-on-a-Chip

2071 HEFNER, Allen R., Jr. (PL)
5420 AFRIDI, Muhammad Y. (CNR)
2069 BERNING, David W.
2236 ELLENWOOD, Colleen E.
5484 GEIST, Jon (CNR)
6757 SALCEDO, Javier (GR)
6757 VARMA, Ankush (GR)

Power Device and Thermal Metrology

2071 HEFNER, Allen R., Jr. (PL)
8777 AKUFFO, Adwoa (CNR)
2081 DUONG, Tam (CNR)
2236 ELLENWOOD, Colleen E.
8776 HERNANDEZ, Madelaine (CNR)

MicroElectroMechanical Systems

2070 GAITAN, Michael (PL)
5484 GEIST, Jon (CNR)
4796 HONG, Jennifer (CNR)
4739 HUANG, John (S)
4710 JAHN, Andreas (GR)
4110 MacARTHUR, Daniel (S)
2049 MARSHALL, Janet C.
2052 McGRAY, Craig (PD)
6367 MIJARES, Geraldine I.
2045 MORGAN, Nicole (PD)
2492 NABLO, Brian (PD)
6347 POLK, Brian
5466 REYES-HERNANDEZ, Darwin
2305 SHAH, Jayna (GR)
3095 SUNDARESAN, Siddarth (GR)

Wire Bonding to Cu/Low-κ Semiconductor Devices (FA)

2097 HARMAN, George G. (FL)

CMOS and Novel Devices Group (812.06)

4723 VOGEL, Eric M. (GL)
2053 St. CLAIR, Melissa, Secretary

Nanoelectronic Device Metrology

2082 RICHTER, Curt A. (PL)
2078 EDELSTEIN, Monica D.
2233 HACKER, Christina
2087 KIRILLOV, Oleg
8755 KOO, Sang-Mo (GR)
3241 LI, Qiliang (CNR)
5291 RAMACHANDRAN, Ganesh (CNR)
2247 SUEHLE, John S.
4723 VOGEL, Eric M.
3377 WANG, Wenyong

Electronic Materials Characterization

2089 KOPANSKI, Joseph J. (PL)
5974 AMIRTHARAJ, Paul (GR)
2084 CHANDLER-HOROWITZ, Deane
2060 EHRSTEIN, James R.
2088 JELIAZKOV, Stoyan (CNR)
3241 LITTLER, Chris (GR)
2044 NGUYEN, Nhan V.
2048 PARK, Seong Eun (GR)
2067 THURBER, W. Robert (GR)

Advanced MOS Device Reliability and Characterization

2247 SUEHLE, John S. (PL)
2078 EDELSTEIN, Monica D.
8687 HEH, Da-Wei (GR)
8755 KOO, Sang-Mo (GR)
4723 VOGEL, Eric M.
2111 ZHU, Baozhong (GR)

Theoretical Solid-State Physics for Semiconductors (FA)

2079 BENNETT, Herbert S. (FL)

Legend:

AO = Administrative Officer
CNR = Contractor
FA = Focus Area
FL = Focus Area Leader
FM = Facility Manager
GL = Group Leader
GR = Guest Researcher
PD = PostDoctoral Appointment
PL = Project Leader
S = Student

Telephone numbers are: (301) 975-XXXX (replace XXXX with the four-digit extension as indicated)

NIST AML Nanofabrication Facility & SED Microfabrication Facility

2699 HAJDAJ, Russell (FM)
2242 BUCK, Laurence M.
5623 OWEN, James C.
2095 KESWANI, Vinay (CNR)
2096 ROPPOLO, Richard

Electronic Information Group (812.07)

3644 BRADY, Kevin G. (GL)
2053 St. CLAIR, Melissa, Secretary

Infrastructure for Integrated Electronics Design and Manufacturing

4284 MESSINA, John (PL)
8778 ARONOFF, Matthew
4951 BABOUD, Julien (GR)
5108 BERTON, Dominique (GR)
3644 BRADY, Kevin G.
4229 DEVAULX, Frederic (GR)
2432 GRIESSER, Art
8581 KHALILI, Neda (S)
3263 KOSTICK, Jennifer A.
5319 LI, Ya-Shian
3246 MOORE, David (GR)
3956 SIMMON, Eric
5319 SMITH, Nathan (S)

Knowledge Facilitation

3263 KOSTICK, Jennifer A. (PL)
4479 MEYER, Mariana (S)
8747 NEWTON, Meridel (S)

Legend:

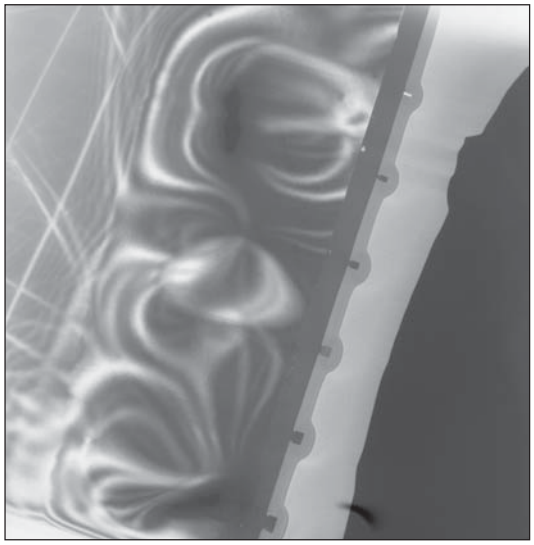
AO = Administrative Officer
CNR = Contractor
FA = Focus Area
FL = Focus Area Leader
FM = Facility Manager
GL = Group Leader
GR = Guest Researcher
PD = PostDoctoral Appointment
PL = Project Leader
S = Student

Telephone numbers are: (301) 975-XXXX (replace XXXX with the four-digit extension as indicated)

Electrical Test Structure Metrology

Goals

Develop test-structure based metrology utilizing electrical and other techniques: characterize the efficacy of interconnect materials, with emphasis on ultra-high-density copper interconnects; apply MEMS-based silicon-patterning techniques to the fabrication of test structures for critical dimension (CD) and overlay extraction by optical, electrical, or other methods; and contribute to standards organizations supporting the extension of metrology standards to copper interconnect.



HRTEM cross section of a CD test structure, comprised of six reference features optimized for calibration to the structure's silicon lattice.

Customer Needs

In order to meet new clock-frequency demands, research by the semiconductor industry has focused on lower-resistance interconnect materials. The primary material replacing aluminum as an interconnect material is copper because of its nominally low resistance properties and its improved reliability characteristics. For example, Intel's most-recently announced fabrication process will feature transistors having 35 nm gate length, which will be the smallest and highest-performing complementary metal oxide semiconductor (CMOS) transistors in high-volume production. The process integrates eight copper interconnect layers that increase the signal speed inside the chip and reduce chip power consumption. Intel will continue to use copper interconnects for several more technology nodes. However, there is concern that the projected benefits of copper may not map into interconnect features with dimensions projected by the International Technology Roadmap for Semiconductors (ITRS) because relatively little research has been reported on the limiting physics of electron transport in ultra-narrow metal conductors.

Interconnect fabrication processes involve a sequence of up to several tens of lithographic operations, each requiring close alignment of the patterned resist to features that have been etched after the previous such operation. Successful manufacturing typically requires alignment accuracies in the low several nanometers range. The demand for accurate alignment is increasingly challenging not only for the lithographic tool manufacturers and users, but also for the metrologists contributing to the process-control infrastructure. For example, the ITRS, which specifies the overlay requirements for each technology node (DRAM half-pitch), specifies 3.3 nm for the 2005 / 90 nm node decreasing to 1.6 nm for the 2010 / 45 nm node. Thus the metrology challenge to which this project proposes to contribute is the verification of metrology tool performance. Overlay quality is the closeness to zero of the overlay vector, which traditionally has been measured by optical metrology tools. At earlier lithography nodes, these tools have performed adequately. However, at smaller lithography nodes, corrections called shifts have increased in size relative to the measured overlay. These shifts are extracted from the wafer-tool interaction and applied to local measurements of the overlay vector. As design rules have further decreased to the sub-tenth micrometer region, a new challenge has arisen from the fact that the metrology is fundamentally optical in nature. In general, the local value of the measured optical overlay, even when corrected for shifts, does not adequately match the local value of the interconnect system's performance. The problem is that *electrical* overlay is the functionally relevant quantity from the viewpoint of circuit performance. We plan to use a test structure patented by project staff that provides the relationship between the optically-extracted overlay and the electrical overlay thereby enabling established overlay metrology tooling to be applied to the latest generations of scaled interconnect systems.

The emerging metrology known as optical-diffraction process (ODP) control scatterometry translates broadband light, diffracted from an on-wafer grating patterned into the resist or film, into

Technical Contact:
Michael W. Cresswell

Staff-Years (FY 2004):
3.5 professionals
1.5 guest researchers

accurate profiles of the grating's features from which key parameters, such as CD, can be extracted. Whereas currently favored metrology tools such as CD scanning electron microscopes require a vacuum wafer environment, optical scatterometry does not and is fast and non-invasive. The possibilities of ODP extend to characterizing the sidewall angle and height of critical features. Until physical standards are available, the full promise of ODP control scatterometry may not be met.

The ITRS has warned that the photomask industry is beginning to trail the requirements of the semiconductor manufacturers, especially with regard to CD metrology. Co-development of an adequate photomask CD-metrology infrastructure is essential to support the technical and manufacturing needs of optical lithography below 100 nm. At the present time, there is no established technique that meets the stated requirements. Optical transmission microscopy has been the primary metrology method used by photomask makers and has the advantage of traceability, but this technique is not readily available to photomask users. Whereas International SEMATECH (ISMT) is developing an atomic force microscopy (AFM) implementation through the use of carbon nanotubes as robust measurement tips, this approach could prove costly and may be fundamentally too slow for full-mask inspection. In addition, AFM is inherently slow and requires contacting the surface of the photomask, which can be a cause of contamination. Scanning electron microscopy (SEM), although increasingly used for CD measurements on photomasks, is limited by charging of the quartz substrate. On the other hand, electrical metrology has no known lower CD limits and could be contamination free except for the fact that it is a contact metrology with inherent particulate hazards. Interestingly, no references to scatterometry for mask CD-control have been reported, and it seems that this is one application where ODP metrology could offer unique benefits.

Technical Strategy

Challenges associated with advanced interconnect include the understanding of charge transport in very narrow features. The charge transport is affected by the interaction of the charge carriers with grain boundaries and sidewalls. When the size of either the grains or lines is significantly larger than the mean free path of the electrons, the conductivity of the wires is similar to that of bulk. However, when these dimensions are less than or equal to the mean free path, the conductivity is expected to increase significantly. There are two "features" of conventional copper interconnect systems that complicate any experiments. The first feature is the barrier layer that is needed to keep the copper from diffusing into the surrounding insulator and silicon layers. This barrier layer is usually comprised of a metal, such as tantalum, which is a poor conductor. The second feature is that the planarization in the damascene patterning process can lead to dishing or erosion, which leads to the sheet resistance being a very non-linear function of dimension. Decoupling the contributions to a measured sheet resistance of these two effects is difficult, if not impossible.

In this project, we are taking several approaches to address these issues: The first approach is to develop a model from which the sheet resistance can be calculated for an arbitrary set of dimensions, grain sizes, and scattering coefficients. The results from this model will be compared with measurements of patterned and unpatterned copper films at a range of temperatures. To simplify analysis of the material, we will initially measure copper films with no barrier layer and later extend the measurements to films with barrier layers.

A new challenge in overlay metrology is emerging as a consequence of scaling. The problem is that a planar definition of overlay does not provide for functionally relevant electrical overlay which has three-dimensional qualities. On the other hand, an electrically readable overlay test-structure has been proposed by us earlier. It requires a two-level metal interconnect process and will be the first time that the concept, for which NIST holds several patents, will have been reduced to practice. A key element of the test structure is the combination of a standard overlay frame-in-frame target, appended to an electrically testable component. The composite test structure has multiple elements, each having staggered built-in overlays. The latter's function is to enable the identification, by electrical testing, of the as-replicated cell that has zero electrical overlay, which can then be used as a calibration artifact for normal optical, SEM, or AFM metrology tools by providing corrections to such systems that are based on functionally relevant behavior of the fabricated patterns. In other words, the test structure addresses the problem that overlay extraction by optical means is challenged by the complex interaction of errors known as wafer-induced shift and tool-induced shift. It separates these errors and allows for their correction. It is fabricated on production wafers

just as are other test structures that are inspected by fabrication-line metrology tools. However, after fabrication and optical and electrical testing, it serves as a means of calibrating the optical tools that are used to monitor overlay on that particular fabrication line. Its fundamental attribute is that it enables the user to identify the critical relationship between the readings of his/her conventional optical metrology tools during inspection of product wafers and the "functionally relevant" overlay properties of the interconnect system under fabrication.

The project will incorporate a "Mask ECD" (Electrical Critical Dimension) task that would build on our previous experience working with a major U.S. mask supplier to the semiconductor industry. In that work, we devised a direct means of comparing measurements of features made on the mask with the replicated features transferred from the mask to the wafer. We plan to take this work to the implementation stage with an industry partner. In addition, we will explore the feasibility of extracting CDs from electrical test data made on an alternating aperture phase-shift mask. Other workers in test-structure metrology also have claimed that such electrical measurements have the potential to be both faster and more repeatable than optical or CD-SEM methods and provide the motivation for continued study of this approach. Two exciting extensions of mask metrology using neither SEM nor optical tools are being considered. One extension is non-contact ECD, which would draw heavily on knowledge and experience of staff in EEEL's Boulder, Colorado, site and may result in a collaborative activity exploring the development of a microwave sensor specifically for the mask-CD metrology application. The second extension to our mask CD metrology approach is scatterometry. The application of scatterometry to mask-CD metrology would provide a powerful tool for mask CD-control.

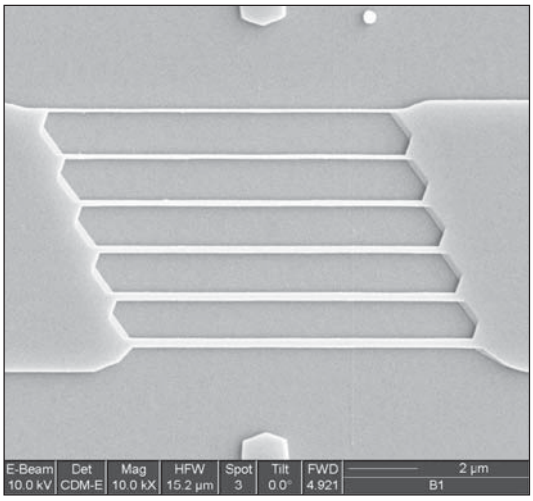
There also is a need for standards, especially related to interconnects. In this project, we will continue to participate in JEDEC and SEMI standards committees with special emphasis on those relating to interconnect reliability and process control.

DELIVERABLE: Draft and submit manuscript on surface-dominated conduction-electron scattering in copper films and patterned features. Develop process for patterning recesses in silicon wafers to accommodate patterned chips for copper-seeding, electro-deposition, and CMP planarization. Complete L-EDIT CAD for mask to facilitate comparison of CDs extracted electrically by ODP scatterometry from the same features.

DELIVERABLE: Develop process for seed-layer deposition on SCCDRM chips. Make initial electrical measurements on a selection of SCCDRM features. Prepare draft standard on ECD extraction for review by SEMI.

DELIVERABLE: Complete CMP processing of first copper-interconnect test wafers and initiate fabrication of overlay test-structure wafers. Make ECD and scatterometry-CD (probably in collaboration with a scatterometry CD tool manufacturer) measurements on scatterometry test-structures. Prepare draft of paper on modulating current through SCCDRM features by electrical or other means.

DELIVERABLE: Report on initial electrical measurements on first copper-interconnect test wafers as the latter become available from fabrication. Make ODP measurements on electrical scatterometer test structures. Complete fabrication of first lot of electrical-overlay test structures.

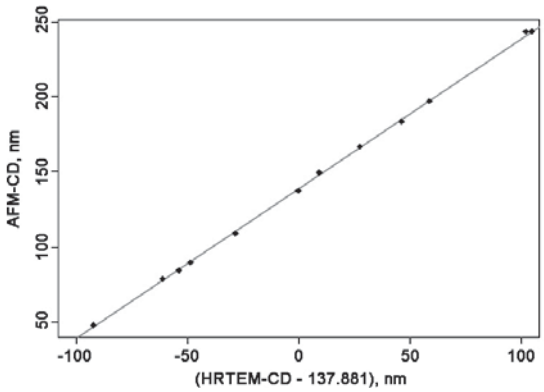


SEM image of the new test structure. (Lengths of the lines shown are approximately 10 µm, and the widths range from about 45 nm to 210 nm.)

Accomplishments

■ Delivered to ISMT, in collaboration with NIST's Manufacturing Engineering Laboratory (MEL) and Information Technology Laboratory (ITL), ISMT, and VLSI Standards, 10 chips containing NIST calibrated CD reference features. These chips, which have been distributed to ISMTs 10 member companies, including Intel, IBM, TI, AMD, and Freescale/Motorola, were delivered with sub-100 nm CDs and combined uncertainties less than 5 nm. The improvement in uncertainty resulted from the implementation of a new type of HRTEM-target test structure, the extensive use of SEM inspection to identify targets with superior CD uniformity, and the use of advanced AFM to serve as the transfer metrology. Commercialization

of these reference features is being considered by VLSI Standards.



Example of AFM transfer calibration from a single HRTEM target.

■ Introduced a new HRTEM test structure target. This target contains six features with a distribution of drawn linewidths, positioned in such a way as to allow for HRTEM measurement of all six lines from a single sample preparation process, the most time-consuming and costly part of HRTEM. HRTEM provides the essential absolute primary measurement of CD, since it is traceable to the known spacing of the lattice planes of mono-crystalline silicon. This new target is also optimized for AFM imaging which, for these chips, provided the transfer calibration since HRTEM imaging destroys the chips.

■ Developed, in collaboration with NIST's MEL and ITL, a measurement and data analysis procedure to minimize the expanded uncertainty associated with the CD reference features delivered to ISMT. The expanded uncertainty is derived statistically from the calibration function, which enables tracing the AFM measurements to the silicon lattice-plane spacing using HRTEM imaging. The previous generation of reference materials, which was delivered in 2001 and used electrical CD as the transfer calibration, had uncertainties of approximately 14 nm. The second generation units distributed to the ISMT member companies have CDs as low as 45 nm and uncertainties, based on statistical analyses performed by personnel of NIST's Statistical Engineering Division, of between 1.5 nm and 3 nm. This decrease in uncertainty is of major importance to the end-user of these reference features.

Besides the advances represented by the novel design of the described test structure, and the role played by NIST in leading the development of world-class three-dimensional AFM metrology at ISMT facilities in Austin, two other innovations were implemented to help this project-team's members achieve the remarkable reduction in CD uncertainty. The first was the installation and maintenance of a database to archive and rank several thousand SEM images of candidate features according to nanoscale CD uniformity. The second was the introduction of ultrasonically agitated patterning etches which are believed to have made at least some contribution to the feature uniformity, which in turn is essential for a low-uncertainty product. The third was devising a scheme for reliably extracting the lattice-plane counts from ultra-high-magnification electron-transmission phase-contrast images of reference features' cross sections. Finally, the contributions in statistical analysis made by our partner in ITL played a critical role in enabling us to conclude this phase of the project with such spectacular results.

■ Distributed to the ISMT member companies, as well as archiving at ISMT, a Technology-Transfer Document containing all essential details of the final phase of the SCCDRM program; its November 2004 delivery served as the completion of the SCCDRM program.

■ Participated in completion of the JEDEC JESD33B standards for measuring and using the temperature coefficient of resistance to measure the temperature of aluminum and copper interconnect lines. Participating in the revision of the JEDEC JESD87 and JEDEC JEP139 standards. Each is being revised to make them applicable to copper as well as aluminum lines.

FY Outputs

Collaborations

International SEMATECH, Development of SEM imaging and AFM CD-profile extraction

NIST ITL, Traceability statistics and procedures

NIST MEL, AFM CD-profile extraction

VLSI Standards, Substrate implant and anneal specifications, photo lithography and hard-mask engineering solutions

Accurel Systems, Design of HRTEM targets and formulation of appropriate imaging procedures

University of Edinburgh, United Kingdom, Advanced copper interconnect

Standards Committee Participation

Electrical Test Structures Task Force, Co-chair (Richard A. Allen)

SEMI International Standards Micro-lithography Committee, member (Richard A. Allen)

Recent Publications

N. Guillaume, W. K. Kahn, R. A. Allen, M. W. Cresswell, M. E. Zaghloul, "Application of Conformal Mapping Approximation Techniques: Parallel Conductors of Finite Dimensions," IEEE Transactions on Microwave Theory and Techniques, Vol. 53, No. 3, pp. 812-821 (01-JUNE-2004)

N. Guillaume, R. A. Allen, M. W. Cresswell, M. Lahti, L. W. Linholm, M. E. Zaghloul, "Non-contact Electrical CD Metrology Sensor for Chrome Photomasks Featuring a Low Temperature Co-fired Ceramic Technology," IEEE Trans. on Semiconductor Manufacturing, Vol. 17, No. 1, pp. 25-34 (01-MAY-2004)

R. A. Allen, M. W. Cresswell, L. W. Linholm, "Junction-Isolated Electrical Test Structures for Critical Dimension Calibration Standards," IEEE Trans. Semiconductor Manufacturing, Vol. 17, No. 2, pp. 79-83 (01-MAY-2004)

R. A. Allen, R. I. Patel, M. W. Cresswell, C. E. Murabito, B. Park, M. D. Edelstein, L. W. Linholm, "Recent Developments in Producing Test-structures for Use as Critical Dimension Reference Materials," ICMTS IEEE International Conference on Microelectronic Test Structures, March 22-25, 2004, Awaji, Japan, pp. 35-40 (01-MARCH-2004)

R. A. Allen, M. W. Cresswell, C. E. Murabito, R. Dixson, E.H. Bogardus, "Critical Dimension Calibration Standards for ULSI Metrology," Characterization and Metrology for ULSI Technology: 2003, International Conference on Characterization and Metrology for ULSI Technology, March 24-28, 2003, Austin, Texas, pp. 421-428 (30-SEPT.-2003)

R. A. Allen, B. A. am Ende, M. W. Cresswell, C. E. Murabito, T. J. Headley, W. F. Guthrie, L. W. Linholm, C. H. Ellenwood, E.H. Bogardus, "Test Structures for Referencing Electrical Linewidth Measurements to Silicon Lattice Parameters Using HRTEM," IEEE Transactions on Semiconductor Manufacturing, Vol. 16, No. 2, pp. 239-248 (01-MAY-2003)

R. A. Allen, M. W. Cresswell, L. W. Linholm, "Junction-Isolated Electrical Test Structures for Critical Dimension Calibration Standards," 2003 ICMTS IEEE International Conference on Microelectronic Test Structures, March 17-20, 2003, Monterey, California, pp. 3-7 (31-MARCH-2003)

J. von Hagen, H. A. Schafft, "Temperature Determination Methods on Copper Material for Highly Accelerated Electromigration Tests (*e.g.*, SWEAT)," 2002 IEEE International Integrated Reliability Workshop Final Report, 2002 Integrated Reliability Workshop, Oct. 21-24, 2002, Lake Tahoe, California, pp. 45-49 (01-FEB.-2003)

H. A. Schafft, J. R. Lloyd, "Electromigration Discussion Group Summary," 2002 IEEE International Integrated Reliability Workshop Report, 2002 IEEE International Integrated Reliability Workshop, Oct. 21-24, 2002, Lake Tahoe, California, pp. 204-206 (01-FEB.-2003)

H. A. Schafft, L. M. Head, J. Gill, T. D. Sullivan, "Early Reliability Assessment Using Deep Censoring," Microelectronics Reliability, Vol. 2003, No. 43, 16 pp. (01-JAN.-2003)

N. Guillaume, M. Lahti, M. W. Cresswell, R. A. Allen, L. W. Linholm, M. E. Zaghloul, "Non-contact Electrical Critical Dimensions Metrology Sensor for Chrome Photomasks," Proc. Intl. Soc. for Optical Engineering (SPIE), 21st Annual BACUS Symposium on Photomask Technology, Oct. 02-05, 2001, Monterey, California, Vol. 4562, pp. 822-829 (01-OCT.-2002)

Metrology for System-on-a-Chip (SoC)

Technical Contact:
Allen R. Hefner, Jr.

Staff-Years (FY 2004):
.75 professional
1.75 guest researchers

Goals

The goal of the project is to develop solutions to key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry. These include development of measurement methods and standards for characterizing embedded-sensor (ES) virtual components (ES-VCs), a critical class of building blocks from which SoCs are developed. The goal of this project is to promote and support the development of hardware and software standards for specifying ES-VCs compatible with the SoC integration methodology used for digital IC design.

This NIST effort will enable ES-VCs to be included in SoC computer-aided design (CAD) libraries and enable integration of ES-VCs with the existing digital VCs used ubiquitously by industry to design large ICs. The methods and standards developed as a result of this work will be essential for the realization of integrated, smart, low-cost, homeland security and environmental sensor systems.

One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs, including MEMS-based VCs, into SoCs. The project activities include: multi-technology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ES-VCs compatible with digital methodologies, and testing standards and verification standards. The NIST MEMS-based integrated gas-sensing VC will be used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies will be used to facilitate the adoption of these MT-VCs into new homeland security and industrial applications.

Customer Needs

The driving force in today's semiconductor industry is the need to maintain a rate of performance improvement of 2x every two years in high-performance components. Historically, these improvements have relied exclusively on advances made by semiconductor miniaturization technology. The 2003 International Technology Roadmap for Semiconductors (ITRS) suggested that, "innovations in circuit design and architecture will be needed to design chips with both the desired performance and power dissipation." Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple technologies into a single chip referred to as System-on-a-Chip (SoC). The design challenges for SoC devices will be overcome with the use of platform-based design approaches that emphasize design reuse (*e.g.*, the development of ES-VCs that can be used as cost-effective building blocks for SoC devices).

The direct customers for this infrastructure building will be the makers of system design software, companies manufacturing ES-SoCs, and systems designers.

An October 20, 2003, article entitled "SoC Creation Requires Rules" written by Thomas L. Anderson, EE Times, states "While EDA vendors may provide detailed instructions and methodology guides for their specific tools, there has not been much industry activity in establishing more general rules, guidelines and best practices."

Technical Strategy

1. To develop ES-VCs for SoC design methodology successfully, the first step in this multi-step process is to develop the ability to produce the ES-VC devices via a standard CMOS compatible process. To demonstrate this capability we have chosen a MEMS microhotplate-based ES-VC, including operational amplifiers, decoders, and an analog-to-digital converter (ADC) to process the data.

DELIVERABLE: Develop post processing technology that will enable the microhotplate to scale to standard submicron mixed signal IC foundry processes.

2. The second step in making the ES-VC is to make it compatible with the digital SoC design methodology. This approach will require the ES-VC to have digital interface circuitry and to have Design-for-Test (DFT) and Built-In-Self-Test (BIST) functionality features. To facilitate this approach we will develop methodologies and standards for adding digital shells to ES-VCs and demonstrate them on the gas sensor VC described above.

DELIVERABLE: Develop methodologies for designing digital interface shells, develop DFT and BIST functionality for ES-VCs, and demonstrate their viability via the NIST microhotplate gas sensor technology.

3. The predominant design approach used by industry for SoC devices is top-down design. This

requires that high-level HDL models exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ES-VCs are at best poorly developed. To address this need, high-level models are being developed for ES-VCs using Analog and Digital HDLs, and methodologies are being developed to validate the models.

DELIVERABLE: Develop methodologies and standards for developing high-level models for ES-VCs and demonstrate their viability via the NIST micro hotplate gas sensor technology.

4. After the high-level simulation of the system in the top-down design process is successfully completed, the next step is to synthesize the individual VCs. Compared to those for digital VCs, the methodology and standards for ES-VC synthesis are at best poorly developed. To address the need for synthesizing ES-VCs, we are developing standards and metrologies for a non-digital synthesis like process that is compatible with digital synthesis. This process is based upon libraries of existing designs and the device design equations.

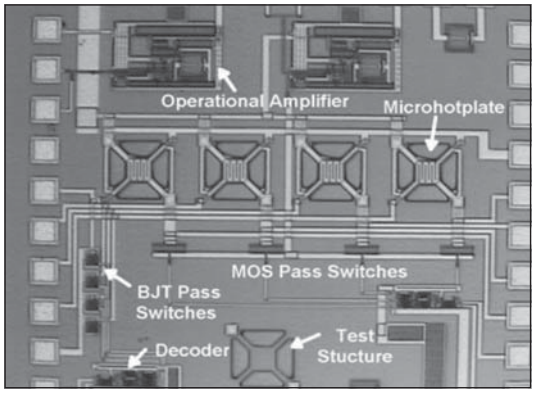
DELIVERABLE: Develop Gas Sensor SoC system architecture utilizing the ES-VC and synthesize system design demonstrating viability of ES-SoC methodology.

5. The testability of ES-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use BIST techniques. To facilitate this approach, we will develop methodologies and standards for adding BIST to ES-VCs and interface them via the digital shell.

DELIVERABLE: Develop test bed for evaluation of gas sensor VC built-in self test function demonstrating DFT requirements for ES-SoC design methodology.

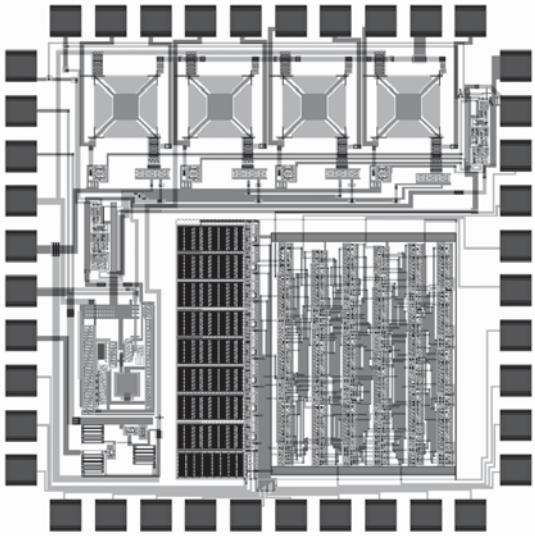
Accomplishments

■ A monolithic micro-gas-sensor system was designed and fabricated in a standard CMOS process. The gas-sensor system incorporated an array of four microhotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SnO_2) as a sensing material. The interface circuitry on the chip has digital decoders to select each element of the sensing array and an operational amplifier to monitor the change in conductance of the film. The chip is post-processed to create microhotplates using bulk micro-machining techniques. Detection of gas concentrations in the 100 parts-per-billion range was achieved. This represents a factor of 100 improvement in sensitivity compared to existing MEMS-based microhotplate gas sensors.



Micrograph of gas-sensor system to be used as demonstration vehicle.

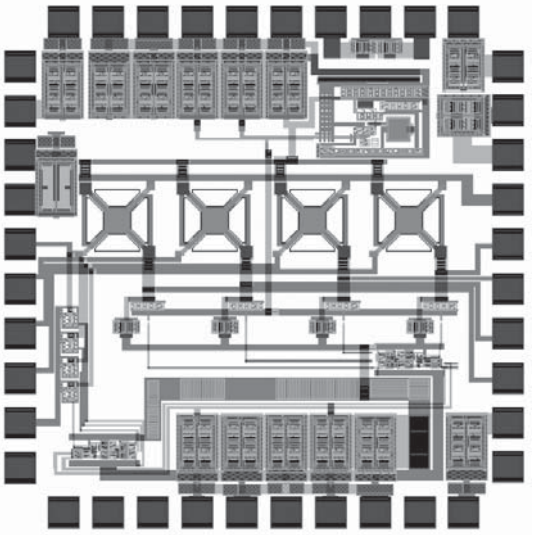
■ A monolithic CMOS four element gas sensor VC was designed and submitted for fabrication. The design includes both analog and digital integrated circuits. The digital part of the circuit has an 8-bit analog-to-digital converter (ADC). The objective of the design is to make it compatible with the SoC design methodology.



Layout of the four element gas sensor VC with analog-to-digital control.

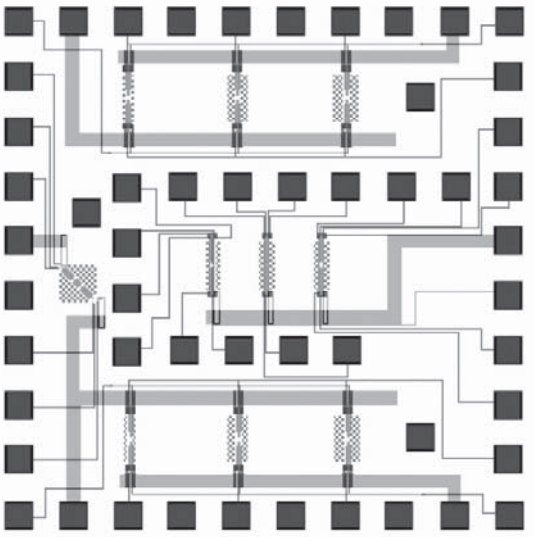
■ The four element gas sensor VC was electrically characterized. The performance of the 8-bit ADC superceded the gas sensor VC design requirements.

■ An initial design of a four element gas sensor VC with electrostatic discharge (ESD) protection was implemented in 1.5 micron standard CMOS technology.



Layout of the four element gas sensor VC with electrostatic discharge (ESD) protection circuitry.

■ New microhotplate test structures were designed and fabricated to improve thermal efficiency and their feasibility to be fabricated in the CMOS sub-micron technology.



New microhotplate test structures layout.

FY Outputs

Collaborations

University of Maryland, Metrology for multi-technology System-on-a-Chip (SoC)

Recent Publications

M. Y. Afridi, A. R. Hefner Jr., D. W. Berning, C. H. Ellenwood, A. Varma, B. Jacob, S. Semancik, "MEMS-based Embedded Sensor Virtual Components for SoC," Solid State Electronics, Vol. 48, pp. 1777-1781 (24-JUN-2004)

M. Y. Afridi, A. R. Hefner Jr., D. W. Berning, C. H. Ellenwood, A. Varma, B. Jacob, S. Semancik, "MEMS-based Embedded Sensor Virtual Components for SoC," 2003 International Semiconductor Device Research Symposium, pp. 500-501 (25-NOV-2003)

M. Y. Afridi, J. S. Suehle, M. E. Zaghloul, D. W. Berning, A. R. Hefner Jr., R. E. Cavicchi, S. Semancik, C. B. Montgomery, C. J. Taylor, "A Monolithic CMOS Microhotplate-based Gas Sensor System," IEEE Sensors Journal, Vol. 2, No. 6, pp. 644-655 (01-DEC-2002)

Power Semiconductor Device and Thermal Metrology

Goals

The goals of the project are to (1) develop electrical and thermal measurement methods and equipment in support of the development and application of advanced power semiconductor devices and (2) develop advanced thermal measurements for characterizing integrated circuits (ICs) and devices.

David Berning measuring silicon carbide diodes using NIST-developed, specialized equipment. Copyright Robert Rathe

Customer Needs

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient long distance high voltage power transmission. Rapid technical advances are occurring in the development of new power semiconductor materials and designs to address these needs. With the introduction of these new materials and designs comes new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the introduction of SiC power Schottky diode products in the 400 V to 1200 V range and led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 15 kHz power switching capability.

Several industry and government programs are currently underway to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE) is to develop half-bridge modules with 15 kV, 110 A, 20 kHz capability in the next few years. The emergence of HV-HF devices with such capability is expected to revolutionize utility and military power distribution and conversion by extending the use of Pulse Width Modulation (PWM) technology, with its superior efficiency and control capability, to high voltage applications.

The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which include advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements. In addition, HV-HF power devices are an enabling technology for alternative energy sources and storage systems. The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements.

While overcoming thermal limitations has always been at the forefront of power semiconductor technology, this has only come to the fore recently in CMOS-based microelectronic circuits. The major issues include: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (*e.g.*, SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in

Technical Contact:
Allen R. Hefner, Jr.

Staff-Years (FY 2004):
2.25 professionals
3.25 guest researchers

"In 2004, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: 'his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in … more efficient/compact power supplies, and higher efficiency power distribution/transmission systems.'"

"[The Project] … continues to lead industry needs by providing state-of-the-art capability for the measurement of unique power device characteristics at critical operating conditions."

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

the interconnects. In order to address these issues, reliable methods for measuring the temperature distribution in ICs and power devices are required.

Technical Strategy

The strategy is to support the measurement infrastructure of the semiconductor industry by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of devices and ICs. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters to aid in application insertion. NIST is taking a lead role in developing the device metrology and performance metrics necessary for both the DARPA and EPRI efforts and the new industries envisioned by these programs. NIST is also pioneering electrical and thermal measurement methods for HV-HF devices and advanced thermal metrology for high density ICs.

Performance, Reliability, and Application Characterization for DARPA-WBST-HPE Devices and Module Packages

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable Solid State Power Substations (SSPS) for future Navy warships. Current distribution approaches being considered for the next generation of aircraft carriers and destroyers employ a 13.8 kV AC power distribution that is stepped down to 450 V AC by using large (6 ton and 10 m^3) 2.7 MVA transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the $50 M Phase 2-3 program for 2005 through 2008.

Metrology for Mapping SiC Power Bipolar Device Degradation

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for bipolar structures is an observed degradation in the electrical characteristics over time. The degradation occurs from latent defects such as Basel Plane Dislocations that result in the formation and growth of stacking faults activated by excess carrier recombination. The defects cause severe current nonuniformities to occur, resulting in on-state voltage, switching, and thermal performance degradation.

DELIVERABLE: Develop automated stress and degradation monitoring systems to assess degradation of SiC devices after 10,000 hours of operation.

DELIVERABLE: Utilize NIST one-of-a-kind high speed thermal image measurements to characterize SiC power diode conduction uniformity performance before and after stress conditions and correlate results with light emission stacking fault measurements (with NRL).

Metrology for Nondestructive Switching Failure

Power devices undergo their greatest electro-thermal stress under switching conditions. There are a number of known catastrophic failure mechanisms that occur as a device is switched off with an inductive load. NIST has developed a nondestructive system to test for the failure limits under inductive switching, has done extensive research on Si device failure limits, and will extend that work to include SiC power devices.

DELIVERABLE: Perform unclamped inductive switching measurements for SiC MOSFETs and IGBTs produced by DARPA WBG program.

Circuit Simulator Models for SiC Power Switching Devices

Parameter extraction is a critical component in developing and using device models in circuit and system simulations and in establishing performance benchmarks for new device technologies. For new devices, not only must new models be developed, but methods must be modified and new ones developed for extracting the parameters for the models.

DELIVERABLE: Utilize NIST IMPACT model parameter extraction tools to characterize SiC power MOSFETs and IGBTs introduced by the DARPA WBST-HPE program.

Develop Thermal Metrology for Power Semiconductor Package and Cooling System

The cooling systems for power electronic devices and modules are often quite sophisticated and complex. In evaluating the efficiency and effectiveness of cooling systems, it is critical to be able to measure the temperature of a packaged chip accurately during actual operation. This means

that temperature measurement methods are needed that use a chip electrical parameter as the thermometer. Also, validated electro-thermal device models are needed to speed the system design. New HV-HS semiconductor devices present new packaging challenges and technologies that must be evaluated for high temperature performance, die attack voiding, and thermal cycling capability.

DELIVERABLE: Perform thermal cycling and thermal shock experiments on DARPA WBST-HPE program devices. Use unique NIST high current IGBT TSP system and high speed thermal imaging system to identify die attach and DBC integrity before and after thermal stress.

High-Speed Thermal Image Microscopy for On-Chip Temperature

A limitation of commercially available infrared (IR) thermal imaging systems is their inability to make high speed transient measurements. NIST has modified a commercial IR system to be able to make such high speed temperature maps of a device surface with a better than 1 μs time resolution and a spatial resolution of about 15 μm to 20 μm. Current work involves enhancing the performance and applicability of this unique test method and exploring the potential for addressing critical metrology issues in advanced digital integrated circuits and power devices.

DELIVERABLE: Develop procedure for coating chips with thin high emissivity paint and characterize the performance for high speed IR thermal metrology.

DELIVERABLE: Apply high speed thermal imaging system to characterize the performance of advanced digital integrated circuits including dynamic thermal performance enhancement (with UMD).

Accomplishments

- *Extended capabilities of IMPACT parameter extraction software*. The capabilities of the parameter extraction software, *IMPACT*, were extended to include MOSFETS (in addition to IGBTs) and three polytypes of SiC material (in addition to Si). This was done in collaboration with the University of Puerto Rico, Mayaguez, and two SURF (Summer Undergraduate Research Fellow) students.

- *High voltage curve tracer and reverse recovery systems*. The development of a 25 kV variable pulse width curve tracer for both 2 and 3 terminal devices was completed. Safety protection and an interlock system have been tested and qualified. A high voltage reverse recovery test system with 3 kV, 15 A capability was also developed. These systems are critical components in the SiC power semiconductor device metrology tasks.

- *Chip temperature measurements for power multichip modules*. Developed test system and procedures for thermal characterization of Integrated Power Electronic Module (IPEM) and developed electro-thermal model and validation for IPEM. Applied this new measurement and modeling method to commercial high power IGBT half bridge module, commercial six pack IGBT module, and prototype NSF Center for Power Electronic Systems IPEM.

- *High speed transient infrared thermal imaging system.* The high-speed transient imaging capability has been extended to include a burst method. This feature has been found to be very useful in measuring current uniformity of SiC power devices before and after degradation without degrading the device during the measurement.

- *Played a major role in planning and evaluating progress of DARPA Wide Bandgap Power Device program.* Developed the metrology, measured device deliverables to government from DARPA contractors, and used NIST data to provide assessment of program to DARPA director.

- *Initiated new program with EPRI to develop solid state power distribution transformers using ultra high voltage semiconductor devices*. The goal is to replace all existing power distribution transforms with Intelligent Universal Transformers that provide better control of the power grid, provide power factor correction at point of use, improve power quality, and enable plug-and-play insertion of alternate energy sources. NIST aided in mapping existing power semiconductor technologies for this application and in establishing an EPRI road map for development of ultra-high-voltage semiconductor devices.

- *Played a major role in initiating and planning a new DARPA/Navy SiC shipboard power distribution program*. The program involves insertion of power distribution technologies enabled by ultra-high-voltage semiconductor devices into next generation more electric Navel carrier, destroyer, and submarine platforms.

- *Completed development of SiC power MOSFET model and completed development of IMPACT extraction tools for SiC power device model parameter extraction.* Performed parameter extraction for SiC MOSFETs produced by DARPA WBG program and validated simulations.

FY Outputs

Collaborations

Avanti Inc., Parameter extraction for IGBT library component models

Avanti Inc./University of Arkansas, SiC power device modeling

Avanti Inc./UPRM, Characterization and modeling of electronic packages for thermal model library component models

NIST Division 812, Electronic Materials Characterization Project/Advanced MOS Device Reliability and Characterization Project, Benchmarks for quantum-mechanical device simulation

NIST/CREE, Development of SiC MOSFET electro-thermal model

Participants for DARPA contract (including NRL, ARL, Virginia Tech, CREE, University of Arkansas, Rockwell, etc.), Wide bandgap power device program

Rockwell Science Center/NIST, Development of SiC transistor models

University of Maryland, Metrology for multi-technology System-on-a-Chip (SoC)

Virginia Polytechnic Institute and State University, SiC power device utilization

External Recognition

Allen R. Hefner, elected IEEE Fellow "for contributions to the theory and modeling of power semiconductor devices"

Recent Publications

R. Singh, A. R. Hefner Jr., "Reliability of SiC MOS Devices," Journal of Solid-state Electronics, Vol. 48, No. 10-11, pp. 1717-1720 (24-JUNE-2004)

T. R. McNutt, A. R. Hefner Jr., A. Mantooth, J. Duliere, D. W. Berning, R. Singh, "Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator," IEEE Trans. Power Electronics, Vol. 19, No. 3, pp. 573-581 (01-MAY-2004)

D. W. Berning, J. V. Reichl, A. R. Hefner Jr., M. Hernandez, C. H. Ellenwood, J. Lai, "High Speed IGBT Module Transient Thermal Response Measurements for Model Validation," Proc., IEEE Industry Applications Society (IAS) Annual Meeting, Oct. 12-16, 2003, Salt Lake City, Utah, pp. 1826-1832 (12-OCT.-2003)

X. Huang, P. Elton, J. Lai, A. R. Hefner Jr., D. W. Berning, S. Chen, T. Nehl, "EMI Characterization with Parasitic Modeling for a Permanent Magnet Motor Drive," Proc., IEEE Industry Applications Society (IAS) Annual Meeting, Oct. 12-16, 2003, Salt Lake City, Utah, pp. 416-423 (12-OCT.-2003)

T. R. McNutt, A. R. Hefner Jr., A. Mantooth, D. W. Berning, S. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," Proc., Power Electronics Specialist Conference, Power Electronics Specialist Conference, Acapulco, Mexico, 10 p. (11-JUNE-2003)

R. Singh, K. G. Irvine, D. C. Capell, J. T. Richmond, D. W. Berning, A. R. Hefner Jr., J. W. Palmour, "Large Area, Ultra-high Voltage 4H-SiC PiN Rectifiers," IEEE Trans. Electron Devices, Vol. 49, No. 12, pp. 2308-2316 (01-DEC.-2002)

R. Singh, D. C. Capell, A. R. Hefner Jr., J. Lai, J. W. Palmour, "High-Power 4H-SiC JBS Rectifiers," IEEE Trans. Electron Dev., Vol. 49, No. 11, pp. 2054-2063 (01-NOV.-2002)

J. J. Rodriguez, J. V. Reichl, Z. R. Parrilla, A. R. Hefner Jr., D. W. Berning, M. Velez-Reyes, J. Lai, "Thermal Component Models for Electro-Thermal Analysis of Multichip Power Modules," Proc., 2002 IEEE Industry Application Society, IEEE Industrial Applications Society Meeting, Oct. 13-18, 2002, Pittsburgh, Pennsylvania, pp. 234-241 (24-OCT.-2002)

MicroElectroMechanical Systems

Goals

The MicroElectroMechanical Systems (MEMS) Project works to apply micro and nanofabrication technologies (MNT) to advance the state of the art of single molecule measurements, single cell measurements, and DNA separations for forensic applications. In addition, we support domestic and international MEMS standardization by working with standards groups to develop and provide the MEMS industry with test structures, test methods, measurement standards, and standard manufacturing practices.

Customer Needs

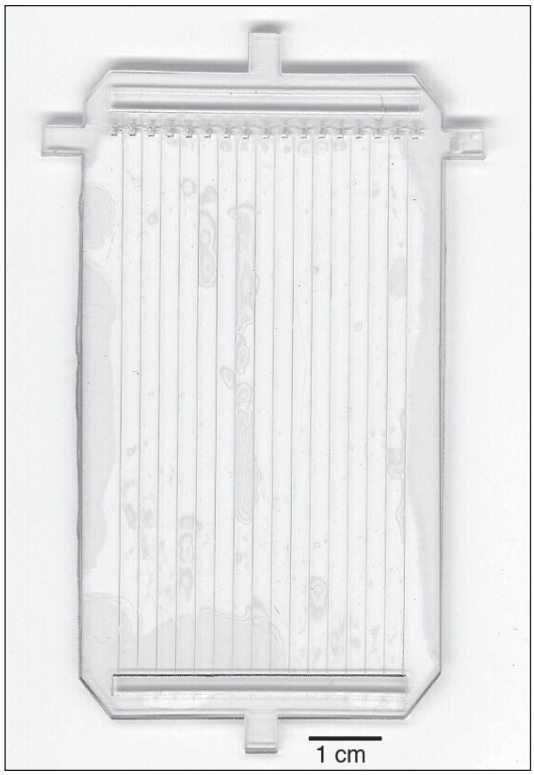
MEMS technology continues to mature, resulting in growing opportunities for U.S. industry, which in turn results in an increasing need for measurement standards and also for new opportunities for research. Our project aligns its new efforts with NIST's core mission and with NIST's strategic focus areas in biosystems and health, and nanotechnology. As a result, the MEMS Project has developed four main focus areas: single molecule measurements, bioelectronics, DNA separations for forensic applications, and MEMS standardization.

Single Molecule Manipulation and Measurement

The biotechnology and healthcare industries require measurements of large sample arrays as part of their combinatorial approach to disease recognition and drug development. For example, manufacturers of technologies such as DNA and protein arrays are striving to make larger arrays that can more efficiently support larger combinatorial measurements. As the size of the sensors is decreased, the sample size (and hence the number of molecules in the sample) also decreases. Since biological molecules are expected to have variation in their behavior, a question arises concerning whether the statistical variation of biological molecules will affect the accuracy of those measurements; *e.g.*, is there a minimum sample size that is required to yield a result that is comparable to traditional ensemble measurements. The ability to measure the structure and function of single biomolecules will yield the statistical behavior of their large populations.

Bioelectronics

Our vision of bioelectronics is interfacing integrated circuit technologies to biological systems. Experiments in cell biology have been virtually unchanged for many decades, involving manual handling of cell culture flasks, changing the cell media (feeding the cells), exposing the cell culture to a compound of interest, and observing cell response and viability using a microscope. For this reason, cell biology experiments are typically very time consuming and labor intensive. Recently, the trend has been to conduct studies that involve large arrays of small cell cultures by automating these steps as much as possible using robotic instrumentation, but the experiments are still essentially the same. A true paradigm shift is to utilize micro- and nanofabrication technologies to perform these experiments on single cells or small cell clusters in continuous flow microfluidic systems with integrated microsensors and MEMS.



Prototype 16 channel device for DNA fingerprinting.

Technical Contact:
Michael Gaitan

Staff-Years (FY 2004):
4.5 professionals
1.0 post doc
4.75 guest researchers

DNA Separations for Forensic Applications

The Department of Justice recognizes an urgent need to improve the efficiency, speed, and accuracy of DNA testing in order to alleviate a growing backlog of forensic DNA testing for criminal cases. Results of DNA testing have become a critical component of criminal investigations and are often used as evidence in court proceedings. NIST has played a key role in the validation and standardization of forensic DNA testing protocols over the past decade that has facilitated a growing acceptance of this type of analysis for criminal investigations.

Microfluidic technology is a promising alternative to current capillary-based techniques due to its great potential to miniaturize, simplify, integrate, automate, and multiplex the analysis with higher throughput and speed. This technology has already shown that it is the next revolution in DNA technology, with analysis often complete in ten percent of the time required for more traditional capillary technology. Although DNA analysis systems based on microfluidics technology have been recently commercialized, these systems do not meet the specific needs of the forensic community due to poor separation resolution of the relatively long fragments (on the order of 100 bps to 400 bps) as well as incompatibility with the standard test procedures.

Measurements and Standards for MEMS

MEMS is a rapidly growing technology with a forecasted annual growth rate that exceeds that of the semiconductor electronics industry as a whole. Manufacturers of MEMS products, such as acceleration sensors for automotive air bags and deformable mirror displays for video projection, are producing these devices in Integrated Circuit (IC) manufacturing lines. This integration of mixed technologies is part of the semiconductor industry's revolution toward "system-on-a-chip." System-on-a-chip links the functionality of the IC (an information processor) with information gathering (sensing the environment) and actuation (acting on decisions). New test structures, test methods, and standards are required for device characterization to improve manufacturing and design.

In support for the need of measurement standards for MEMS, the project is working with ASTM Task Group E08.05.03 on Structural Films for MEMS and Electronic Applications. This task group has undertaken sponsorship of a round robin experiment for measuring in-plane length, residual strain, and strain gradient. MEMS test structures used in these experiments are designed and then fabricated on a test chip that is passed among participating laboratories. These dimensional and film properties are important to the fabrication of MEMS devices. Participation in the ASTM Task Group gives NIST a leadership role in the development of measurement standards for the industry.

The MEMS Project is also working with SEMI's new MEMS Materials Characterization Task Force to develop standardization for MEMS technology. Our prime effort with this group is working to support the development of compact models for MEMS devices that can accurately simulate their response in advanced circuit simulators.

MEMS test structures have applications to measuring the mechanical properties of thin films in ICs, a need identified in the International Technology Roadmap for Semiconductors. As IC devices continue to shrink, thermo-mechanical stress in the thin films that interconnect them is an ever-increasing reliability concern. Current state-of-the-art IC technology uses five or more interconnect layers with aspect ratios (height/width) that can exceed 1.8. Despite the increasing number of interconnect layers in IC technology, existing stress determination and modeling studies have been limited to single level metallization, with few exceptions. This is due, in large part, to the lack of experimental techniques for measuring strain in narrow line widths (less than 10 μm) and in multilayer structures.

MEMS-based IC test structures allow, for the first time, the measurement of strain in multilayer structures in fully fabricated ICs. These measurements can be used to characterize the mechanical stress in these multilayer films. Results can then be used to verify finite element models of the stress in the films and to correlate mechanical stress data with reliability testing. MEMS-based test structures being developed in this project offer new ways to characterize the mechanical stress in multilayer films.

Technical Strategy

NanoBioTechnology is a new and rapidly growing field that is focused on the development of nanotechnology for biomedical research and applications. The Semiconductor Electronics Division sees a new opportunity for the application of nano-

fabrication methods to create structures to probe biological systems at the single cell and single molecule level. The top-down nanofabrication methods that have been developed by the semiconductor electronics industry can be coupled with bottom-up self-assembly techniques to create new tools to probe life's processes. We believe that the ability to measure the behavior of individual cells or biological molecules, which are traditionally characterized by ensemble measurements, will provide fundamentally new information about how those biological processes work. We have three main focus areas in our nanobiotechnology effort: Single Molecule Manipulation and Measurement (SM^3), where we seek to develop new tools to probe the structure of DNA electronically and optical methods to characterize the structure and conformations of proteins; Bioelectronics, where we seek to sense single cell behavior electrochemically; and DNA separations for forensic applications, where we seek to develop a plastic-based microfluidic device that will decrease the time to perform a separation at a lowered cost. Our work is carried out with multidisciplinary teams that span laboratories within NIST and the National Institutes of Health.

Single Molecule Manipulation and Measurement

The semiconductor electronics industry has driven the development of fabrication tools that are capable of patterning structures that are smaller than cellular dimensions (*i.e.*, on the order of 100 nm). In combination with micromachining methods developed by MEMS research, it is possible to create three-dimensional structures that are commensurate with the size of biomolecules. We will utilize nanofabrication methods and enhanced surface coatings to develop novel solid-state structures for the control and manipulation of single biomolecules. These methods will be based on electrofluidic, electromechanical, optical, and magnetic transport of biomolecules in confined nanometer-scale environments.

Interactions of single molecules with nanoscale mechanical structures, restriction elements, and other single molecules will be probed by electronic, electromechanical, and optical techniques. The effort will result in a well-characterized SM^3 platform integrated with AFM, FRET (Fluorescence Resonance Energy Transfer), optical microscopy, and electronics, thereby enabling a wide variety of single-molecules studies. DNA structure determination will be performed by directly interrogating ordered bases as they are threaded through a well-characterized nanopore.

DELIVERABLE: Develop a platform that integrates nanometer-scale fluidic restrictions, fluidic networks, switches, and workstations that support the electronic and optical control and measurement of single molecules of DNA and RNA.

Bioelectronics

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the *in vitro* measurement systems, developing stable and drift-free electrodes for accurate measurements, invaried buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid *in vitro* environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We will focus our initial research efforts on the study of retinal (neuronal) cells and will later progress to other cell systems.

DELIVERABLE: Develop an array of micro-electrochemical cells and methods to pattern cells on the array for single-cell electrochemical measurements.

DNA Separations for Forensic Applications

Our team will draw on our extensive expertise in microfluidics, microfabrication, DNA separations, as well as state-of-the-art optics and detection to build a prototype system that can be used as a model to demonstrate the advantages of applying these latest technologies for forensic identification. There are two overall requirements that must be satisfied to meet the needs of the Department of Justice: (1) development of a reliable, easy-to-use, high-throughput, microfluidics-based system that is smaller and faster than capillary-based techniques; and (2) validation of the system that would support the adoption of this technology by the judicial system.

DELIVERABLE: Develop a breadboard microfluidic forensic DNA separation system for demonstration to forensic scientists.

Measurements and Standards

The MEMS technical community, composed of companies, universities, and government laboratories, has developed many types of test structures to characterize the fabrication process and device performance. The MEMS Project plays an active role in ASTM Task Group E08.05.03 on Structural Films for MEMS and Electronic Applications and in SEMI's MEMS Materials Characterization Task Force to supply the community with standardized test methods.

DELIVERABLE: Complete the round robin experiment for in-plane length, residual strain, and strain gradient measurement standards to determine the precision and bias of these measurements; incorporate these results in the ASTM MEMS standards for balloting.

IC Interconnect Characterization

Micro-machining techniques, test structures, and test methods are being developed to characterize the stress, elastic modulus, and adhesion properties in the thin films comprising ICs. These test structures are fabricated in the standard IC process on fully fabricated ICs. Fixed-fixed beam and cantilever test structures with and without interconnect layers are micro-machined in the fully processed IC. Measurements of deflection of buckled beams give information on the strain in each layer. Measurements of mechanical resonance give information on the elastic modulus of the films. These test structures can also be integrated with micro heating elements for accelerated testing.

DELIVERABLE: Develop a method based on the use of an optical vibrometer to measure the resonant frequencies of the various cantilevers in a CMOS process in order to extract the elastic modulus of the thin films with a higher degree of accuracy.

Accomplishments

■ *Method to formulate liposome nano-cells (or nano-vials).* A method has been developed to form liposome nano-vials in a continuous flow system. Microfluidics is used to elicit control over the spontaneous self-assembly of liposomes from a solution of dissolved phospholipids. In this work, we hydrodynamically focus a stream of lipid tincture at a microchannel cross-junction between two aqueous buffer streams. In a typical procedure, isopropyl alcohol (IPA) containing the dissolved lipids plus a fluorescent dye ($DiIC_{18}$) flows through the center inlet channel, and an aqueous phosphate buffered saline solution flows through the two side inlet channels. $DiIC_{18}$ is a membrane-intercalating dye that exhibits enhanced fluorescence when trapped in a lipid membrane as compared to the fluorescence of the dissolved dye. The flow rates of the IPA and buffer channels are adjusted to control the degree of hydrodynamic focusing and the width of the center stream, thus controlling the IPA/buffer dilution process.

■ *Method to adhere retinal cells on micropatterned polyelectrolyte multilayer (PEM) lines adsorbed on poly(dimethylsiloxane) (PDMS) surfaces using microfluidic networks.* PEMs were patterned on flat, oxidized PDMS surfaces by sequentially flowing polyions through a microchannel network that was placed in contact with the PDMS surface. Polyethyleneimine (PEI) and poly(allylamine hydrochloride) (PAH) were the polyions used as the top layer cellular adhesion material. The microfluidic network was lifted off after the patterning was completed and retinal cells were seeded on the PEM/PDMS surfaces. The traditional practice of using blocking agents to prevent the adhesion of cells on unpatterned areas was avoided by allowing the PDMS surface to return to its uncharged state after the patterning was completed. The adhesion of rat retinal cells on the patterned PEMs was observed 5 h after seeding. Cell viability and morphology on the patterned PEMs were assayed. These materials proved to be nontoxic to the cells used in this study regardless of the number of stacked PEM layers. Phalloidin staining of the cytoskeleton revealed

no apparent morphological differences in retinal cells compared with those plated on polystyrene or the larger regions of PEI and PAH; however, cells were relatively more elongated when cultured on the PEM lines. Cell-to-cell communication between cells on adjacent PEM lines was observed as interconnecting tubes containing actin that were a few hundred nanometers in diameter and up to 55 μm in length. This approach provides a simple, fast, and inexpensive method of patterning cells onto micrometer-scale features.

■ *Method to create nanofluidic restrictions by electroplating silver on micrometer scale pores*. Electrodeposition of silver was investigated as a fabrication tool for constricting large (10^3 μm^2) vias in silicon substrates while leaving a small opening in the center of the via. Silver reduction from ammoniacal silver nitrate was studied at electrodes of novel geometry (*i.e.*, the edge of the vias) with respect to reduction potential, reduction pulse type, and pulse duration. A variety of crystal nucleation and growth patterns was observed and characterized by scanning electron microscopy. It was found that electroplated silver occluded the vias to leave open areas of less than 1 μm^2. Such occlusions might be used as restrictions in microfluidics systems, forming a type of solid-state micropore or nanopore.

■ *Cantilever test structures and an analysis to extract the elastic modulus from the measurement of their mechanical resonance were developed.* These test structures are from IC thin films in fully fabricated Complementary Metal-Oxide Semiconductor (CMOS) ICs. A test chip containing the new cantilever test structure designs was fabricated on a commercial CMOS foundry through the MOSIS service. The test structures are silicon micro-machined as a post process in order to release them mechanically. These test structures complement the doubly clamped beam test structures that have been developed and used to measure the strain in CMOS films. The combination of data from strain measurements and elastic modulus measurements will enable the measurement of thin-film stress. Proof-of-concept thickness, resonant frequency, and Young's modulus values have been obtained on three processing runs.

■ *Seven laboratories participated/are participating in the web-based ASTM length and strain round robin experiment.* This experiment is planned to be completed this coming year. Repeatability data has been obtained and, once the remaining reproducibility data are submitted to the round robin, the draft precision and bias statements for the three standards can be completed and the standards submitted for balloting. The MEMS terminology is also expected to be balloted this coming year.

■ *NIST was awarded a patent on the invention of a new type of accelerometer*. The convective accelerometer, as it is named in the patent, operates on the principle that hot air rises. This device differs from the traditional MEMS-based accelerometers in that its operation is not based on a solid proof mass. The device consists of microheating elements and thermocouple sensors separated by a gap and placed in differential configurations. Thermocouple sensors measure the temperature difference between the two sides of the microheater caused by the effect of acceleration on free convection in the surrounding gas. The devices show a small error in linearity of <0.5 % under tilt conditions from -90 °C to 90 °C, and <1.6 % under acceleration from 0 g to 8 g. The sensitivity of the devices is a linear function of heater power (temperature). A sensitivity of 20 μV/g to 30 μV/g was measured for operating power between 35 mW and 45 mW. This invention is a spin-off of research on Micromachined Passive Microwave Components in CMOS Technology that was sponsored by the U.S. Navy.

FY Outputs

Collaborations

National Eye Institute of NIH, S. Patricia Becerra, Patterning neural (retinal) cells on surfaces to improve the understanding and treatment of diseases associated with vision

Instrumentation Research and Development Group of NIH, Paul Smith and Tom Pohida, Development of optical detection methods for forensic DNA separations

National Cancer Institute of NIH, David Robert, Liposome nano-vials for cancer detection and treatment

ASTM Task Group E08.05.03, Structural Films for MEMS and Electronic Applications

SEMI's MEMS Materials Characterization Task Force

NIST Division 831, John Kasianowicz, Nano-pores for electronic measurements of DNA structure

NIST Division 844, Lori Goldner and Angela Hight-Walker, Single molecule nano-vials

NIST Division 842, Kris Helmerson, Single molecule nano-vials

NIST Division 839, Laurie Locascio and Wyatt Vreelnad, Liposome Nanovials

University of Maryland/Georgia Tech, Measuring and modeling bonding temperature rise

Standards Committee Participation

ASTM Task Group E08.05.03, round robin in progress to determine the precision and bias of the 3 recently published MEMS standards (Janet C. Marshall)

SEMI's MEMS Materials Characterization Task Force, working on bringing forward compact models for MEMS devices for standardization (Janet C. Marshall)

External Recognition

Elected chair of the International Micromachine Summit to be held in Dallas, TX, in May 2005 (Michael Gaitan)

Recent Publications

M. Gaitan, "Nanotechnology in Integrative Systems: Introduction to Integrative Systems," Nanoscale Science and Technology, Kluwer Academic Press, pp. 373-388 (17-AUG.-2004)

B. J. Polk, M. Bernard, J. J. Kasianowicz, M. Misakian, M. Gaitan, "Micro-Electroplating Silver on Sharp Edges for Fabrication of Solid-State Nanopores," Journal of the Electrochemical Society, Vol. 151, No. 9, pp. C559-C566 (11-AUG.-2004)

J. C. Marshall, E. M. Secula, J. Huang, "Round Robin for Standardization of MEMS Length and Strain Measurements," SEMI Technology Symposium: Innovations in Semiconductor Manufacturing, Jul 12-14, 2004, San Francisco, California, (12-JULY-2004)

D. R. Reyes, E. Perruccio, S. P. Becerra, L. E. Locascio, M. Gaitan, "Patterning Retinal Cells on Polyelectrolyte Multilayers," The 7th International Conference on Miniaturized Chemical and BioChemical Analysis Systems (μTAS 2003), Oct 05-09, 2003, Squaw Valley, California, pp. 713-716 (18-FEB.-2004)

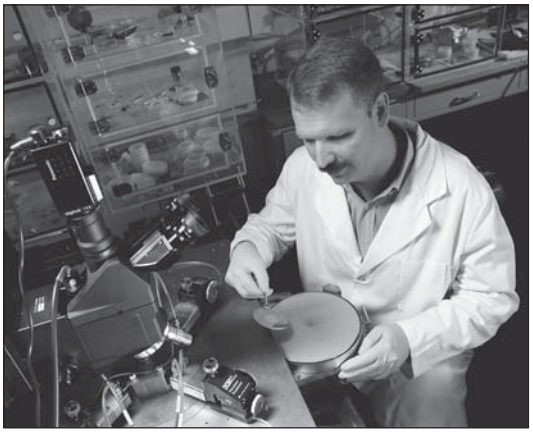
M. Gaitan, "Overview on CMOS MEMS Fabrication Techniques and Applications," Proceedings of 2001 IMAPS, 2001 IMAPS, Oct 09-11, 2001, Baltimore, Maryland, pp. 1-6, (01-NOV.-2001)

S. Shuman, M. Gaitan, Y.K. Joshi, G.G. Harman, "Wire Bond Temperature Sensor," Proceedings of 2001 IMAPS, 2001 IMAPS, Oct 09-11, 2001, Baltimore, Maryland, pp. 344-349, (01-NOV.-2001)

Nanoelectronic Device Metrology

Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) Project is to develop the metrology that will help enable new nanotechnologies (such as Si-based quantum devices, molecular electronics, and organic thin-film transistors) to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop test structures and methods to measure the electrical properties of small ensembles of molecules reliably. Another targeted goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices. A third goal is to develop an integrated and interdisciplinary suite of sophisticated measurement capabilities to enable correlations between organic electronic device performance and the structure, properties, and chemistry of critical materials and interfaces.



Curt Richter loads a molecular electronic sample for electrical characterization. Copyright Robert Rathe

Customer Needs

The CMOS FET (Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The SIA's International Technology Roadmap for Semiconductors (ITRS) shows no known solutions in the short term for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. Two promising beyond-CMOS technologies that each take a very different fabrication approach are molecular electronics and Si-based quantum electronic devices. Molecular electronics is based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches utilized in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices. In addition, electronic devices fabricated with organic materials form a dramatically emerging technology targeting applications (such as printable large-area displays, wearable electronics, paper-like electronic newspapers, low-cost photovoltaic cells, ubiquitous integrated sensors, and radio-frequency identification tags) that are challenging to implement in conventional CMOS.

Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. Research and development for silicon-based nanoelectronics (*e.g.*, Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology. Organic electronics is beginning to revolutionize the future of integrated circuits through the development of new applications that leverage advantages in low-cost, high volume manufacturing, nontraditional substrates, and designed functionality.

The NEDM Project is concerned with fundamental research related to possible future devices that will replace or augment standard CMOS technology. In order to ensure that our research is technically relevant, we plan to align ourselves with research alluded to in the SIA's Roadmap and other similar semiconductor industry organizations and documents as well as that described by the Microelectronics Advanced Research Corporation (MARCO).

The industry for these emerging nanoelectronic devices will require reference data, standards, precision measurement methods, and standardized

Technical Contact:
Curt A. Richter

Staff-Years (FY 2004):
3.5 professionals
0.5 technician
3.5 guest researchers

"…there is no particular reason why Moore's law should continue to hold: it is a law of human ingenuity, not of nature. At some point, Moore's law will break down. The question is when?"

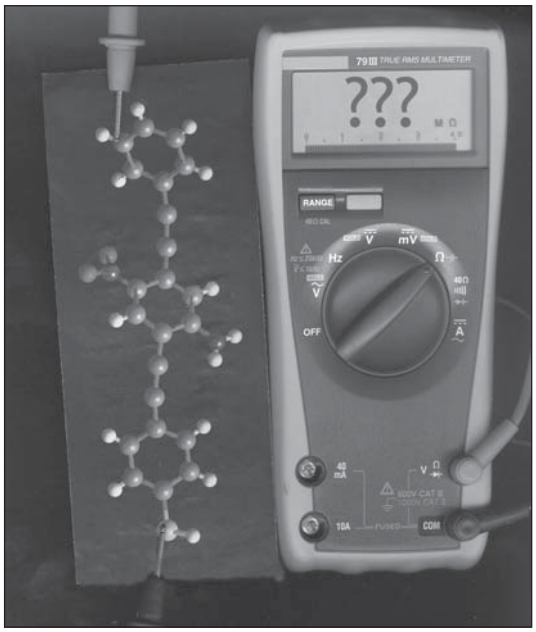
Seth Lloyd, d'Arbeloff Laboratory for Information Systems and Technology, Massachusetts Institute of Technology

test structures and associated measurement protocols to develop into a viable commercial technology. The ultimate objective of this project is to provide the measurement infrastructure to aid this development. Through strong ties with industry leaders and cutting-edge researchers, we are accelerating the pace of our program and focusing our research on the most relevant technologies.

Technical Strategy

The NEDM Project investigates and is developing metrology for three specific areas of nanotechnology: (1) Si-based quantum electronics, (2) molecular electronics, and (3) organic electronics.

The focus of the Si-based nanoelectronics is the physical and electrical metrology of the basic building blocks of silicon quantum electronic devices (*e.g.*, quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.



Electrically measuring molecules: the concept.

A major goal is to fabricate single quantum dots and wires with controllable size. These will be used to establish the relationship between the key fabrication conditions, physical properties (such as the geometry of the quantum-dot and the tunneling barrier), and final electrical properties of these floating silicon devices (*i.e.*, metal-oxide-silicon-oxide-silicon [MOSOS] devices). Production of MOSOS capacitor structures is an intermediate step en route to this end goal. This research will provide the information necessary to help identify and address the necessary electrical and physical characterization methodologies.

DELIVERABLE: Complete systematic investigation of carrier mobility in Si-nanowire FETs nanofabricated from SOI wafers.

In molecular electronics, our major objectives are a NIST standard suite of molecular test structures and a fundamental understanding of charge transport through molecules and molecular ensembles.

We are developing robust molecular test structures in order to use them to measure the electrical properties of molecules. Specifically, we are developing nanofabricated test-structures for assessing the electrical properties and reliability of moletronic molecules. These in-house test structures and prototypical ME devices obtained from leading researchers outside of NIST are thoroughly assessed to determine if they are viable test vehicles. In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used in the validation of predictive theoretical models.

DELIVERABLE: Complete a documented NIST standard suite of molecular electronic test structures.

Two of the most critical elements to forming a successful ME device structure are the formations of a high-quality molecular monolayer and a top-metal/molecule interface. The NEDM is investigating ways to improve the characterization and control of these top and bottom molecular interfaces. To do this, the NEDM is optimizing self-assembly of molecular films onto both metals such as gold and directly onto Si surfaces. The direct attachment of organic molecules to the silicon surface is of increasing importance for emerging molecular electronics applications as devices incorporating molecules chemically bonded to silicon are amenable to integration with existing Si processing techniques. In order to determine optimal top-metallization techniques, we are developing new characterization approaches to determine metal/molecular interactions. Empirically, new deposition tech-

niques and new top-metals (such as organic conductors) are being assessed to determine their viability as top metal contacts.

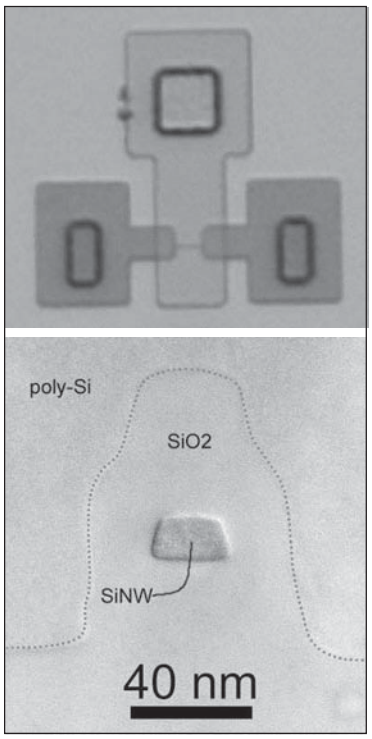
DELIVERABLE: Assess and improve methods for solution-based direct attachment of organic molecules to Si.

DELIVERABLE: Develop and demonstrate FTIR-based technique to characterize top-metal/molecular interfaces. Investigate initial metal/molecule interfaces.

The current state of organic electronics is analogous to the early stages of the silicon semiconductor industry, with the concurrent development of multiple material platforms and processes, no standardization of measurements between laboratories, and a lack of diagnostic probes, tools, and methods necessary to address critical technological challenges. A principal goal of the new organic electronics task is to determine experimentally the correlation between device performance and the structure, properties, and chemistry of critical materials and interfaces. The first step is to develop a preliminary set of test structures, fabrication techniques, and measurement methodologies to characterize the electrical properties of OFETS (organic field effect transistors) systematically.

DELIVERABLE: Design initial OFET test structure suite and fabricate prototypical organic devices. Prepare report.

Developing the metrology for "beyond-CMOS" nanoelectronic devices is a challenging and multidisciplinary task; therefore, it is important to be teamed with strong collaborators. The Si-based nanoelectronics team works closely with scientists in the Quantum Electrical Metrology Division as well as researchers at NTT. The ME staff is part of a NIST Competence Project on Molecular Electronics with the Chemical Science and Technology Laboratory (CSTL). CSTL provides many of the molecules we use, provides insights into SAM formation, performs precise structural characterization, and performs advanced quantum chemistry theoretical analysis. In addition, the ME team is working with various companies, universities, and government laboratories (*e.g.*, Hewlett-Packard, Yale University, University of Texas at Dallas, Naval Research Labs). A new (for FY 2005) NIST Competence Project on Organic Electronics has been established, forming a team of scientists from the NEDM, the Materials Science and Engineering Laboratory (MSEL), and CSTL. This combination of interdisciplinary talent will allow the electrical behavior of organic FETs to be correlated with the results of unique, state-of-the-art physical characterization methods in order to form a better understanding of the fundamental mechanisms that are determining final device performance in this new category of devices.



Si nanowire field-effect transistor.

Accomplishments

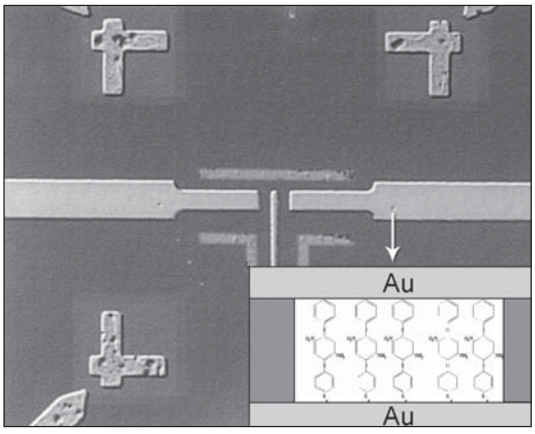
■ *Joint NIST/HP Research Progresses Toward Critical Molecular Electronics Measurements.* Research at the NEDM and Hewlett Packard (HP) Laboratories is progressing toward reliable methods for measuring the electrical behavior of molecular electronic devices, an emerging nanotechnology eyed for future integrated circuits. By using a crossbar test structure consisting of a molecular monolayer sandwiched between a series of perpendicular metal wires, collaborators at separate facilities recorded nearly identical electrical measurements. This step, along with others taken to eliminate potential sources of error, ensures that the measured behavior is directly attributable to the device and not the experimental set up. Electrical (current-voltage, or IV) measurements of crossbar devices containing eicosanoic acid exhibit a controllable, two-state switching behavior that is due to the presence of the molecular layer. However, the molecular monolayer is not the sole cause. Rather, the switch-like behavior most likely arises from the interaction of the molecules with the electrodes. This example illustrates that the properties of molecular electronic devices are

often determined not by the molecule alone, but by the entire device that consists of both the molecules and the attachment electrodes. This two-state behavior was independently measured in two separate laboratories, indicating that it is not a measurement artifact and illustrating that these devices are robust enough to ship via conventional methods and remain active. In addition to IV measurements, what well may be the first capacitance-voltage (CV) measurements of molecular monolayer-based devices were taken at NIST. These CV curves also show two-state behavior.

■ *Improved Methods to Attach Long-Chain Aliphatic Molecules to Silicon Developed.* Dr. Christina Hacker and colleagues have developed an improved solution-based method for the direct attachment of long-chain aliphatic molecules to Si. In this method, ultraviolet (UV) radiation is used to assist the attachment of alcohols to the hydrogen-terminated Si(111) surface to form molecular monolayers successfully. To investigate the quality of these organic monolayers, they were physically and chemically characterized with infrared spectroscopy, spectroscopic ellipsometry, and contact angle measurements. The electrical properties of these organic films were probed by using IV and CV measurements obtained from a metal-organic-silicon test structure fabricated by post-monolayer metal deposition. The effect of differing alkane chain length on the electrical properties was investigated, and the CVs are in agreement with traditional theory for a metal-insulator-semiconductor.

■ *Enhanced Inversion Mobility in Silicon Nanowire Field Effect Transistors Demonstrated.* Dr. Sang-Mo Koo and colleagues have demonstrated that silicon nanowire (SiNW) field effect transistors (FETs) fabricated by a standard 'top-down' approach exhibit substantially enhanced transport performance. A systematic study on the inversion electron transport properties of SiNWs with different channel geometries has shown that a SiNW device exhibits enhanced inversion channel current density: the extracted electron inversion mobility of the 20 nm width nanowire channel (1000 cm^2/Vs) is found to be 2 times higher than that of the reference MOSFET of large dimension (W >1 μm). The enhancement is attributed to the possible suppression of inter-valley phonon scattering due to strain in SiNW caused by the oxidation process. As the feature sizes of FETs are scaled downward, the semiconductor industry is working to meet the increasing challenges of nanoscale devices that are smaller and yet can be manufactured with minimal deviation from today's standard manufacturing processes. These results strongly suggest that lithographically fabricated SiNW FETs, which are compatible with Si ULSI technology, can bring about significant performance benefits in nanoscale electronics, preserving the basic silicon technology infrastructure upon which current industry relies.

■ *Molecular Electronic Test Structure (METS) Assessment Methodology.* An effective test protocol was developed for METS to ensure that electrical results can be attributed to the molecules and are not an artifact of the test structure itself. Current-voltage curves were obtained for devices with no molecules and for devices containing long-chain alkanethiols (such as octadecanethiol). These two limits, a conducting short and an insulating film in the nanopore, respectively, characterize the METSs and allow the properties of conducting molecules of interest to be measured reliably. In addition to applying this methodology to the METSs being fabricated in the NEDM Project, we apply these techniques to investigate METSs of other researchers. For example, we have characterized Si_3N_4-based nanopore devices in a collaboration with Yale University (M. A. Reed) and crossbar type devices in collaboration with Hewlett-Packard.



nano-Bucket molecular electronic test structure.

■ *Development of nano-Bucket Fabrication Processes.* Individual nano-Bucket devices have been fabricated successfully from nanopores (down to ~30 nm in diameter) etched through both thermally-grown SiO_2 and dielectrics deposited via chemical-vapor deposition (CVD) techniques. The most promising of these techniques relies on CVD dielectrics and an organic conductor to form a top contact to the molecular monolayer. This vehicle has been assessed and easily passed the no-

molecule criterion (as a dead short) and the no-nanopore criterion (as a no-leakage open circuit).

■ *Establishing Infrastructure for the Nanoelectronic Device Metrology Project.* In FY 2002, the Nanoelectronic Device Metrology Project was established. Extensive plans were developed and funding was acquired for this project. There are three areas of infrastructure that have been improved: personnel, equipment, and funding. In addition to the joint CSTL/EEEL Molecular Electronics Competence (started FY 2001) and funding from the National Nanotechnology Initiative (started mid-year FY 2001), the NEDM Project was part of two recently funded ATP Intramural Awards: "The Missing Plateau: Confined Silicon Devices for ULSI Nanotechnology," (EEEL/MSEL) and "Model-Guided Screening of Electrically-Active Molecules for Nanoelectronics" (CSTL/EEEL). In FY 2005, new funding will begin from DARPA and the MSEL/EEEL/CSTL Organic Electronics Competence.

■ *Personnel.* Since the project was formed in 2001, two new full-time researchers have joined NIST and the NEDM Project. Oleg A. Kirillov (Rochester Institute of Technology [RIT]) was hired as a processing engineer. Dr. Christina Hacker (U. Wisconsin at Madison) was hired on after working in the NEDM Project as a post-doctoral candidate through the NRC Research Associate Program. At the start of FY 2005, three postdoctoral guest researchers will be working in the NEDM; Dr. Wenyong Wang (Yale University) will concentrate on electrical characterization of ME devices while Drs. Sang-Mo Koo and QiLiang Li (NCSU) will concentrate on Si-nanoelectronic device structures. Dr. Jin-Wan Park (Seoul National University) and Dr. Jin-Ping Han (Yale University) both left during FY 2004 after working with us for two years each as guest researchers.

FY Outputs

Collaborations

Hewlett-Packard, R. Stanley Williams, Interface properties of molecular electronic test structures

Naval Research Laboratories, James Kushmerick, Molecular test structure assessment

NIST Division 817, Dr. Neil Zimmerman, Metrology for nanoelectronic devices

NIST Division 837, Dr. L. Richter, Optical characterization of molecular and organic interfaces

NIST Division 837, John Henry Scott, High-resolution TEM studies of molecular test structures

NIST Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project

NIST Division 854, Dr. Eric Lin et al., Organic Electronics Competence Project

NTT, Akira Fujiwara, Si-nanowire metrology

The Pennsylvania State University, Prof. T. Mayer, Molecular electronics

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures

External Recognition

Elevated to IEEE Senior Member status (Curt A. Richter)

Recent Publications

J. Han, S. Koo, C. A. Richter, E. M. Vogel, "Influence of Buffer Layer Thickness on Memory Effects of $SrBi_2Ta_2O_9$ /SiN/Si Structures," Appl. Phys. Lett., Vol. 85, No. 8, pp. 1439-1441 (23-AUG.-2004)

L. J. Richter, C. S. Yang, P. T. Wilson, C. Hacker, R. D. van Zee, J. J. Stapleton, D. L. Allara, J. M. Tour, "Optical Characterization of Oligo(phenylene-ethynlyene) Self-Assembled Monolayers on Gold," J. Phys. Chem. B., Vol. 108, No. 33, pp. 12547-12559 (19-AUG.-2004)

C. Hacker, J. D. Batteas, J. C. Garno, M. Marquez, C. A. Richter, L. J. Richter, R. D. van Zee, C. D. Zangmeister, "Structure and Chemical Characterization of Self-Assembled Mono-Fluoro-Substituted Oligo(phenylene-ethynlyene) Monolayers on Gold," Langmuir, Vol. 20, No. 15, pp. 6195-6205 (22-JUNE-2004)

C. A. Richter, C. Hacker, L. J. Richter, E. M. Vogel, "Molecular Devices Formed by Direct Monolayer Attachment to Silicon," Solid State Electronics, Vol. 48, pp. 1747-1752 (17-JUNE-2004)

C. A. Richter, C. Hacker, L. J. Richter, "Molecular Devices Formed by Direct Monolayer Attachment to Silicon," Proceedings of the International Semiconductor Device Research Symposium, 2003 International Semiconductor Device Research Symposium, Dec 10-12, 2003, Washington, District of Columbia, pp. 417-418 (10-DEC.-2003)

C. A. Richter, C. Hacker, L. J. Richter, "Electrical Characterization of Molecular Monolayers Formed by Direct Attachment to Si," Workbook of the IEEE Semiconductor Interface Specialist Conference, IEEE Semiconductor Interface Specialist Conference, Dec 04-06, 2003, Arlington, Virginia, pp. P15-1-P15-2 (04-DEC.-2003)

C. A. Richter, D. R. Stewart, "Metrology for Molecular Electronics," GOMAC Digest of Technical Papers, GOMACTech 2003, Mar 31, 2003 to Apr 03, 2003, Tampa, Florida, Vol. 28, pp. 281-284 (31-MARCH-2003)

C. A. Richter, J. S. Suehle, M. D. Edelstein, O. Kirillov, R. D. van Zee, "Molecular Electronic Test Structures," Bulletin of the American Physical Society, Vol. 47, No. 1, pp. 285-285 (01-MARCH-2002)

Y. J. Cho, N. V. Nguyen, C. A. Richter, J. R. Ehrstein, B. H. Lee, J. C. Lee, "Spectroscopic Ellipsometry Characterization of High-κ Dielectric HfO_2 Thin Films and the High-Temperature Annealing on Their Optical Properties," Applied Physics Letters, Vol. 80, No. 7, pp. 1249-1251 (18-FEB.-2002)

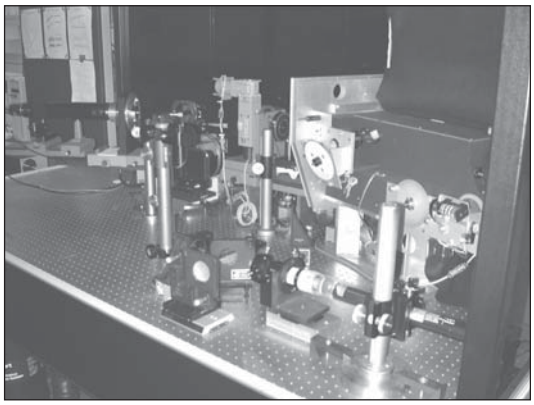
Electronic Materials Characterization

Technical Contact:
Joseph J. Kopanski

Staff-Years (FY 2004):
4 professionals
3 guest researchers

Goals

The goal of this project is to develop new or improved measurements, models, reference data, and measurement traceability mechanisms for select silicon CMOS front-end process technologies. Major focus is placed on metrology requirements for high-κ gate stacks (the bottom interface, the high-κ dielectric, the top interface, and the gate metal) and ultra-shallow junctions as detailed in the International Technical Roadmap for Semiconductors (ITRS). Additional work is undertaken as possible on low-κ materials, polymers, silicon-on-insulator (confined silicon), strained silicon-germanium, and compound semiconductors.



NIST custom-built high accuracy ellipsometer.

Customer Needs

Front end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2003 ITRS near-term (through 2009) difficult challenges for front end processes include: *metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization, introduction of metal gate electrodes with appropriate workfunctions, and metrology issues associated with 2D dopant profiling.*

Scaling is driving a continuous decrease in the gate dielectric film thickness. An effective oxide thickness of 1.0 nm with process control tolerance needs of less than 0.1 nm is being projected for the 0.1 μm CMOS technology node in 2006, dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below 2.0 nm, SiO_2 will be replaced, initially by oxynitride or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal-silicates. Spectroscopic ellipsometry (SE) is expected to continue as a preferred measurement for process monitoring of future gate dielectric films. Integrated Circuit (IC) fabrication metrology needs: (1) improved methods to determine film thickness; (2) techniques to determine the composition of films and the interfaces between them; (3) an improved understanding of the relationship between physical, electrical, and optical determination of film properties; and (4) mechanisms for traceability of measurements to NIST.

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon IC industry. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begins to influence device operation. Scanning Capacitance Microscopy (SCM) is a strong contender to provide two-dimensional carrier profiles. *Structural and elemental analysis at device dimensions (for example 3D dopant profiling) is identified in the ITRS as one of the challenges beyond 2009. Two- and preferably three-dimensional dopant profiling, activated dopant profiles, and related TCAD modeling and defect profiles are necessary for developing new doping technology.*

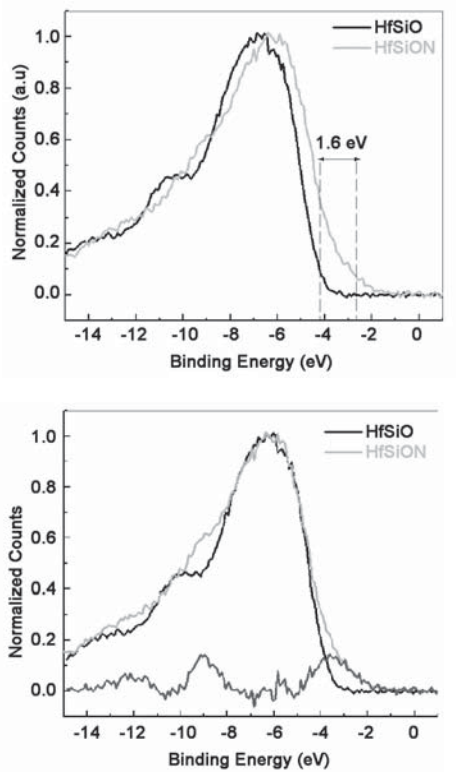
Technical Strategy

The Electronic Materials Characterization (EMC) project conducts research on front-end process topics for next-generation silicon ICs and also on a few beyond the roadmap technologies. Project staff are working with International SEMATECH, IC companies, SRC university staff, and other NIST researchers in the following focus areas:

Structural and Optical Models for Ellipsometry

We seek to develop spectroscopic ellipsometry (SE) measurement metrology and models required for high-κ materials and have them in place and on time for their introduction into standard fabrication processes. A custom-built, high-accuracy ellipsometer (see above figure) with a spectral range of 1.5 eV to 6.2 eV and a commercial vacuum ultraviolet (VUV) ellipsometer, which extends the spectral range to 9.5 eV, are available for this task. Project staff are optically characterizing advanced oxyni-

trides, oxide/nitride stacks, and more complex compounds, such as hafnium silicon oxynitride and hafnium-aluminum silicate. Since many of these materials have bandgaps just below 6 eV, the measurement range obtainable with the VUV ellipsometer enables the investigation of processing related structure in the index of refraction, which shows up in the absorbing region above the bandgap energy. Project work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and the variability of these parameters due to differences in fabrication processes. Work is also directed at extracting accurate bandgap values and interpreting the processing related structure found in the dielectric function. Analysis has been done primarily with software developed at NIST for SE, which allows the addition of the latest published or custom-developed optical response models for each material system investigated.



Soft X-ray photoelectron spectroscopy spectra of HfSiO and HfSiON thin films, which gives information about the valence band edge, but not about the full band-gap. Inclusion of nitrogen into the silicate network decreases the valence band offset (about 1.6 eV, top panel) by introducing states in the gap. A shift in the O2p edge is also observed. In the lower panel, the aligned spectrum is shown along with the calculated difference spectrum, which shows the states due to nitrogen.

DELIVERABLE: Determine the optical properties of technologically relevant high-κ thin films (ZrO_2, HfAlO, and Hf-based alloys) and their optical bandgaps by using VUV spectroscopic ellipsometry.

Relation Between the Optical, Electrical, and Physical Measurements of High-κ Material Properties

We seek to develop fundamental understanding of the physical properties of high-κ dielectric films via comparison of structural, optical, and electrical characterization. These multimethod studies utilize techniques such as transmission electron microscopy (TEM), soft X-ray photoemission (SXPS), X-ray absorption spectroscopy (XAS), grazing incidence angle X-ray diffraction (GIXRD), capacitance-voltage (C-V) and current-voltage (I-V) analysis, as well as SE, reflectivity, and FTIR-ATR.

DELIVERABLE: Determine the crystal structure of high-κ dielectric films by physical techniques and demonstrate the relevance of the crystalline phase to electrical properties and other important material properties.

Thin films of nominally the same composition prepared by different methods can have quite different physical and electrical properties and may be in metastable states. The crystalline phase of various high-κ dielectric films can depend on film thickness, stress, grain-size, and impurities. The degree of crystallinity, interface roughness, chemical homogeneity, and stoichiometry can have a direct effect on the dielectric properties and the leakage current across such dielectric layers. Strain, interface properties, and the effects of surface contamination species can also have important effects. The figure (see left) illustrates the use of XPS (as part of a study including SE and XAS measurements as well) to determine effects of the oxygen and nitrogen on the electrical properties of HfSiO and HfSiON films. SE is used to determine the dielectric function, XPS yields information about the valence band edge, and XAS can be used to determine the O:N ratio.

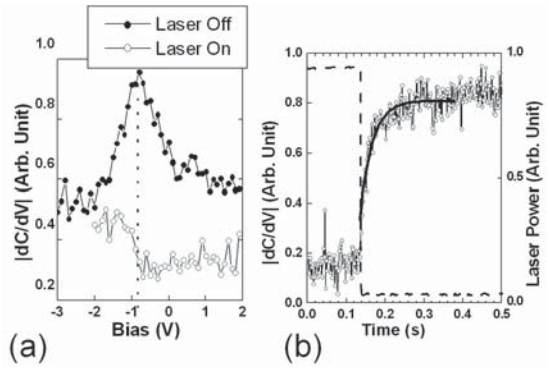
DELIVERABLE: Complete a systematic study of the valence band offsets of hafnium-based high-κ dielectric films. (The valence band offset is a critical parameter in determining leakage and power dissipation for a given dielectric composition.)

Metrology for Metal Gates

Channel autodoping associated with boron out-diffusion from the polysilicon gate and polysilicon depletion will eventually require the phase out of

dual-doped polysilicon gate material. Work function, resistivity, and compatibility with CMOS technology are key parameters for new candidate gate electrode materials. Different materials may be needed for the PMOS and NMOS transistor gates to achieve acceptable threshold voltages. Eventual introduction of single-gate, fully-depleted ultra thin body SOI devices with intrinsic channels will change the optimal values of the gate work function, suggesting that tunable workfunction systems are of high importance.

DELIVERABLE: Develop test structures and measurement capabilities to measure with high accuracy the metal gate work function and barrier height. Determine the differences in work function measurements from Scanning Kelvin Probe Microscopy (SKPM), Internal Photoemission (IPE), and MOS capacitor flatband voltage as a function of oxide thickness.



(a) dC/dV curves between the SCM tip and silicon with a thin oxide layer, measured with the AFM laser on and with the AFM laser off. (b) Transient capacitance signal measured as a function of time. The laser power intensity (dashed line) is used to synchronize the transient with the change in illumination. The carrier lifetime is estimated from an exponential fit to the measured transient.

Silicon Optical Constants and Advanced Silicon Materials

The project also conducts research into materials needed to extend CMOS beyond its current and conventional implementation. As part of this work, project members are using SE and Raman Scattering to characterize silicon-on-insulator materials, strained silicon, and other materials for confined silicon applications. We also have an effort to characterize silicon compatible light emitters and detectors.

DELIVERABLE: Determine the structural qualities of Silicon on Insulator by SE and Raman Scattering.

Metrology for Ultra-Shallow Junctions

We have developed tools that enable scanning capacitance microscopes to function as two-dimensional dopant profiling tools. This work is divided into three tasks. Task 1 is to develop SCM measurement methodologies. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. Task 2 is to develop theoretical models of the SCM. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Task 3 is the interpretation of SCM data and technology transfer. Our expertise with interpreting SCM images is being transferred to industry through our software program *FASTC2D*. The program features an easy to use interface, rapid profile extraction, and operation in a Windows environment. The figure (see left) shows an extension of the SCM measurement that uses a pulsed laser and precisely synchronized SCM measurements of the induced capacitance transient to obtain a local measurement of carrier lifetime with spatial resolution limited only by the carrier diffusion length.

DELIVERABLE: Demonstrate SCM-measured dopant profiles with improved spatial resolution through use of sample beveling and refined data interpretation.

Wide Bandgap Materials

Emerging wide bandgap (WBG) semiconductor materials, such as Gallium Nitride and Silicon Carbide, are capable of unique high-frequency, high-power, and high-temperature applications. As opposed to silicon, the materials technologies for WBG are relatively immature, with corresponding greater materials characterization needs. Solution of WBG materials based problems is the key to achieving device performance, yield, and reliability. We are developing three techniques that will provide information about WBG material quality and uniformity on both the wafer and device scale. Surface PhotoVoltage Spectroscopy is being used to measure diffusion length in GaN and SiC wafers. Diffusion length is an important indicator of crystalline quality for electrical applications, and the wafer-level uniformity of diffusion length would make for a non-destructive means of access wafer uniformity. Scanning Capacitance Microscopy and Scanning Spreading Resistance Microscopy are being used to measure quantitative dopant profiles in GaN and SiC, and are being used as a method for defect analysis. Wafer-level resistivity

mapping with a lithographic contact array provides wafer- and chip-level uniformity maps of substrate resistivity. Resistivity mapping also provides measurement of metal-semiconductor contact resistivity as a function of substrate doping.

DELIVERABLE: Demonstrate quantitative SCM-based dopant profiling and resistivity mapping of GaN and other wide bandgap semiconductors.

Accomplishments

- Completed participation in an international, multimethod investigation of the ability to measure the thickness of very thin SiO_2 films traceable to the SI unit of length. Participants included representatives from five national laboratories. Spectroscopic and single-wavelength ellipsometry measurements were contributed by project members. Results, analyzed by the sponsoring laboratory, the United Kingdom's National Physical Laboratory (NPL), were sufficiently encouraging to prompt the planning of a formal "key comparison."

- SE measurements and data analyses on two series of ZrO_2 in collaboration with the University of Minnesota and Stanford University showed that: (i) optical bandgap and the dielectric function of ZrO_2 increase with increasing film thickness; (ii) optical bandgap and the dielectric function of ZrO_2 increase when annealed at high-temperatures; and (iii) ZrO_2 phase changes from the amorphous state to the tetragonal polycrystalline state when the film thickness is greater than 80 Å or the film is annealed at a temperature above ~600 °C.

- Completed an extensive set of SE, SXPS, inverse photoemission, and TEM measurements on a specially designed set of SiO_2, SiON, HfO_2, $HfSiO_2$, and HfSiON films. This study investigated the effects of compositional components, particularly Hafnium and Nitrogen, on the dielectric function, band-gap, band offsets, and near band-edge density of states, as well as our ability to determine nitrogen concentration from ellipsometry measurements.

- Completed a set of SE, SXPS, internal photoemission, and Rutherford backscattering measurements on a family of HfTiO samples with varying compositional ratios; measurements were taken both before anneal and after anneal at three different temperatures. This material system, which potentially has a high enough dielectric constant for use as a 0.5 nm equivalent oxide thickness (EOT) dielectric, is believed to undergo some unusual structural changes when composition is within a narrow window around a 50:50 ratio of HfO_2:TiO_2 and the films are annealed at a temperature above about 700 °C. Under these conditions, the material appears to become a compound and crystallizes, which gives it the high dielectric constant.

- Completed comparison of oxide thickness determination methods of 2 nm SiO_2 films by Ellipsometry, C-V, and HRTEM/STEM. Determined that the dominant uncertainty in ellipsometer-based thickness (due to choice of optical model and best optical constants for the silicon substrate and the oxide film) was less than the uncertainty in C-V based thickness (due to differences resulting from available Q-M corrections for 2-D quantization of states in the silicon substrate and poly-layer depletion). However, the largest overall uncertainty results from the uncertainty of HRTEM-based thickness (approximately ±0.2 nm).

- Completed SE measurement and analysis for a set of hafnium aluminate films grown by Atomic Layer Chemical Vapor Deposition. Combined with HRTEM, RBS, and NRA measurements, the optical bandgaps and composition dependence of these films were determined and shown to vary with aluminum content in the films.

- Prototyped measurement techniques needed to characterize candidate gate metals for next generation CMOS with high-κ gate dielectrics. Fabricated test structures and extracted work function values using the flatband voltage as a function of oxide thickness method, Scanning Kelvin Probe Microscopy (SKPM), and Inverse Photo Emission (IPE). A mask set containing a variety of test structures with which to calibrate and compare these measurement methods has been designed and procured. The test structures contain up to four levels of different interleaved metal layers, MOS capacitors, and sheet resistors.

- From SE and Raman scattering data, we have shown that the SmartCut SOI wafers contain slight structural defects in the SOI layer. These defects manifest a slightly different dielectric function used for the SOI layer in the SE data analysis and the observation of a weak extra feature at 495 cm^{-1} in Raman spectrum that is not observed in the spectra of device quality crystalline silicon substrates.

- Implemented optical pumping and voltage spectroscopy of SCM for local measurement of carrier lifetime. Using a pulsed laser and precisely synchronized SCM measurements of the induced capacitance transient, local carrier lifetime can be

measured with spatial resolution limited only by the carrier diffusion length.

- Measured, for the first time, diffusion length of GaN using the Surface PhotoVoltage technique. Presented data at the Materials Research Society 8th Wide-Bandgap III-Nitride Workshop and at the 2004 American Physical Society March Meeting.

- Certified and transferred to sales inventory 160 sets of 3 different silicon resistivity Standard Reference Materials (SRMs). This brings to a total of just over 3000 the number of individually certified single-wafer and multi-piece sets of resistivity-based SRMs that have been put in stock over the lifetime of this activity.

Collaborations

Arizona State University, Candi Cook, Photoreflectance measurements of Ge:Sn:Si samples

Army Research Lab, SEDD, Kenneth Jones, GaN and SiC device, process, and material characterization

IBM, E. Gusev

International SEMATECH, P. Y. Hung, SE of high-κ dielectrics

NIST, 836 Process Measurements Division, J. Maslar and Roger van Zee, Molecular electronic thin film (SAM films)

NIST, 837, T. Jach and D. Simons

NIST, 852, I. Levin and L. Robins

NIST, 855, A. Davydov

Northrop-Grumman, J. Giagante, Boron and Aluminum implanted SiC for dopant profiling with SCM and SSRM

Northrop Grumman Corp., Advanced Technology Laboratories, Anthony Margarella, Oxynitride film characterization

Pennsylvania State University, Prof. R. Collins, SE modeling

Rutgers University, E. Garfunkel and R. Bartynski

Stanford University, P. J. McIntyre

Texas Instruments Inc., Drs. J. Chambers and M. Visokay

UCLA, Prof. J. Chang

University of Delaware, Prof. R. Opila

University of Minnesota, Prof. Campbell

Recent Publications

Y. D. Hong, T. Y. Yeow, W. K. Chim, K. M. Wong, J. J. Kopanski, "Influence of Interface Traps and Surface Mobility Degradation on Scanning Capacitance Microscopy Measurement," IEEE Trans. Electron Devices, Vol. 51, No. 9, pp. 1496-1503 (01-SEPT.-2004)

D. B. Migas, L. Miglio, M. Rebien, W. Henrion, P. Stauss, A. Birdwell, A. V. Davydov, V. L. Shaposhnikov, V. E. Borisenko, "Structural, Electronic and Optical Properties of B-($Fe_{1-x}Co_2$)Si_2," Phys. Rev. B, Vol. 69, pp. 115204-1-115204-7 (11-MARCH-2004)

A. Birdwell, T. J. Shaffner, D. Chandler-Horowitz, G. H. Buh, W. Henrion, M. Rebien, P. Stauss, G. Behr, L. Malikova, F. H. Pollak, C. L. Littler, R. Glosser, S. Collins, "Excitonic Transitions in B-$FeSi_2$ Epitaxial Films and Single Crystals," J. Appl. Phys., Vol. 95, No. 5, pp. 2441-2447 (01-MARCH-2004)

J. F. Marchiando, J. J. Kopanski, "On Calculating Scanning Capacitance Microscopy Data for a Dopant Profile in Semiconductors," J. Vac. Sci. Technol., Vol. 22, No. 1, pp. 411-416 (01-FEB.-2004)

G. H. Buh, C. Tran, J. J. Kopanski, "PSPICE Analysis of a Scanning Capacitance Microscope Sensor," J. Vacuum Sci. Technol. B, Vol. 22, No. 1, pp. 417-421 (01-FEB.-2004)

J. J. Kopanski, J. F. Marchiando, B. G. Rennex, D. S. Simons, Q. Chau, "Towards Reproducible SCM Image Interpretation," J. Vacuum Sci. Technol. B, Vol. 22, No. 1, pp. 399-405 (01-FEB.-2004)

T. Jach, J. A. Dura, N. V. Nguyen, J. Swider, G. Cappello, C. A. Richter, "Comparative Thickness Measurements of SiO_2 /Si Films for Thicknesses Less than 10 nm," Surf. Interface Anal., Vol. 36, No. 1, pp. 23-29 (01-JAN.-2004)

J. R. Ehrstein, C. A. Richter, D. Chandler-Horowitz, E. M. Vogel, D. R. Ricks, C. Young, S. Spencer, S. Shah, D. Maher, B. C. Foran, A. C. Diebold, P. Hung, "Thickness Evaluation for 2nm SiO_2 Films, a Comparison of Ellipsometric, Capacitance-Voltage and HRTEM Measurements," Characterization and Metrology for ULSI Technology: 2003, 2003 International Conference on Characterization and Metrology for ULSI Technology, Mar 24-28, 2003, Austin, Texas, No. 331, 336 pp. (30-SEPT.-2003)

D. Chandler-Horowitz, N. V. Nguyen, J. R. Ehrstein, "Assessment of Ultra-thin SiO_2 Film Thickness Measurement Precision by Ellipsometry," Characterization and Metrology for ULSI Technology: 2003, 2003 International Conference on Characterization and Metrology for ULSI Technology, Austin, Texas, pp. 326-330 (30-SEPT.-2003)

N. V. Nguyen, J. Han, J. S. Kim, Y.J. Cho, W. Zhu, Z. Luo, T. Ma, "Optical properties of Jet-Vapor-Deposited TiAlO and HfAlO Determined by Vacuum Ultraviolet Spectroscopic Ellipsometry," Characterization and Metrology for ULSI Technology: 2003, International Conference on Characterization and Metrology for ULSI Technology, Mar 24-28, 2003, Austin, Texas, pp. 181-185 (30-SEPT.-2003)

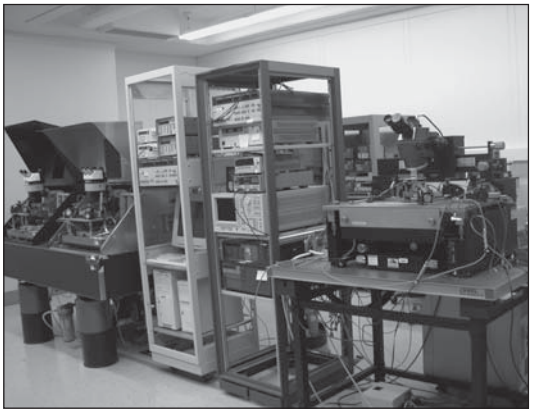
G. H. Buh, J. J. Kopanski, "Atomic Force Microscope Laser Illumination Effects on a Sample and Its Application for Transient Spectroscopy," Appl. Phys. Lett., Vol. 83, No. 12, pp. 2486-2488 (23-SEPT.-2003)

G. H. Buh, J. J. Kopanski, J. F. Marchiando, A. Birdwell, Y. Kuk, "Factors Influencing the Capacitance-voltage Characteristics Measured by the Scanning Capacitance Microscope," J. Appl. Phys., Vol. 94, No. 4, pp. 2680-2685 (15-AUG.-2003)

Advanced MOS Device Reliability and Characterization

Goals

The goal of this project is to provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future Metal Oxide Semiconductor (MOS) devices. The project aims to increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.



The project's newly renovated laboratory space.

Customer Needs

The MOSFET (Metal Oxide Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 2 nm is identified as a critical front-end technology issue in the SIA's International Technology Roadmap for Semiconductors (ITRS) with effective thickness values of 1.4 nm, or less, being projected in 2004, dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO_2 must be replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal-silicates.

Due to increased power consumption, intrinsic device reliability, and circuit instabilities associated with SiO_2 of this thickness, a high permittivity gate dielectric (*e.g.*, Si_3N_4, HfSixOy, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FETs) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

Technical Strategy

The strategy of this effort is to develop robust electrical characterization techniques and methodologies to characterize charge trapping kinetics, V_t instability, defect generation rates, and time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the metal oxide and silicate dielectrics for a variety of high-κ samples subject to different deposition and gate electrode processes. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization.

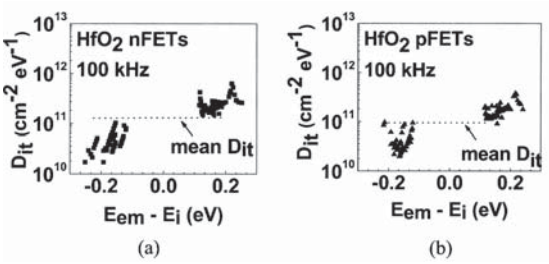
Technical Contact:
John S. Suehle

Staff-Years (FY 2004):
2 professionals
1 technician
3 guest researchers

"The success of this project's methodologies and its ability to provide standards for the entire U.S. industry is attested to by the fact that the same standards are now being adopted internationally and are being used in the qualification of offshore foundries."

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

The understanding generated in this research will be used to continue generating standard measurements through a NIST-coordinated collaboration between EIA-JEDEC (Electronic Industries Association-Joint Electron Device Engineering Council) and the ASTM (American Society for Testing and Materials). Studies on the reliability of high dielectric constant dielectrics also will be performed.



Energy distribution of interface traps as determined by rise and fall time dependence of charge-pumping currents for HfO_2-gated MOSFETs. (a) n-MOSFET. (b) p-MOSFET.

DELIVERABLE: Deliver experimental results of charge stability and trapping in HfO_2 films including defect generation rates due to constant voltage stress.

DELIVERABLE: Conduct gate polarity dependent studies of the long-term wear-out and breakdown of advanced high-κ dielectrics.

DELIVERABLE: Complete comparison study of various electrical techniques to determine interface trap spectra for a variety of control samples.

DELIVERABLE: Provide test technique(s) and analysis to quantify electrical trap densities at multiple interface stacks.

DELIVERABLE: Provide correlation study of electrical parameters to results from materials analysis on a select number of samples fabricated with different metal gate processing.

Accomplishments

■ *Energy dependence of interface traps in HfO_2 was characterized.* A series of experiments was conducted to characterize the energy dependence of interface trap density in *n* and *p*-channel HfO_2 FETs supplied by IBM. The study demonstrated that the mobility reduction observed in *n*-channel devices is due to positions of interface traps in the upper half of the Si energy band.

■ *New JEDEC standard, JESD-92, is published.* The standard describes several techniques that can be used to detect soft breakdown in ultra-thin gate oxides, where detection can be difficult. The standard also includes guidelines for designing test structures and data analysis procedures.

■ *Mechanistic study of progressive breakdown in small area ultra-thin gate oxides was completed.* A study was completed to investigate two gate oxides. One breakdown mode features a conducting filament that is stable until hard breakdown occurs, and a second mode features a filament that continually degrades with time. The acceleration factors are different for each mode, indicating different physical mechanisms are involved in the evolution and formation of the final hard breakdown event. Unstable filaments that result from the first soft breakdown progressively degrade and change physical structure until their leakage current becomes unacceptably large. A set of voltage and temperature acceleration parameters different from oxide wear-out is necessary to project the leakage current with time.

■ *Study of anomalous threshold voltage roll-up behavior observed in HfO_2 MOSFETs*. Reverse short channel effect (RSCE) was observed of high-κ (HfO_2 on SiON buffer, Al_2O_3 on SiON buffer) gated submicron n-MOSFETs. SiO_2 or SiON control samples show normal short channel effect (SCE) behavior. The possible causes such as inhomogeneous channel doping profile and gate oxide thickness variation near S/D ends have been ruled out. The results indicate that the channel length dependent interface trap density is the main cause of the RSCE, while oxide charge also plays a role.

FY Outputs

Collaborations

Agere Technologies, Ultra-thin gate oxide reliability

General Electric, Gate dielectric integrity of SiC electronics

Jet Propulsion Laboratory, Ionizing radiation effects in high-κ gate dielectric materials

N.C. State University (oxynitrides, nitrides, ultra-thin SiO_2), Alternative gate dielectrics

National Semiconductor, Ultra-thin gate oxide reliability

NIST Divisions 836, 837, 838, Roger van Zee et al., Molecular Electronics Competence Project

NIST Divisions 836, 837, 838, Roger Van Zee et al., Spectroscopic ellipsometry of molecular electronics

Penn State University, Ultra-thin gate oxide reliability

Sharp Microelectronics, Characterization of Hafnium-oxide dielectric films

International SEMATECH, Electrical and Reliability Characterization of HfO_2 based gate dielectrics

Texas Instruments, Ultra-thin gate oxide reliability

The Pennsylvania State University, Molecular electronics

University of Maryland, College Park, Ultra-thin gate oxide reliability

University of Maryland, Gate dielectric reliability

University of Minnesota, Alternate Gate Dielectrics

Standards Committee Participation

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

Invited Presentations

J. S. Suehle, "Reliability Implications of Scaling Gate Oxides in Deep Submicron CMOS Technologies," 2004 GOMACTech, Monterey, CA, March 2004.

J. S. Suehle, "Reliability Metrology for the Semiconductor Industry at NIST," 2004 GOMACTech, Monterey, CA, March 2004.

J. S. Suehle, "Reliability Year In Review: Gate Dielectrics," 2004 IRPS.

J. S. Suehle, "Long-Term Reliability Projection Issues for Ultra-Thin Gate Dielectrics," Workshop on Aging and Long Term.

E. M. Vogel, "Characterization Needs for Emerging Research Materials and Devices," ITRS Emerging Research Materials Workshop, San Francisco, CA, July 11, 2004.

E. M. Vogel, "Challenges of Electrical Measurements of Advanced Gate Dielectrics in MOS Devices," Applied Materials, February 9, 2004.

J. S. Suehle, "Reliability Characterization and Projection Issues of Advanced Gate Dielectrics," University of Maryland, Dept. of Reliability Engineering, March 3, 2003.

J. S. Suehle, "Potential Reliability Issues for Molecular Electronics," The Aerospace Corporation, Los Angeles, CA, December 5, 2002.

E. M. Vogel, "Issues with Electrical and Reliability Characterization of Advanced Gate Dielectrics," 12th Workshop on Dielectrics in Microelectronics, Grenoble, France, November 20, 2002.

J. S. Suehle, "Molecular Electronics: What Will Be the Reliability Issues?" 2002 Integrated Reliability Workshop, Lake Tahoe, CA, October 22, 2002.

Recent Publications

J. Han, S. Koo, C. A. Richter, E. M. Vogel, "Influence of Buffer Layer Thickness on Memory Effects of $SrBi_2Ta_2O_9$ /SiN/Si Structures," Appl. Phys. Lett., Vol. 85, No. 8, pp. 1439-1441 (23-AUG.-2004)

J. S. Suehle, B. Zhu, Y. Chen, J. B. Berstein, "Acceleration Factors and Mechanistic Study of Progressive Breakdown in Small Area Ultra-thin Gate Oxides," 2004 IEEE International Reliability Physics Symposium Proceedings, International Reliability Physics Symposium, Apr 25-29, 2004, Phoenix, Arizona, pp. 95-101 (29-APRIL-2004)

J. S. Suehle, "Reliability Implications of Scaling Gate Oxides in Deep Submicron CMOS Technologies," GOMAC Digest of Technical Papers, GOMACTech, Mar 15-18, 2004, Monterey, California, pp. 213-216 (18-MARCH-2004)

J. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. Heh, J. S. Suehle, "Asymmetric Energy Distribution of Interface Traps in n- & p- MOSFETs with HfO_2 Gate Dielectric on Ultra-thin SiON Buffer Layer," Electron Device Letters, Vol. 25, No. 3, pp. 126-128 (01-MARCH-2004)

J. S. Suehle, "Ultra-Thin Gate Oxide Breakdown: A Failure That We Can Live With?" Electronic Device Failure Analysis, Vol. 6, No. 1, pp. 6-11 (01-FEB.-2004)

E. M. Vogel, G. A. Brown, "Challenges of Electrical Measurements of Advanced Gate Dielectrics in Metal-Oxide-Semiconductor Devices," Characterization and Metrology for ULSI Technology: 2003, 2003 International Conference on Characterization and Metrology for ULSI Technology, Mar 24-28, 2003, Austin, Texas, pp. 771-781 (30-SEPT.-2003)

J. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. Heh, J. S. Suehle, "Energy Distribution of Interface Traps in High-κ Gated MOSFETs," Tech. Dig., VLSI Technology, 2003 Symposia on VLSI Technology and Circuits, June 10-14, 2003, Kyoto, Japan, pp. 161-162 (01-JUNE-2003)

D. Heh, E. M. Vogel, J. B. Bernstein, "Impact of Substrate Hot Hole Injection on Ultra-thin Silicon Dioxide Breakdown," Appl. Phys. Lett., Vol. 82, No. 19, pp. 3242-3244 (12-MAY-2003)

E. M. Vogel, C. A. Richter, B. G. Rennex, "A Capacitance-Voltage Model for Polysilicon-Gated MOS Devices Including Substrate Quantization Effects Based on Modification of the Total Semiconductor Charge," Solid-State Electronics, Vol. 47, pp. 1589-1596 (10-MARCH-2003)

E. M. Vogel, D. Heh, J. B. Bernstein, "Impact of the Trapping of Anode Hot Holes on Silicon Dioxide Breakdown," IEEE Electron Device Letters, Vol. 23, No. 11, pp. 667-669 (01-NOV.-2002)

Infrastructure for Integrated Electronics Design & Manufacturing

Technical Contact:
John Messina

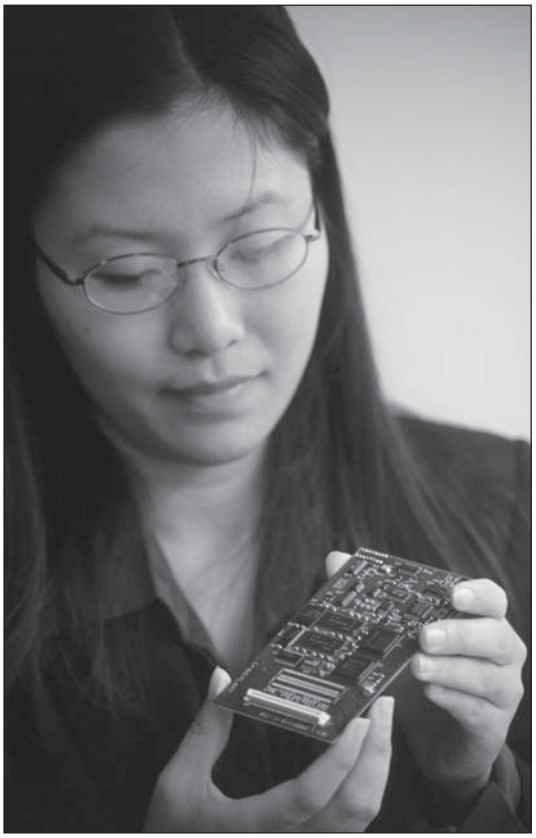
Staff-Years (FY 2004):
6.0 professionals
1.0 guest researcher

Goals

The primary goal of the Infrastructure for Integrated Electronics Design & Manufacturing (IIEDM) Project is to contribute actively to the technical development of neutral product data and e-manufacturing exchange specifications and advanced interoperable e-business infrastructure components. In pursuit of its primary goal, the IIEDM Project aids the growth of the electronics and semiconductor industries by providing two valuable services: technical expertise in an impartial forum in the development of standards and assistance in resolving interoperability issues between similar, and often conflicting, standardization efforts. The neutral nature of NIST allows industry consortia, academic bodies, and standards organizations to accept free technical advice on how to improve their data exchange standards from the IIEDM staff without concerns of favoritism or bias. This impartiality enables the IIEDM Project to work with groups of industry members to solve data exchange problems that are facing the industry as a whole. The second service that the IIEDM project provides focuses on helping the industry deal with multiple conflicting and overlapping standards. Due to the nature of the industry, with no single organization dictating standard development, companies are often faced with no clear optimal choice when it comes to data exchange standards. The IIEDM staff focus on creating environments in which companies can evaluate newly emerging standards and how differing standards can interoperate with each other successfully.

Customer Needs

To maintain a globally competitive posture, semiconductor and electronics manufacturers are quickening their pace of production and innovation. Electronic products are transitioned rapidly to a commodity status, production sites are constructed and decommissioned in shorter timeframes, and manufacturers are globally outsourcing an expanding scope of production process — and in some cases, the entire design and production process. To achieve the flexibility and quick turn-around they require, manufacturers rely on a distributed supply network and the ability to "mix and match" hardware and software within their own enterprise. This rapid reconfigurability needed by industry depends upon a robust IT infrastructure, consisting of standards for collaboration, business process integration, and the exchange of technical data. Industry also needs neutral test beds in which to evaluate new standards and the risks associated with technology adoption.



Ya-Shian Li holds a printed circuit board. The project brings printed circuit board standards development techniques and technologies to the semiconductor industry.

Technical Strategy

This project is working with industry to enable the infrastructure needed to support electronic commerce for both electronic components and manufacturing. The technical areas being addressed by this project are: the fundamental terminology used to describe components, the organization of the component data and metadata, and the ability to access this data and incorporate it into a product's lifecycle from design all the way through manufacturing. Development of standards within this do-

main is crucial in order for U.S. electronics and semiconductor manufacturers to take advantage of the global marketplace. This project assists industry in the development of standards that are critical to the infrastructure, but that no single company will pursue because of the broad-based benefit. Industry and standards groups in Japan and Europe are actively working on electronic commerce and manufacturing related projects. In working with these groups, NIST will try to minimize the overlapping standards development and ensure interoperability between U.S. and international standards.

DELIVERABLE: Organize an international effort to support the inclusion of material component information into existing electronic dictionaries formats.

One key aspect of this work, as identified by industry, is the need for on-line traceable dictionaries in order to distribute electronic component data effectively via the Internet. On-line dictionaries enable the industry to evaluate electronic component information properly. In support of on-line dictionaries, NIST has been working with large industry consortiums and standards groups, such as RosettaNet and the IEC, providing technical expertise in the design of both the electronic dictionary formats and the software tools necessary to access and use those newly created dictionaries.

While the project's original work focused on creating a common electronic dictionary format usable by everyone. It soon became evident that the electronics industry would always create new dictionaries that were focused on very specific domains, and these separate dictionaries would be in different formats. At that point, the project switched from creating a generic dictionary format to organizing an international effort to ensure that all the different dictionary formats would be interoperable with each other. Under the umbrella of the IEC Technical Committee 93 Working Group 6, the IIEDM staff have been working to create international dictionary mapping experiments that study the overall interoperability problems and try to determine the steps that can be taken by current and future dictionary formats to ensure interoperability between all the electronic dictionary formats.

DELIVERABLE: Develop a package of software tools designed to support the electronics industry migration from the Gerber file format to the new IPC 2581 standard.

In conjunction with the dictionary work, the IIEDM Project continues to work with the electronics manufacturing industry, identifying and addressing new electronic data exchange needs. One aspect of the project's continuing work with the electronic industry is working with the National Electronics Manufacturing Initiative (NEMI) on their bi-annual roadmapping activity. NEMI's roadmap seeks to survey the electronics industry and identify the major development trends for the industry for the next two years. By working with NEMI on the roadmapping activity, the IIEDM Project has the ability to work with industry to identify future needs and start developing solutions to those needs early enough to be in place by the time they are needed.

In addition to its activities within the electronics manufacturing industry, the IIEDM Project is taking its technical expertise in designing electronic data exchange specifications and applying it to the semiconductor industry. In the Printed Circuit Board (PCB) industry, the move toward outsourcing over the last several years has pushed the development of data standards that can accurately exchange product information between any two partners in a manufacturing design chain. This exchange of information can occur anywhere in the process from trading purchase order information between trading partners to exchanging design information between factory floor equipment. The semiconductor industry is now facing the same need to outsource various manufacturing and design activities that the PCB industry faced several years ago. While the actual standards needs are different for the semiconductor industry due to the differing manufacturing process and the products being developed, the design process for making the needed standards is still the same. Toward that end, the IIEDM Project is teaming up with leading industry consortiums and companies in the semiconductor industry in order to address their data exchange needs. The project's activities include becoming involved in standards development activities, developing prototype software systems to test new standards, and leading roadmapping activities to help identify future industry problems.

DELIVERABLE: Develop an augmented domain modeling environment for standards development that improves the quality of the standards through the use of software visualization tools.

Accomplishments

- NIST chaired the IEC Technical Committee 93 Working Group 6 that authored the IEC report 61908

"The valuable conversion of the formats to XML Schema was not a simple one. NIST personnel spent significant and painstaking efforts to ensure that the finished format is the best it can be."

IPC Award Speech at IPC Printed Circuits Expo (APEX), February 2004 on the development of the IPC 2581 standard board format

"NIST provides unique capabilities that have greatly improved the definition of industry standards that are required for useful implementation of data collection software capabilities for e-Manufacturing"

International SEMATECH letter to NIST, July 8, 2004

"The Technology Roadmap for Industry Data Dictionary Structure, Utilization and Implementation." The report studied interoperability for electronic dictionary formats on an international level and has been accepted by the IEC as a Final Draft International Standard (FDIS).

- Developed a new software tool ("Hydra 3D") which is a unique three-dimensional viewer and editor for XML files. The software is currently available on CD ROM and on the Internet (http://hydra3d.sourceforge.net).

- Established a new work agreement with International SEMATCH (ISMT) in order to bring the project's standards development skills from the printed circuit board industry to the semiconductor industry. The collaboration between NIST and ISMT has had considerable success within its first year with the various tasks leading to four submissions being accepted to ISMT's Advanced Equipment Control/Advanced Process Control (AEC/APC) Symposium XVI.

- Helped the Institute for the Packaging of Electronic Circuits (IPC) complete a new board layout standard IPC 2581 "Offspring" designed to be the next generation replacement for the Gerber board layout currently being used by industry.

- Developed several software tools designed to assist with industry's adoption of the IPC 2571 standard including an IPC 2571 board viewer tool and a Gerber to IPC 2571 software translator.

- Chaired the NEMI 2004 Roadmapping activity designed to identify future industry issues on product lifecycle management.

FY Outputs

Collaborations

We are currently working with ISMT, a leading semiconductor industry consortium, by providing technical expertise in the development of data exchange specifications and reference software implementations.

We are working with the IPC on the development of software tools to assist the industry in the migration from Gerber board layouts into the new IPC 2571 standard board layouts.

We are currently working with a group of organizations (RosettaNet, Electronic Commerce Code Management Association [ECCMA], and the IEC) on electronic formats for dictionary and parts catalogues.

External Recognition

The "3D Hydra" software tool and an accompanying paper were accepted at the Extreme Markup Conference 2004 in Montreal, Canada, and at the 31st International Conference on Computer Graphics and Interactive Techniques (SIGGRAPH 2004).

The IIEDM Project Leader, John Messina, was invited to give a talk on electronic dictionaries and parts catalogues at the ECCMA 4th Annual Conference.

The IPC gave NIST an award for its significant and painstaking efforts in the development of the IPC 2571 standard.

ISMT sent NIST a letter thanking the IIEDM Project for its efforts in the development of data exchange specifications and software tools for the semiconductor industry.

The collaboration between NIST and ISMT led to four papers on XML standard work being accepted at ISMT's Advanced Equipment Control/Advanced Process Control (AEC/APC) Symposium XVI.

Recent Publications

Y. Li, B. Van Eck, E. Simmon, "Running Out of Time: Improvements Required in Current Semiconductor Factory and Equipment Clock Synchronization for Supporting Future Real-Time Data Collection," AEC/APC Symposium XVI Proceedings/(CD format), AEC/APC Symposium XVI, September 18-23, 2004, Westminster, CO, USA. (23-SEPT.-2004)

E. Simmon, G. Crispieri, "Measuring the Performance of XML-Based Data Standards," AEC/APC Symposium XVI Proceedings, AEC/APC Symposium XVI, September18-23, 2004, Westminster, CO, USA (23-SEPT.-2004)

A. Griesser, "Ensuring High Quality Data Transfer Standards," AEC/APC Symposium XVI Proceedings (CD format), AEC/APC Symposium XVI, September 18-23, 2004, Westminster, CO, USA (23-SEPT.-2004)

M. L. Aronoff, J. V. Messina, K. G. Brady, "Seeing in Three Dimensions: an Alternative Technique for Viewing Large Information Spaces," NISTIR 7093 (30-AUG.-2004)

M. L. Aronoff, "Hydra Users' Guide," NISTIR 7087 (30-AUG.-2004)

J. D. Gale, Y. Li, "Time Synchronization for Electronic Distributed Systems," NIST Interagency/Internal Report (NISTIR) 7116 (28-MAY-2004)

D. Zwemer, M. Bajaj, R. Peak, T. Thurman, K. G. Brady, S. McCarron, A. Spradling, M. Dickerson, L. Klein, G. Liutkus, J. V. Messina, "PWB Warpage Analysis and Verification Using an AP210 Standards-based Engineering Framework and Shadow Moiré," 5th International Conference on Thermal, Mechanical and Thermo-mechanical Simulation and Experiments in Micro-electronics and Micro-systems, EuroSimE 2004, May 11-13, 2004, Brussells, Belgium, pp. 121-132 (10-MARCH-2004)

Y. Li, B. Van Eck, "Semiconductor Factory and Equipment Time Synchronization," NIST Interagency/Internal Report (NISTIR) 7088 (25-FEB.-2004)

Y. Li, B. L. Goldstein, "Semiconductor Industry IT Needs: Lessons Learned from Across the Engineering Chain," 12 p. (01-JUNE-2003)

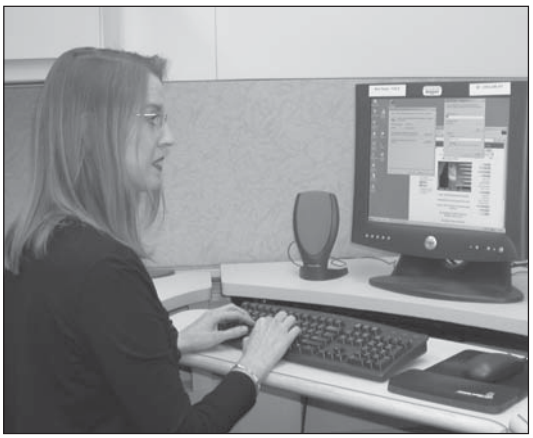
Knowledge Facilitation

Goals

- To eliminate paper-intensive and manual operations by automating tasks, decreasing the administrative requirements of the technical and support staff, increasing responsiveness to customers, and implementing a secure eNIST paperless environment.

- To provide Information Technology security policies, procedures, guidelines, and baselines and ensure compliance with Federal Information Security Management Act (FISMA) requirements.

- Develop an XML schema based security model for information sharing for the Department of Justice.



Jennifer Kostick configures a machine to use the Landesk centralized support software in order to increase security and centralize PC support.

Customer Needs

Scientists need time to work on their research, testing, calibrations, etc. However, managers need project plans, status, and similar information, and customers should have access to information in a timely manner. To best enable all of these functions, we have developed several web-based applications to minimize the time and efforts of technical staff and project leaders, while providing customers with up-to-date information.

As more and more of our data is stored electronically, it is natural to progress toward sharing the information, maximizing the benefits while minimizing the number of times it has to be entered.

As we grow to rely on the data in our computers, and that data is shared more frequently, the need for security of that data also grows. Our customers depend upon the confidentiality, integrity, and availability of the information. Confidentiality refers to allowing access to our data only to the people who should have it. Integrity refers to ensuring the data is what it should be and no one has tampered with it. And, availability refers to making sure the data is there when it is needed.

The Federal Government has established FISMA Guidelines that allow agencies to provide more secure information systems within the Federal Government including the critical infrastructure of the United States. These guidelines provide a framework for us to develop and implement policies and procedures, implement training and awareness programs, and secure our assets.

Through our experience and knowledge gained from internal efforts of securing our electronic transfer of data, we have been given the opportunity to assist the justice community in their efforts. We are assisting a global group of justice organizations made from local, state, tribal, federal, and international justice entities to develop an XML schema based security model allowing the justice and safety community to share information securely. The sharing of information is critical to provide timely defense to ensure safety. Protecting the confidentiality, integrity, and availability of that information is paramount.

Technical Strategy

A web-based application has been created to store and track all of the Electronics and Electrical Engineering Laboratory's publications and reports provided to management. Management is able to obtain access to the information they need easily, and the administrative burden on the technical staff has been alleviated. Generation of required paperwork has been automated, removing that responsibility from the support staff. The applications also serve as a warehouse for all publications and reports.

We developed the Information System to Support Calibrations (ISSC), which is a structured-query language database-driven application. The ISSC stores all of the administrative, technical, and financial data involved with items calibrated at NIST. The system has over 250 NIST users and provides status information to over 1400 calibration customers. The web-based system allows access from an unlimited number of different machines and

Technical Contact:
Jennifer A. Kostick

Staff-Years (FY 2004):
1.0 professional
0.5 guest researcher
1.0 student

operating systems used by personnel at NIST. The ISSC has reduced the time to complete the required paperwork by automating the entire workflow process. The ISSC was migrated to Technology Services for maintenance in 2003. We are collaborating with the National Research Council (NRC) Institute for National Measurement Standards (INMS) to assist them in the development of an application similar to the ISSC.

A project reporting system, also developed as a web application, is being created to reduce the duplication of the storage of information while providing management with immediate access to project data without interrupting project staff. This application contains all project-related information such as funding, milestones, staff, etc. Access to the application is controlled by a role-based access control — what you have access to is contingent upon who you are.

A web-based information system is being developed to support the clean rooms. Scientists will use the system to reserve equipment in the clean rooms. The system will automatically keep track of the time that equipment is used. Access will be limited to staff with proper training. This is being developed in collaboration with Stanford University.

A web-based information system was created to log and track all paper documents through the administrative process. Status of required paperwork can be easily determined.

A web-based information system was developed for use by NIST's Conference Facilities personnel to automate all the processes of conferences from registration to billing.

To ensure the security of our systems, we have developed and implemented IT Security policies and procedures and a training and awareness program. We have met all FISMA requirements, such as developing detailed security plans, risk assessments, self assessments, security tests and evaluations, rules of behavior, business impact analysis, contingency plans, plans of actions and milestones, asset inventories, and architecture and network diagrams for all of the systems within EEEL.

To augment the efforts of the Security Working Group of the Global initiative to create a security model for information sharing in the justice communities, we created a Unified Modeling Language (UML) model from the document developed by the group, Applying Security Practices to Justice Information Sharing. The UML diagrams were created from each category of the Justice Interconnection Services (JISN) Model section. At this stage of the project, the information used to create the UML diagrams is a literal translation from the text. In the next stage, efforts will be taken to weed out the redundant information and shape the diagrams based on input from both the text and the designers of the diagrams. This will help to create a more natural means to express the JISN text into UML.

Accomplishments

- Implemented Information System to Support Calibrations (ISSC) NIST-wide.
- Transitioned ISSC to Technology Services.
- Met annual FISMA requirements.
- Developed Bibliography Information System.
- Developed NIST Conference Registration System.
- Created Electronic Logbook.
- Created Document Information System.
- Developed UML model for information sharing in the justice community.

FY Outputs

Collaborations

Kevin Brady is collaborating with Stanford University in the creation of the Clean Room Information System.

Jennifer Kostick is collaborating with the National Research Council (NRC) Institute for National Measurement Standards (INMS) to assist them in the development of an application similar to the ISSC.

External Recognition

Kevin Brady, Jennifer Kostick, and John Messina received the Department of Commerce Bronze Medal Award for their work with the ISSC.

Recent Publications

J. Lindeman, "Information System to Support Calibrations (ISSC) Data Entry User's Tutorial" (27-MARCH-2003)

Major Facilities / Laboratories

Microfabrication Process Facility

See next page for facility description

Contacts: Russell Hajdaj, 301-975-2699
Richard Roppolo, 301-975-2096

Materials Characterization Labs

High-Resolution Optical:

Spectroscopic Ellipsometry, High-Resolution Fourier Transform Infrared Spectroscopy, Photoluminescence, Raman Scattering, Photoreflectance, and other Modulation Spectroscopies

Electrical:

Resistivity, Spreading Resistance, Lifetime, Hall Effect, Deep-Level Transient Spectroscopy, Deep-Level Optical Spectroscopy, Charge-Pumping Measurements, Capacitance-Voltage (high frequency & quasi-static), Surface Photovoltage, AC Impedance Analysis, Scanning Capacitance/Atomic Force Microscopy

X-Ray:

Double-Crystal Rocking Curve, Laue Orientation Facility

Device and Test Structure Characterization Labs

Electrical and Thermal Package Evaluation
Power Device Model Extraction and Validation
Packaging, Assembly, and Bonding Evaluation
Package Interconnect
Scanning-Electron Microscope
Scanning-Probe Microscope
Automatic Wafer-Level Measurement
Gate Dielectric Integrity
MEMS Electrical, Mechanical, Optical, and Microwave

Computer-Aided Design Labs

Test Structure Layout and Design
Integrated Circuit Layout, Design, and Simulation
Finite Element Thermal Analysis Tools and Computational Fluid Simulations
System, Device, Process, Interconnect, and Virtual Fabrications Simulations

Microfabrication Process Facility

Description

As integrated circuit (IC) sizes increase to more than 1 cm^2 and feature sizes within the circuits decrease to less than 1 μm, critical demands are placed on the measurement capability required to control and monitor IC fabrication successfully. To meet the demand, NIST researchers are developing state-of-the-art measurement procedures for microelectronics manufacturing.

The Microfabrication Process Facility provides a quality physical environment for a variety of research projects in semiconductor microelectronics as well as in other areas of physics, chemistry, and materials research. The laboratory facilities are used for projects addressing many areas of semiconductor materials and processes, including process control and metrology, materials characterization, and the use of IC materials and processes for novel applications.

The laboratory complex, approximately half of which is composed of Class 1000 cleanroom space, occupies about 2900 square meters. Within the cleanroom, work areas are maintained at Class 100 or better. The facility is designed so the work areas can be modified easily to accommodate the frequent equipment and other changes required by research.

Metallization: sputter and evaporation.

Objective

Current objectives are to develop and fabricate structures and devices to fulfill the needs of metrology projects within SED and NIST. These structures include MEMS-based devices, microelectronic devices, and other specialized devices.

Capabilities

The facility has a complete capability for IC fabrication. A list of principal processing and analytical equipment follows.

Diffusion, Oxidation, and Annealing

Six furnace tubes for up to 75 mm diameter wafers and five tubes for up to 100 mm diameter wafers.

Mask Alignment

The Karl Suss Mask Aligner model MA/BA6 is capable of sub-micron resolution (< 0.75 μm) and also has the ability to expose the backside of a substrate, which can be aligned to the front side features. The tool also is designed to be upgraded to a wafer-to-wafer bond aligner.

Plasma Etching and Deposition

The Unaxis 790, a plasma etching and deposition system, is capable of etching Si, SiO_2, Silicon Nitride, and polyamides. Low temperature (< 300 °C) film depositions of SiO_2 and silicon nitride can also be accomplished using Plasma Enhanced Chemical Vapor Deposition.

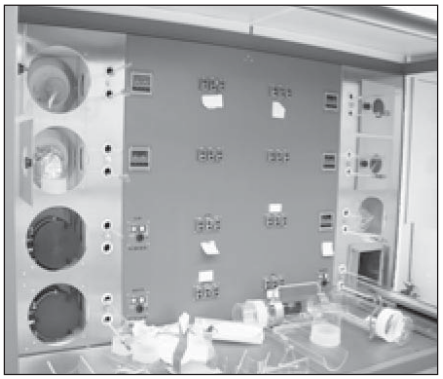
Unaxis 790 plasma etching and deposition system. [Property of Unaxis Wafer Processing, reprinted with permission]

Photolithography

Research mask aligner (proximity and contact) for wafers up to 100 mm in diameter and irregularly shaped samples and 10 × direct-step-on wafer system for 75 mm diameter wafers. Photoresist spin coating and developing and related chemical processing, including oxygen plasma stripping. E-beam writing and scanning electron microscope examination for nano-features on 75 mm diameter wafers.

Film Deposition

Low-pressure chemical vapor deposition systems for depositing silicon nitride, polysilicon, and low-temperature silicon dioxide. Radio frequency and dc vacuum sputtering of metals and dielectrics.



Film deposition and diffusion furnaces.

Etching

Wet and dry etching processes. Plasma barrel etching of nitride films and wet chemical etching of silicon for micromachining. Xenon Difluoride silicon etch process.

Wet chemical processing.

Analytical Measurements

Thin-film reflectometry and other thickness measurements, optical microscopy, and grooving and staining. Detak 6M Profilometer providing step height measurements and thin film stress analysis software.

Post Processing Equipment

DISCO HI-Tech America Inc. 8" wafer dicing saw and SEM cross section sample prep equipment.

Applications

Small quantities of specialized semiconductor test specimens, experimental samples, prototype devices, MEMS, and BioMEMS structures can be produced. The processes and processing equipment can be monitored during operation to study the process chemistry and physics. The effects of variations in operating conditions and process gases and chemical purities can be investigated. Research is performed under well-controlled conditions.

A research-oriented facility, the laboratory is not designed to produce large-scale ICs or similar complex structures. Rather, the laboratory emphasizes breadth and flexibility to support a wide variety of projects.

Automatic 8" wafer dicing saw.

Currently, research projects address many aspects of microelectronic processing steps and materials as well as silicon micro-machining. Examples include: metal-oxide-semiconductor measurements; metal-semiconductor-specific contact resistivity; uniformity of resistivity, ion-implanted dopant density, surface potential, and interface state density; characterization of deposited insulating films on silicon carbide; ionization and activation of ion-implanted species in semiconductors as a function of annealing temperature; electrical techniques for dopant profiling and leakage current measurements; and processing effects on silicon-on-insulator materials. A simple Complementary

Metal-Oxide Semiconductor (CMOS) process has been established. Recent work has also begun in the field of molecular electronics.

Availability

Facility staff welcome collaborative research projects consistent with the research goals of the NIST semiconductor program. Work is performed in cooperation with the technical staff of the laboratory.

The most productive arrangements begin with the development of a research plan with specific goals. The commitment of knowledgeable researchers to work closely with NIST staff and the provision of equipment and other needed resources are required. Because hazardous materials are present, laboratory staff must supervise all research activities.

Tasks

- Fabrication of test structures on silicon and gallium nitride (MIS) for AFM
- Fabrication of a refrigerant expansion valve using sub resist (1200 nm)
- Investigation of neuron growth in microfluidic devices
- Development of nano-metrology standards based on surface atomic spacing
- Fabrication of a magnetic spin inject device

NIST Advanced Measurement Laboratory Nanofabrication Facility

Goals

The NIST Advanced Measurement Laboratory (AML) Nanofabrication Facility (NF) will: enable fabrication of prototypical nanoscale test structures, measurement instruments, standard reference materials, electronic devices, MEMS, and bio-devices critical to NIST's Strategic Focus Areas (Nanotechnology, Homeland Security, Biosystems and Health) and the Nation's Nanotechnology Needs; provide access to expensive nanofabrication tools, technologies, and expertise in a shared-access, shared-cost environment to NIST and its partners; foster internal collaboration in nanotechnology across NIST's Laboratories; and foster external collaboration in nanotechnology with NIST's partners.

Customer Needs

To continue to respond to U.S. science and industry's needs for more sophisticated measurements and standards in the face of heightened global competition, NIST is constructing one of the most technologically advanced facilities in the world - the Advanced Measurement Laboratory, or AML. The NIST Nanofabrication Facility (NF) is one of five buildings in the AML at the Gaithersburg, MD, campus. The AML Nanofabrication Facility will provide researchers at NIST working on a variety of semiconductor and other nanotechnology research the ability to fabricate prototypical nanoscale test structures, measurement instruments, standard reference materials, and electronic devices.

Technical Strategy

The AML contains 2 above ground instrument buildings, 2 completely below ground metrology buildings, and 1 class 100 clean room building which will house the NIST AML Nanofabrication Facility. The AML will provide NIST with superior vibration, temperature and humidity control, and air cleanliness. The NIST AML NF has approximately 1672 m^2 of Class 100, raised floor, bay and chase, clean room space. NIST has invested in a complete suite of new equipment (capable of processing 150 mm wafers) that will be installed over the upcoming year. This includes furnaces (2 banks of 4 tubes each), LPCVD (poly, nitride, LTO), rapid thermal annealer, 3 reactive ion etchers (SF_6/O_2, Metal, Deep), 3 metal deposition tools (thermal, e-beam, sputterer), contact lithography (front- and back-side alignment), e-beam lithography, focused ion beam, and numerous monitoring tools (FESEM, spectroscopic ellipsometer, contact profilometer, 4-point probe, microscope with image capture, etc.).

The NIST Advanced Measurement Laboratory.

The NF will be operated as a shared-access user facility. This means that the staff of NIST and its partners, subject to provisions, training, and user fees, will be permitted to operate the equipment independently. The tools will be operated in a manner such that a wide variety of materials can be processed. The facility will be directed by NIST's Semiconductor Electronics Division. Unlike other NFs, the AML NF is unique in that, being located at NIST, it is next to the most advanced metrology tools in the world, and its focus will be on fabricating nanoscale structures necessary for metrology and standards in support of the semiconductor industry, nanotechnology, biotechnology, and homeland security.

It is anticipated that the fit up of the facility and equipment will be completed by the first quarter of 2005, with the facility becoming fully operational by the fourth quarter (also 2005).

Technical Contacts:
Eric M. Vogel
Russell Hajdaj

"The planned AML, with clean-room capability that is to be shared by all NIST laboratories, is believed to be essential to support the exacting future metrology needs that have been identified by the semiconductor and other nanotechnology industries."

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

National Research Council (NRC) Post-Doctoral Opportunities

The Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), in cooperation with the National Research Center (NRC), offers awards for post-doctoral research for American citizens in the fields described below. The Division conducts research in semiconductor materials, processing, devices, and integrated circuits to provide, through both experimental and theoretical work, the necessary basis for understanding measurement-related requirements in semiconductor technology.

NIST affords great freedom and an opportunity for both interdisciplinary research and research in well-defined disciplines. These technical activities of NIST are conducted in its laboratories, which are based in Gaithersburg, a large complex in a Maryland suburb of metropolitan Washington, DC. Applications for NIST Research Associateships are evaluated by the panels only during February. To be eligible for review in February, completed application materials must be postmarked no later than February 1, 2005. This time will also be approximately the same in 2006.

Molecular Electronics: Electrical Metrology

In Molecular Electronics — a field that is predicted to have important technological impacts on the computational and communication systems of the future — molecules perform the functions of electronic components. We are developing methods to reliably and reproducibly measure the electrical properties of small ensembles of molecules in order to investigate molecular conduction mechanisms. Specifically, we are developing test-structures based on nanofabrication and MicroElectroMechanical Systems processing techniques for assessing the electrical properties and reliability of moletronic molecules. In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties will be correlated with systematic characterization studies by a variety of probes and the results used in the validation of predictive models. This task is part of a cross-disciplinary, inter-laboratory effort at NIST, whose overall role is to develop the measurement science that will enable molecular electronics to blossom into a viable industry.

Contact: Curt A. Richter, 301-975-2082, or John S. Suehle, 301-975-2247

Scanning Probe Metrology

We are developing scanning probe microscopes to characterize and manipulate the physical and electrical properties of electronic devices, semiconductors, and related materials at the nanometer resolution scale. Projects are aimed at impacting silicon technology 5 to 10 years in the future or at characterization problems unique to compound semiconductors, molecular electronic devices, or quantum devices. We recently developed scanning capacitance microscopy as a tool for measuring the two-dimensional dopant profile across a silicon p-n junction. We are particularly interested in projects to develop techniques to measure material properties in three dimensions and that have spatial resolution below 1 nm. Our interests extend to other scanning probe techniques, including variable temperature scanning tunneling microscopy in UHV, surface photovoltage microscopy, and other optically pumped probes.

Contact: Joseph J. Kopanski, 301-975-2089, or David G. Seiler, 301-975-2054

Electrical Overlay- and CD-Metrology Development for Characterization of Advanced Lithography Instruments

Projected CD and overlay control-tolerances for new generations of ICs are reducing metrology uncertainty down to the several-nanometer region. However, the development of CD and overlay metrology is not keeping pace with lithographic resolution capabilities of advanced imaging systems. In addition, preferred processing options such as chemical/mechanical polishing tend to render existing overlay-metrology less effective for key process steps. The Enabling Devices and ICs Group seeks individuals interested in conducting further research in: (1) novel electrical overlay-sensing instruments and techniques; (2) the design and optimization of reference materials for scatterome-

try metrology; (3) noncontact electrical CD-measurement and extraction methodologies; and (4) design, fabrication, and certification of CD standards in the range 0.05 μm to 0.10 μm. We also encourage applicants with research experience in noncontact/nonintrusive electrical CD extraction and multimode overlay-sensor development, including MEMS-based overlay and CD reference-material implementations.

Contact: Michael W. Cresswell, 301-975-2072

Novel Test Structures for Characterizing the Performance of Advanced Multilevel Interconnection Systems

As the complexity of advanced integrated circuits continues to increase, new materials (copper, low-κ dielectrics) need to be characterized in order to perform parameter extraction for modeling on-chip interconnect systems. Extensions of traditional wiring technologies are no longer practical. The Enabling Devices and ICs Group seeks individuals interested in developing electrical test structures, measurement methods, and analysis models needed to evaluate copper based, multilevel interconnection systems. Of particular importance are methods to measure interconnect and barrier film thickness, dimensional control, by filling, interfacial contact resistance, planarity, defect density/yield, dishing, stress effects, median-time-to-failure, and high-frequency performance. Emphasis is placed on developing test structures for use with high-measurement speed, low-frequency electrical test techniques.

Contact: Michael W. Cresswell, 301-975-2072

Electrical and Optical Characterization of Semiconductors and Devices

Research focuses on understanding the electronic, optical, and magneto-optical behavior of semiconductor materials and devices. Areas of interest include the role of impurities and native defects in bulk crystals, and novel and useful properties induced by quantum confinement in reduced dimensional structures (heterostructures, quantum wells, superlattices, and quantum wires and dots). A broad range of optical techniques is available for reflection, transmission and absorption, and modulation spectroscopy; photoluminescence and photoluminescence excitation; Raman and resonant-Raman scattering; spectroscopic ellipsometry; and surface photovoltage. A wide variety of electrical and magnetotransport techniques is also utilized to characterize the electronic properties. Emphasis is placed on understanding fundamentals and technologically relevant properties as well as developing accurate measurement techniques.

Contact: David G. Seiler, 301-975-2054

Physics of Semiconductor Devices and C and BN Nanotubes

Theoretical solid-state physics research for electronic applications is in progress in order to understand the operation of advanced electronic devices and to provide more physically correct and numerically robust carrier transport models. Such transport models are used to interpret measurements and to enable predictive computer simulations of electronic devices. For example, topics include densities of states, band structures, high-concentration effects, carrier lifetimes, and carrier mobilities. The approach involves careful examination, extension, and experimental verification of the theoretical basis used in device models for elemental and compound semiconductors and for metallic, semiconducting, and insulating nanotubes. We are interested in extending such research to include magnetic semiconductors and nanotubes (spintronics), such as manganese-doped GaAs.

Contact: Herbert S. Bennett, 301-975-2079

Microelectronic Package Characterization

Research focuses on the thermal properties of microelectronic packages and interconnects. Our objectives are to improve methods for characterizing these properties for advanced packages and modules; improve measurement methods and techniques; and verify "compact" electrical and thermal models for packages and modules, and parameter extraction techniques for the models. We have fully equipped thermal characterization laboratories including an infrared thermal imager with μs temporal and 20 μm spatial resolution, and several computer workstations with a compliment of thermal and electrical modeling and analysis software.

Contact: David L. Blackburn, 301-975-2068

Quantum Devices for ULSI Circuits

The complementary-metal-oxide-semiconductor (CMOS) field-effect-transistor is showing fundamental limits associated with the laws of quantum

mechanics and the limitations of fabrication techniques. This is driving research on innovative solutions to augment or replace CMOS technologies. Quantum devices such as quantum dots, resonant tunneling devices, and single-electron transistors, deliberately exploit quantum and size effects. We are interested in fundamental research in all aspects of quantum devices, particularly those that are compatible with Si technologies. Our interests include, but are not limited to, fabrication, simulation, and characterization of device structures and constituent materials/processes. Our primary expectation is to be able to identify and address critical metrology issues for this emerging technology of silicon-based quantum devices. In support of this research, we have a clean room with a variety of fabrication equipment including furnaces, evaporators, and optical and electron-beam lithography. We have numerous device, electrical, and physical simulation software available including the NanoElectronic Modeling program, NEMO, and the molecular simulation program, CeriusII/CASTEP. We have a wide range of electrical characterization equipment that allows device characterization at temperatures ranging from approximately 1 K to 700 K. This includes ultra-low noise probe stations, cryostats, semiconductor parameter analyzers for current-voltage measurements, ac capacitance-conductance-inductance measurements, specialized setups for Hall and magnetotransport measurements, and a variety of additional electronics. We also have numerous supporting analytical measurement techniques available including spectroscopic ellipsometry, atomic force microscopy, and scanning capacitance microscopy.

Contact: Eric M. Vogel, 301-975-4723, or Curt A. Richter, 301-975-2082

Modeling Advanced Semiconductor Devices for Circuit Simulation

Accurate circuit simulator models for advanced semiconductor devices are required for effective computer-aided design of electronic circuits and systems. However, the semiconductor device models provided in most commercial circuit simulators (*e.g.*, simulation program with integrated circuit emphasis) are based on microelectronic devices, and they do not adequately describe the dynamic behavior of advanced semiconductor devices. Therefore, research focuses on the following: (1) physics-based models for advanced semiconductor devices such as power and compound semiconductor devices (these models are implemented into available circuit and system simulation programs; (2) parameter extraction algorithms for obtaining model parameters from terminal electrical measurements; and (3) characterization procedures for verifying the models' ability to simulate the behavior of the devices within application circuits. NIST also works closely with commercial software vendors, to make the new models available to circuit design engineers, and has established the NIST/IEEE Working Group on Model Validation to develop comprehensive procedures for evaluating the performance of circuit simulator models. (For more information, see ray.eeel.nist.gov/modval.html.)

Contact: Allen R. Hefner, Jr., 301-975-2071

MicroElectroMechanical Systems

The MicroElectroMechanical Systems (MEMS) project focuses on the development of new MEMS-based sensors and actuators for measurement applications. It functions in a multidisciplinary environment with collaborations in the NIST laboratories in Chemistry, Materials Science, Physics, Biotechnology, and Building and Fire Research. Current activities in the project include thermal-based elements, mechanically resonant structures, microwave elements, and microfluidic systems. The project is also developing MEMS test structures, test methods, and standards to characterize device properties for device performance and reliability testing. These MEMS-based test structures are being utilized to characterize thin-film properties in mainline semiconductor fabrication processes. We are interested in postdoctoral applications not only from individuals who have specialized in MEMS research but also from individuals of other science disciplines who wish to learn microfabrication methods and apply their expertise for new measurement applications.

Contact: Michael Gaitan, 301-975-2070

NanoBioTechnology for Single Cell and Single Molecule Manipulation and Measurements

Our work focuses on developing microfluidic systems and nanofluidic restrictions for cell and biomolecule transport and detection. We are interested in methods to pattern cells on surfaces, cell adhesion, sorting, and electronic and electrochemical monitoring of cell activity. We are also interested in nanofluidic systems for DNA, RNA, and protein transport and detection to determine the

structure and function. This project is part of a multidisciplinary program with collaborations in the NIST laboratories in Chemistry, Materials Science, Physics, and Biotechnology. Research will focus on the development of new fabrication methodologies, design and fabrication of new and novel nanofluidic systems, and measurement methods.

Contact: Michael Gaitan, 301-975-2070

Reliability of Integrated Circuit Dielectric Films

Aggressive scaling of gate oxide thickness used in silicon integrated circuits necessitates the understanding of physical mechanisms responsible for dielectric degradation and breakdown. We are particularly concerned with the reliability of ultrathin gate oxides that are in the direct tunneling regime during circuit operation. Research focuses on (1) identifying parameters to determine the physics of time-dependent dielectric breakdown of ultrathin dielectric films in the tunneling regime, (2) determining the effectiveness of highly accelerated stress tests to predict long-term reliability of thin dielectric films, (3) relating analytical characterization of oxide bulk and interfaces to electrical behavior, (4) identifying and controlling fabrication process parameters that affect intrinsic and extrinsic failure modes, and (5) characterizing and evaluating alternate dielectrics for use as substitutes for silicon oxide in advanced circuit technologies.

Contact: John S. Suehle, 301-975-2247

Physical and Electrical Properties of Advanced Gate Dielectric Films

It is increasingly difficult to characterize ultrathin gate dielectric films (typically 0.1 nm to 3.0 nm) used in MOS devices as technology drives them ever thinner. We are developing electrical test methods (using conventional techniques such as I-V and C-V, as well as low-temperature magnetotransport techniques) to measure the physical properties (*e.g.*, film thickness and permittivity) of alternate gate dielectric materials such as high-κ metal oxides as well as ultrathin SiO_2. Electrical results are compared with those of optical and other measurement methods, and fundamental physical models are developed to be effective for more than one measurement technique. Because the interface between the dielectric film and the silicon substrate is critical to understanding these measurements, we are developing techniques to characterize buried interfaces (*i.e.*, interface roughness) and are determining how the interface and physical properties affect device performance and reliability.

Contact: Eric M. Vogel, 301-975-4723, or Curt A. Richter, 301-975-2082

Optical and Physical Characterization of Thin Films Used in Integrated-Circuit Devices

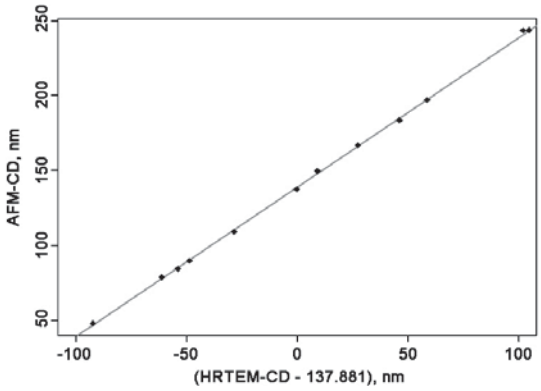
The continued scaling of integrated-circuit (IC) technology requires more stringent precision and accuracy for the optical and physical measurements of thin films. Our research involves the development of optical measurement techniques, specifically spectroscopic ellipsometry and the enhancement of data analyses and modeling. Input from various physical, optical, and electrical techniques is needed to improve our knowledge of the structure and composition of these thin films. With a broad collaboration from various thin-film measurement groups within NIST, our research will focus on relating the analyses of HR-TEM, scanning probe methods, X-ray reflectance, Fourier-transform infrared, photo reflectance, Raman scattering, and various electrical techniques to improve our understanding of these films and also validate some of the optical models used in the analysis of the ellipsometric data. Simple actual IC devices can be fabricated in-house for electrical test structures.

Contact: Curt A. Richter, 301-975-2082, Nhan V. Nguyen, 301-975-2044, or Eric M. Vogel, 301-975-4723

Division Highlights

Uncertainties of CD Reference Features Significantly Reduced

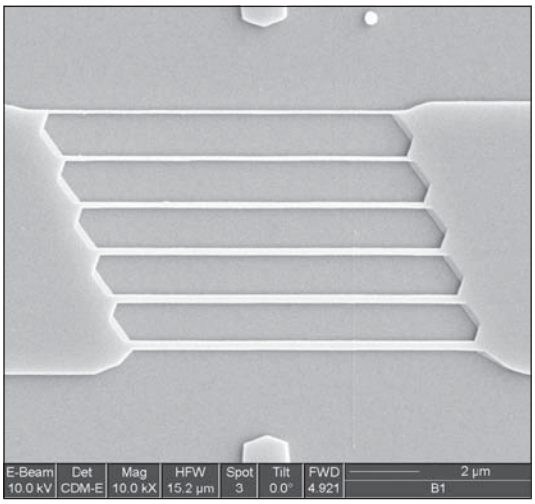
Researchers in the Electrical Test Structure Metrology Project, in collaboration with NIST's MEL and ITL along with International SEMATECH (ISMT) and VLSI Standards, have significantly reduced the uncertainty in critical dimension reference features that were delivered to 10 member-companies of ISMT in September 2004. The improvement in uncertainty results from the implementation of a new type of HRTEM-target test structure, the extensive use of SEM (Scanning Electron Microscope) inspection to identify targets with superior critical dimension (CD) uniformity, and the use of advanced Atomic Force Microscopy (AFM) implemented at ISMT by NIST's Manufacturing Engineering Laboratory personnel on special assignment to serve as the transfer metrology. Researchers anticipate that features on other available chips will eventually be distributed as NIST-traceable artifacts to other end users in the semiconductor industry for metrology-tool development by VLSI Standards Corporation.



Example of AFM transfer-calibration from a single HRTEM target.

The calibration function relating the HRTEM and AFM CDs is derived from measurements of the new HRTEM-target test structures, each of which contains six features with a distribution of drawn linewidths, on three chips. HRTEM provides the essential absolute primary measurement of CD, since it is traceable to the known spacing of the lattice planes of mono-crystalline silicon. AFM provides a transfer calibration since HRTEM imaging destroys the chips.

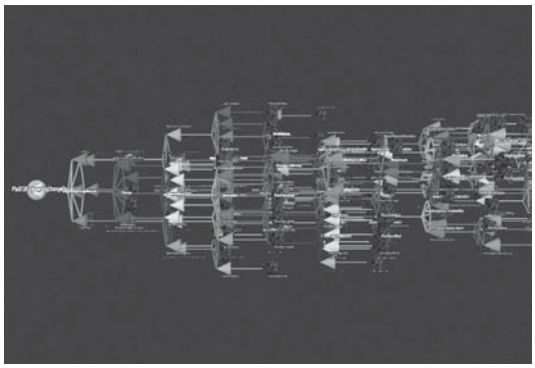
A key attribute of each distributed CD reference feature is its uncertainty, which is derived statistically from the calibration function which enables tracing the AFM measurements to HRTEM metrology. The previous generation of reference materials, which was delivered in 2001 and used electrical CD as the transfer calibration, had uncertainties of approximately 14 nm. The second generation units, which are being distributed to ISMT at this time, have CDs as low as 45 nm. The calculated standard uncertainty ranges upwards from 1.5 nm. At this time, the chips are being distributed with a stated standard uncertainty of no less than 4 nm, pending additional analysis by NIST's Statistical Engineering Division.



SEM image of the new test structure. (The lengths of the lines shown are approximately 10 µm.)

SED Researcher Develops Novel 3D XML Browser/Editor

Matthew Aronoff, of the IIEDM Project, has developed what some have called a "novel" 3D XML Browser/Editor: Hydra3D. The work was initiated by a request from RosettaNet which is developing a wide range of XML based information exchange standards for the printed circuit board industry. RosettaNet and many others in the electronics industry are developing XML-based standards and have an appreciation of the benefits of XML; however, they are not XML experts. They inquired as to whether NIST might be able to provide a tool that could help them manage the complexity of the XML based standards they are developing. Aronoff's 3D Browser/Editor accomplishes this by providing a hierarchical 3D view of any XML document. The tool provides the user with the ability to view the entire document, or only those portions of interest. The tool allows the user to manipulate the document; *e.g.*, zoom in and out, rotate, search, and filter out portions of the document and save different views of the document.



Screenshot of the Hydra3D XML Browser/Editor.

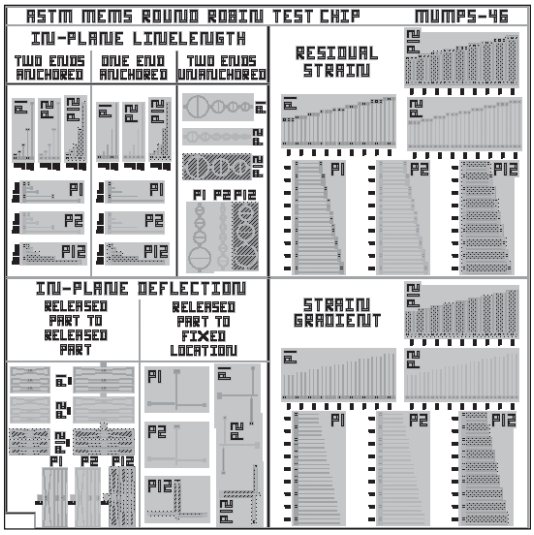
Although the tool is still under further development, several groups both internal and external to NIST have requested copies of the software for their own use. BFRL has requested the software for use on XML standards they are developing with their construction industry customers. MEL researchers have also expressed interest in the tool. Researchers from Georgia Tech have requested copies of the software. International SEMATECH and SEMI researchers have requested a variation of the software for support of XML based standards that they are developing for the semiconductor industry. The software is currently available on CD ROM and on the Internet (http://hydra3d.sourceforge.net). The software runs on Linux and Windows. A Mac version has also been completed and will be available pending optimizations.

A user's guide for the tool was published as a NIST internal report, and a paper on the tool was presented at the Extreme Mark-Up Conference in August 2004. It is hoped that commercial XML tool providers who heard about the tool at the conference will consider adopting Aronoff's ideas into some of their products.

SED Writes First MEMS Standards

The first MicroElectroMechanical Systems (MEMS) standards in the world were published in the Annual Book of ASTM Standards in the summer of 2003. The three standard test methods are for measuring in-plane lengths, residual strain, and strain gradient.

Written by MEMS Project staff member Janet Marshall (who, for her efforts, received an award of appreciation from the Committee on Fatigue and Fracture), these test methods are based on the research and analyses detailed in NIST Interagency Report 6779. The residual strain and strain gradient standard calculations can be performed on the NIST Semiconductor Electronics Division Web site (www.eeel.nist.gov/812/test-structures/) to facilitate quick and easy calculations.



The round robin test chip.

MEMS is a rapidly growing component of the semiconductor industry. Applications for MEMS demand high performance and reliability. The standard test methods are crucial for tightening the variations in the parametric measurements between laboratories. These international standards are expected to facilitate international commerce in MEMS technologies and improve manufacturing yields.

All three test methods apply to thin films such as found in MEMS materials, which can be imaged using a non-contact optical interferometer. The first test method shows how to measure an in-plane length (or deflection) measurement, given that each end is defined by a distinctive out-of-plane vertical displacement. The second test method shows how to calculate the residual strain from two cosine functions that are used to model the out-of-plane shape of fixed-fixed beams. The third test method shows how to measure the strain gradient from a circular function that is used to model the out-of-plane shape of cantilevers.

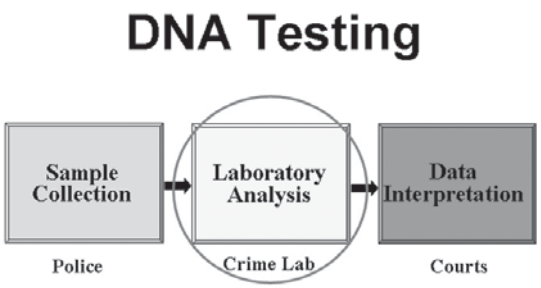
A MEMS Length and Strain Round Robin Experiment is underway to compare results from these test methods. The goal is to demonstrate the reproducibility of measurements performed using the same test methods at independent laboratories as well as the repeatability of measurements when performed using the same test method, in the same laboratory, by the same operator with the same equipment, in the shortest practicable period of time.

For the round robin, a test chip (the design of which is shown in the figure) was passed from laboratory to laboratory, and measurements were taken on random test units using the procedures given in the ASTM standard test methods. Data (*i.e.*, x or y and/or z values) from these measurements are fed into a NIST web-based program for analysis. The analysis also provides a means for verifying the data before submitting the results to NIST for collection. Currently, eight laboratories (NIST, Kavlico, Motorola, Lucent Technologies, Veeco Metrology, Zygo, FLX Micro, and Delphi) are participants in this round robin. The final results will be recorded in the three related ASTM standard test methods for re-balloting.

These test methods are under the jurisdiction of ASTM Committee E08 on Fatigue and Fracture and are the direct responsibility of Subcommittee E08.05 on Cyclic Deformation and Fatigue Crack Formation.

New Microfluidic DNA Analysis System for Forensics Applications Demonstrated

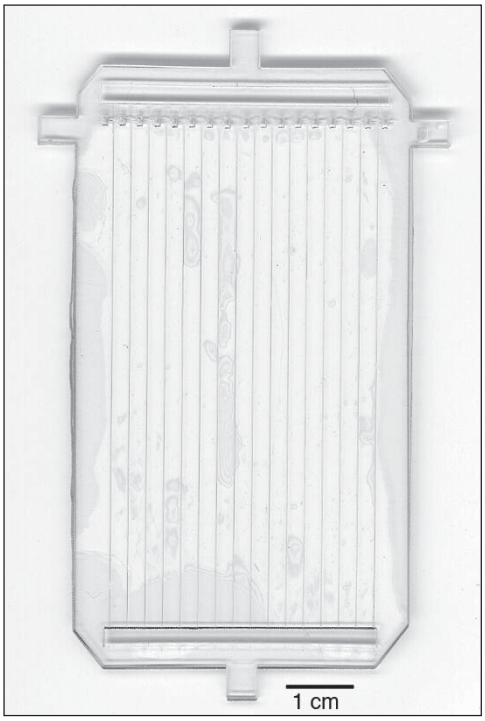
Modern forensic DNA analysis systems are currently based on the separation of DNA fragments by capillary electrophoresis, a process which typically takes 30 m. Recognizing an urgent need to improve the efficiency, speed, and accuracy of the DNA testing to alleviate a growing backlog of forensic DNA testing for criminal cases, The Department of Justice has requested NIST's guidance on the development of new measurement technology for DNA separation. Using a newly developed microfluidic device, NIST researchers in EEEL and CSTL have demonstrated a separation of a DNA ladder with fragments ranging from 50 to 550 base pairs in 4 m.



The three phases of DNA testing. NIST efforts are focused on the "Laboratory Analysis" phase.

This effort to develop a rapid DNA Analysis System for Forensics using microfluidic systems is being sponsored by the Department of Justice (National Institute of Justice, Office of Science and Technology, Investigative and Forensic Sciences Division's Program on DNA Research and Development). The research team will draw on its extensive expertise in microfluidics, microfabrication, DNA separations, as well as state-of-the-art optics and detection to build a prototype system that can be used as a model to demonstrate the advantages of applying these latest technologies for forensic identification. There are two overall requirements that must be satisfied to meet the needs of the Department of Justice: (1) development of a reliable, easy-to-use, high-throughput, microfluidics-based system that is smaller and faster (by a factor of 10) than capillary-based techniques; and (2) validation of the system that would support the adoption of this technology by the judicial system.

A final goal of this effort is to develop a device that will integrate sample preparation functionality with the current DNA separation process. It is anticipated that this integration will further decrease the laboratory analysis time. The prototype of such a device is pictured below.



Prototype 16 channel device for DNA fingerprinting.

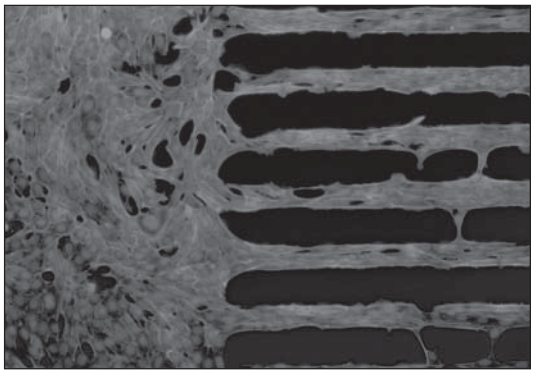
Microfluidic technology is a promising alternative to capillary-based techniques due to its great potential to miniaturize, simplify, integrate, automate, and multiplex the analysis with higher throughput and speed. Although DNA analysis systems based on microfluidics technology have been recently commercialized for DNA sequencing applications, these systems do not meet the specific needs of the forensic community due to poor separation resolution of the relatively long fragments (order 100 bps to 400 bps) as well as incompatibility with standard test procedures.

The team involved in this effort includes the Semiconductor Electronics Division (EEEL), the Analytical Chemistry Division (CSTL), the NIH, Northwestern University, and Cambridge Research and Instrumentation of Woburn, Massachusetts.

Patterning PDMS Surfaces with Microfluidic Networks Provides Foundation for Bioelectronics

The EEEL NIST Director has recently awarded a 3-year collaborative effort to the MEMS Project (Semiconductor Electronics Division) and the Electromagnetic Properties of Materials Project (Electromagnetics Division) entitled Bioelectronics. The overall goal of this effort is to develop methods in EEEL to interface microelectronic and microwave circuits to single cells or small cell clusters. As such, Bioelectronics is an interdisciplinary field that integrates elements of chemistry, biology, physics, electronics, nano- and biotechnology, and materials science.

One of the first outcomes of bioelectronics is a new method to pattern neural (retinal) cells on biocompatible non-biological cell adhesive materials; an important first-step towards our goal to interface them to microelectrodes, microelectrochemical cells, and microwave circuits. This work has been recently reported in the journal Langmuir by Darwin R. Reyes, Elizabeth M. Perruccio, S. Patricia Becerra, Laurie E. Locascio, and Michael Gaitan entitled "Micropatterning Neuronal Cells on Polyelectrolyte Multilayers" (Langmuir 2004, 20, 8805-8811).



Fluorescent images of the cytoskeleton and nuclei of R28 cells on polystyrene.

This method employs a nanofabrication process, which consists of a sequential deposition of polyelectrolyte layers (PEMs) on polydimethylsiloxane (PDMS), a soft biocompatible polymer material that is resistant to cell adhesion. The patterned PEMs film creates a cell "adhesive" where the cells will preferentially plate while leaving the bare PDMS surface free of cells. Our method to pattern the PEMs film on the PDMS is based on using a microchannel network, placed on PDMS, to flow the polyelectrolyte over the desired pattern on the PDMS surface. Consecutive steps of rinsing and flowing oppositely charged polyelectrolytes rendered the desired patterned multilayer films. After the films were formed and dried, the microchannel network was removed, exposing the PDMS surface with a patterned PEMs film on it.

To assess the behavior of cells on the patterned surfaces, two basic tests were carried out: a viability test, which reveals if the cells are alive or dead, and a morphological analysis, which determines if the shape of the cells changes with the surface and chemical composition of the material. The cells were first seeded on the PEMs/PDMS surface and then preferentially positioned on the PEM regions. A viability test carried out 24 h after seeding the cells showed normal activity within the cell, demonstrating that cells were alive while on the patterned biocompatible material. The cell cultures were allowed to grow for up to 14 d. The morphology of cells on the PEMs was also observed. Specifically, the major structural proteins that provide the cellular architecture were observed and compared in tissue culture material and on the PEM patterns. The cells looked similar in both materials — when there was enough available space in which to grow. In more constrained areas they tended to elongate in order to accommodate a higher number of cells within the PEM areas. But in general, they seemed to preserve the same morphological appearance.

There is a plethora of information that can be gathered from cells almost instantaneously when they are interfaced with microelectronic devices. We envision the development of tools to study the progression of diseases, such as those associated with neuron degeneration, by creating array of cells that could be interrogated in parallel. Also, we foresee the development of pioneer electronic methods to probe cellular activity and to improve cell handling and culturing.

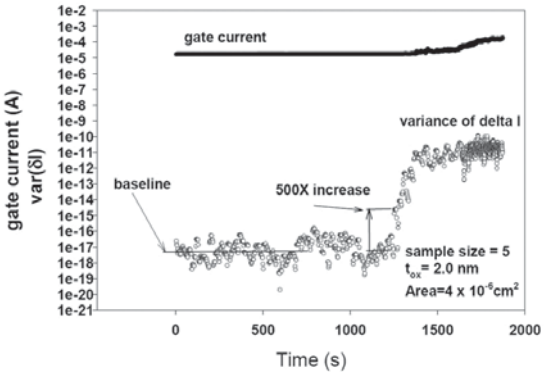
This work was done in a collaboration involving Darwin R. Reyes and Michael Gaitan from Semiconductor Electronics Division, Laurie Locascio from Chemical Science Technology Laboratory, and Patricia Becerra from the National Eye Institute of the NIH.

SED Leadership Produces Unique Standard on Time-Dependent Breakdown of Ultra-Thin Gate Dielectrics

Dr. John Suehle, leader of the Advanced MOS Device Reliability and Characterization Project, chaired the committee that developed the new JEDC (Joint Electron Device Engineering Council) standard: JESD92, "Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics." Dr. Suehle is the Chairman of the JEDEC JC14.2 Working Group on Dielectric Reliability. This new standard was published in August 2003.

This standard is the first of its kind to define a constant voltage stress test procedure for characterizing time-dependent dielectric breakdown or "wear-out" of the newer ultra-thin (2 nm or below) gate dielectrics. The standard uses special techniques to detect breakdown in ultra-thin oxide films that exhibit large tunneling currents and soft or noisy breakdown characteristics. Representatives from a majority of the U.S. semiconductor industry provided input in the development of the standard. It will be used in the qualification of gate dielectric processes in domestic and overseas semiconductor manufacturing facilities. The standard is available to view on-line free-of-charge at www.jedec.org/-download/search/JESD92.pdf.

As the semiconductor industry continues to increase integrated circuit performance by decreasing the lateral dimensions of metal-oxide-semiconductor (MOS) devices, the thickness of the gate dielectric, which is projected to continue to be in use over the next five years, must also be scaled downward. The thickness of the gate dielectric in state-of-the-art microprocessors is 2.0 nm or below and will continue to decrease over the next several years, leading to serious concerns about the reliability of the gate dielectric.



Stress gate current vs. time and gate current noise vs. time for a 2.0 nm thick SiO_2 film with an area of 4 x 10^{-6} cm^2. The onset of breakdown is detected by a >500X increase in the current noise.

Congressman Wolf Visits MEMS Laboratory

House Appropriations Subcommittee on Commerce, Justice, State, the Judiciary, and Related Agencies Chairman Frank Wolf (R-VA) visited the NIST Gaithersburg, Maryland, campus on April 20, 2004. Under Secretary of Commerce for Technology Phillip Bond; Arden Bement, NIST Director/Acting National Science Foundation Director; Hratch Semerjian, NIST Deputy Director/Acting Director; Dave Karmol, American National Standards Institute Vice President of Public Policy and Government Affairs; and Verna Hines, NIST Director of the Office of Congressional and Legislative Affairs, accompanied Wolf.

Chairman Wolf visited the MEMS Laboratory, where he heard about DNA forensics and diagnostics testing research.

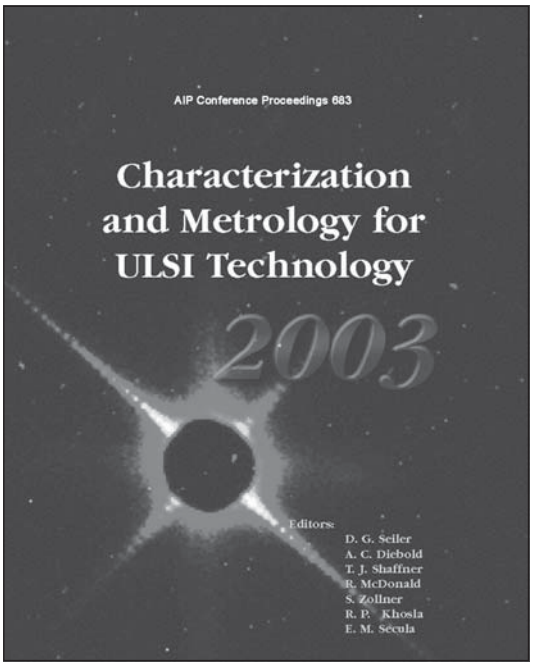
Chairman Wolf stated that he was impressed with NIST staff and programs. He added that NIST's activities should be more visible, and that NIST should devote greater effort to getting the word out to the highest levels of industry, and specifically to Congress.

Hratch Semerjian, Arden Bement, Frank Wolf, Phillip Bond, and Dave Karmol.

Phillip Bond, Michael Gaitan, Frank Wolf, Laurie Locasio, and Jayna Shah.

SED Leads Major Semiconductor Metrology Conference Series

Dr. David Seiler, Chief of the Semiconductor Electronics Division, provided critical leadership and co-chaired the 2005 International Conference on Characterization and Metrology for ULSI Technology, which was held in March 2005 at the University of Texas at Dallas. This was the fifth meeting in the only conference series devoted exclusively to characterization and metrology for the ULSI silicon industry. The conference assembled hundreds of attendees from industry, government, and universities from around the world. The conference proceedings, to be published by the American Institute of Physics in a hard-bound volume with CD-ROM, will be published in fall 2005.



Cover of the proceedings for the 2003 International Conference on Characterization and Metrology for ULSI Technology, which was published in September 2003.

Led and co-sponsored by NIST, the conference series provides a forum to present and discuss critical issues, future directions, and key measurement capabilities and limitations related to the manufacture and diagnostics of silicon devices. The conferences consist of invited presentation sessions and poster sessions for contributed papers, which cover new developments in characterization/metrology technology.

Among the many distinguished members of the semiconductor industry scheduled to speak at the conference were Bob Helms (UT Dallas), Michael Polcari (International SEMATECH), Hans Stork (Texas Instruments), Dan Hutcheson (VLSI Research, Inc.), and Alain Diebold (International SEMATECH).

Keynotes speakers from past conferences in this series include Craig Barrett (President, Intel), Mark Melliar-Smith (President and CEO of SEMATECH), Dennis Buss (Vice-President of Mixed-Signal Technology, Texas Instruments), and Kenneth L. Schroeder (President and CEO of KLA-Tencor).[1]

Other sponsors for the 2005 conference included International SEMATECH, Semiconductor International, the American Physical Society, the National Science Foundation, Semiconductor Equipment and Materials International, Semiconductor Research Corporation, and the University of Texas at Dallas.

For additional information on the conference series, or to view slides from many of the invited presentations, visit the conference website at www.eeel.nist.gov/812/conference/.

"SED's role in the organization of the ongoing International Conference on Characterization and Metrology for ULSI [ultralarge-scale integration] Technology is seen as a particularly valuable leadership activity."

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

[1] Titles and affiliations were those held at the time of presentation.

NIST's Gaithersburg, Maryland, Campus and Surrounding Area

NIST MISSION –
To develop and promote measurement, standards, and technology to enhance productivity, facilitate trade, and improve the quality of life.

NIST VISION –
To be the global leader in measurement and enabling technology, delivering outstanding value to the nation.

"Washington is located in a region that is rich in historic lore and natural beauty. From the bustling sounds of a Chesapeake Bay harbor to the utter stillness of a Blue Ridge mountaintop, from the small, old tobacco farms of southern Maryland to the grand estates of Virginia's hunt country, you will find a richness of scenery and history."

"Welcome to Washington" brochure, National Park Service, U.S. Department of the Interior

About NIST

The National Institute of Standards and Technology (NIST) is an agency of the U.S. Department of Commerce's Technology Administration. NIST was established in 1901 by Congress "to assist industry in the development of technology ... needed to improve product quality, to modernize manufacturing processes, to ensure product reliability ... and to facilitate rapid commercialization ... of products based on new scientific discoveries."

Location

Located approximately 40 km northwest of Washington, D.C., on a 234 hectare campus, NIST Gaithersburg offers the advantages of being in close proximity to government offices, while maintaining the seclusion of a rural setting. The site is beautifully landscaped and features mature trees and ponds, as well as a herd of white-tailed deer and gaggles of Canada geese. Walking paths and picnic areas provide easy and pleasant access for outdoor repasts, biking, walking, and jogging. The campus also is easily accessible, with a shuttle service to a nearby metro (subway) station and is in close proximity to near three major airports.

NIST's 11-story Administration Building.

Staff

NIST's staff is composed of about 3,300 scientists, engineers, technicians, business specialists, and administrative personnel. About 1,500 visiting researchers complement the staff. In addition, NIST partners with 2,000 manufacturing specialists and staff at affiliated centers around the country.

Some Nearby Attractions

Landmarks

Bureau of Engraving and Printing
Capitol Building
Ford's Theater
Franklin Delano Roosevelt Memorial
I.R.S. Building
J. Edgar Hoover F.B.I. Building
Jefferson Memorial
Library of Congress
Lincoln Memorial
National Archives
Supreme Court
Union Station
Vietnam Veterans Memorial
Washington Monument
White House

The NIST Gaithersburg, Maryland campus is home to many different types of wildlife.

Museums and Other Attractions

Capital Children's Museum
Corcoran Gallery
Kennedy Center
MCI Center
National Geographic Society
National Sports Gallery
National Theater
Smithsonian Institute
United States Holocaust Memorial Museum

Outdoor Attractions

Antietam National Battlefield Site
C&O Canal National Historical Park
Clara Barton National Historic Site
Eisenhower National Historic Site
Fort McHenry
Fort Washington
Gettysburg National Military Park
Glen Echo Park
Great Falls Park
Greenbelt Park
Mount Vernon
Oxon Hill Farm
Prince William Forest Park
Rock Creek Park
Shenandoah National Park
Wolf Trap Farm Park for the Performing Arts

Division/Office Publication Editor:	Erik M. Secula
Publication Coordinator:	Erik M. Secula
Printing Coordinators:	Deirdre McMahon Ilse Putman
Document Production:	Technology & Management Services, Inc. Gaithersburg, Maryland

January 2005

For additional information contact:
Telephone: (301) 975-2054
Facsimile: (301) 975-6021
On the Web: http://www.eeel.nist.gov/812/