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NIST Workshop on the Computer Interface to Flat Panel Displays

Editors:
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[1] At Boulder, CO 80303.
[2] Some elements at Boulder, CO 80303.

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January 13–14, 1994;
San Jose Hilton and Towers;
San Jose, California

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Contents

A. Preface

Television, computers, and telecommunications have been considered largely separate technologies. Today, they are merging to provide a powerful tool for the information age. This merger will provide new capabilities for diverse applications in education, engineering, manufacturing, robotics, entertainment, medicine, defense, security, transportation, business, and government.

Cathode ray tubes (CRTs) are used in current television sets and in most personal computers. They produce light by scanning an electron beam (the "cathode ray") across a phosphor screen to stimulate the emission of light. CRTs have high brightness, good color reproduction, and reasonably wide viewing angles. However, since CRTs are evacuated devices, they must be made from strong materials to withstand the pressure of the atmosphere. The tubes become increasingly difficult to implement in large screen sizes.

In contrast, emerging flat panel displays (FPDs) are considerably smaller and lighter for a given screen size. FPDs are being integrated into laptop, notebook, and hand-held form factors. In addition, flat panel monitors are becoming commercially available for desktop computers and workstations.

However, FPDs are currently a value added product which requires the development of a unique computer interface for each display. This results in needless expense and integration difficulties for the end-user. In addition, the lack of standards may slow down the implementation of FPD technologies in the market place.

In order to achieve interoperability and flexibility comparable to CRTs, it is necessary to develop logical, electrical, and mechanical standards for the computer interface to FPDs. Further, the wide variety of FPD technologies may require either an advanced computer interface architecture to accommodate the varying requirements of different displays, or a series of standards that address the requirements of different technologies.

FPD technologies have reached a point where it is worthwhile to consider the development of voluntary industry standards for the computer interface. Therefore, the Computer Systems Laboratory (CSL) at NIST sponsored this workshop to bring together flat panel display manufacturers, computer systems manufacturers, graphic controller chip manufacturers, industry and government users, and others who have a material interest.

B. Summary

On January 13 & 14, 1994, the NIST Workshop on the Computer Interface to Flat Panel Displays was held at the San Jose Hilton and Towers in San Jose, California. The meeting was attended by approximately 55 people from over 40 computer, flat panel display, and graphics controller companies. Representatives from the civilian and military sides of the government were also present.

The objectives of this workshop were: to determine the need for a standard or a series of standards for the computer interface to flat panel displays (FPDs); to identify what types of standards are needed; to identify approaches for developing FPD interface standards; and to obtain a consensus on a coordinated plan for standards development.

The workshop attendees agreed that a standard flat panel display interface for integrated devices is needed. Furthermore, the workshop attendees agreed that efforts should be made to encourage all of the flat panel display manufacturers to participate in these standards activities.

The consensus reached at this workshop resulted in the following action items:

1) Form a Video Electronics Standards Association Special Interest Group (VESA SIG) to undertake the development of a standard or a series of standards for the interface between a FPD and its controller. This interface standard will address both active and passive FPDs in integrated devices. It will cover both the electrical and the mechanical (connector) specifications. An organizational meeting will be held on February 9, 1994, at the VESA headquarters with the intention of having a proposal ready to discuss with manufacturers of flat panel displays at the Society for Information Display (SID) meeting in June.

2) NIST will seek to inform all materially interested parties, especially the flat panel display manufacturers of the standards plans, and encourage their participation.

3) VESA will distribute the February 9, 1994, meeting announcement and agenda.

4) The interface for remote FPDs requires additional technical discussions before a standard can be written. Additional workshops on display interfaces and /or technical sessions at the SID Symposium should be explored. In addition, the VESA Monitor Committee invited interested parties to participate in their committee which will be considering interfaces and connectors to desktop and remote FPDs in addition to their cathode ray tube (CRT) interface work.

   Dr. Paul Alt of IBM will seek to set up a technical session at future SID meetings to consider these long-term display interface requirements. It is too late to add a technical session on interface topics at SID '94. However, an interface session may be possible for SID '95.

C. Minutes

The Workshop began at 12:30 PM on January 13, 1994 at the San Jose Hilton and Towers and continued until 4:00 PM on January 14. The agenda for the Workshop is section (1) and the list of attendees is section (2). Mark Williamson of NIST acted as chairman of the workshop and Bill Burr of NIST was secretary.

Mark Williamson of NIST opened the workshop by introducing the NIST participants and stated the objectives of the workshop:

- Determine the need for a standard or a series of standards for the computer interface to flat panel displays (FPDs).
- Identify what types of flat panel standards are needed.
- Identify approaches for developing FPD standards.
- Obtain a consensus on a coordinated plan for standards development.

Mark Williamson's presentation is section (3).

Mr. Thomas Leedy of NIST made a presentation on the NIST Advanced Technology Program (ATP). Mr. Leedy's presentation is section (4). The NIST ATP works with industry to co-fund high-risk technology development programs. Enabling, high-value technologies that promise large or strategic long term benefits to the U.S. economy are emphasized. ATP awards are based on a competition of both the technical and business merit of the proposals. Cost sharing is required: single company awards are limited to $2M over three years and the government does not pay overhead, while joint ventures (involving at least two companies) may take up to 5 years, and there is no limit on the award, however the ATP funding is limited to less than 50% of the total cost. The ATP has made several awards in the general area of flat panel technology; these are summarized in section (4). In response to a question, Mr. Leedy stated that any firm that is not a "United States-owned company" (i.e., that does not have a majority ownership or control by individuals who are citizens of the United States) may receive an ATP grant if the Secretary of Commerce finds that the company's participation in the Advanced Technology Program would be in the economic interest of the United States, and the Secretary finds that the country in which the company or its parent company is incorporated affords United States-owned companies similar opportunities and adequate and effective protection for intellectual property rights. Further details on these eligibility requirements for foreign-owned corporations are available from the ATP.

Dr. Victor DaCosta of Xerox Palo Alto Research Center (PARC) presented a discussion of the issues involved in interfacing active matrix FPDs. Dr. DaCosta's presentation is section (5). Dr. DaCosta pointed out two themes that other speakers were to return to:

- The cathode ray tubes (CRTs) which have predominated as display devices are strict left to right, top to bottom raster scan devices, while active matrix liquid crystal displays (AMLCDs), like most other flat panel technologies, are row and column oriented. Thus the timing and ordering of signals on CRT oriented interfaces are not well suited for flat panel displays;

- There is no standard interface to the flat panel, and the characteristics of FPDs vary, so each panel requires a highly optimized and customized display adapter in the host computer to handle the specific characteristics of the particular FPD.

Dr. DaCosta identified four issues and problems in driving high resolution AMLCDs:

- Analog vs. digital interface;
- An inherent speed mismatch between the frame buffer output and the panel driver integrated circuit (IC) input;
- Different color filter mosaics;
- Different color/gray level control and correction schemes.

Dr. DaCosta stated that a flat panel interface standard is needed to provide a flexible and consistent interface to a wide range of FPD devices. He further proposed that this could be accomplished by incorporating within the panel electronics a flat panel controller IC that provides a simple and standardized interface to the flat panel by performing all the specific display dependent processing needed for the row and column drivers of the flat panel. That is, the customization should occur in the panel itself, so that there can be a consistent interface. Dr. DaCosta stated that an example of such an AMLCD flat panel controller had been developed by Xerox PARC and would be presented at the ISSC94 conference.

Ms. Carol Wedding of Photonics Systems made a presentation on the interface issues for alternating current plasma display panels (AC-PDPs). Her presentation is section (6). Ms. Wedding began by discussing the requirements for future FPDs. She noted that displays must keep pace with computers and said that displays of at least 1280 by 1024 pixels with at least 256 colors will be required for some applications. She noted that it is basically a CRT-oriented world, and that CRTs generally use an analog raster scan Red, Green, Blue (RGB) interface. All (or at least most) flat panel technologies must interface a digital panel to an analog signal or develop a special card to interface between the host and flat panel display. Photonics has pursued both paths. She summarized the following advantages and disadvantages of analog interfaces:

Advantages:

- Nearly universally available;
- Remote displays practical;
- Noise resistant.

Disadvantages:

- Added cost of digital in controller to analog in interface to digital in display;
- Cost of phase lock of different clock frequencies in display;
- Bandwidth degradation.

Ms. Wedding noted that a partial solution to the problems with analog interfaces would be to include a dot clock with the RGB signal in the interface, eliminating the need for a phase locked loop (PLL) in the display to recover the clock. She then summarized the advantages and disadvantages of digital display interfaces:

Advantages:

- Eliminate cost of digital-to-analog (A/D), analog-to-digital (D/A) conversion;
- Eliminate cost of PLL clock recovery;
- Reduce clock jitter.

Disadvantages:

- Not presently universal;
- Not noise resistant (or requires a large data bus);
- Very high data rate for 60 Hz or higher frame rate and high resolution displays.

Ms Wedding proposed two possible solutions to the problems with digital display interfaces at high resolutions and frame rates:

- Use an emmiter-coupled logic (ECL) twisted pair interface for its better high frequency electrical characteristics;
- Embed the computer itself on the back of a high resolution FPD.

While Ms. Wedding's talk was concerned primarily with plasma displays, she stated that all FPDs use row and column drivers and load data in column form. She described displays that load gray levels one at a time. However, other participants pointed out that liquid crystal displays (LCD) do not necessarily use gray levels one at a time. Ms. Wedding postulated that a "dream interface" for flat panels, or at least AC-PDPs, would be digital and organized in a row and column architecture, with gray level data processed in separate subplanes. She concluded that by exploiting the similarities of FPDs and discarding the preconceived notion of a CRT interface it should be possible to define a flat panel interface that is cost effective and technically acceptable to a wide variety of flat panel technologies.

Mr. Marc Klingelhofer of Sun Microsystems gave a presentation from the perspective of a workstation vendor. His slides are section (7). Mr. Klingelhofer began by describing the CRT interfaces used with workstations, where unlike the personal computer (PC) market (where the Video Graphics Adapter, VGA, standard provides some order), there is great variation. Workstation CRT interfaces are predominantly analog RGB over coax

with BNC connectors. Various synchronization styles are employed, including Horizontal/Vertical drive or composite synchronization, which may be embedded in the green signal or a separate signal. A plethora of horizontal and vertical resolutions and blanking characteristics are employed. All CRT interfaces, however, scan pixel-by-pixel horizontally, line-by-line vertically.

Mr. Klingelhofer went on to describe flat panel and particularly LCD interfaces. LCDs use bit parallel RGB plus clock and control over ribbon cables. Pixel depths per primary color are typically 6 to 8 bits per primary color. Various synchronization and control modes are employed and there are numerous resolutions. They rasterized first in columns then in horizontal rows. He noted that other FPD technologies are even less standardized than LCDs. Mr. Klingelhofer noted the following shortcomings of FPD interfaces:

- The pixel depth is not standardized - typically 6 to 8 bits;
- Pixel interleaving, if present, is display dependent;
- The cables must be short (certainly less than 10 m) and bulky, with 40 to 80 signals;
- Clock and control functions are not standardized;
- The row and column rasterization is incompatible with CRTs and most display drivers.

Mr. Klingelhofer also noted the similarities between FPDs and CRTs:

- Both use RGB pixels of 6 to 8 bits per primary;
- Both are two dimensional with a row and column matrix, and each pixel has an "address;"
- Sequences of lines constitute frames, and the frames can be identified.

Mr. Klingelhofer noted an industry trend to high bandwidth digital serial networks, smart displays, self identifying data streams, and scalability so that feature and performance enhancement are easy. He therefore proposed a relatively high level approach to a "unified display interface" that would use serial network technology and could support various display devices, including CRTs and LCDs. He proposed a serial interface, rather than a parallel ribbon cable, that could be scaleable, supporting various display types and resolutions, and be automatically configurable. The physical interface would include standardized copper or optical fiber media, with a fixed low level protocol for clock and bit serialization. The benefits would include common interface circuits, as well as standard connectors and cables, resulting in high volumes and low costs for these components. Moreover, very sophisticated display drivers then could support any standard display type and resolution without cabling or synchronization concerns.

He proposed that there be a standardized sequencing of color information ordering with pixels sent row by row rather than column by column and with fixed headers to identify resolutions and pixel positions. A low-end version of the protocol would be comparable to analog RGB, with pixels sent line-by-line; in this case the display would lock into and

accept incoming data with no handshaking or feedback. A higher level standard protocol would allow the driver to sense the display characteristics and allow the driver to set the resolution according to the application as well as allow the driver to alter display characteristics such as brightness and contrast.

Mr. Klingelhofer concluded by raising two open issues:

- Should such an interface directly support 3-D images rather than only 2-D? Present displays are 2-D and deal with 3-D by showing the projection of a 3-D image on a plane, but perhaps future displays may be 3-D displays;

- Are 8 bits per primary color per pixel enough?

A brief discussion followed Mr. Klingelhofer's talk. Two subjects were discussed: compression and cost. Should such an interface carry compressed data? If so, would the interface include a protocol like an X-terminal? Mr. Klingelhofer was asked what proportion of the cost of the display would be the embedded electronics needed for such an interface. Mr. Klingelhofer responded ,"a lot." Sun is apparently developing such a serial display interface, and may be able to discuss the subject in more detail in the future.

Mr. Gary Manchester of Molex gave a presentation on the future requirements for input/output (I/O) connectors in video applications. Mr. Manchester's presentation is section (8). He began by summarizing the history of video I/O connectors and the D subminiature connector commonly used by the VGA and extended graphics adapter (XGA) standards with CRT displays. In limited markets (e.g., workstations) where performance is an issue, designers have used standard coax systems. Current trends are requirements for smaller connectors with more contacts, low insertion force and yet increased life, perhaps as many as 10000 insertions. High volume consumer markets are developing, so cost becomes a major factor.

Mr. Manchester believes there is a need for a mixed layout connector supporting both coax and unshielded lines in one connector, as well as possibly power lines. The connector must be suitable for low cost manufacturing. Molex is now capable of providing a connector with three or four 75 Ω coax lines as well as 50 additional signal lines in the same space as a 15 pin VGA connector. With such a connector Mr. Manchester believes that it will be possible to package RGB video coax plus a fourth coax high speed sync line, mouse I/O, battery charger lines, serial port lines, keyboard lines, phone lines, parallel port lines, pen I/O, audio I/O, and a network interface all in one connector at a cost per mated line comparable to currently available I/O connectors.

Standardized connectors are required for such applications since the cost of connectors is very strongly a function of production volume. A standard will also promote the atmosphere to development of suitable connector technologies.

Mr. Bob Myers of Hewlett Packard gave a talk on issues in FPD interfaces of PCs and workstations. His presentation is section (9). Mr. Myers identified a distinction that previous talks had hinted at and that was later amplified on: there are really two FPD applications with potentially two interface standards. Those applications are FPDs in portable computers or other computers that include the display integrated in the same physical package as the video controller, and separate standalone monitor FPDs that may be some distance from the computer. The integrated FPD-video controller interface requires a very short, direct connection and consequently has less concern with Electromagnetic Interference (EMI) issues. The separate monitor interface must support a display removed from the controller by at least 1 m, and preferably should support longer distances. The interconnect EMI performance and signal integrity are therefore a much greater concern. At least the monitor interface must support both FPDs of various technologies and CRTs as well. The current analog video standard is a poor solution for both CRT and FPD monitors. Moreover, High Definition Television (HDTV) will make the standalone monitor FPD a big concern.

Mr. Myers discussed the bandwidth required for high resolution monitors with up to 60 frames per second. HDTV format displays and high resolution workstation displays will require pixel rates on the order of 60 to 130 MHz for flat panels and 160 MHz to more than 200 MHz for CRTs. At 24 bits per pixel that translates to data rates of 180 to 390 Mbytes/s for FPDs and 480 to 600 Mbytes/s for CRTs. Mr. Myers pointed out that as high as these rates are, multilevel coding can reduce the bandwidth needed for "digital" transmission.

Mr. Myers stated that a successful interface must be cost-competitive while allowing compliance with EMI requirements and providing for additional needed features (e.g., display ID, human I/O device connectivity). A successful interface must work within the constraints of existing technologies yet be flexible enough to support different display technologies and formats, including flat panels and CRTs. Mr. Myers said that computer manufacturers cannot afford separate interfaces for both CRTs and flat panels and CRTs will dominate in monitor applications for the foreseeable future.

Although he did not characterize it as a proposal, Mr. Myers outlined his thoughts on a possible common interface. It would have 4 signal lines per color, one of which is capable of analog video or of a binary or a quaternary digital signal, with three other lines capable of four level digital signals. The 12 lines could then provide analog video for CRTs, 4-bit color for simple digital FPDs, or 8 bits per subpixel digital color for high quality FPDs (in this mode all four lines are quaternary). The interface would also include horizontal and vertical sync as well as lines for an identification (ID) standard and probably human I/O and analog audio. The total would be 20 to 24 signal lines plus ground. Each display type would connect only to those outputs it needed, and provide an ID capability to allow the host to configure to the display's needs.

Mr. Myers was questioned about the cost of the multilevel drivers in the host. He felt that the cost would not be great in quantity very large scale integration (VLSI), and observed that every host might not support all features.

Dr. Bill Hale of Wright-Patterson Air Force Base discussed the need for plug and play displays in flight instruments systems and the difficulty commercial display vendors have in doing business with DOD. The greatest opportunities are probably in transport aircraft. Vendors wanting more information on the Air Force needs can call Dr. Hale at (513) 255-8261.

The first day concluded with a question and answer session for the speakers. Mr. Klingelhofer was asked just how much of network protocols he proposed to adopt for displays: just the physical layer or entire packet structures such as Asynchronous Transfer Mode (ATM) frames? He said that Sun is working on such an interface and that there might be a more concrete proposal in the future.

There was a discussion of parallel versus serial interfaces and the needs for relatively long (i.e., 100 m) distances between hosts and displays. What are the applications for such distances? One apparently is parallel processors supporting many users. It was observed that the X-terminal provides a partial solution for the remote intelligent display application.

There was a discussion of costs. An interface standard between the graphics controller and flat panel will add hardware costs to systems. However, there is a considerable cost in the ad hoc engineering required to adapt specific panels with nonstandard interfaces to systems. A part of that cost is not so much monetary as in time to market.

Dr. Bob Pinnel opened the second day of the workshop with a talk on the United States Display Consortium (USDC). Dr. Pinnel's visuals are section (10). The USDC is supported by Advanced Research Projects Agency (ARPA) and based on the premise that the United States must become a leading player in the manufacturing of FPDs to be competitive in future computer and electronic products markets. Manufacturers, suppliers, users and government must cooperate for this to happen. The USDC focuses on developing the U.S. flat panel display infrastructure, particularly the needed manufacturing and equipment expertise. The USDC is an industry-led public/private partnership and a nonprofit, non-manufacturing organization that provides a common platform for FPD manufacturers, developers, their supplier base, and users to develop plans and specifications for next-generation FPD manufacturing equipment and materials.

The USDC focus is on the needs of the wide range of FPD technologies. The USDC follows a vertically integrated approach to include all elements of the FPD food chain from equipment and materials suppliers to systems integrators. Nine Requests for Proposals have been issued, and the first selected involves equipment to do on-axis optoelectrical inspection of assembled FPD cells before attachment of the drive electronics.

Ms. Jill Seman of Chips and Technologies provided a very informative perspective on the interfaces used in flat panels for PCs. Her presentation is section (11). The VGA resolution of 640x480 is common in FPDs for PCs. Several kinds of displays are used, including dual scan monochrome LCDs, dual scan color passive matrix LCDs, color thin film transistor (TFT) and monochrome plasma and electroluminescent (EL) displays. These differ in the panel characteristics: different interfaces and various problems occur due to the lack of standardization.

Monochrome dual scan FPDs are the most prevalent displays in the PC market. They use a dual drive scanning scheme that requires data from two separate controller memory locations at the same time. Typically they have 8 data lines for 8 pixels per clock and 3 control signals: horizontal sync (LP), vertical sync (FLM) and Shift Clock (SHFCLK). Two power supply voltages are required. Panel interfaces differ by manufacturer and product. Even products from the same manufacturer and product line may differ. There is no standard cabling scheme and different panels have different connectors and pinouts. There is no standard labeling scheme and LCD voltages differ from panel to panel. There is no standard panel sequencing method and both horizontal and vertical timing differ for every panel.

Color dual scan LCD panels are most prevalent in the mid-range notebook PC market. They also use a dual drive scheme with LP, FLM and SHFCLK control signals. They have 8 or 16 data lines with 2 2/3 or 5 1/3 subpixels per clock, and require two power supply voltages. Interfaces are not standard and have all the same variations as the monochrome LCD displays. In addition clock divide schemes vary from panel to panel.

Color TFT panels are most prevalent in the high-end notebook PC market. They use a single panel, single drive scheme that requires data from one memory location at a time. Four control signals, Horizontal sync (HSYNC), vertical sync (VSYNC), SHFCLK and BLANK are normally used. HSYNC, VSYNC and BLANK timings are similar to a CRT. There may be 9, 12, 18 or 24 data lines with one pixel per clock. Again, two power supply voltages are required. Sharp is the dominant supplier of TFT panels and its interface is something of a de facto standard. However there are no standard cabling schemes, connectors or pinouts, and LCD voltages differ from panel to panel.

Monochrome plasma and EL panel screens are most common in embedded instruments. These are single panels with a single drive scheme. Four control signals, HSYNC, VSYNC, SHFCLK and BLANK are used with 8 data lines and 1, 2, 4 or 8 pixels per clock. Two different power supplies are used. Panel interfaces vary by manufacturer and product, with no standard cabling, connectors or pinouts. Bias voltages vary from panel to panel. There is no standard power sequencing method. Clock divide-by schemes vary and HSYNC and VSYNC timing vary from panel to panel.

Ms. Seman pointed out several challenges for present PC flat panel interfaces. There are both dual and single drive formats, as well as color and monochrome screens with various data formats. Control signals must be programmable, with independent generation of LP,

FLM, SHFCLK and BLANK signals, several divide schemes and different panel power sequencing. Variable voltage supplies are required for different panels. The challenge to controller vendors is how to support multiple panels with one controller design.

Ms. Seman was asked if the variation was product by product or by product line. Ms Seman replied that it is primarily by product line. Mr. Kevin Warren of IBM commented that the details generally don't have to do with the display technology. Rather, there are two reasons for the variations:

- To simplify the displays;
- Customers ask for them.

Ms. Seman was asked whether a standardized interface would make cheaper systems. Ms. Seman replied that a standardized interface would make things a lot easier to understand but would not necessarily result in less expensive controllers. Tim Kriegel of Hewlett Packard expressed the view that the big payoff to a flat panel interface standard would be in reducing the time to market for new products.

Mr. Sunder Velamuri of Cirrus Logic made a presentation on high resolution color LCD interface issues. His presentation is section (12). Mr. Velamuri pointed out that expanding applications are going to require much higher resolution displays than the currently common 640x480 VGA displays. He expressed the view that a standard would concentrate on active matrix displays, since the passive matrix market is relatively mature and is a "minefield" of idiosyncrasies. He sees three distinct market segments for color TFT LCDs:

- Personal Digital Assistants (PDAs) with resolutions of 640x480 or 320x240 and less than 8" diagonals;
- Notebook computers with resolutions of 800x600 or 640x480 and a 256k color palette;
- Monitors and workstation laptops with resolutions of 1280x1024 or 1024x768 and a 16.7M color palette.

Key issues for high resolution TFT LCDs include color uniformity and consistency, a color matching capability and the ability to have RGB color correction. In addition, the module form factor (thickness, weight and display area), power consumption, refresh rates, and cost are also key issues. A panel interface standard must have:

- Minimal EMI generation;
- A minimum number of data lines;
- Upward/downward expandability,
- Minimal power dissipation, the ability to drive cables of lengths greater than 3 feet;
- Appropriate hooks for multimedia;
- Expandability (i.e., 640x480, 800x600, 1024x768, 1280 x 1024, etc.).

Multimedia must be supported, including full motion video and existing video standards. The bezel width must be minimal to have a large screen and the cost impact of this cannot be large.

Mr. Velamuri outlined several interface options:

- A CRT-like panel interface with analog RGB, HSYNC and VSYNC. Gamma correction would be in the analog domain and display quality optimization would require multiple external devices to condition devices to provide opposite output voltage polarities on adjacent pixels. Among the disadvantages to this approach are the need for a high frequency PLL to recover the dot clock, cost and power dissipation and the number of ICs required;

- An analog interface that includes the dot clock. High speed A/D converters would be used to convert data to the digital domain and gamma correction would be performed with a control application specific integrated circuit (ASIC) using look-up tables. Data would then be converted back into the analog domain with high speed D/A converters. A data inverting circuit would be used to optimize display quality. Again, disadvantages would include the number of ICs and board space as well as the high cost and power consumption;

- A digital interface that is an extension of existing interfaces. It would consist of 24 data lines for one pixel per clock plus HSYNC, VSYNC, data clock (DCLK) and data enable (DE), and would have an existing base of controllers that could support this interface. Digital logic is moving from 5 V levels to 3.3 V levels. The disadvantage of this kind of digital interface would be either high frequency (to reduce the data lines) or a large number of data lines to allow lower operating frequencies.

Whatever the interface, Mr. Velamuri said that it must satisfy several compatibility requirements. First, it must be compatible with the Video Electronics Standards Association (VESA) monitor timing and 60Hz, 72 Hz and 75 Hz frame rates. Second, it must allow software driver compatibility for different resolutions and frame rates.

Mr. Velamuri was asked whether the panel standard should be strictly compatible with CRT timings. His answer was that the CRT blanking imposes too big a penalty on flat panels. Rather, it is software driver compatibility that must be achieved.

Mr. Velamuri was asked which of the alternatives he had outlined was his choice. He preferred the extension of the parallel digital interface, however he had no solution to offer to the problem of very wide buses. He felt that the multilevel logic proposal was interesting but he had many questions about it.

Mr. Velamuri was asked what additional considerations for multimedia are required. His reply was that there are two approaches: (1) concentrate the hardware in the panel, or (2)

perform the function in the controller and send it over the regular interface. Mr. Velamuri thinks that it is better to do it in the controller. When asked why not then just embed the controller in the display, Mr. Velamuri replied that it is better not to embed the controller in the display because controllers change more rapidly than panel designs.

Mr. Bill Burr, of NIST, made a presentation on the voluntary standards process. His presentation is section (13). By "voluntary standards" Mr. Burr means the published standards worked out in rather formal recognized or "accredited" standards processes. The American National Standards Institute (ANSI) is the preeminent U.S. voluntary standards organization. ANSI does not develop standards, instead it "accredits" the processes of organizations that do. ANSI is also the U.S. member of the International Standards Organization (ISO) and the International Electrotechnical Commission (IEC). Joint Technical Committee 1 (JTC1) of the ISO and IEC are the recognized international standards organizations for information technology. Mr. Burr stated that ANSI accredited procedures for developing standards are meant to ensure fairness and consensus and to reduce the risks of antitrust actions resulting from standards activities. The price for this deliberate procedure is that it takes time, and time is often what is most critical in the computer industry. Mr. Burr outlines several ways that standards originally drafted in less formal, and perhaps quicker acting, industry groups might eventually be recognized as ANSI or ISO/IEC standards.

Mr. Thomas Mock described the Electronic Industries Association (EIA) standardization process. His presentation is section (14). He stressed that the EIA is in the business of establishing information technology standards. The EIA has an extensive program in consumer electronics and audio and video standards, and its sister organization, the Telecommunications Industry Association (TIA) has one in communications-oriented standards. With the apparent fusion of the traditional computer, communications and consumer electronics industries the EIA is a key player in the information technology voluntary standards arena. The EIA (and its sister organization the TIA) are accredited by ANSI and many of the standards developed there become ANSI standards. He stated that the EIA would enjoy working with the industry on flat panel interface standards.

Mr. Daniel Chen, of Mitsubishi Electronics America, Inc., supplemented Mr. Mock's remarks by describing the activities of the components group of the EIA and their effect on standards for ICs.

Mr. Scott Vouri of Binar Graphics made a presentation on the Video Electronics Standards Association. His presentation is section (15). VESA, established in 1989, is the industry organization that has set the prevalent standards for display controllers, video BIOS, and monitors in the PC market. VESA has also established the VESA local bus (VL Bus) standard, which is now very widely used in the PC industry to provide a fast path between the CPU, memory, high speed peripherals and video controllers. Many major manufacturers of PCs, video controllers, monitors and flat panels are VESA members. VESA has five technical committees:

- Monitor;
- Local Bus;
- Advanced Video Interface;
- Software standards;
- Advanced Graphics Interface.

VESA is now developing the VESA Advanced Feature Connector (VAFC) and VESA Media (VM) Channel standards. VAFC provides a 32 bit, 150 Mbps standard for 1280 x 1024 displays that is implementable now with some cost reductions. It connects a video source (such as an MPEG processor card) to a video display adapter. It allows only a single source, is unidirectional, and cost reductions are modest. The VM channel will provide a 32-bit bus supporting 16-bit color that can connect cameras, other video sources such as VCRs, video processors, and the like to a video display adapter. This will be a bi-directional bus and will provide a greater overall cost reduction.

Mr. Vouri described possible panel display standards including an electrical interface and internal laptop connector, and an external monitor connector and a television connector. He stated that he believes VESA is the organization that has the right participants to do the job and could do it quickly and effectively by establishing a special interest group to address the controller-to-display interface. He proposed that interested individuals meet at the VESA office on Feb. 9.

The questions following Mr. Vouri's talk centered on greater participation by volume panel manufacturers, particularly Japanese firms, who were not as well represented at the workshop as the system and controller suppliers. Mr. Vouri said that VESA can reach out to the Electronic Industries Association of Japan (EIAJ), but the thing that will really bring the panel vendors in will be interest and participation of their customers, that is the system vendors. Mr. Knox of Compaq Computer noted that the panel vendors cannot react very quickly, but if customers want a standard, and allow a reasonable time for deliveries of panels with standard interfaces (18 months or so), there wouldn't be a big problem. Mr. Anders Frisk, of ICL and chairman of the VESA Monitor committee, noted that they had scheduled a meeting for March 10 to consider future monitor interfaces, and supported the idea of a meeting on the 9th to consider flat panel interfaces.

Mr. Burr moderated a panel discussion. The members of the panel were:

Mr. Thomas Credelle - Apple Computer;
Dr. Paul Alt - IBM Corporation;
Mr. Rick Knox - Compaq Computer;
Mr. Ron Pacheco - Digital Equipment Corporation;
Mr. Chuck Whelchel - Sharp Electronics Corporation;
Mr. Sunder Velamuri - Cirrus Logic.

Mr. Burr opened the discussion by asking whether a single interface standard that supports both CRTs and flat panels is required. Dr. Alt's response was that there are two different levels of interface that can and should be standardized. One of these, the remote monitor interface, should broadly support CRTs and flat panel technologies through one connector. However, it would probably be premature to immediately begin to standardize this interface; there are at present too many unknowns, including multimedia requirements, and it involves the very paradigm of computing (e.g., networked workstations versus more centralized parallel processors serving a number of relatively "dumb" terminals). Rather, additional workshops and study would be appropriate before plunging into an effort to develop a standard interface. The interface that is now ripe for immediate standardization is the interface for "captive" or "embedded" flat panel displays, such as those that are used in notebook computers. Dr. Alt believed this could be done quickly.

This position was broadly accepted by the participants and the discussion that followed was couched in those terms. Although the discussion was free-ranging and switched back and forth between the two interfaces, in the interest of clarity these minutes summarize the discussion by subject rather than in the order of occurrence.

The participants broadly agreed that in the interim until a general standard can be agreed on, the de facto standard for many remote monitor applications will be the VGA CRT interface. This standard, although deficient in some respects, is very broadly accepted in the huge IBM-compatible PC market. The workstation market is much more diverse, with a number of variations on the CRT interface.

However, there are many problems with this, especially for flat panel technology. Although now uncommon as desktop monitors, LCD panels for projection displays are becoming fairly common. The major difficulty is the range of variation in the coding of the analog video signals and the lack of a dot clock. There was a discussion of the difficulties of recovering the clock for a flat panel. There is a significant challenge to develop clock recovery that works well over the range of video sources found in computers, but it can be done.

There was no definite consensus about the range of distances that must be supported by a monitor interface, although there seemed to be agreement that something more than a few meters was desirable. Nor was it certain whether a monitor interface should be analog or

digital. Mr. Myers of Hewlett Packard returned to the theme that there need not be a sharp distinction between the two, when multilevel digital signals are included. It may be that a standard connector could support both. The precise requirements for multimedia and the level of intelligence required in the display were both discussed. There was broad support for the idea that monitor display should be able to identify themselves and their capabilities to the display controller, and that the controller should be able to configure to the display without operator intervention.

There was broad agreement among the speakers that the time is ripe to standardize the flat panel device interface for embedded displays, such as those in notebook computers and PDAs. Even in this area, there are three fairly distinct markets: PDAs with relatively small screens, notebook computers with at least 640 x 480 resolution, and laptop engineering workstation displays which need a minimum resolution of 1024 x 768. Moreover, both active and passive matrix color and monochrome displays are in fairly wide use. Mr. Burr asked the panel if it is sufficient to cover only the AMLCD displays in the standard and assume that the other technologies are mature and not in need of standardization. The response from the panel was that the other technologies are not disappearing any time soon and that, to be effective, the interface standard should not be limited to just AMLCD displays, but should be applicable to other LCD, plasma, and EL displays.

Although the amount of "intelligence" required on the panel for various applications was not settled by the discussion, broad support was expressed for the idea that enough functionality should be contained in the panel to regularize the interface, in the interest of supporting diverse displays with one interface. This concept, first expressed by Dr. DaCosta in his talk on the previous day, seems to offer a good prospect of a single interface that broadly encompasses various display technologies. The amount of extra functionality incorporated on the panel itself may depend on the application and the intended market niche. Much sentiment was expressed that the panel itself, and not the video controller, is the proper place for such functions as gamma correction and temperature compensation.

Digital versus analog interfaces were again discussed. Most LCD panels expect a digital input. However, some panels are entirely analog. The general trend in data transmission is digital, and most participants felt that gamma correction and temperature compensation could best be done in the digital domain. There was some discussion about requirements for temperature compensation and gamma correction. Many applications may not be particularly sensitive to precise color matching or consistency, but many other image intensive applications are quite sensitive to these factors.

Mr. Burr noted that there are broadly useful de facto standards for the physical "footprint" of storage peripherals, as well as their interfaces. This, he noted, greatly facilitates plug and play substitution of peripherals by end users. Is it appropriate to consider similar footprint standards for displays? The consensus of the panel was that this would be unwise. Not only are the physical packages for displays evolving, but the physical size of

the display is directly related to and largely determined by its function. This is not the case for storage peripherals. There is no reason simply to change the size of a disk drive for its own sake, but there are applications for displays of many sizes.

A final concern expressed was that mass market FPD vendors were not as well represented on the panel and in the workshop as were computer system manufacturers and controller vendors. This had been sounded earlier in the workshop and would be repeated in the following discussion of proposals for standards development. The feeling seemed to be that it took some time for panel vendors to respond to such initiatives, but if system vendors expressed their interest to their panel suppliers, then they would participate.

At the conclusion of the panel discussion, Mr. Williamson opened the floor to specific proposals on how to proceed. Mr. Vouri made the proposal that VESA establish a special interest group to address the controller to captive flat panel interface in a timely manner. He proposed that interested individuals meet at the VESA office in San Jose on 9 February. Mr. Burr took the floor and led a discussion to develop a consensus about the specific conclusions and action items resulting from the workshop.

The consensus reached at this workshop resulted in the following action items:

1. Form a Video Electronics Standards Association Special Interest Group (VESA SIG) to undertake the development of a standard or a series of standards for the interface between a flat panel display and its controller. This interface standard will address both active and passive FPDs in integrated devices. It will cover both the electrical and the mechanical (connector) specifications.

   An organizational meeting will be held on February 9, 1994, at the VESA headquarters with the intention of having a proposal ready to discuss with manufacturers of FPDs at the Society for Information Display (SID) meeting in June. Inputs are requested by March 9, 1994.

2. NIST will seek to inform all materially interested parties, especially the flat panel display manufacturers, of the standards plans, and encourage their participation.

3. VESA will distribute the February 9, 1994, meeting announcement and agenda.

4. The interface for remote FPDs requires additional technical discussions before a standard can be written. Additional workshops on display interfaces and /or technical sessions at the SID Symposium should be explored. In addition, the VESA Monitor Committee invited interested parties to participate in their committee which will be considering interfaces and connectors to desktop and remote FPDs in addition to their CRT interface work.

Dr. Paul Alt will seek to set up a technical session at future SID meetings to consider these long-term display interface requirements. It is too late to add a technical session on interface topics at SID '94. However, an interface session may be possible for SID '95.

The meeting adjourned at 4:00 PM on January 14.

1

Workshop Agenda

UNITED STATES DEPARTMENT OF COMMERCE
National Institute of Standards and Technology
Gaithersburg, Maryland 20899-0001

Workshop on the Computer Interface to Flat Panel Displays
San Jose Hilton and Towers
San Jose, California

January 13, 1994

11:30 AM **Check In**

12:30 PM **Opening remarks**
Mr. Mark Williamson, NIST

12:45 PM **"NIST's Advanced Technology Program"**
Mr. Thomas Leedy, NIST

1:10 PM **"Issues in Interfacing Flat-panel Active Matrix TFT LCDs"**
Dr. Victor Da Costa, Xerox PARC

1:35 PM **"High Performance, Cost-Effective Computer and Video Interfacing to Megapixel AC-PDPs"**
Ms. Carol A. Wedding, Photonics Systems

1:50 PM **"Sun's Proposal for a Unified Display Interface"**
Mr. Marc Klingelhofer, Sun Microsystems

2:15 PM **"I/O Connectors for Video Applications, History, Requirements, and Technology to Meet Those Needs"**
Mr. Gary Manchester, MOLEX, Inc.

2:40 PM BREAK

3:00 PM **"Issues in FPD Interfaces for PC and Workstation Use"**
Mr. Bob Myers, Hewlett-Packard Co.

3:25 PM **"Plug and Play Flight Instruments"**
Dr. Bill Hale, Wright-Patterson AFB

3:50 PM **Q&A, Speaker Interviews, General Discussion**

4:30 PM **Reception**
Hot and cold hors d'oeuvres and cash bar

Workshop on the Computer Interface to Flat Panel Displays
San Jose Hilton and Towers
San Jose, California

January 14, 1994

9:00 AM **Opening remarks**
Mr. Mark Williamson, Mr. Dana Grubb, NIST

9:10 AM **"United States Display Consortium"**
Dr. Bob Pinnel, United States Display Consortium

9:30 AM **"Issues Related to Interfacing Flat Panel Displays"**
Ms. Jill Seman, Chips and Technologies

9:55 AM **"High Resolution Color LCD Interface Issues"**
Mr. Sunder Velamuri, Cirrus Logic

10:20 AM BREAK

10:40 AM **"The Voluntary Standards Process"**
Mr. Bill Burr, NIST

11:10 AM **"Electronic Industries Association (EIA)"**
Mr. Thomas Mock, EIA.

11:30 AM **"Video Electronics Standards Association (VESA)"**
Mr. Scott Vouri, Binar Graphics, Inc.

12:00 PM LUNCH

1:00 PM **Panel Discussion, "Are Standards Needed for the Computer Interface to Flat Panel Displays?"**
Moderator: Mr. Bill Burr, NIST
Panel Members: Mr. Sunder Velamuri, Cirrus Logic
Mr. Charles Whelchel, Sharp Electronics
Mr. Thomas Credelle, Apple Computers
Mr. Rick Knox, Compaq Computer
Dr. Paul Alt, IBM Corporation
Mr. Ron Pacheco, Digital Equipment Corp.

2:30 PM **Proposals for Standards Development and Future Activities, Invited**

3:00 PM BREAK

3:20 PM **Discussion of Proposals and Action Items**

4:00 PM **End of Workshop**

2

List of Attendees

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3

Opening Remarks

Mark P. Williamson, NIST

NIST Workshop on the Computer Interface to Flat Panel Displays

January 13 - 14, 1994

San Jose Hilton and Towers

San Jose, California

NIST
UNITED STATES
DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS
AND TECHNOLOGY

Introductions

- Mr. Dana Grubb, Co-chairman
- Mr. William E. Burr, Secretary, Moderator
- Mr. John Roberts
- Mr. Thomas Leedy, ATP
- Mr. Mark P. Williamson, Organizer, Chairman

Workshop Objectives

- Determine the need for a standard or a series of standards for the computer interface to flat panel displays
  - logical, electrical, & mechanical
    - » integrated device displays
    - » FPD monitors
    - » entertainment displays

Workshop Objectives

- Identify what types of standards are needed
  - de facto standards
  - formal national standards
  - formal international standards
- Identify viable approaches for developing flat panel display interface standards
  - industry groups
  - formal standards committee

Workshop Objectives

- Obtain consensus on a coordinated plan for standards development

NIST Activities in Flat Panel Displays

- NIST - the nation's leading measurement and standards laboratory
- Computer Systems Laboratory
  - Flat panel display interfaces
- Electronics and Electrical Engineering Lab
  - Display performance and quality metrics
- Physics Laboratory
  - Radiometric, colorimetric & photometric calibration
- Advanced Technology Program
  - American Display Consortium

NIST Flat Panel Display Interface Project

- **Support standards development**
  - initiate and participate in standards activities
  - provide a neutral laboratory for prototyping and feasibility studies
  - represent government agencies' interest in standards development

NIST Flat Panel Display Interface Project

- Support the implementation of advanced display technologies
  - research and development of advanced interfaces
  - prototype and demonstrate high risk / advanced interfaces
  - develop meaningful performance measurements

4

NIST's Advanced Technology Program

Mr. Thomas Leedy, NIST

NIST

Advanced Technology Program

Thomas Leedy
Project Manager

National Institute of Standards and Technology
Technology Administration
Department of Commerce

Advanced Technology Program

MISSION

- Stimulate U.S. economic growth through the development and application of high-risk technologies by companies.

ATP STRATEGY

Work with U.S. industry to plan, execute, and co-fund high-risk technology development programs. Develop technologies that are:

- ENABLING - - provide technical basis for process- and product-specific applications

- HIGH VALUE - - offer large and/or strategic long-term benefits to the U.S. economy

ATP ELIGIBILITY

- Individual companies
  - No more than 3 years
  - Up to $2 million total
  - ATP pays only direct costs

- Joint ventures
  - No more than 5 years
  - No limit on award amount
  - ATP share less than 50%

- No direct funding to universities, government agencies or non-profit independent research institutes

MAJOR CHARACTERISTICS OF THE ATP

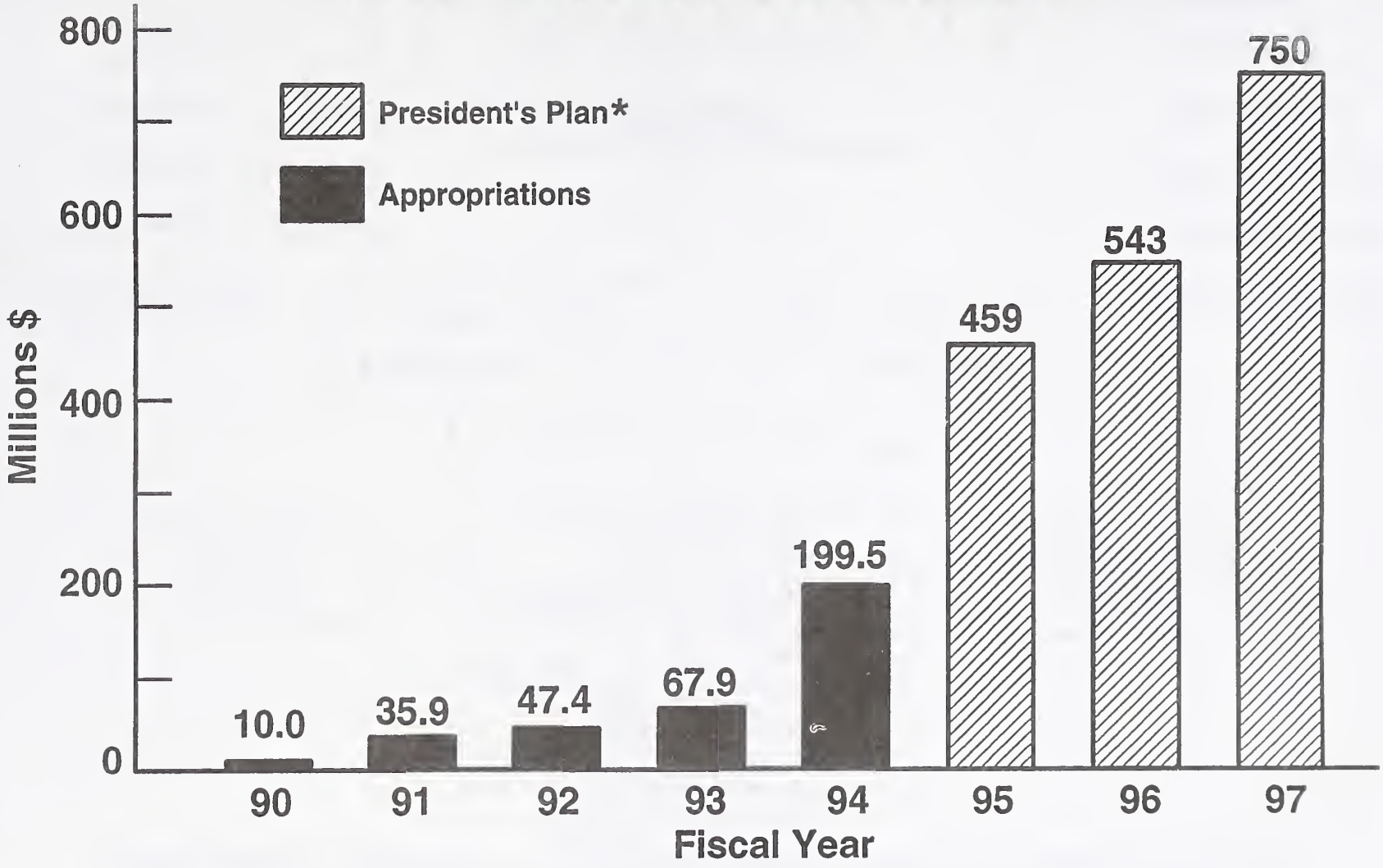
- Development / application of high-risk technologies to stimulate economic growth
- Market oriented -- industry proposes ideas, shares costs, and performs work
- Competitive selection process - - technical and business merit
- Cost sharing

ADVANCED TECHNOLOGY PROGRAM
Important Statistics - - 3 Competitions

Proposals Submitted	660
Participating Organizations*	1232
Total ATP Funding Requested	$1 B
Total Estimated Cost Share	$1 B
Number of Awards	60
(Joint Ventures)	(18)
(Single Applicants)	(42)
Participating Organizations*	150
Total ATP Funds Committed	$187 M
Total Estimated Cost Share	$210 M
Award Size - - Range	$500K - $20 M

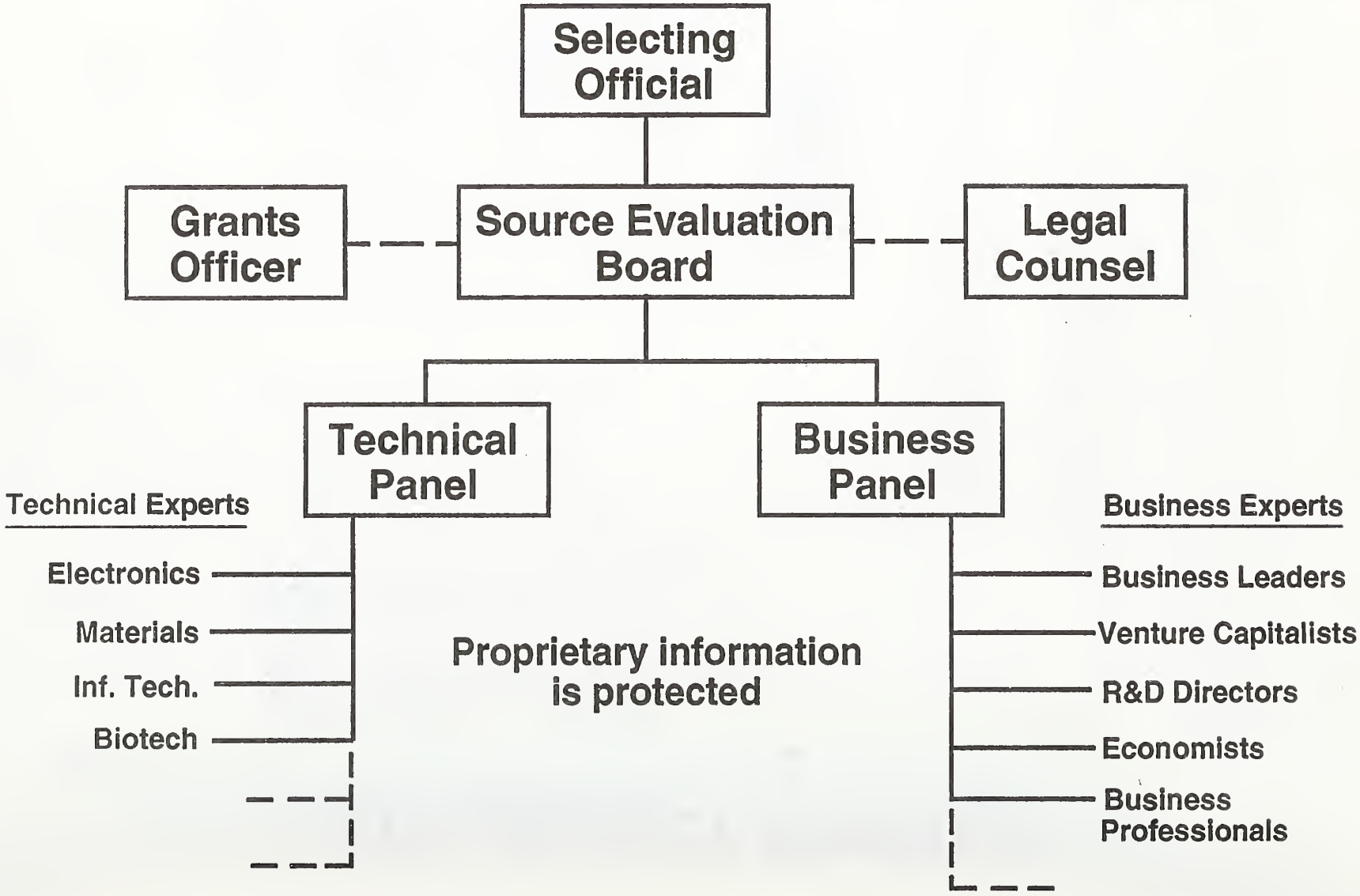
* Excludes Subcontractors

ATP BUDGET PROFILE



* Based on "A Vision of Change for America," President Clinton's Economic Plan - - February 17, 1993

SELECTION PROCESS MANAGEMENT

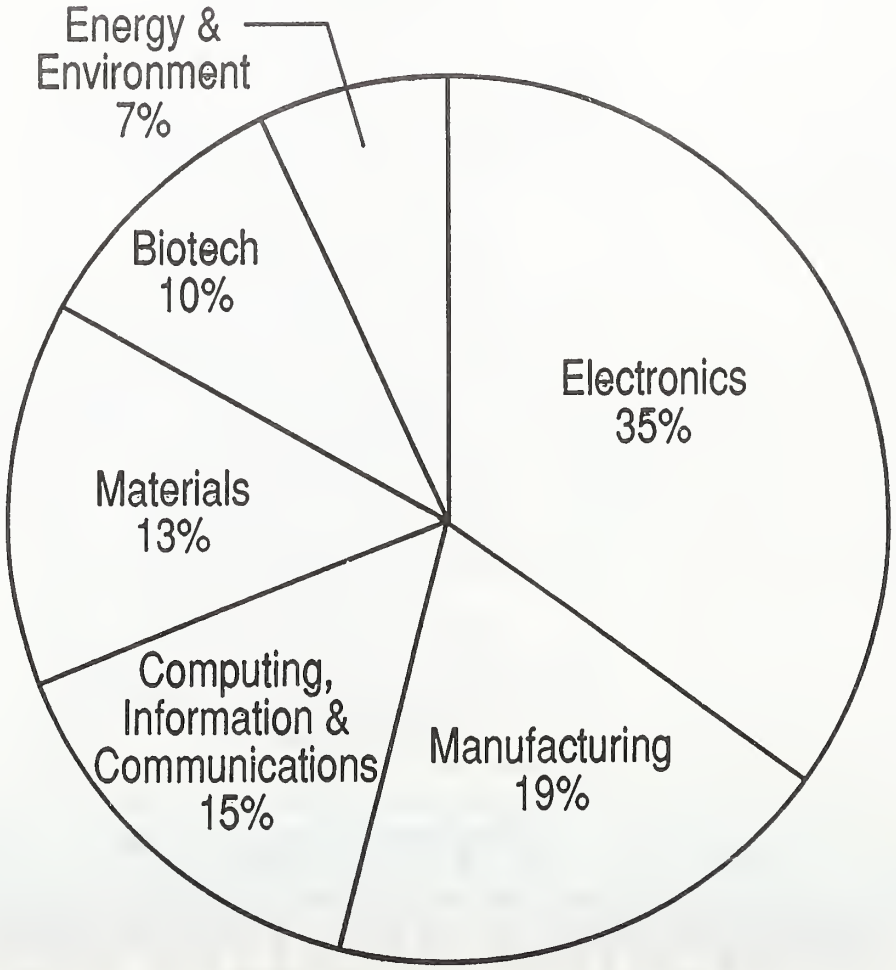


ATP SELECTION PROCESS

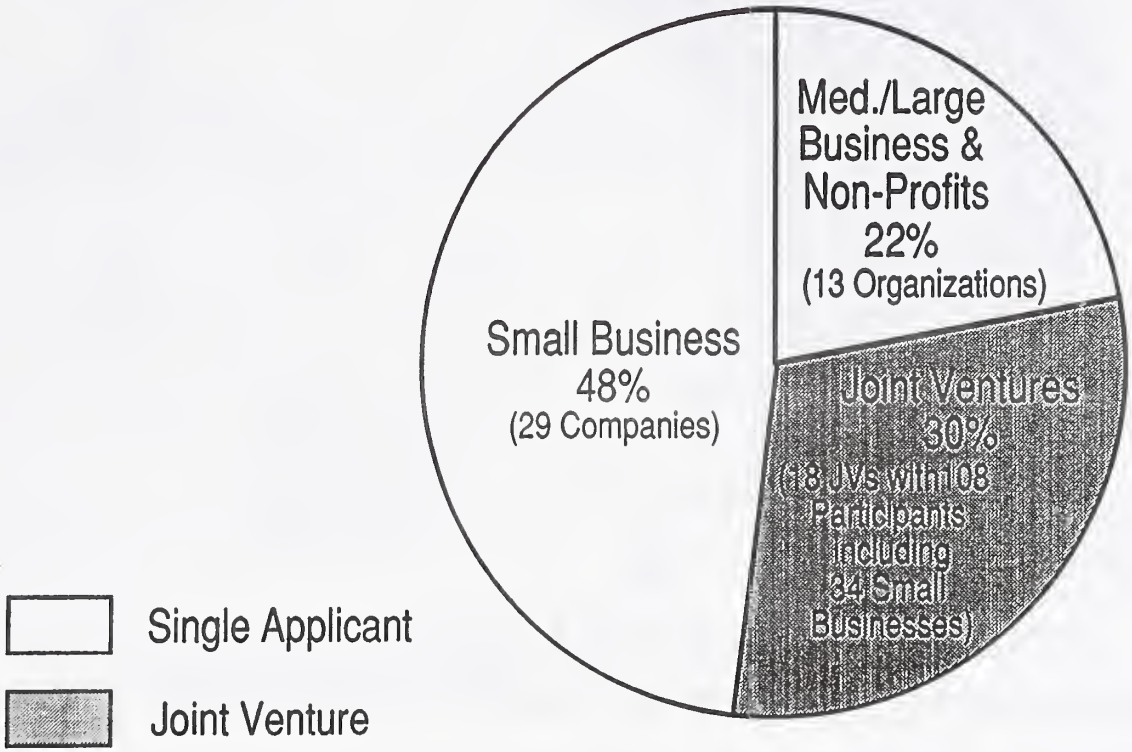
ATP COMPETITIONS 90-01, 91-01, & 92-01

TECHNOLOGIES FUNDED BY ATP

As a percent of $187 M Awarded

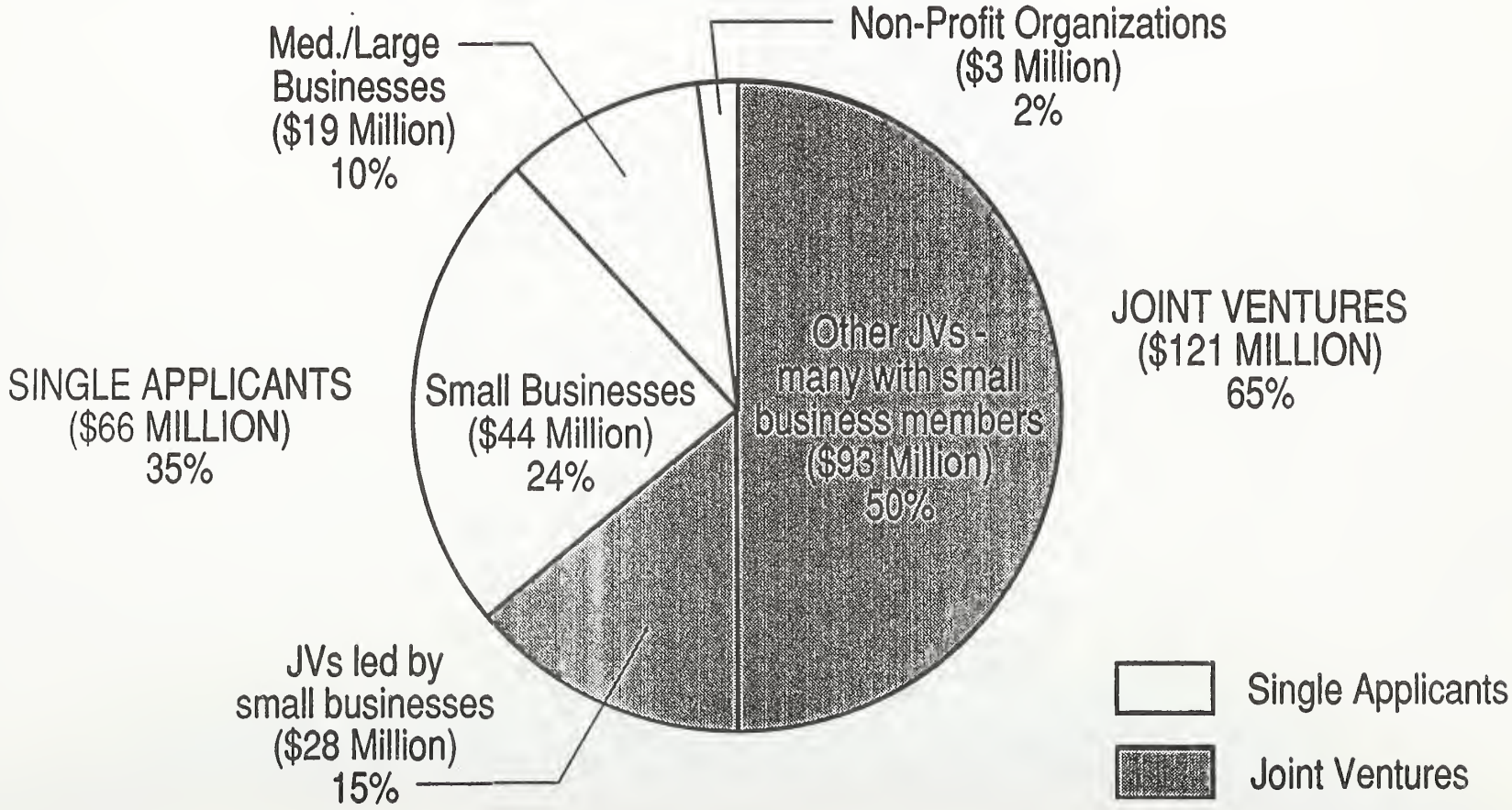


ATP 60 AWARDEES
BY TYPE OF ORGANIZATION



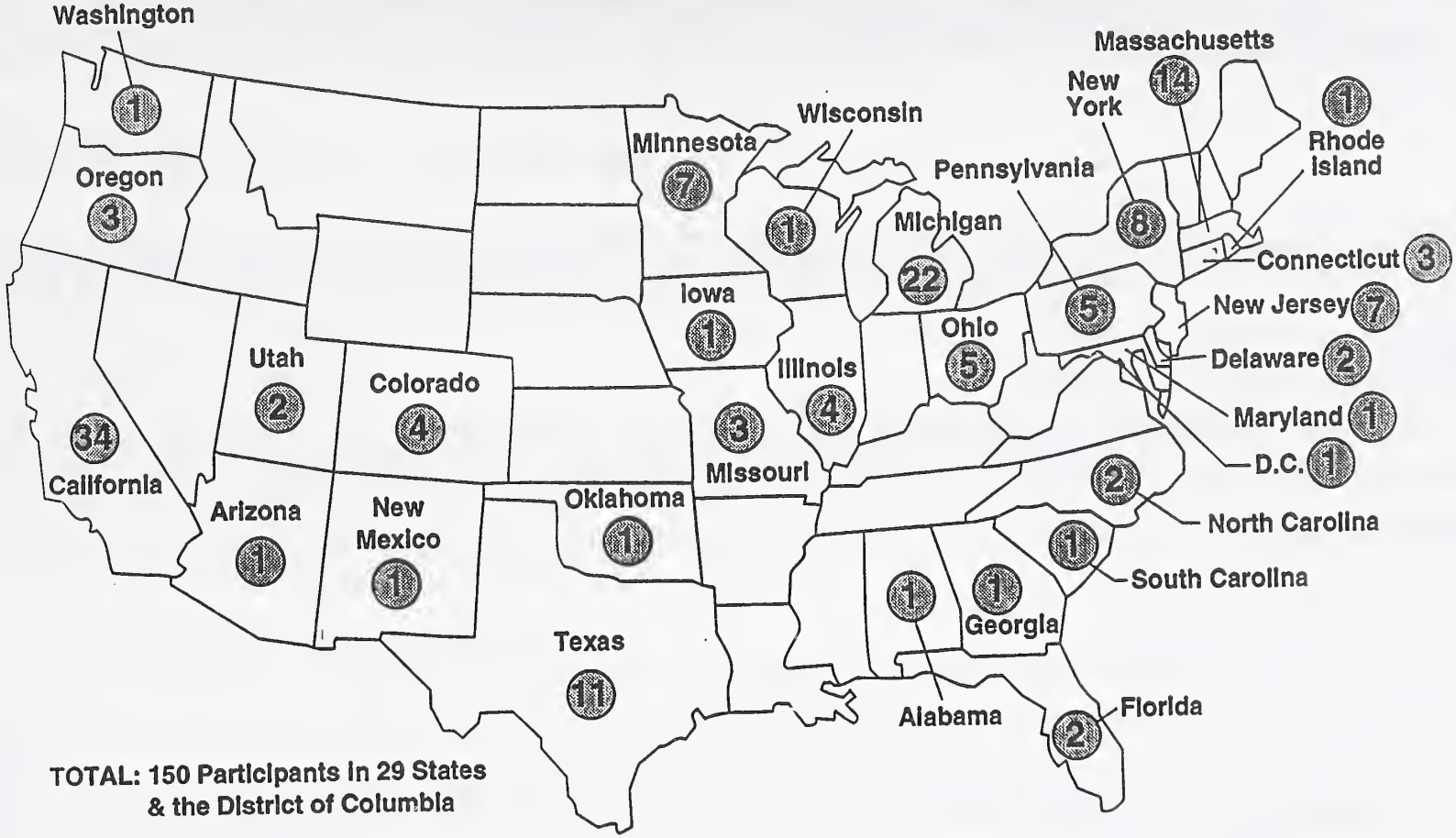
ATP COMPETITIONS 90-01, 91-01, & 92-01

$187 MILLION OF ATP FUNDS AWARDED
BY TYPE OF ORGANIZATION



ATP COMPETITIONS 90-01, 91-01, & 92-01

ATP PARTICIPANTS* BY STATE



TOTAL: 150 Participants in 29 States & the District of Columbia

* "Participants" includes joint venture members, and excludes subcontractors, informal collaborators with joint ventures, and collaborators and strategic partners of single applicants.

Display Technology

Advanced Manufacturing Technology for Low-Cost Flat-Panel Displays

American Display Consortium,

A joint venture by several U.S. producers of flat-panel displays for computers – competing against large, vertically integrated Japanese firms – to develop key production and testing technologies for a multi-billion-dollar industry.
ATP Award: $7,305 K Project budget: $14,909 K

Scalable High-Density Electronics Based on MultiFilm Modules

The MultiFilm Venture, Taunton, MA

Develop high-density electronic circuit modules based on thin-film silicon circuits which can be closely packed laterally and vertically.
ATP Award: $2,776 K Project budget: $5,705 K

Display Technology

Large Area Digital HDTV Field Emitter Display Development

FED Corporation

Develop manufacturing techniques for large-scale, flat panel displays based on arrays of field emitters to make a sort of "flat CRT."

ATP Award: $2,000 K

Project budget: $2,943 K

Patterning Technology for Color Flat-Panel Displays

The American Display Consortium

Develop a group of patterning technologies necessary for the manufacture of color flat-panel displays, including large-area photoexposure tools, printing tools, panel alignment methods, and a final inspection tool.

ATP Award: $6,464 K

Project budget: $13,192 K

Display Technology

Optically Controlled Alignment Materials for Liquid-Crystal Displays

Hercules, Inc.

Develop a novel technology for optically aligning liquid crystals using polarized light, leading to an improved method of manufacturing liquid crystal displays at lower costs and greater yield.

ATP Award: $1,671 K Project budget: $3,042 K

Advanced Cathode for Flat Fluorescent Light Source

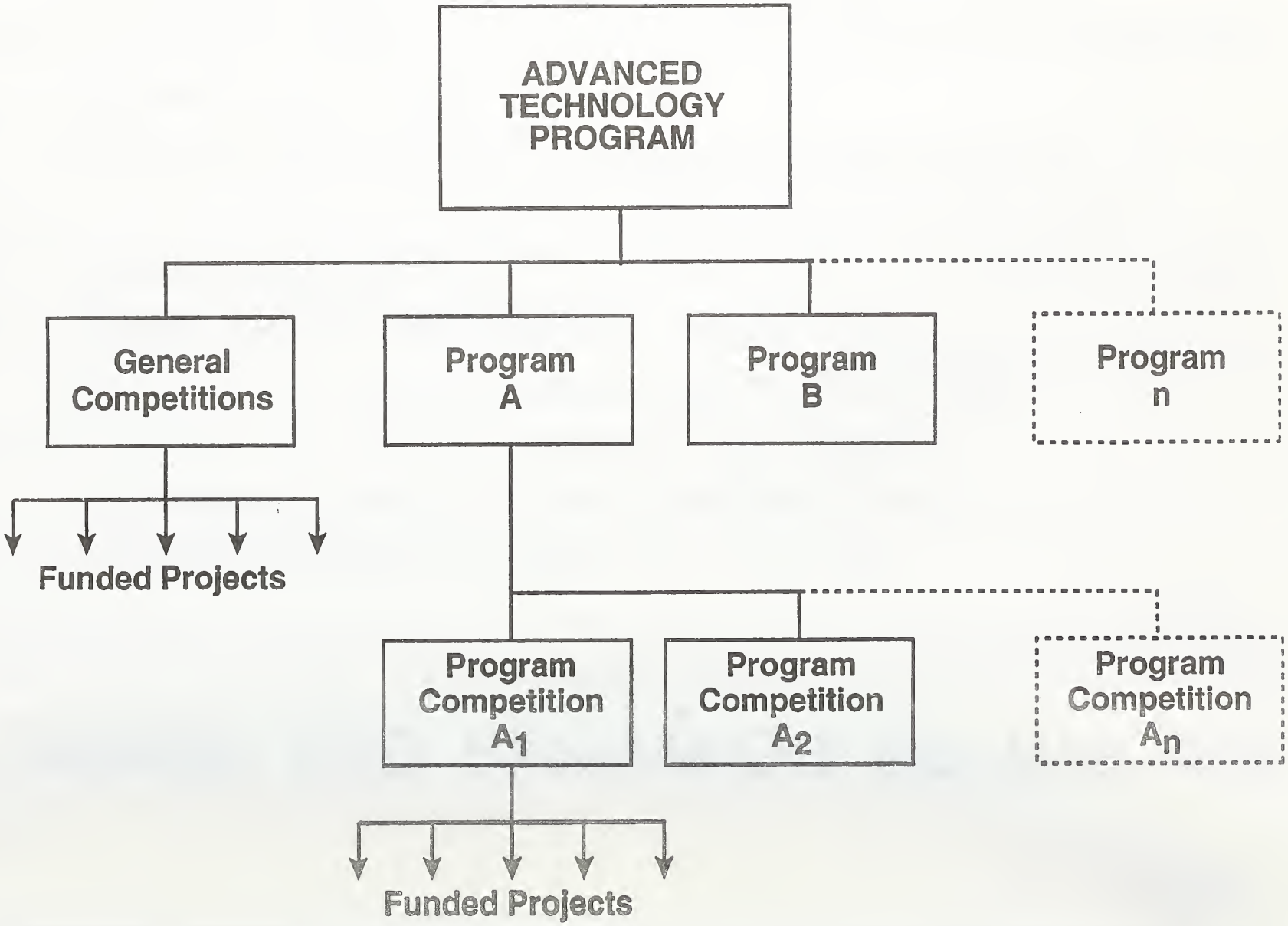
Thomas Electronics, Inc.

Develop a novel barium dispenser cathode for flat fluorescent lights, making possible a new generation of high-efficiency, high reliability area light sources for use in flat panel displays.

ATP Award: $718 K Project budget: $933 K

ROADMAP FOR EXPANSION OF THE ATP 1994 TO 1997

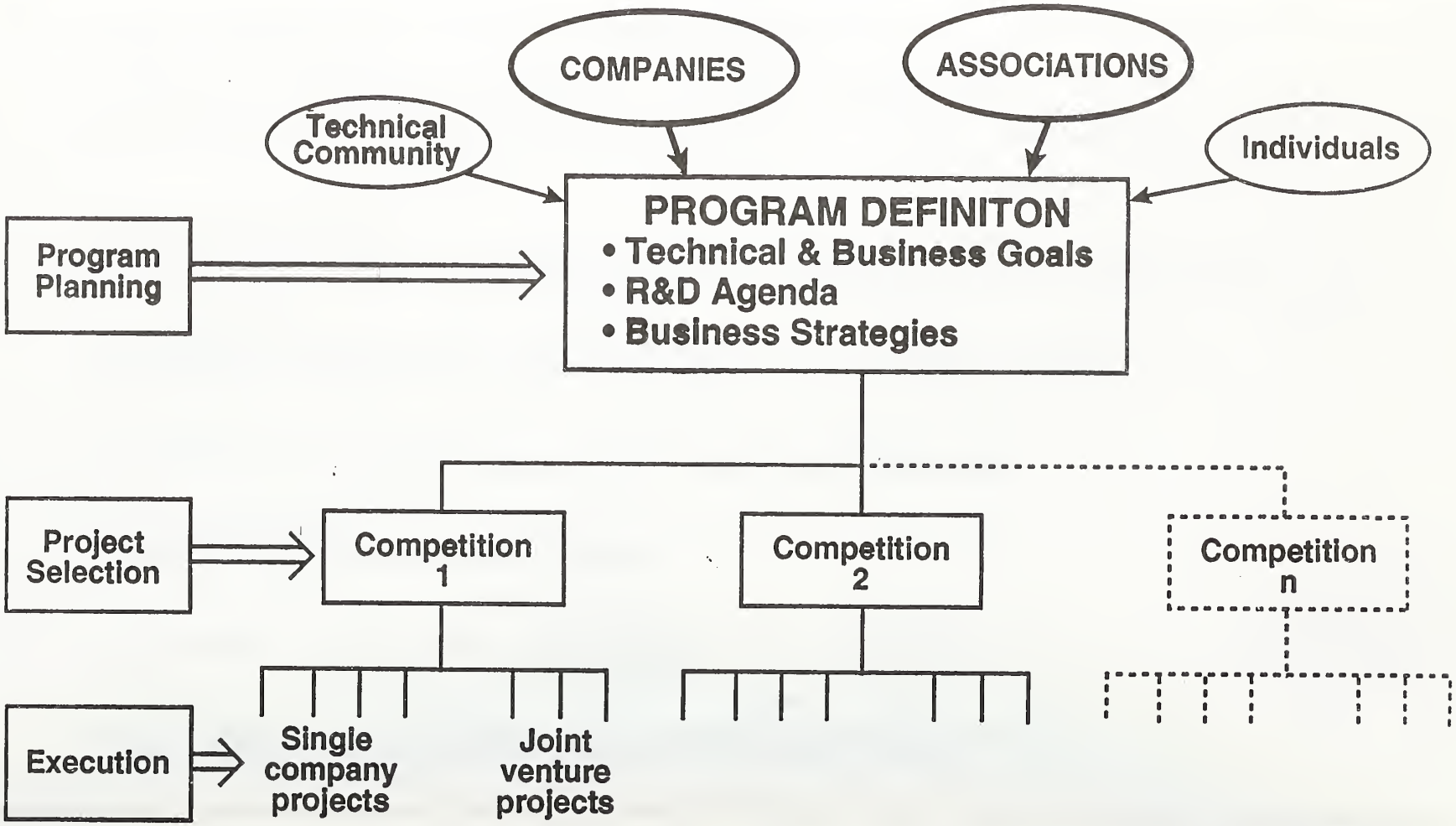
- Establish programs under the ATP with well-defined technical and business goals
- Establish an administrative framework to get industry ideas and evaluate, define, and select programs
- Increase the number of projects funded through program competitions
- Continue to hold general competitions - - open to all areas of technology


ADVANCED TECHNOLOGY PROGRAM
General Competitions
Program A
Program B
Program n
Funded Projects
Program Competition A_1
Program Competition A_2
Program Competition A_n
Funded Projects

DESIRED PROGRAM CHARACTERISTICS

- Well-defined technical and business goals
- Pathway from R&D to market
- Well-defined research plan
- Measurable impact on U.S. economic growth
- Program duration: approximately 5 or more years
- Program funding: in the range of $20-50 million per year (federal share)
- Multiple competitions per program - - each competition can result in multiple projects - - single companies and joint ventures
- Performance measures linked to technical / business goals and ultimate impact on economic growth

PROGRAM DEFINITION AND EXECUTION



CRITERIA FOR ATP PROGRAM SELECTION

1. POTENTIAL U.S. ECONOMIC BENEFIT
2. GOOD TECHNICAL IDEAS
3. STRONG INDUSTRY COMMITMENT
4. OPPORTUNITY FOR ATP FUNDING TO MAKE A MAJOR DIFFERENCE

ATP Program Planning and Execution

KEY CONCEPTS

- ATP listens to industry
- Joint development of technology and business goals and R&D plans
- Industry executes R&D and commercialization
- Cost-sharing essential
- Aim to enhance U.S. economic growth
- Success depends on good ideas and cooperation from industry

SEND US YOUR PROGRAM IDEAS!

HOW TO SUBMIT A PROGRAM IDEA

- Submit a letter or brief white paper (< 10 pages) that describes the proposed technical and business goals and addresses program selection criteria to:

Program Ideas
Advanced Technology Program
NIST
A430 Admin. Bldg.
Gaithersburg, MD 20899

Tel. 1 - 800 - ATP - FUND (General Information)
Facsimile 1 - 301 - 926 - 9524
E-Mail ATP@MICF.NIST.GOV

NO PROPRIETARY INFORMATION SHOULD BE SUBMITTED!

5

Issues in Interfacing Flat-panel Active Matrix TFT LCDs

Dr. Victor Da Costa, Xerox PARC

Issues in Interfacing Flat-panel Active Matrix TFT LCD's

Victor M. Da Costa and David D. Lee

Xerox Palo Alto Research Center

3333 Coyote Hill Road

Palo Alto, CA 94304

XEROX

PARC

No standard interface to flat panel displays

- Characteristics or requirements of FPDs vary among technologies and applications.
- This leads to customization and complexity in interface design

Need for

- A consistent and flexible interface to the widest possible range of FPDs.

Contents

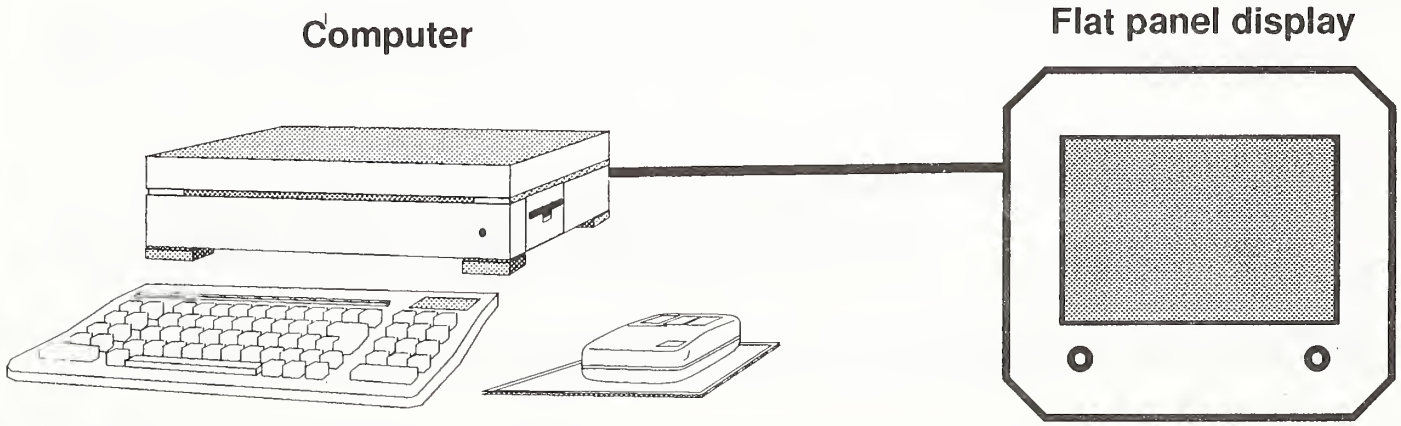
1. Basics of Matrix driven FPDs interfaces.

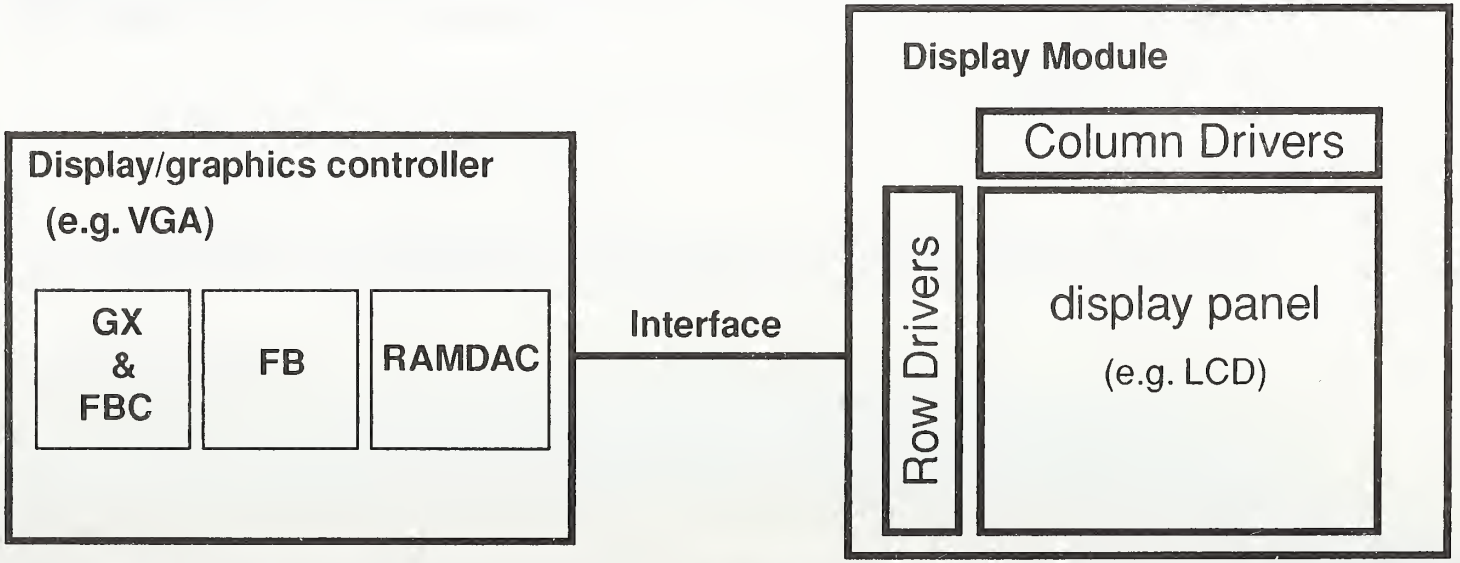
2. Interfacing problems in driving AMLCD's.

3. Summary and conclusions.

This talk will be AMLCD specific, but the basic concepts apply to FPDs in general.

Components in flat panel display interface





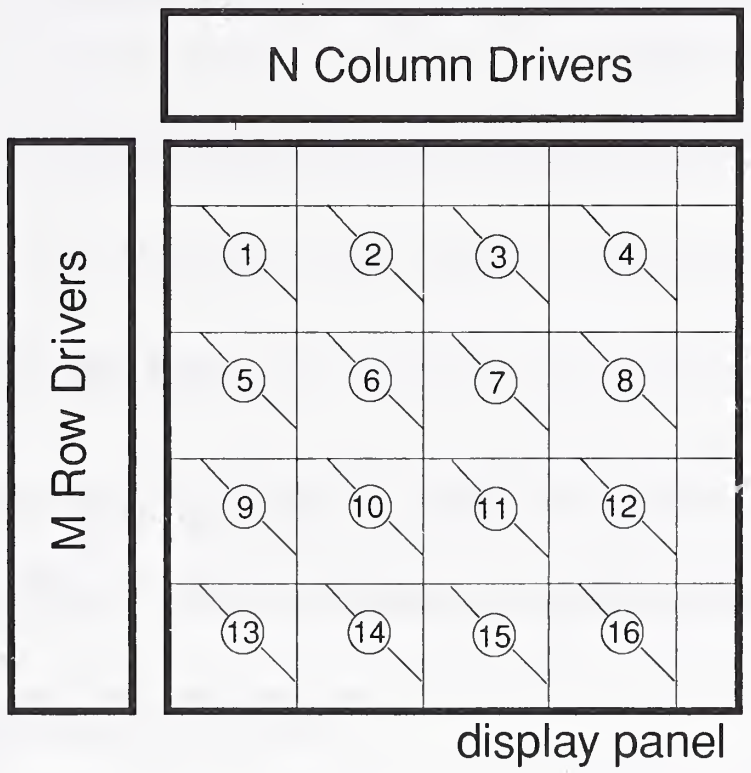
XEROX PARC

A Matrix Driven FPD

To address NXM pixels requires N+M drivers (minimum).

Two types of drive schemes:

Passive STN LCD - uses time multiplexed drive.
Active Matrix LCD - a transistor at each pixel provides drive at all times.



CRT display:

single ***pixel*** scan

Matrix driven FPD:

single ***row*** scan

Trends are to:

Highly optimized/customized display adapter to handle display dependent functions.

This leads to:

- complexity in the display controller ASICs.
- similar displays in function having different signals/connectors.
- the controller needing to change as the display parameters (resolution, number of colors) change.

Simple and generalized column and row driver ICs

- They tend to have common characteristics (# of drive outputs, output voltage levels).

Contents

1. Basics of Matrix driven FPDs Interfaces

2. Interfacing problems and issues

3. Summary and conclusions

Active Matrix LCD

Characteristics of future AMLCDs:

- wide range of technologies and driver electronics will be used

  TFT technologies - Poly Si, α-Si
  LC materials
  driver IC and packaging

- very high resolution and more colors

  more than 1000 lines and 1000 color pixels per line
  3 or more subpixels per color pixel with 6-8bit gray levels per subpixel.

- high image quality

  active matrix technology will be better than a CRT

Problems and Issues in Driving High Resolution AMLCD's

1. Analog or digital interface, which one?
2. Speed mismatch in frame buffer output and panel driver IC input.

Image Quality Issues:

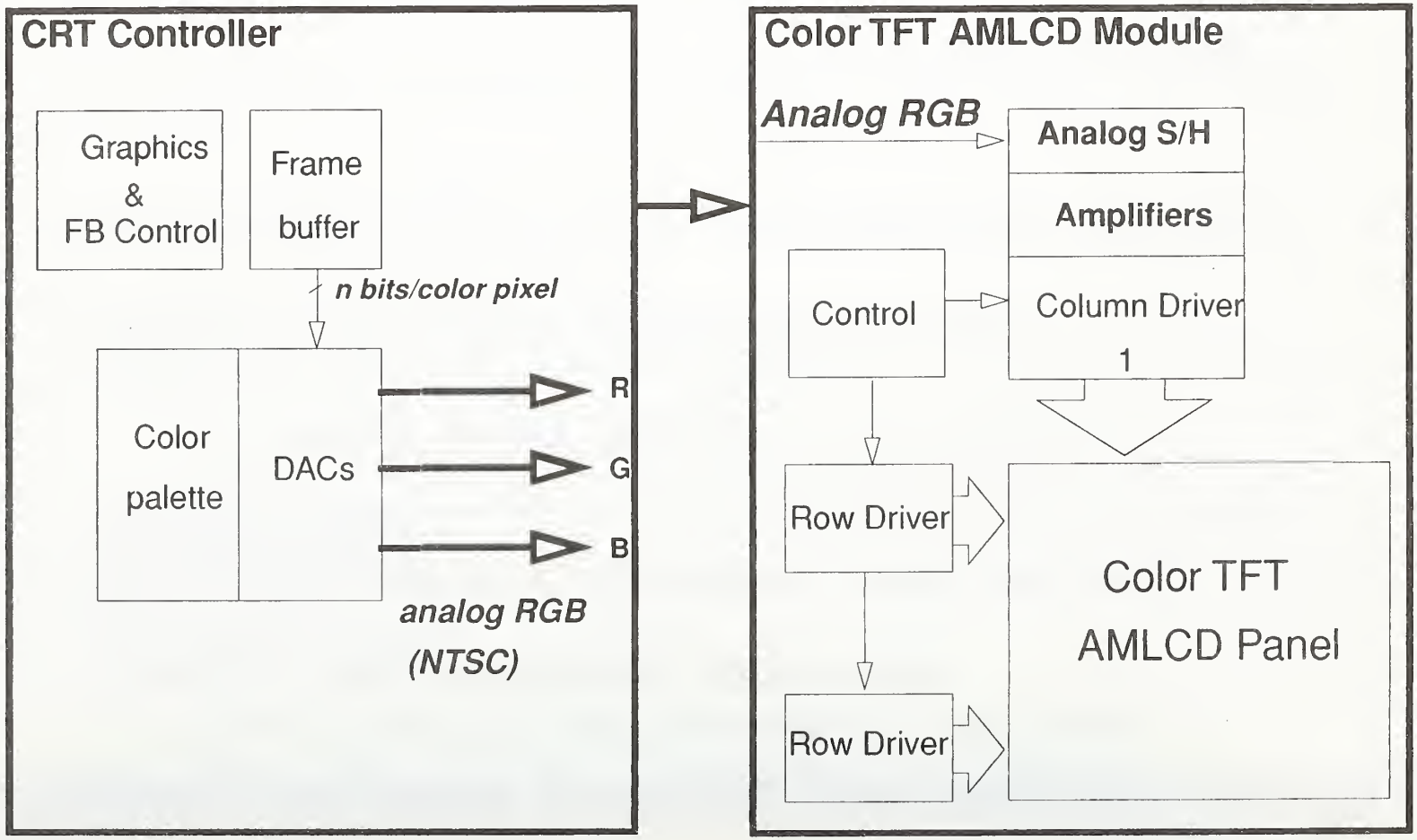
3. Different color filter mosaics may be used.
4. Differing Color/grey level control/correction schemes

→ These issues lead to complexity in interface design.

This results in highly customized graphics adapters to handle AMLCD-specific controls.

Analog or Digital Interface

Analog interface:



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Analog vs. Digital Interface

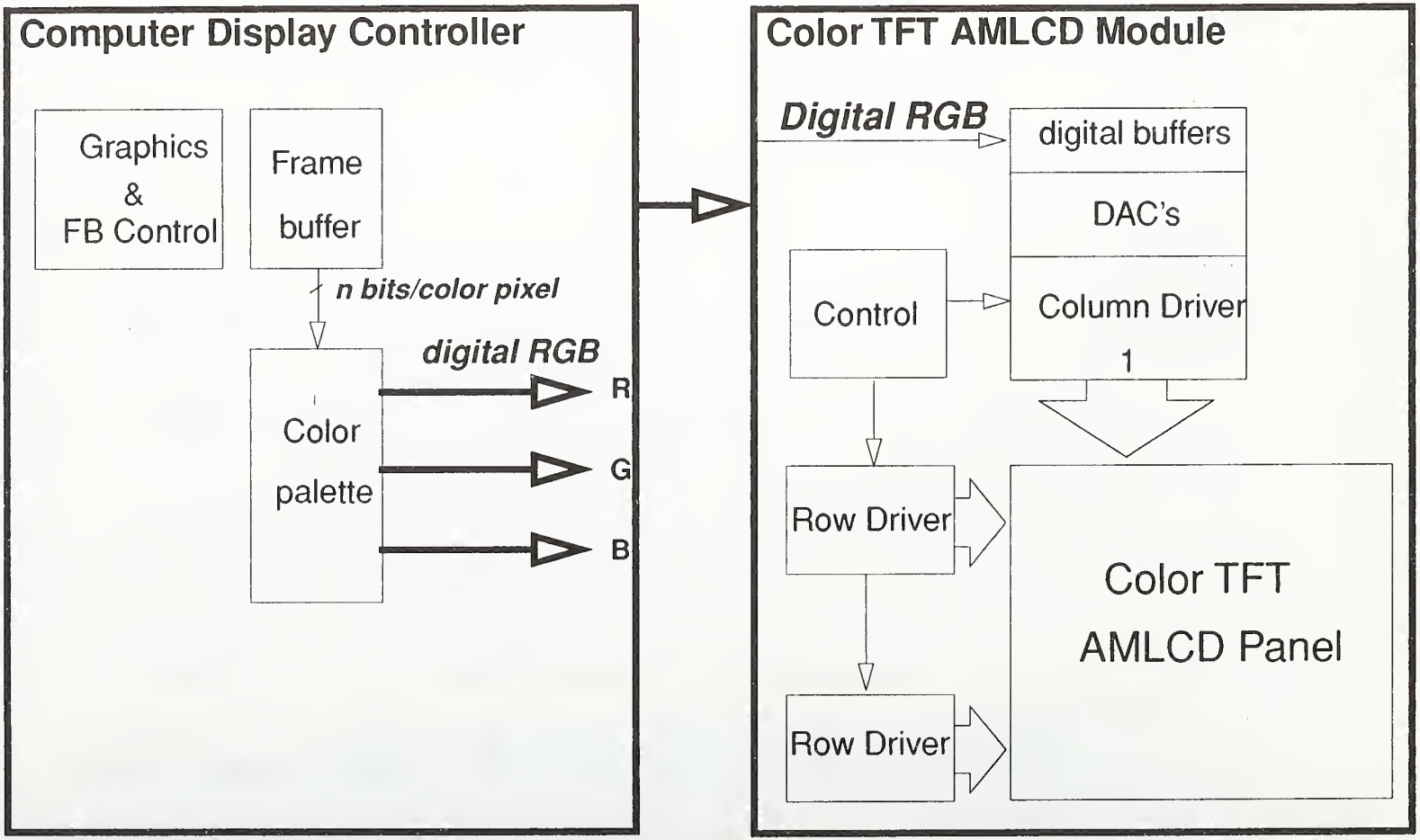
Color TFT AMLCD with 60 Hz refresh rate

Display	Resolution	Line Time	Pixel Time - Color (sub-pixels)
VGA AMLCD	3 X 640 X 480 (921,600 pixels)	34.7 *u*sec	**54.3 *n*sec** (17 *n*sec)
Super VGA/ XGA AMLCD	3 X 1024 X 768 (2,334,720 pixels)	21.9 *u*sec	**21.4 *n*sec** (7.1 *n*sec)
High Resolution AMLCD	3 X 1280 X 1024 (3,932,160 pixels)	16.3 *u*sec	**12.7 *n*sec** (4.2 *n*sec)

Analog sample and hold column drivers become too difficult to implement at these speeds and densities.

Analog vs. Digital Interface

Digital interface:



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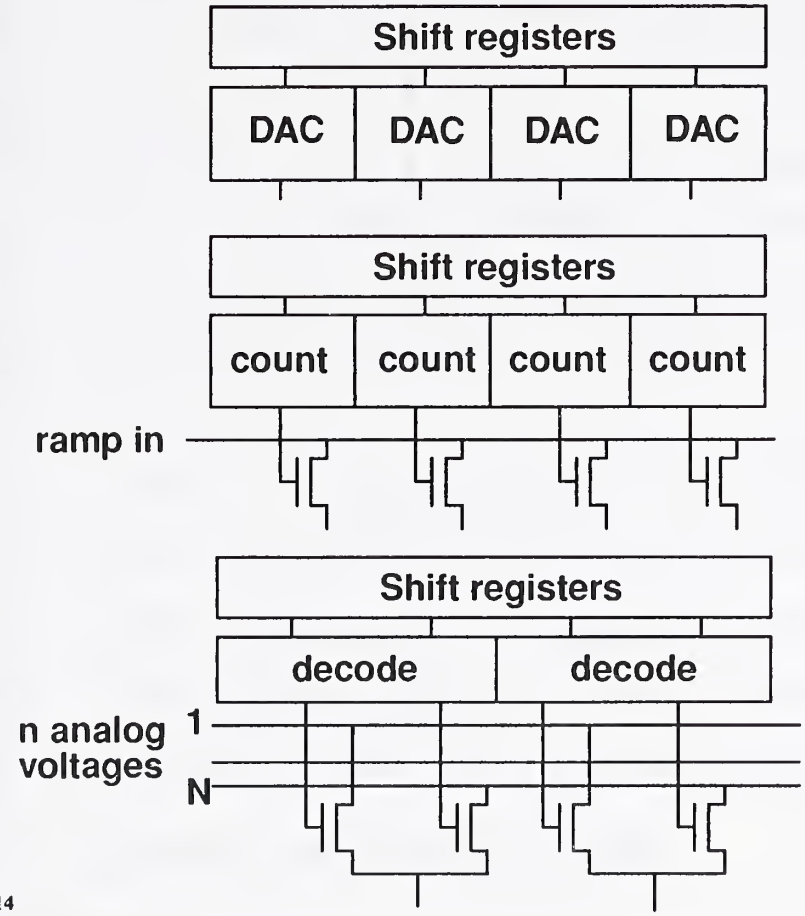
Digital Panel driver (column) ICs

Digital RGB inputs (9-12bits), 192 outputs (at ~20V moving to 5V) typically.

Pin-limited, high voltage output requirement (low speed).



DACs

- digital inputs
- many DAC per chip

Sampled ramp

- programmable ramp, digital inputs
- complex digital circuits

1-of-N selector

- programmable voltage levels
- many pass gate per data line

Problems and Issues

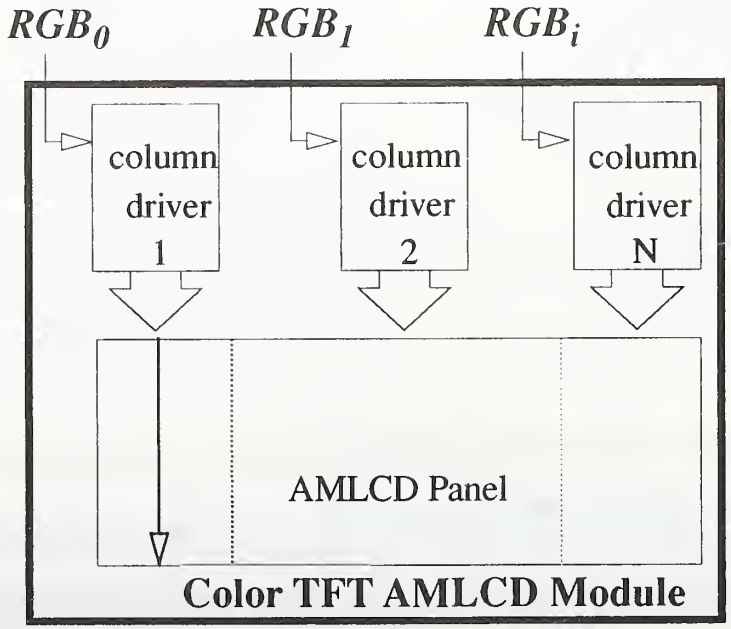
2. Mismatch between frame buffer output and panel driver IC input

Higher resolution → shorter line time and requires more drivers

High bandwidth VRAM serial port vs. slow column drivers

One Solution: Parallel loading of panel driver IC's

→ requires serial to parallel conversion of data stream



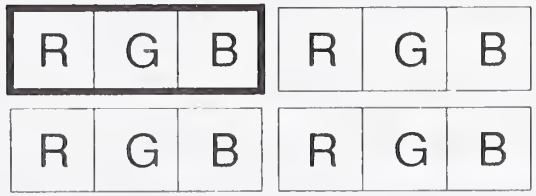
Problems and Issues

3. Color filter arrangements

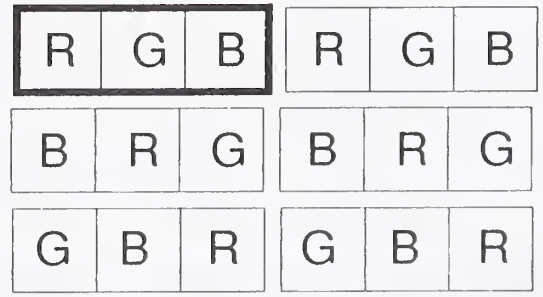
Application & image quality dependent color mosaics

→ This requires line buffering and data rearrangement

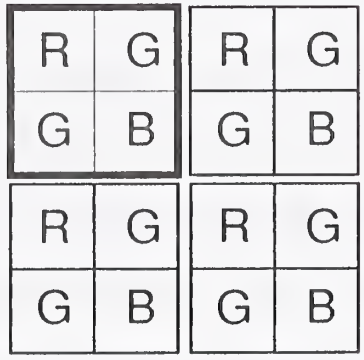
Vertical Stripe



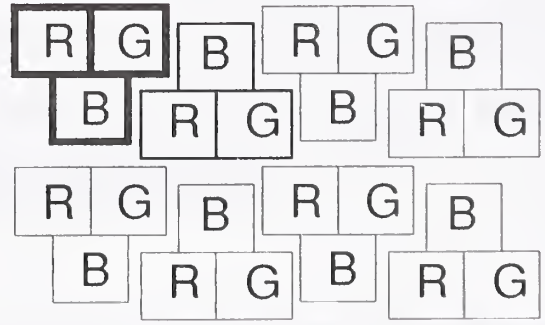
Diagonal Stripe



Quad Green



Delta Triad



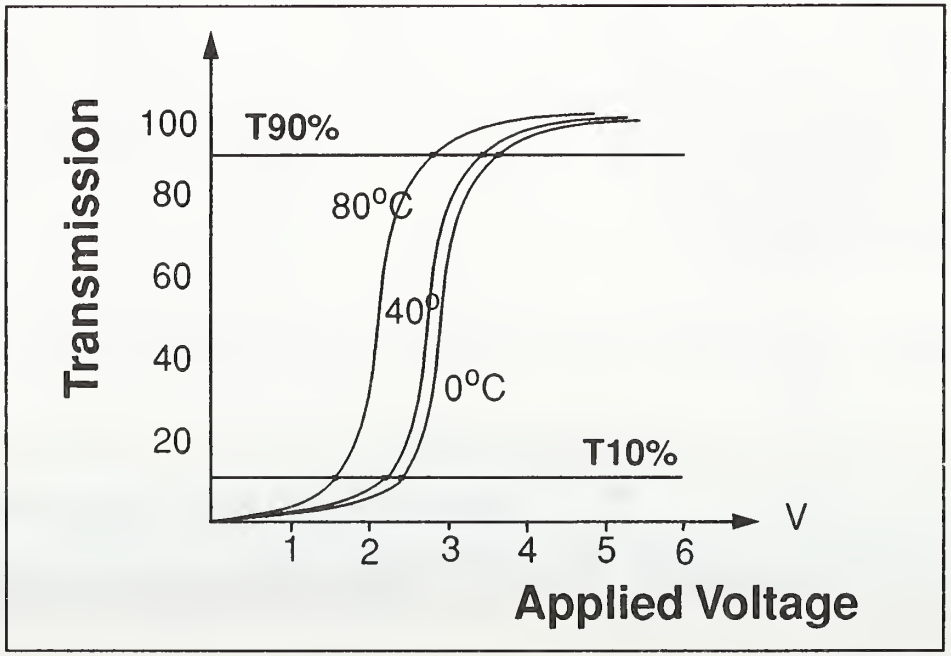
XEROX PARC

Problems and Issues

4. Color/grey level control / correction

- LC's materials transmission characteristic "gamma" determines the grey-level.
- Transmission characteristics vary with temperature and the LC material.
- Differing analog drive schemes correct for the display's "gamma" differently.

→ This requires specialization of the interface depending on the driver scheme used.



Where to implement or customize AMLCD-specific controls?

Display adapter / controller would need:

- higher integration, it must also include FPD specific functions.
- new VRAM architecture to provide parallel data streams.
- multiple line buffers in addition to frame buffer.

Panel Driver IC's would need:

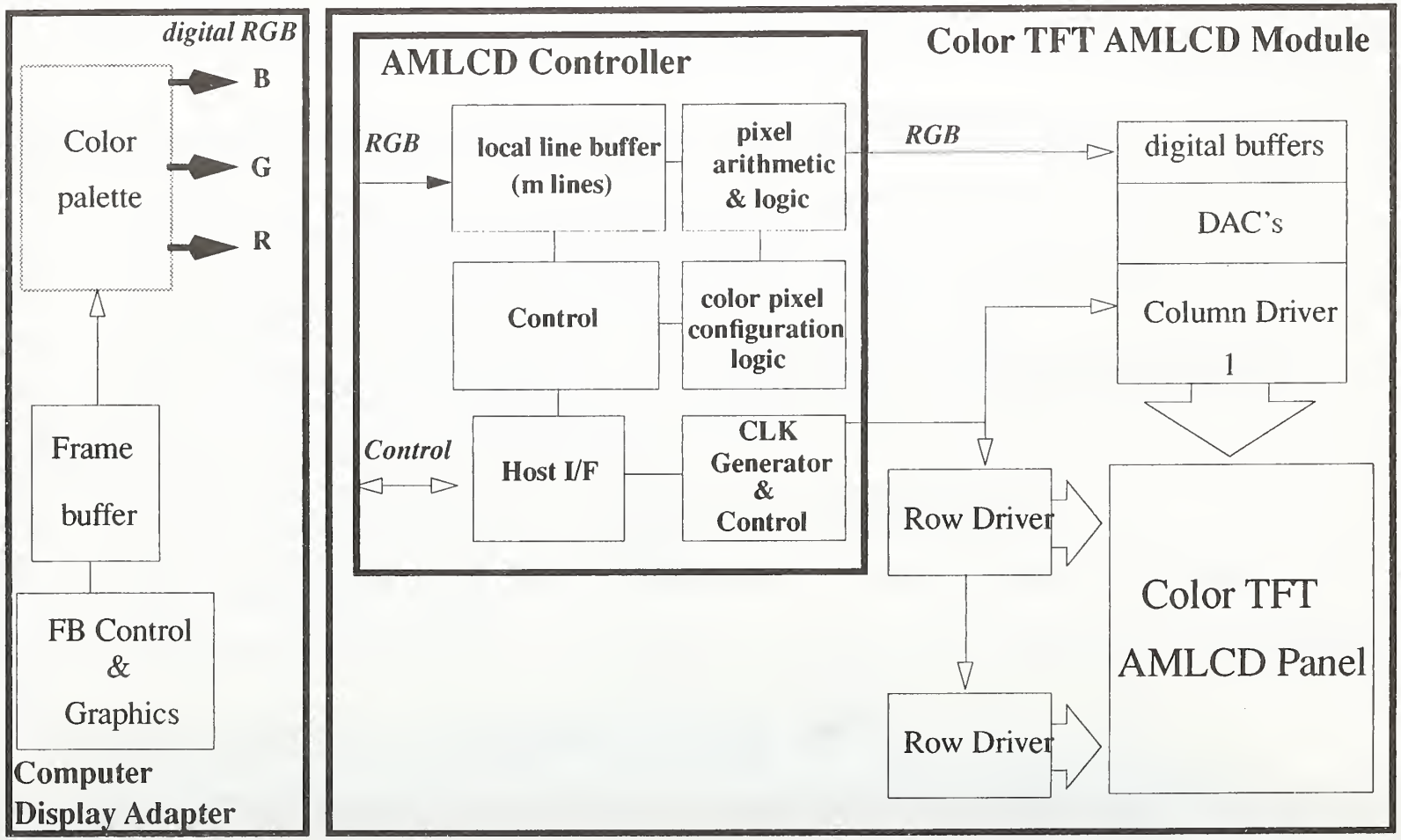
- much higher integration to handle panel specific functions, in addition to their output drive requirements.
  This would also lead to replication since multiple driver chips are needed for a single display.

→ **A Universal AMLCD Controller IC built into the FPD**

It enables a consistent display interface among different AMLCD's, like CRT's.

It simplifies both the host graphics adapter and the panel driver ICs.

AMLCD Controller



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Summary and Conclusions

Interfacing matrix based displays

- problems and issues in interfacing AMLCDs.

Display dependent control requires customization

- to standardize, display specific controls must be handled within the display module.

We need a consistent, universal interface to different types of FPDs

- this can be accomplished with a universal controller chip integrated into the display package.
- enables FPD interchangeability and allows for independent development of graphics adapters and display panels.

6

High Performance, Cost-Effective Computer and Video Interfacing to Megapixel AC-PDPs

Ms. Carol A. Wedding, Photonics Systems

High Performance, Cost-Effective Computer and Video Interfacing to Megapixel AC-PDPS

High Performance Displays

-The world is becoming more complicated

- Computers, local area networks, multi-media, and advanced applications software have given us the ability to manipulate large amounts of data and make decisions based on many complex variables

- A new world of possibilities awaits us due to these technological advances.

- Interactive TV, video conferencing, HDTV, Information highways, Federal and civil C4 I are just a few of the possibilities.

- Just as the eye is the key to the mind the display is the key to this new world

To meet the technological challanges
a high performance display must...

Meet the demands of the application!

This means

If the application is full motion video
it must be displayed without ghosting or
smearing. This requires a high update rate.

If the application is topological in nature
a high number of gray levels and colors may
be necessary to display all the details.

If the application is word processing or
desktop publishing the image must be stable
and flicker-free to prevent eye strain.

If the application is multimedia it may
require all the above plus high resolution.

Photonic's Megapixel Displays AC-PDP

- Photonics AC Plasma displays already meet the previously mentioned criteria.

- Photonics has recently developed a full color, 1024-768, with 256 gray levels per color.

- This display may be updated at a rate of over 60Hz.

- It has a 30 inch diagonal and a depth of 4 inches.

- A full color 1280-1024 with 256 gray levels per color is now under developement.

A cost effective challenge
for interfacing to video and computer sources

- Its a CRT world

- All flat panel displays are faced with the same challange of interfacing a digital source to an analog signal or developing a special card to interface between the host and the flat panel display.

- Photonics has presued both paths

- Our analog receivers accept standard VGA input analog red, green, blue, horizontal and vertical sync

- Our digital receivers accept
  vertical sync
  horizontal sync
  dot clock
  red data bus
  green data bus
  blue data bus

Advantages of an analog interface

- Relatively universal

-Can have the display remote from the source

- Noise resistant

Disadvantages of an analog interface

- Added system cost to go from digital to analog to digital

- Expensive to phase lock to all the different clock frequencies on all the different video cards

- Band width degradation

Possible solutions

- Including a dot clock on the data connector along with the RGB and sync.

Advantages of digital interface

-Eliminate a costly reciever circuit

-Eliminate uncertainty due to clock jitter

-May eliminate an entire frame buffer

Disadvantages

- Not universal

- Not noise resistant (requires a large data bus)

- Difficult to transmit data at a rate to maintain 60Hz frame rate (with present FPD controllers and memory)

Possible solutions

- Sending signals from the host to the source ECL twisted pair

- By embedding the computer on the back of the AC plasma display noise and frame rate problems can be eliminated with out the use of ECL

Two things all flat panel displays have in common

- all use row drivers and column drivers, data is loaded in a column form

- all use gray levels one at a time

Dream Interface

- Data loaded in a more column like fashion

- Data bus sent in separate subframes of gray levels

- Data sent in ECL twisted pair for noise immunity

7

Sun's Proposal for a Unified Display Interface

Mr. Marc Klingelhofer, Sun Microsystems

sun microsystems

Unified Display Interface

Marc Klingelhofer
Sun Microsystems, Inc.

sun microsystems

CRT Interfaces

- Predominantly analog RGB over coax with BNCs:
  - 0.7V p-p, 1.0V p-p, 4.0V p-p, above or below ground
- Various synchronization styles:
  - H/V-Drive
  - Composite sync—embedded ('sync on green') or separate
- Plethora of H/V resolutions and blanking characteristics
- Rasterized pixel-by-pixel horizontally, then line-by-line vertically

sun microsystems

Shortcomings of CRT Interfaces

- Analog RGB signals using coaxial cables and BNCs:
  - Voltage swings and offsets are not standardized
  - Analog signals on coax are susceptible to noise and generate EMI
  - Equalization is necessary for high-frequency response and/or long cables
  - Transmission-line characteristics are critical but sensitive to cable abuse
  - Multi-drop feeds are possible using taps (tees) but performance deteriorates
  - Cable mismatch between primary colors causes pixel blur
  - Bulky—3 coax cables are necessary (4 or 5 if separate sync is used)

- Synchronization:
  - Formats (amplitude, polarity, and timing) are not standardized
  - Analog timing references reduce regenerated clock stability

sun microsystems

Flat Panel Display Interfaces

- **LCDs:**
  - Bit-parallel RGB plus clock and control over flat cables:
    - Pixel depths of 6 to 8 bits per primary color are common
    - Pixel interleaving reduces clock rates, supports increased resolution
  - Various synchronization and control methods
  - Numerous resolutions
  - Rasterized vertically, then horizontally
- **Other Flat Panel Displays:**
  - Even *less* standardization that LCDs!

sun microsystems

Shortcomings of Flat Panel Display Interfaces

- Bit-parallel RGB plus clock and control over flat cables:
  - Pixel depth is not standardized—*typically* 6-8 bits per primary color
  - Pixel interleaving, if present, is display dependent
  - Cables must be very short (certainly < 10m)
  - Bulky—40-, 50-, and 80-pin cables are the norm
- Synchronization and control:
  - Clock and control functionality and pin-outs are not standardized
- Vertical-then-horizontal rasterization:
  - Incompatible with CRTs and most display drivers

sun microsystems

Similarities Between CRTs and Flat Panel Displays

- RGB pixels:
  - 6-8 bits per primary, typically 8 bits
- 2-dimensional:
  - Row/column matrix:
    - Each pixel has an 'address'
  - Sequences of pixels constitute lines:
    - Start-of-line and line number must be identified
      - ⇒ CRTs have horizontal rows and LCDs have vertical columns
  - Sequences of lines constitute frames:
    - Start-of-frame must be identified
      - ⇒ Frame numbering can be useful, also

sun microsystems

The Case for a Unified Display Interface

- Lack of standardization leads to:
  - Extra design effort for display manufacturers to design new interfaces
  - Extra design effort for display integrators to utilize new interfaces
  - Increased system costs due to low volume
  - Inflexibility due to incompatibility

- Current interfaces suffer from:
  - Non-standard signal definitions
  - Unreliable, poorly performing physical connections
  - Complicated and proprietary synchronization and control

- The Unified Display Interface offers:
  - Common design basis for display manufacturers and integrators
  - Reduced costs
    - ⇒ Greatly reduced costs if this is adopted by the consumer world
  - Reliability and high performance over great distances
  - Scalability and flexibility

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Industry Trends

- Digital serial networks:
  - High bandwidth
  - Low cost
  - Standardized physical interface
  - Reliable
- Smart displays:
  - Remotely configurable and serviceable
  - Self-identifying:
    - Control format
    - Resolution
- Self-identifying data streams:
  - Video vs. audio vs. network...
- Scalability:
  - Feature and performance enhancement is possible and 'easy'

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Unified Display Interface

- Suited to various display devices, including CRTs and LCDs
- Compatible with available display drivers
- Low cost and high reliability:
  - Serial bit streams over copper or fiber
    - ⇒ No ribbon cables or analog video over coax and BNCs
- Scalable:
  - Supports various display resolutions
  - Handles complex display types, such as arrays
- Configurable:
  - Automatic device sensing (self-identifying display devices)
  - Complexity can be skewed towards driver or display
  - Programmable resolution

Physical Interface

- Standardized media:
  - Twisted-pair copper or coax for short distances at low bit-rates
    - ⇒ Suitable for VGA/SVGA resolutions
  - Fiber-optic for standard- and high-resolution displays
- Fixed low-level protocol:
  - Clock conveyance
  - Bit serialization
- Benefits:
  - Common interface circuits —> leveraged designs
    - ⇒ Standard clock mechanism simplifies clock recovery and synchronization
  - Standard connectors/cables —> high volume —> low cost
  - Sophisticated display drivers *could* support various display types and resolutions without cabling or synchronization concerns

Protocols

- Standardized sequencing:
  - Color information ordering
  - Pixels sent row-by-row versus column-by-column
  - Fixed headers identify resolutions and pixel positions
- Low end protocol:
  - Comparable to analog RGB:
    - Pixels sent line-by-line
    - Display must lock to and accept incoming data
      - ⇒ Handshaking and feedback are unnecessary
  - Simple implementations for driver and display
- Standard protocol:
  - Driver senses display characteristics (ala 'Smart Monitor')
  - Display receives pixels or lines from driver
  - Driver sets resolution according to application
  - Driver alters display characteristics (brightness, contrast, etc.)

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Issues

- 3-D support: do we need it?
- Are 8 bits per primary color enough pixel depth?

8

I/O Connectors for Video Applications, History, Requirements, and Technology to Meet those Needs

Mr. Gary Manchester, MOLEX, Inc.

FUTURE REQUIREMENTS

FOR

I/O CONNECTORS IN VIDEO APPLICATIONS

PRESENTED BY MOLEX INCORPORATED

JANUARY, 1993

NIST WORKSHOP

SAN JOSE, CALIFORNIA

GARY MANCHESTER
PRODUCT MANAGER

VIDEO I/O CONNECTORS
HISTORICAL OVERVIEW

INTERCONNECTS USUALLY ARE THE LAST CONSIDERATION IN A NEW SYSTEM DESIGN

HISTORICALLY IT WAS MECHANICAL QUESTIONS
- SIZE
- NUMBER OF CONTACTS
- NORMAL FORCES
- INSERTION FORCES
- CRUDE SHIELDING

THE D-SUB CONNECTOR HAS PROVIDED THE INDUSTRY A SOLUTION THAT MET THE SIZE AND MECHANICAL REQUIREMENTS

VGA AND XGA CONNECTORS

FILTER CONNECTORS WERE CONSIDERED USUALLY AS AN AFTERTHOUGHT

IN LIMITED MARKETS WHERE ELECTRICAL PERFORMANCE WAS AN ISSUE DESIGNERS WENT TO STANDARD COAX SYSTEMS

TYPICAL IN WORKSTATION MARKETS

VIDEO I/O CONNECTORS
DEVELOPING TRENDS

INCREASED MECHANICAL PERFORMANCE FROM STANDARD I/O CONNECTORS IS BEING DEMANDED - HIGHER PIN COUNTS, LOW INSERTION FORCES AND INCREASED CYCLE LIFE

SIZES ARE SMALLER - .050"- .025" AND 1mm CENTERLINE CONTACTS

ELECTRICAL PERFORMANCE IS BECOMING A FACTOR AND CONNECTORS ARE LIMITING SYSTEM PERFORMANCE

INCREASED FUNCTION WITHIN THE CONNECTOR IS DEMANDED - SMART CONNECTORS

HIGH VOLUME CONSUMER MARKETS ARE DEVELOPING FOR THE HIGH PERFORMANCE SYSTEMS - COST BECOMES A BIGGER FACTOR

CRT AND FLAT PANEL ARE SHARING THE SAME SUBSYSTEMS CREATING THE NEED TO INTERFACE TO EITHER

VIDEO I/O CONNECTORS
DEVELOPING REQUIREMENTS

MIXED LAYOUT DESIGNS - COAX AND UNSHIELDED LINES WITHIN ONE CONNECTOR

- VIDEO COAX LINES - 3 OR 4
- HIGH SPEED DIGITAL LINES
- STAND SIGNAL LINES

POWER LINES MAY BE NEEDED - 3V, 5V, 12V

MINIATURE DESIGNS FOR FIT IN THE "PORTABLE" WORLD

LOW COST MANUFACTURING TECHNIQUES

- STAMP AND FORMED CONTACTS
- AUTOMATED ASSEMBLY
- MASS PRODUCTION/MASS MARKET - STANDARDIZATION

HIGH MATING CYCLE LIFE - 1,000 TO 10,000 MATES

BLIND MATE OPTIONS FOR USE BOX TO BOX WITHOUT CABLE - DOCKING CONNECTORS

FIRST MAKE LAST BREAK CAPABILITY

ESD PROTECTION

ADAPTERS FOR BACKWARD COMPATIBILITY

VIDEO I/O CONNECTOR
CONNECTOR TECHNOLOGY CAPABILITY

ABLE TO PROVIDE 3 TO 4 75 COAX LINES AND 50 ADDITIONAL SIGNAL LINES IN THE SPACE OF A 15 PIN VGA CONNECTOR

SUCH CONNECTORS ARE CAPABLE OF OPERATING AT UP TO 1.5 GHz BANDWIDTH

CROSS TALK WILL BE LESS THAN ONE PERCENT @ 1V/1ns RISETIMES

IMPEDANCE CONTROL OF $\pm$ 1 OHM @ 500 ps RISETIMES ON VIDEO LINES, $\pm$ 5 OHMS ON HIGH SPEED DIGITAL LINES

A CYCLE LIFE OF 5,000 MATINGS WILL BE AND IS TYPICAL WITH THE USE OF STANDARD PLATING AND MATERIALS USED IN CONNECTORS TODAY

WITH THE MIXED LAYOUT AND SIGNAL DENSITIES WE SEE IT POSSIBLE TO PACKAGE:

RGB VIDEO COAX
FORTH COAX FOR HIGH SPEED SYNC LINE OR REFERENCE LINES
MOUSE I/O
BATTERY CHARGER
SERIAL PORT LINES
KEYBOARD
PHONE LINES
PARALLEL PORT
PEN I/O
AUDIO I/O
NETWORK INTERFACE

ALL IN ONE CONNECTOR

COSTS PER MATED LINE WILL BE CONSISTENT WITH STANDARD I/O CONNECTORS ON MARKET TODAY

VIDEO I/O CONNECTORS
SUMMARY

SERIES OF MIXED LAYOUT FORMATS ARE DEVELOPING TODAY

DEVELOPMENT OF ELECTRICAL PERFORMANCE BENCHMARKS AND PROTOTYPE UNITS FOR INDUSTRY EVALUATION ARE BECOMING AVAILABLE NOW

LEADING CONNECTOR COMPANIES ARE SUPPORTING EFFORTS TO DESIGN THE INTERCONNECT EARLY TO PROVIDE:

- THE BEST SOLUTION ELECTRICAL AND MECHANICAL
- LESS CHANCE OF TECHNICAL COMPROMISES
- LOW COST SOLUTIONS
- INCREASED CHANCES OF STANDARDIZATION
- DEVELOPMENT OF MULTIPLE SOURCES TO ASSURE PRICE AND SUPPLY OF THE DEVELOPING TECHNOLOGIES

TODAY WE HAVE THE CHANCE TO OPTIMIZE DESIGN FOR LONGEVITY

STANDARDIZATION OF DESIGNS SHOULD OCCUR TO CREATE:

- ECONOMIES OF SCALE
- ATMOSPHERE TO QUICKLY ADDRESS DEVELOPMENT OF TECHNOLOGIES
- A FORUM FOR PRODUCT DEVELOPMENT FEEDBACK FROM AND TO USER GROUPS

CONNECTORS CAN BE LOOKED AT AS A WAY TO ENHANCE SYSTEM PERFORMANCE AND FUNCTION. THEY CAN DO THIS IF WE DEFINE UP FRONT THE TOTAL REQUIREMENTS AND NOT LIMIT OURSELVES TO YESTERDAY'S SOLUTIONS

9

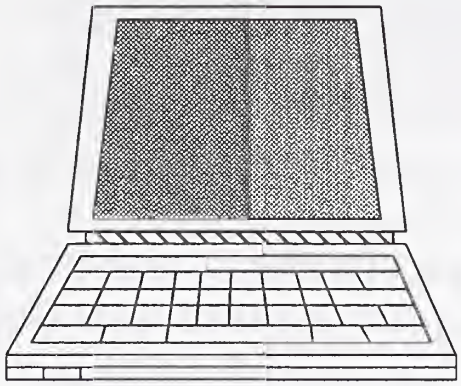
Issues in FPD Interfaces for PC and Workstation Use

Mr. Bob Myers, Hewlett-Packard Co.

Issues in FPD Interfaces for Personal Computers and Workstations

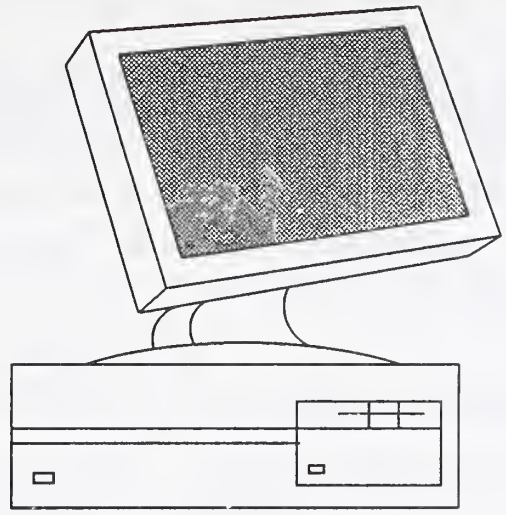
Bob Myers
User–Interface HW Lab
Advanced Systems Div.
Hewlett–Packard Co.

Two Classes of FPD Applications



Portable

* – FPD in same package as controller
* – Very short, direct connection
* – Less of a concern with EMI, etc. in terms of the interface itself.



Desktop/Standalone

* – FPD separate (the "monitor model")
* – Display at least 1m from controller (and preferably has the ability to be further removed).
* – Interconnect EMI performance, signal integrity a greater concern.

The Need for a Common Interface

- The CRT is, and will be for the foreseeable future, the primary desktop/standalone computer display.
- However, there will be a growing number of standalone FPD monitors using various technologies (AMLCD, plasma, EL, etc.).
- Computer manufacturers cannot afford to provide separate versions of computers, video outputs connectors, or video output ICs (e.g., "RAMDACs") to handle CRTs and FPDs.
- Staying with current analog video signal/connector standards is a poor solution – for BOTH types of displays!
- NOW is a very good time to be working on this problem:
  - Standards organizations such as VESA are already working on proposals for next–generation connectors & display ID.
  - HDTV is about to make the standalone FPD a BIG concern!

The Question of Bandwidth

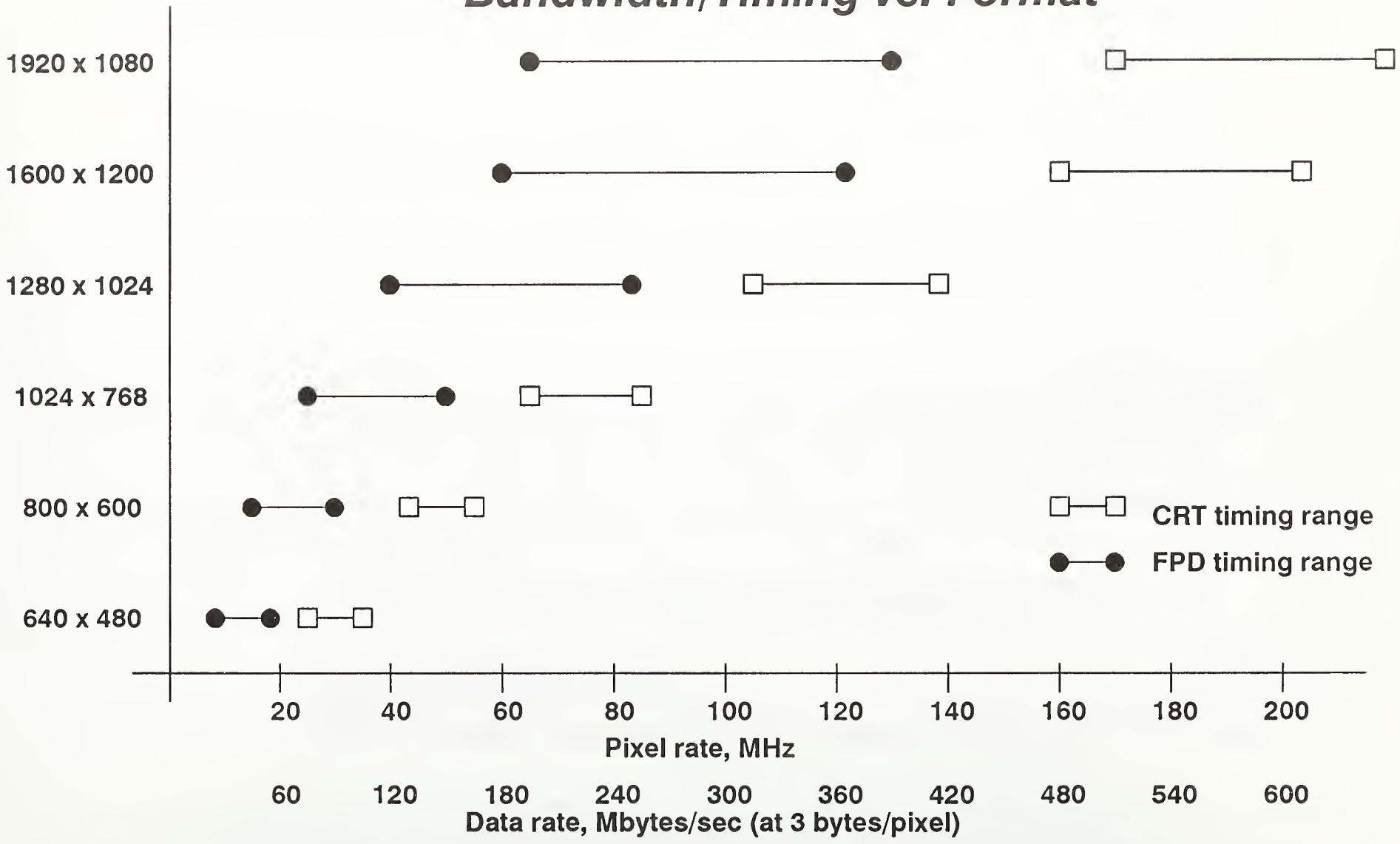
Assume: Require min. 30 frames/sec. (for motion reasons)
Zero "blanking" time

- what is the min. BW/clock required for common formats?

Repeat at 60 fps, 5% "blanking" (dead time) to get maximum (or at least more realistic) clocks for these formats.

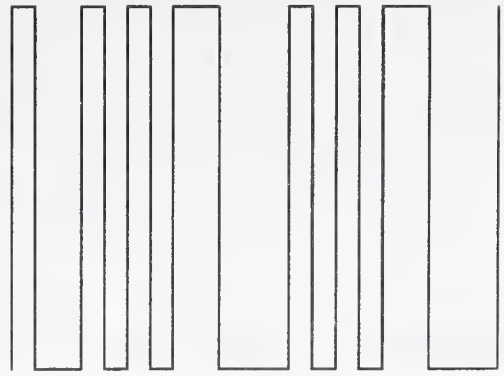
Compare to typical CRT timings for these formats (60–75 Hz refresh, ~25% blanking time)

Bandwidth/Timing vs. Format

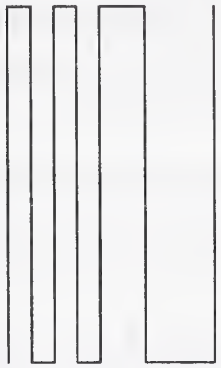


"Digital" vs. "Analog" Interfaces

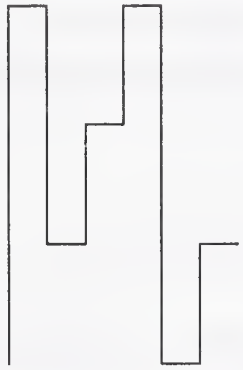
"Analog video"



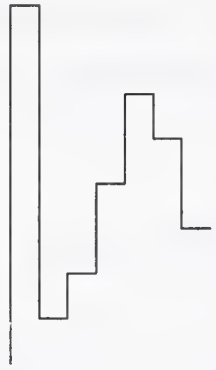
"Digital video"



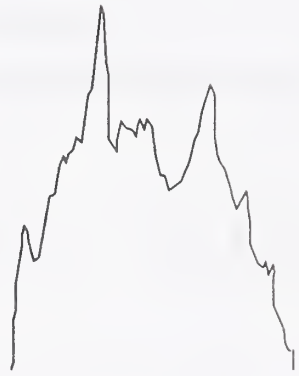
One bit/line
(2 levels)



Two bits/line
(4 levels)



Three bits/line
(8 levels)



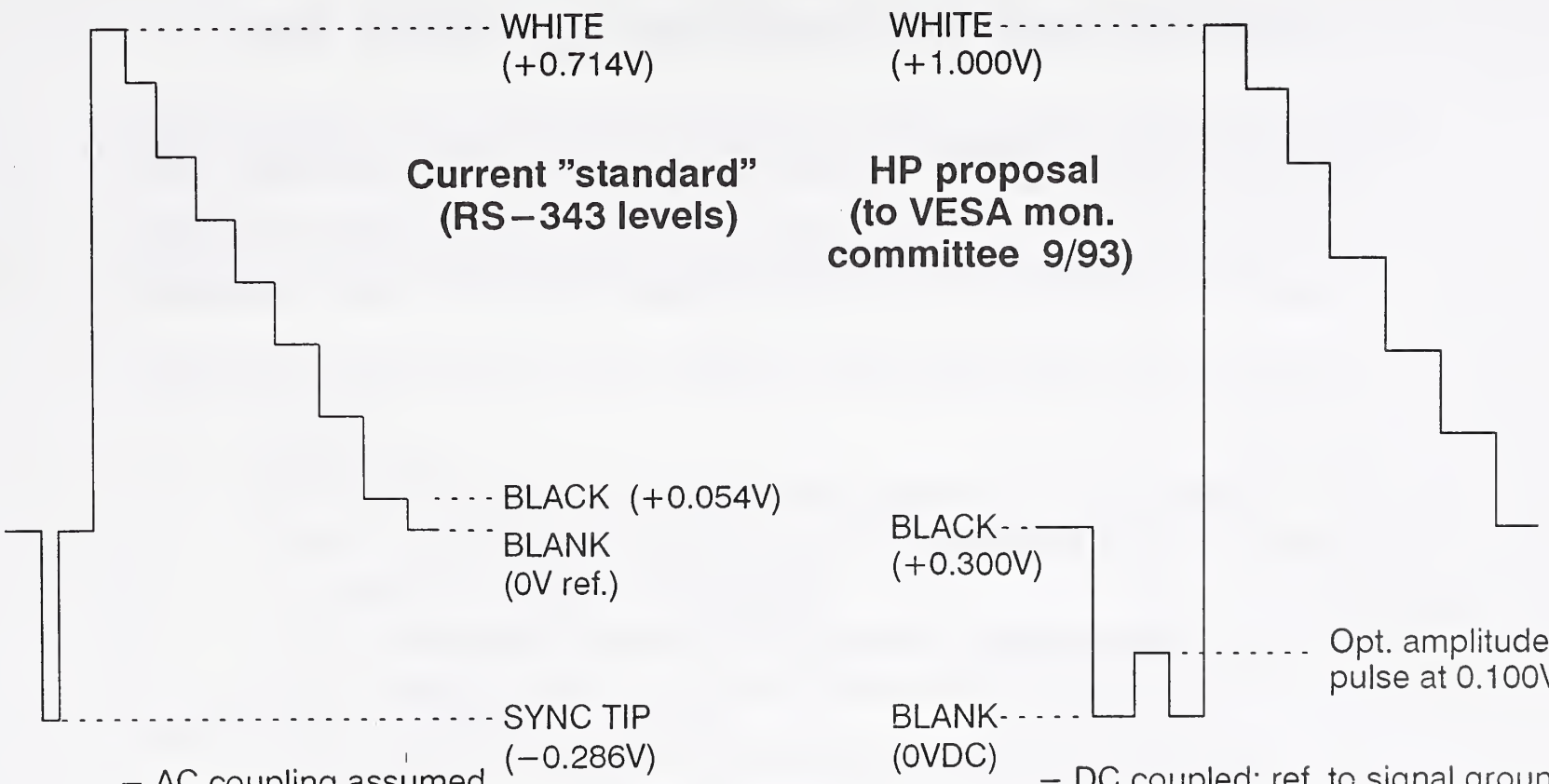
Many bits/line
("Analog")

Other Issues

To be successful, any interface standard must –

- offer a cost–competitive solution
- permit compliance with EMI and other regulatory requirements
- provide for additional features as needed (for displays, this could be expected to include display ID and control, human I/O device connectivity, etc.
- be realizable within the drive, timing, and other constraints of available technologies, and
- be flexible enough for adaptation to different display technologies and formats (preferably including CRTs as well as all FPD technologies).

Video Signal Standards



– Both use 75 ohm line/termination impedance
– Both 1.0V p–p (w/sync in case of RS–343 levels)

A possible common interface

- 4 signal lines per color, max 1.0 V p–p into 75 ohms
  - 1 capable of full "analog video"
  - 3 additional, capable of up to four levels (2–bit DACs)

  12 total lines could then provide
  - Full–range analog video for CRTs or compatible FPDs
  - Up to four bits/color of simple "digital" connection (1 bit/line) for low–end FPDs.
  - Digital information encoded in combinations of two–level and four–level (two bits/line) outputs, up to a full eight bits/color.

- Horizontal and vertical sync signals, plus pixel clock (or clock/4?)

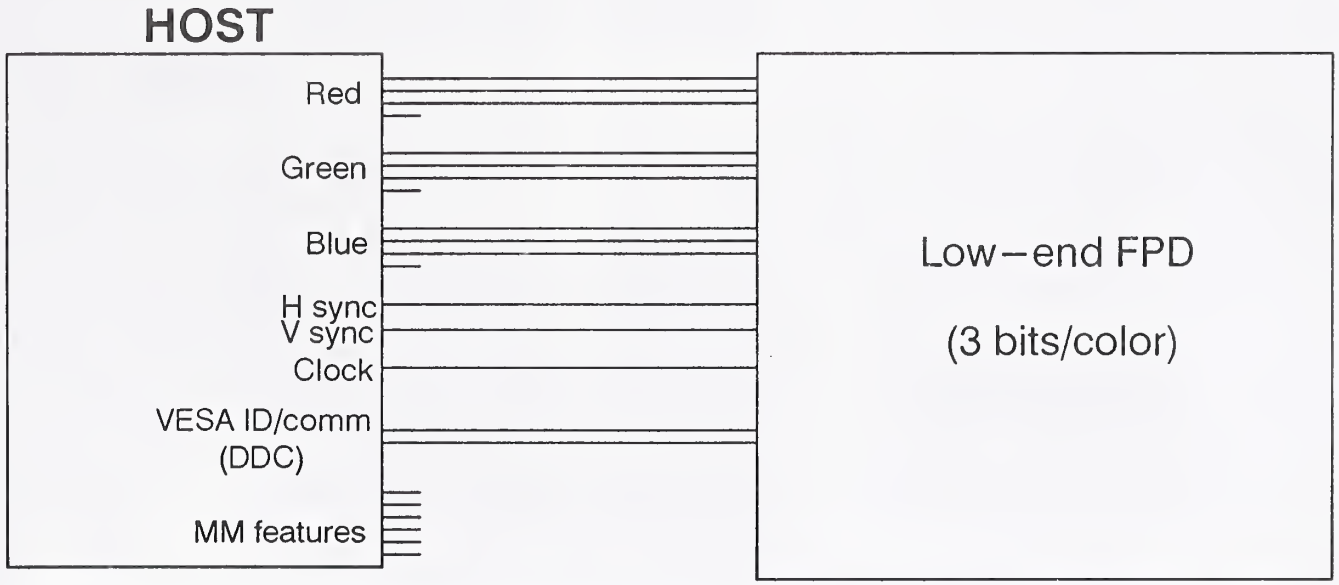
- Additional lines to support VESA display communications and ID standard (and probably human I/O as well).

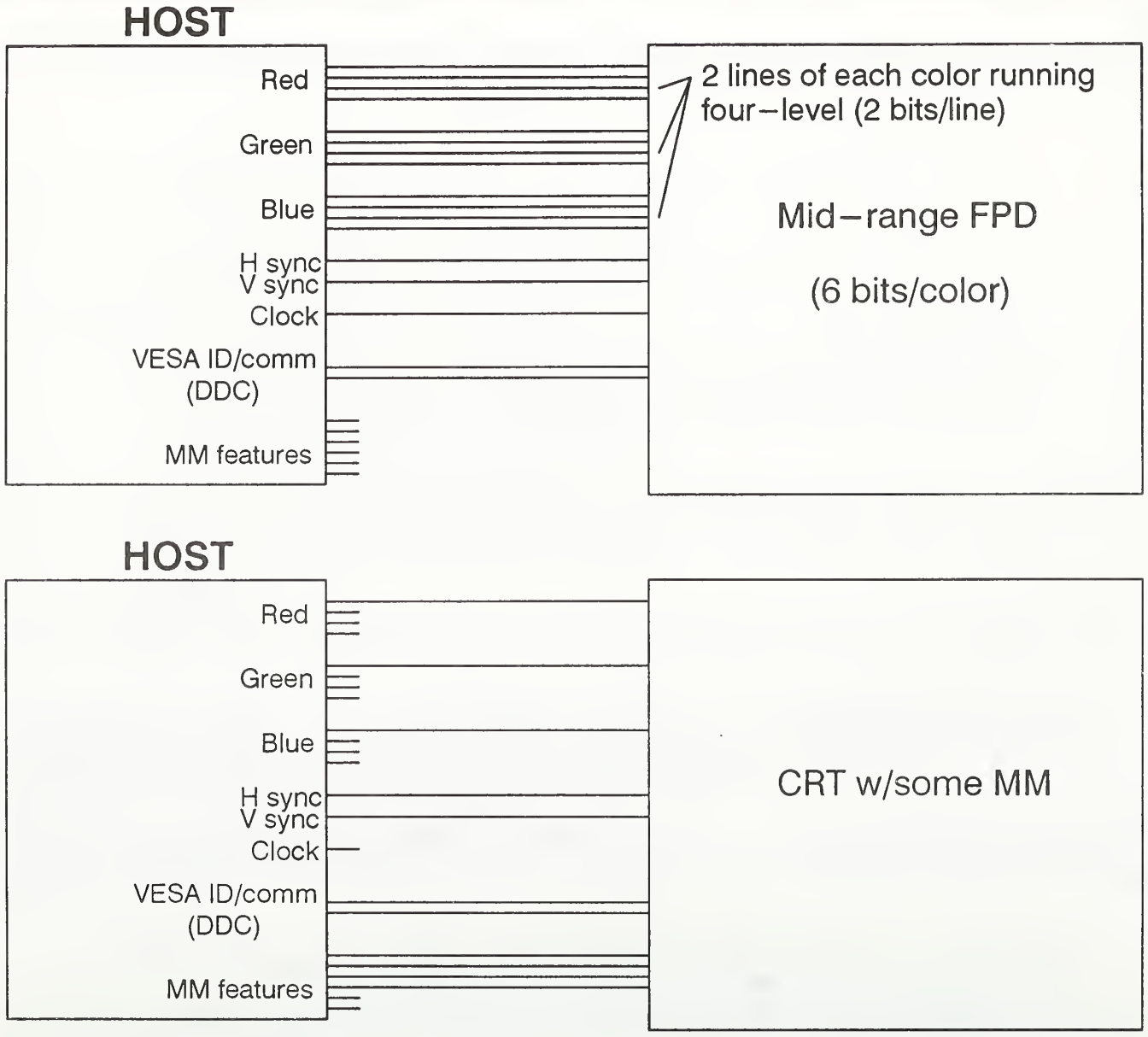
- Other lines to support MM features (such as analog audio lines).

  – Total approx. 20–24 signal lines, plus grounds.

The Common Interface in practice

- **Each display type would connect to only those outputs needed (i.e., very few would use all the lines) – all would provide the basic ID capability, so the host system would automatically configure the video outputs to match the display's needs.**




HOST
Red
Green
Blue
H sync
V sync
Clock
VESA ID/comm
(DDC)
MM features
2 lines of each color running
four–level (2 bits/line)
Mid–range FPD
(6 bits/color)
HOST
Red
Green
Blue
H sync
V sync
Clock
VESA ID/comm
(DDC)
MM features
CRT w/some MM

Issues in FPD Interfaces for Personal Computers & Workstations

Bob Myers
Senior Engineer
Advanced Systems Division
Hewlett–Packard Co.

Introduction

The development of interface standards for connecting flat–panel displays to computers is, by necessity, following a considerably different path than that taken in the course of CRT display standards for computers. CRT display standards were strongly influenced by the existing practices in television equipment, and even today the impact of what are (on the scale of our industry) some very old television standards is very apparent. For example, the most popular computer display standard ever – VGA – is essentially a non–interlaced version of the U.S. television format, and most computer displays still follow the EIA's RS–170 or RS–343 standards in terms of their signal specifications.

Flat–panel displays, of which the matrix–addressed LCD is probably the most important example today, present a different problem, and there is no similar past practice to draw from. These are essentially "digital" devices in terms of their basic operation and interfacing. And yet, many of the same issues which had to be addressed by CRT monitor standards face us when attempt to come up with corresponding standards for FPDs.

There are two major classes of FPD applications to consider, each of which presents unique challenges. The first, in terms of the extent of current usage, is the inclusion of flat–panel displays in portable or transportable products. This category should be taken as including any application in which the display is contained within the same physical package as its host computer or other provider of displayed imagery. In short, there is no requirement for a connection, external to the common packaging, which carries image information to the display proper. A good example of this is the laptop computer, where the FPD typically has a direct connection to a graphics controller located on the main PC assembly.

The second class of FPD application has not yet been very large from the standpoint of current market volume, but will very likely at least equal and possibly exceed the volume of the "all–in–one–box" category in the near future. This is the use of the FPD as a "standalone" display, more like the present model of separate computer and monitor common in CRT display use. Standalone monitors based on FPDs are already finding a place in certain space–critical applications or in environments where the CRT cannot be used, and will find broader use as the cost of such displays continues to drop. Such applications present a unique set of

challenges, not the least of which is the desire for simple interchangeability with CRT displays – which may reasonably be expected to remain in use for the foreseeable future. Requiring two completely separate interfaces to support these two types of displays is clearly not an acceptable solution.

The Issue of Bandwidth

One of the basic factors behind many FPD interface problems is the bandwidth needed in whatever channel delivers the image information to the display itself. As compared to CRT displays, the FPD technologies generally can make more efficient use of a given channel by virtue of not requiring a significant blanking period (which can consume more than 25% of the total time available); thus, for a given format and refresh rate, the overall data rate can be reduced. Still, the rates required for current and expected future display formats can present a formidable challenge.

We can get a better feel for this problem by calculating the minimum requirements for a number of these formats. Such minimums may be found by assuming that no blanking or other "dead" time is required, and that the display technology in question does not require a certain minimum refresh rate in order to avoid wide–area flicker (which means that the refresh rate may be chosen solely on the basis of the need for smooth displayed motion). To further provide a data rate in terms of bytes per second, we can also assume a need for not more than 8 bits/color in the displayed image. These assumptions give the following:

All at 30 frames per second; zero blanking time.

Format	Pixel rate	Date rate at 3 bytes/pixel
640 x 480	9.22 MHz	27.6 Mbytes/sec.
800 x 600	14.40 MHz	43.2 Mbytes/sec.
1024 x 768	23.59 MHz	70.8 Mbytes/sec.
1280 x 1024	39.32 MHz	118.0 Mbytes/sec.
1600 x 1200	57.60 MHz	172.8 Mbytes/sec.
1920 x 1080	62.21 MHz	186.6 Mbytes/sec.

We must keep in mind that the above are absolute minimums for the formats described; more realistically, we should recognize that many technologies will require a faster refresh or update rate due to at least a partial reliance on temporal modulation techniques to obtain gray–scale capability, and the assumption of zero "blanking" time is also unrealistic. More practical rate estimates might be obtained by doubling the update rate to 60 Hz, and allowing approximately 5% of the total as dead time. This would give the following, which might now be assumed to be closer to the upper limit of the expected range of timings for these formats:

All at 60 frames per second; 5% blanking time.

Format	Pixel rate	Date rate at 3 bytes/pixel
640 x 480	19.40 MHz	58.2 Mbytes/sec.
800 x 600	30.32 MHz	91.0 Mbytes/sec.
1024 x 768	49.67 MHz	149.0 Mbytes/sec.
1280 x 1024	82.78 MHz	248.3 Mbytes/sec.
1600 x 1200	121.26 MHz	363.8 Mbytes/sec.
1920 x 1080	130.96 MHz	392.9 Mbytes/sec.

Again, the data rates are based on a three–color system with eight bits per color; if these figures represent the highest rate needed for each format, the lowest rates for each would be either the pixel rate (for a one–bit–per– pixel monochrome system) or three times this rate, for a simple eight–color display. These rates are in all cases lower than those required for an equivalent CRT display – but we should recognize that the rates are not so different so as to make a common interface unreasonable.

"Digital" vs. "Analog" Interfaces

Delivering image data at these rates could be accomplished in any of several ways. The fundamental tradeoff in terms of a digital interface is one of channel width vs. clock rate. However, there are certainly limits to how far one can go in buying a rate reduction through use of a wider channel; it is unrealistic, for example, to assume that one could achieve an eightfold decrease through this means in a full–color (8 bits/color) display. Transmitting eight pixels at one time would require a 192–bit channel, not counting power, grounds, and clock and synchronization signals. Such a massively parallel channel might be conceivable over a very short path, as in a direct connection to the display in a laptop, but is most likely not practical in any case where the display is separated even slightly from the graphics controller. It is probably more realistic in this latter case to assume that the connection is via a purely analog channel, perhaps an adaptation of existing video signal standard. This would permit CRT and FPD displays to share the same hardware port in the host system (although the timings for each would likely be different). Even in the portable applications, an extremely wide parallel interface will cause problems. The economics and physical size constraints are driving very high levels of integration in such systems, and drivers, pads and pins are precious commodities in VLSI devices.

The obvious alternative to a purely "digital" channel (one in which the data is transmitted as one or more simple on/off or high/low signals) is an "analog" transmission scheme, such as what we usually think of as video for CRT displays. Extremely high bandwidths are possible in such a system, as a simple coaxial cable can carry signals at least to several hundred MHz. But the traditional video signal standards are definitely better suited to display devices such as the CRT, in which the video signal need not be accurately sampled and displayed with a

one–to–one correspondence between the pixels of the host frame buffer and those of the display. To do this in an "analog" system requires either the parallel transmission of a high–speed and accurately–aligned sampling clock, or the generation of such a clock by the display itself. (The latter is usually achieved by means of a phase–locked loop synthesizer using the synchronization signals – which also requires that the relationship between these signals and the video be accurately maintained by the host.) Either choice requires additional cost in the display as compared to the simpler digital interface, but can provide benefits beyond high bandwidth – such as making the FP display compatible with other options such as CRT monitors.

It should be noted that there are alternatives between these two. What we usually refer to as "analog" and "digital" interfaces are actually just the two extremes of transmission over a channel – a "continuous" signal and one comprising only two discrete levels. There are intermediate possibilities, which use some number of levels or similar encoding scheme of discrete states to convey more than a single bit of information per sample. Such an encoding system can also be extended over multiple physical channels; for example, two eight–level lines would be sufficient to carry the equivalent of a six–bits–per–pixel video signal. Multiple channels per color in such a system could permit a flexible interface which could be configured for a wide range of formats, without the need for a high density connector or large number of conductors in the interconnect cable.

3. Other Issues

While bandwidth is the basic concern as far as simply defining the interface problem, there are several other factors which need to be addressed in designing a practical solution. These are, in no particular order:

- The cost of implementing the solution,
- The ability of the interface to meet other constraints, such as limits on radiated emissions,
- Additional features, such as display control & ID or human I/O connections, which will use the same physical cabling,
- The limitations, in terms of things such as drive requirements, timing constraints, etc., of the technology used to implement the interface, and
- The flexibility of the interface (if needed) to adapt to different display formats and technologies.

These factors cannot be assigned a single prioritization which will be applicable across all possible FPD designs. Cost will be the highest priority in low–end systems; flexibility and the ability to include additional features may be more important in higher–end applications. The limitations of the interface technology and the need to meet various regulatory requirements will constrain interface design in all applications, but these requirements may differ among specific applications or systems. Standardized interfaces are very important to the

continued success of flat–panel displays, but it may be a mistake to assume that a single interface standard can meet the needs of all possible FPD uses unless careful consideration is given to each of these areas.

4. A Single Standard?

Despite the wide range of possible interfaces and corresponding needs, there are undeniable advantages to a single physical interface standard. An excellent example of this is again found in current PC–CRT practice – while there are as yet no true standards, such de facto standards as the 15–pin D–subminiature connector used for the "VGA" video output connector have proven usable for low–end 640x480–only systems up through high–resolution workstation–class displays. Organizations such as the Video Electronics Standards Association (VESA) are working now on developing the next generation standard for such connectors, and such wide applicability is a basic assumption of these efforts. Is something like this possible for FPD applications? Could a single standard be developed which could be used for all display connections, including both CRT and flat–panel displays?

Current CRT video signals for computer displays are almost entirely based on the RS–343A levels of approx. 0.7 V peak–to–peak, not including sync pulses. This standard amplitude represents the biggest difference between these signals and typical FPD interfaces, which are usually based on standard digital logic families with a peak–to–peak swing of one to five volts. However, the trend in portable systems – those which can be expected to make up the bulk of low–end FPD applications – is to lower–voltage logic with correspondingly lower signal levels. It may be possible to define a single standard for signals and connectors which would meet both the future needs of FPD displays and still provide backwards compatibility with existing CRT displays.

Earlier in this paper, the range of data rates which can be expected to be required for FPDs was presented. This range is slightly below the corresponding figures for CRT displays, owing to the larger percentage of time consumed in the blanking periods used with CRTs (20–30% of the total). Still, the frequencies involved are not so different that we should expect this to be an issue in developing a common interface for both. And a common interface standard is definitely desirable – manufacturers do not wish to produce different versions of their equipment depending on the intended display, nor is requiring separate outputs for CRT and FPD use an optimum solution.

This is a particularly opportune time to consider a common CRT/FPD interface standard; the computer industry, through groups such as VESA, now recognizes the need for new standards in both signals and connectors for CRT displays, including the establishment of standards for the identification and control of the display by the host. Designing these standards right from the start to be usable with flat–panel displays as well should be viewed as a very high priority by all concerned.

Reviewing the issues presented here, we can now define the requirements for such a common standard:

1. The standard should define a connector or connector family and cabling which is inexpensive enough for use by all systems, but which is capable of handling signals in the range of 10 to 250–300 MHz, while permitting the system to comply with all relevant EMI and safety standards. The connector and cabling should provide sufficient conductors for carrying a minimum of eight bits per color at the full rate, possibly through using a multilevel encoding system. The connector standard should also meet the needs of display communications & ID and multimedia features, as are currently being considered by VESA's monitor committee and other groups.

2. There is in addition a need for sets of related format and timing standards, such that a single graphics controller or video output system could easily be programmed to drive both CRT and FPD displays which conform to these standards, using a single standard reference clock. One possible solution would be to base all timings on pixel clocks in the N x 2.25 MHz family, as this is the established base rate used in video timing (as in the SMPTE–240M and CCIR–601 standards). This would provide simple compatibility between the two types of displays as well as with video sources using any of the existing television standards, and hopefully future HDTV standards as well. Some example timings in several standard formats are given in the accompanying figures. This approach was also used in VESA's latest set of timing standards.

3. Finally, a new signal standard will need to be established which will permit a single set of outputs to provide video signals for both CRT and FPD monitors. CRTs can reasonably be expected to continue to use signals which are at least similar to the current standard of approx. 0.7–1.0V p–p at 75 ohms. Some FPD monitors may also use this standard with a single signal each for red, green, and blue, digitized by the display. However, it should also be possible to provide a more economical interface by using the same output design in parallel for a multilevel interface. The "normal" video output could easily be configured to operate in this mode, with simpler outputs operating in parallel to provide additional bits.

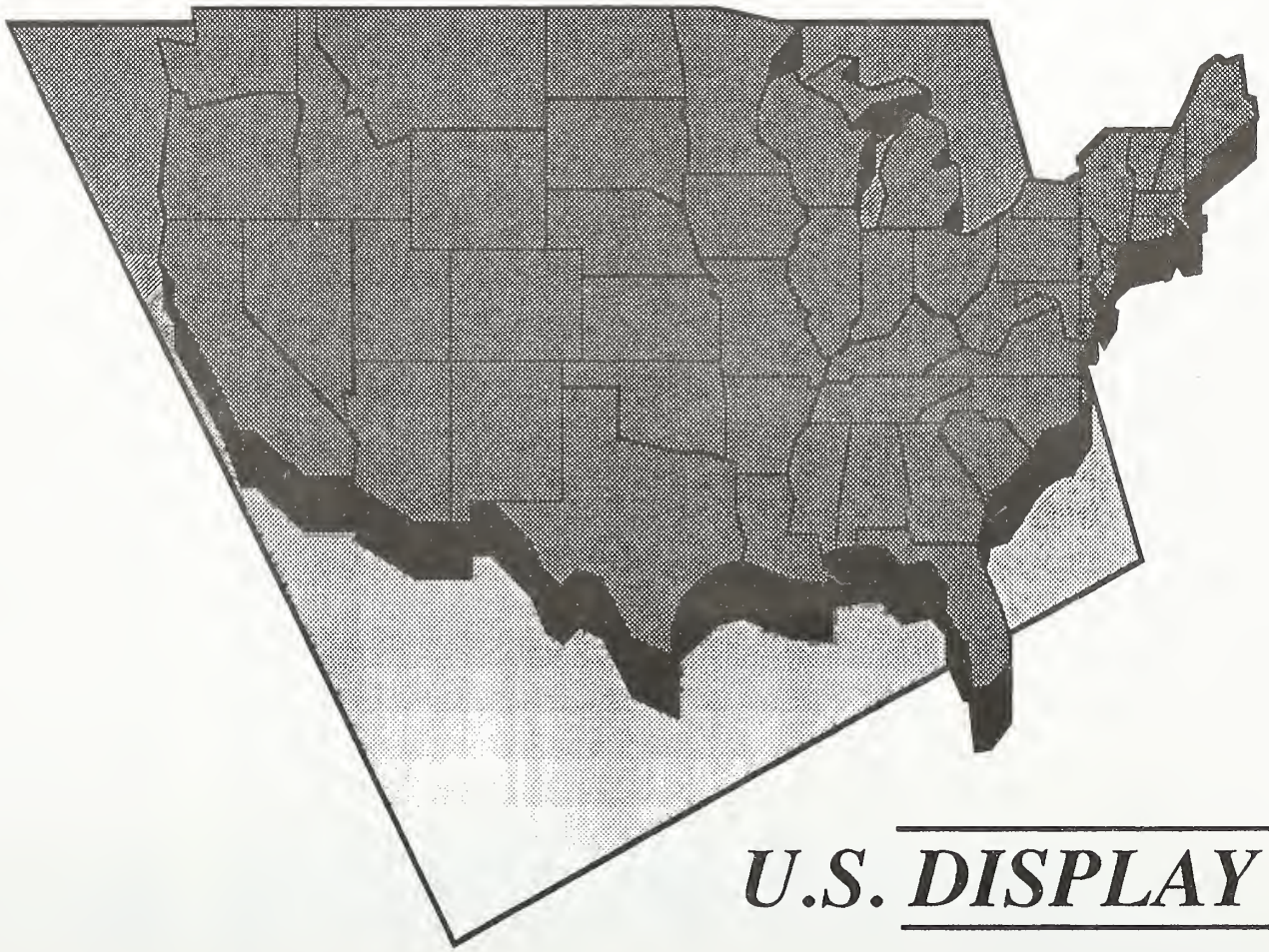
As an example, four outputs per color could be treated as four bits per color, eight bits per color with four levels per line, or as a single eight–bit output as in normal CRT practice. Adding additional lines for the pixel clock (or at least a reference signal which is an integer fraction of that clock), plus the synchronization and communication signals, should still permit a connector and cable of less than two dozen lines which would be usable with all compliant displays. Given the display ID functionality provided by this connector, a single video output design could be automatically configured (in both the outputs used and the timing) for any display selected by the user.

10

United States Display Consortium

Dr. Bob Pinnel, USDC

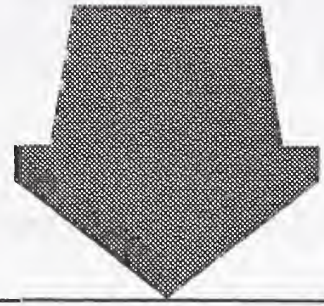
USDC



U.S. DISPLAY CONSORTIUM

Competitive Requirements

- FPD Research and Development
- FPD Equipment and Materials Infrastructure
- FPD Volume Manufacturing



The Creation of a Domestic FPD Industry.

USDC

U.S. DISPLAY CONSORTIUM

Premise

- U.S. must be a leading player in flat panel displays in order to be competitive in the world market for electronic systems (products).
- Manufacturers, Suppliers, Users and U.S. Government must team if U.S. is to successfully compete.
- USDC will focus on developing U.S.-based FPD infrastructure and fostering partnerships between U.S. suppliers, developers, and manufacturers.

USDC Philosophy

- Industry-led, public/private partnership.
- Non-profit, non-manufacturing organization.
- Provide *common platform* for FPD manufacturers/developers, users, and supplier base to develop plans and specifications for next generation FPD manufacturing equipment and materials.
- Consortium to administer funds for equipment and materials suppliers to the FPD industry.
- Wide range of FPD technologies will be addressed.

USDC Mission

Develop and organize
the U.S. manufacturing expertise

to develop the U.S. infrastructure
required to support a world-class
U.S. based manufacturing capability

for high definition displays

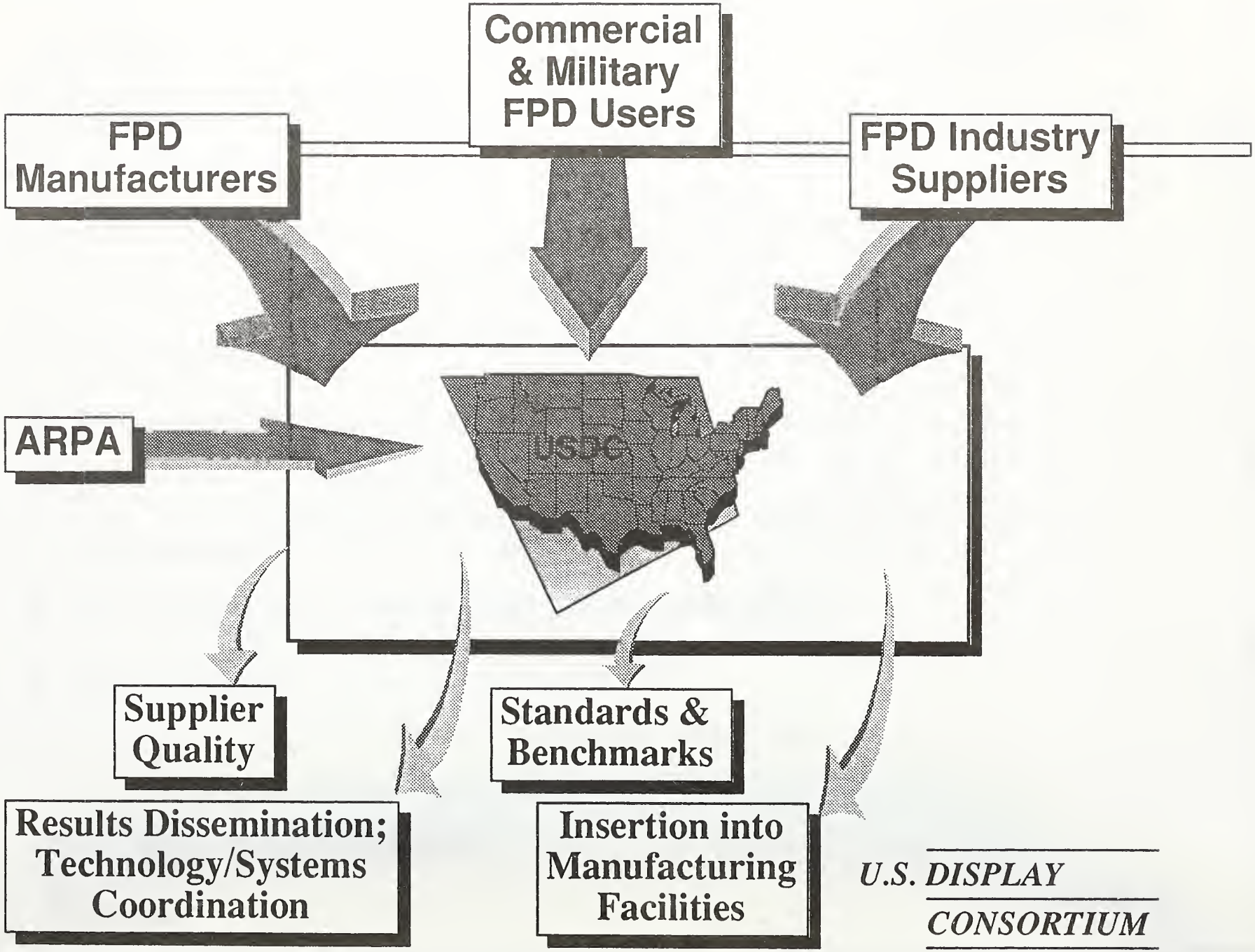
U.S. DISPLAY CONSORTIUM

USDC
Initial Members

- ✓ AT&T
- Electro-Plasma
- Kent Digital Signs
- Norden Systems
- ✓ OIS
- ✓ Photonics Imaging
- ✓ Planar Systems
- ✓ Plasmaco
- ✓ Silicon Video
- Standish Industries
- ✓ Tektronix
- Three-Five Systems
- ✓ Xerox

- ARPA
- Commercial Display Users
- Military/Avionics Display Users
- Equipment/Materials Suppliers (SEMI-NAFPD)

U.S. DISPLAY CONSORTIUM


Commercial & Military FPD Users
FPD Manufacturers
FPD Industry Suppliers
ARPA
USDC
Supplier Quality
Standards & Benchmarks
Results Dissemination; Technology/Systems Coordination
Insertion into Manufacturing Facilities
U.S. DISPLAY CONSORTIUM

USDC Objectives

- Supplier Quality
  Develop a viable U.S.-based supplier infrastructure capable of meeting world-wide requirements for materials, manufacturing systems, and each key equipment module for current and next generation manufacturing processes.

- Insertion into Manufacturing Facilities
  Provide materials, manufacturing systems, and key equipment modules for members to integrate into their proprietary process flows and products.

- Standards & Manufacturing Benchmarks
  Drive the development of industry standards for procurement specifications, computer integrated manufacturing, mechanical interfaces, common processing steps and tools.

- Results Dissemination; Technology/Systems Collaboration
  Provide and maintain open forums for communications, collaboration, consensus building, and technology transfer within the domestic high-definition display industry.

U.S. DISPLAY CONSORTIUM

USDC Governing Board

FPD Manufacturers

Suppliers

ARPA

Military & Avionic Users

Commercial Users

CEO CTO & Staff

General Members

Technical Council

Project Teams

- Supplier Quality & Equipment Insertion
- Standards & Manufacturing Benchmarks
- Information Dissemination

U.S. DISPLAY CONSORTIUM

USDC
Vertically Integrated Approach

Provide Technology Needs, Specifications and Standards Direction

FPD USERS
- **COMMERCIAL**
- **MILITARY**

End-User Systems with FPDs that Differentiate Products

Define Manufacturing Process Needs and Standards

FPD MANUFACTURERS AND DEVELOPERS

State-of-the-Art FPDs

Manufacturing Process Improvements

Develop Specifications Required for Next Generation Equipment and Materials

FPD EQUIPMENT AND MATERIALS SUPPLIERS

Standardized Next Generation Equipment and Materials

U.S. DISPLAY CONSORTIUM

USDC Represents

- The Voice of the Customer
  - Defining Common Needs
  - Setting Common Specifications/Requirements
  - Creating Critical Mass in the Market Size

- A Partnership - Supplier/Fabricator/User/Government
  - Setting Standards
  - Support and Coordination of Resources
  - Common Focus
  - Test Bed for Process/Equipment Integration
  - Available Subject Matter Experts

11

Issues Related to Interfacing Flat Panel Displays

Ms. Jill Seman, Chips and Technologies

Flat Panel Interface Issues: A PC Perspective

Workshop on the Computer Interface to Flat Panel Displays
January 14,1993

Jill Seman
Technical Marketing Manager
Chips & Technologies

Flat Panel Interface Issues for PC Designs

- VGA resolutions of 640x480 are most commonly used in PC flat panel systems
- Predominant 640x480 panel types include:
  - Monochrome LCD-DD
  - Monochrome Plasma & EL
  - Color LCD (DD)
  - Color TFT
- Panels differ by
  - Panel characteristic
  - Panel interface
  - Problems that occur from the lack of standardization

Monochrome LCD-DD Panels Characteristics

• Most Prevalent Panels in the PC Market

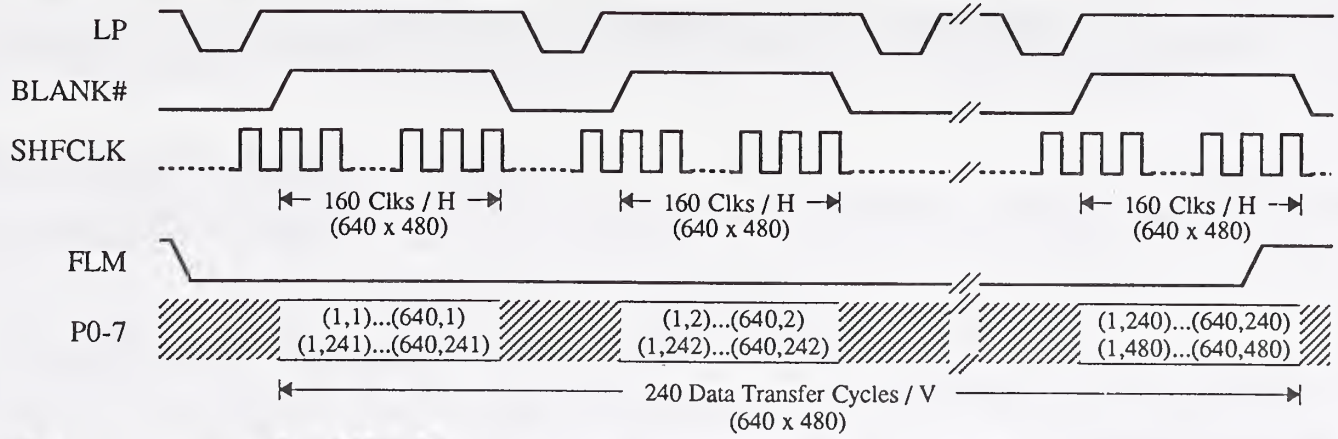
- Cost : $300-500
- Contrast Ratio 1:10
- Response Times : 300-600ms (rise and fall)
- Vertical Refresh Rates : 60-120Hz
- Power Consumption : 0.5W - 1W

• Monochrome LCD-DD Drive Scheme

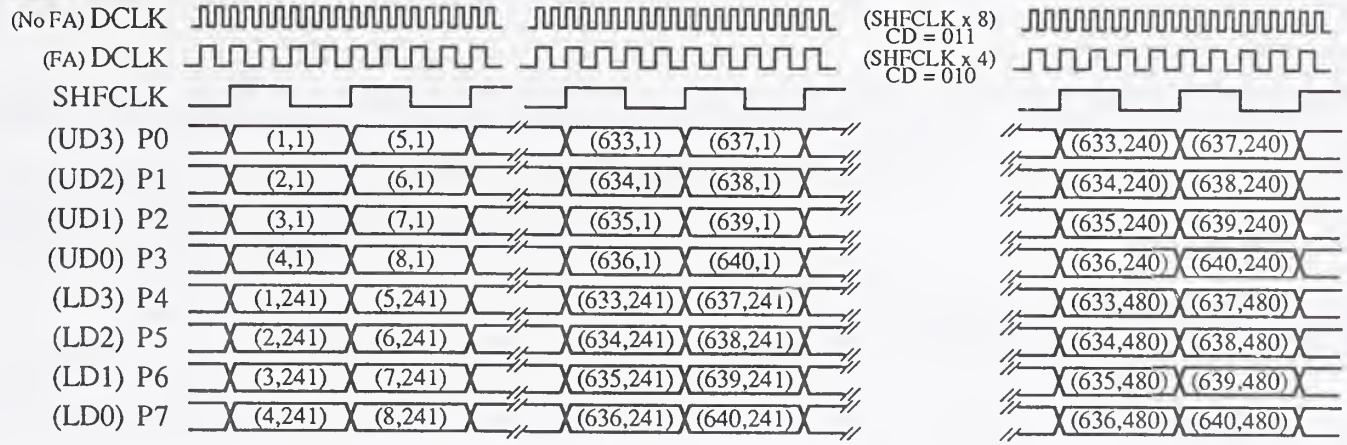
- Dual Panel, Dual Drive scheme:
  Data Required from two separate memory locations
- 3 Control Signals are used LP,FLM and SHFCLK
- 8 data lines - 8 pixels / clock
- 2 Power Supply Voltages required: VDD (+5V) & VEE (LCD)

Monochrome LCD-DD Panel Interface

Panel Output Timing - 640 x 480 Monochrome DD 8-Bit (1 Bit / Pixel, 8 Pixels / Shift Clock)



Panel Output Pixel Order - 640 x 480



FA = Frame Accelerator (Imbedded or External)

Monochrome LCD-DD Panels Interface Issues

- Panel interfaces vary by manufacturer and product
  Products from the same manufacturer and product line differ.

- No standard cabling schemes
  - Each panel type has different pinouts
  - Each panel connector has different size, shape & orientation

- No standard labeling schemes:
  - The LSB/MSB of UD0-3 and LD0-3 is not universal
  - Voltage names change from panel to panel

- LCD voltages differ from panel to panel. LCD voltages range from -40V to +40V

- No standard panel power sequencing method

- Horizontal and Vertical Timing differ for every panel

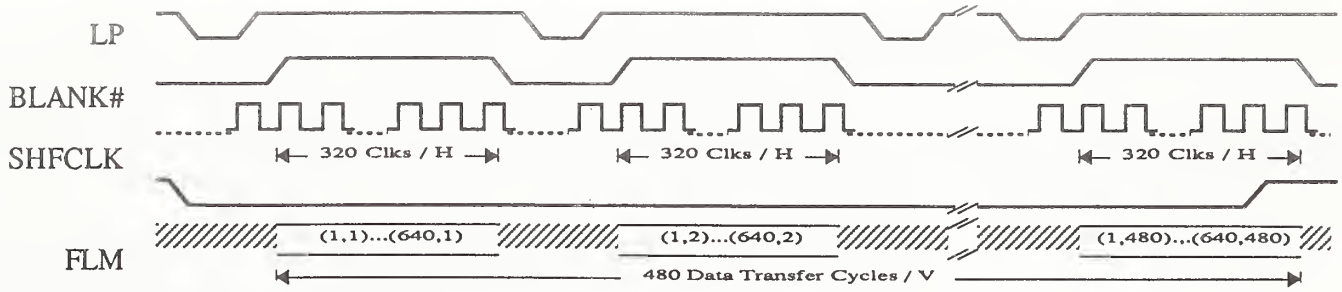
CHIPS®

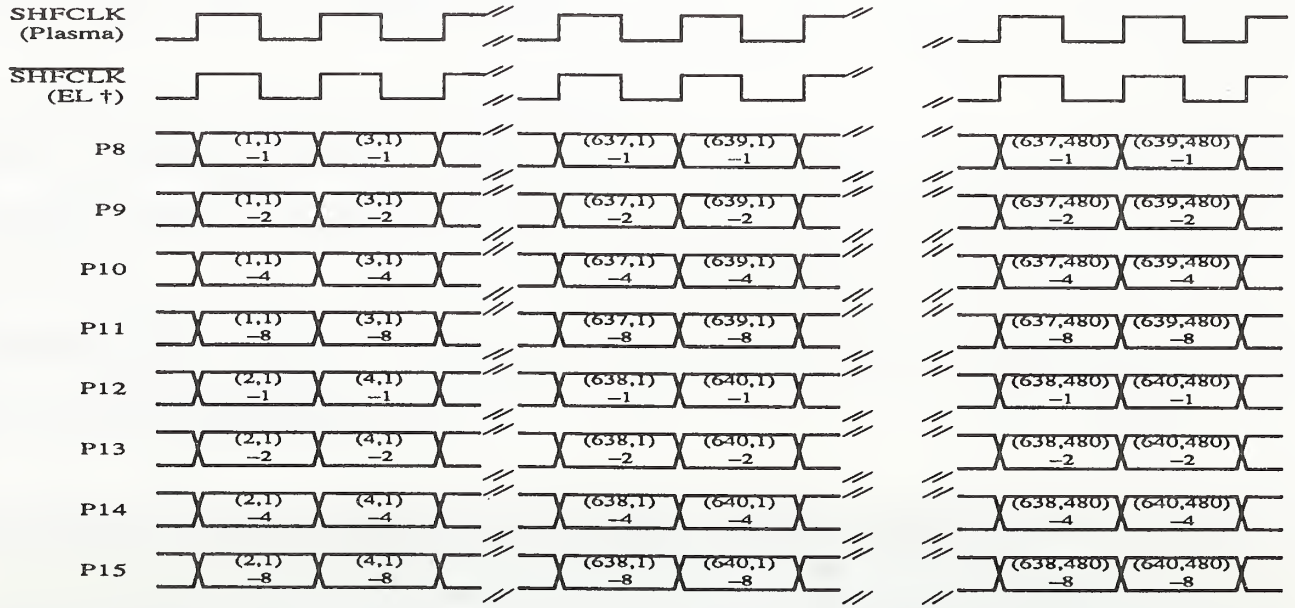
Plasma and EL Panel Characteristics

- **Most Prevalent Embedded Controller/ Instrument PC Market**
  - Cost of $700-1500
  - Luminance : 1:30
  - Response Times : 40-80ms (rise and fall)
  - Vertical Refresh Rates 60 Hz
  - Power Consumption : 20-35W
- **Plasma / EL Drive Schemes**
  - Single Panel, Single Drive scheme:
    Data Required from one memory location
  - 3 Control Signals are used HSYNC, VSYNC, SHFCLK, and BLANK
  - 8 data lines - 1,2,4 or 8 pixels / clock
  - 2 Different Power Supply Signals are used VDD (+5V) & VEE (LCD)

CHIPS®

Monochrome Plasma/EL Panel Interface





† EL panels use the rising edge of SHFCLK to clock in panel data, so the SHFCLK output from the 65540 / 545 must be inverted prior to driving the panel

Monochrome Plasma /EL Panel Interface Issues

- Panel interfaces vary by manufacturer and by product
- No standard cabling
  - Each panel manufacturer has different pinout
  - Each panel connector has different size, shape, orientation
- BIAS voltages differ from panel to panel.
- No standard panel power sequencing method
- Clock divide-by schemes vary:
  - Interfaces can be 1,2,4 or 8 bits /clock
  - Hsync and Vsync timing vary

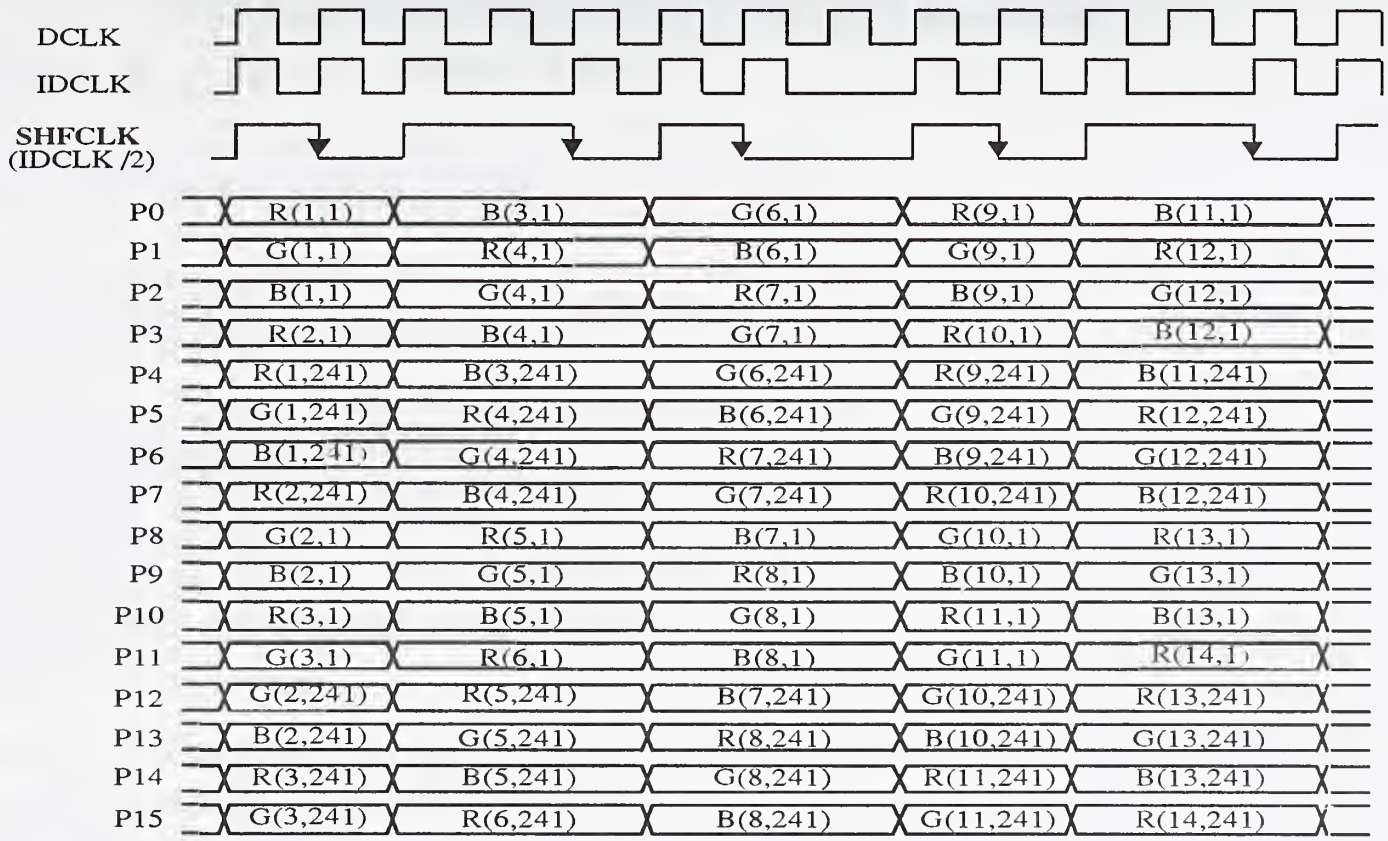
CHIPS®

Color LCD-DD Panel Characteristics

- Most Prevalent Mid-Range Notebook PC Market
  - Cost : $700-1500
  - Contrast Ratio : 1:20
  - Response Times : 250-350ms (rise and fall)
  - Vertical Refresh Rates : 70-110 Hz
  - Power consumption : 0.6 - 1.5W
- Color LCD-DD Drive Schemes
  - Dual Panel, Dual Drive scheme:
    Data Required from two separate memory location
  - 3 Control Signals are used LP, FLM & SHFCLK
  - 8 or 16 data lines - 2 2/3 or 5 1/3 sub-pixels /clock
  - 2 Power Supply Voltages required: VDD (+5V) & VEE (LCD)

CHIPS®

Color LCD-DD Panel Interface



PT:	11 (DD Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	01 (4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer / Acceleration:	Enabled / Enabled

16 Pixels (8 each for the upper and lower panels) are transferred every 8 Dot Clocks (3 Shift Clock Edges)

Color LCD-DD Interface Issues

- Panel interfaces vary by manufacturer and by product.

- No standard cabling schemes
  - Panel manufacturer pinouts (8 & 16 bit) differ
  - Panel connectors differ by size, shape & orientation

- No standard labeling schemes:
  - LSB/MSB differ for UD0-7/LD0-7
  - Voltage names change from panel to panel
  - LCD voltages differ

- No standard panel power sequencing method

- Control signal timing vary:
  - Clock divide by schemes vary
  - Hsync & Vsync timing vary

CHIPS®

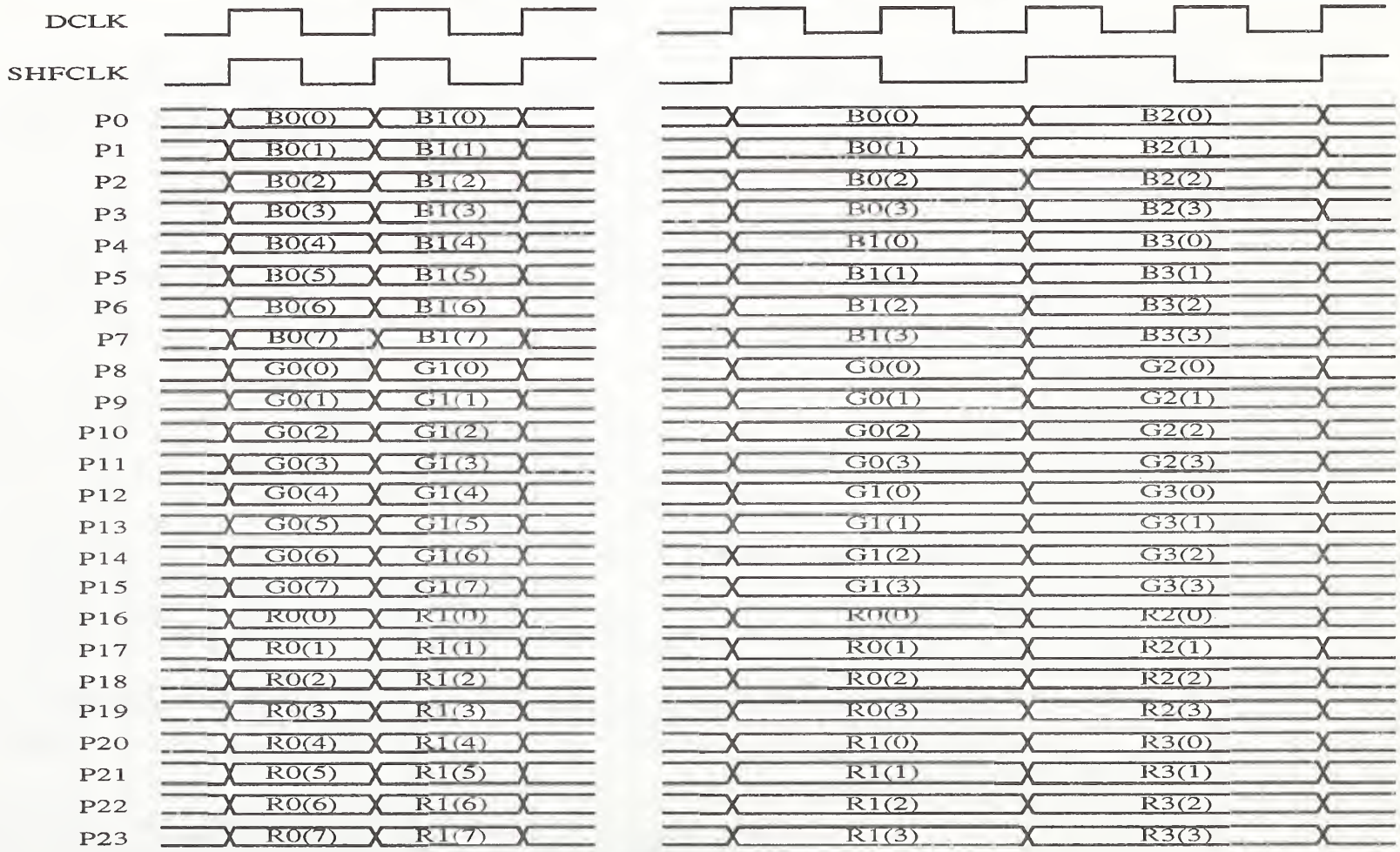
Characteristics of Color TFT Panels

- **Most Prevalent High-End PC Market**
  - Cost : $1000-3000
  - Contrast Ratio : 1:60
  - Response Times : 50-100ms (rise and fall)
  - Vertical Refresh Rates : 60 Hz
  - Power Consumption : 3-8W

- **TFT Drive Schemes**
  - Single Panel, Single Drive scheme:
    Data Required from one memory location
  - 4 Control Signals are used HSYNC, VSYNC, SHFCLK, and BLANK
  - 9,12,18 or 24 data lines - 1pixel / clock
  - 2 Power Supply Voltages are required: VDD (+5V) & VEE (LCD)

CHIPS®

Color TFT Panel Interface



CD:	000 (1 Pixel / Clock)	001 (2 Pixels / Clock)
FRC:	00 (no FRC)	10 (2-Frame)
Bits / Pixel:	111(8 bits/pixel)	100/101 (4 or 5 bits/pixel)
Pixel Format:	8-8-8 RGB	4-4-4 RGB
Data Width:	24-Bit †	24-Bit †

† Panels with 18-bit data interfaces would use this setting and only connect to the msbs of each color

Color TFT Panel Interface Issues

- Sharp has created a standard for TFT
- Hsync, Vsync and Blank timing similar to CRT timing
- No standard cabling schemes
  - Manufacturer pinouts differ
  - Panel connector differ by size, shape, & orientation
- LCD voltage values differ from panel to panel.

PC Design Challenges for Flat Panel Interfacing

- Panel Support Versatility:
  - Dual Drive (DD) and Single Drive (SS) Formats
  - Color and monochrome Support
  - Various data formats
- Control Signal Timing Programmability
  - Independent generation of LP,FLM, SHFCLK and BLANK
  - Several clock divide schemes
  - Programmable Panel Power Sequencing Control Signals
- Variable Voltage Supplies
- Developing methods to support multiple panels with one design

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High Resolution Color LCD Interface Issues

Mr. Sunder Velamuri, Cirrus Logic, Inc.

High Resolution LCD Interface Issues

- Market Trends
- Existing requirements and concerns
- Merging of requirements to standards
- Interface options
- Decision process

CIRRUS LOGIC

LCD Market

- Expanding number of applications
  - Monitors
  - Portable EWS applications
  - Overhead Projector
  - Notebooks
  - Industrial & Automotive applications

CIRRUS LOGIC

Market Segmentation of Color TFT LCDs

- LCDs for PDAs
- LCDs for Notebooks
- LCDs for Monitors & Workstations

CIRRUS LOGIC

Key Issues for Color TFT LCD

- Display resolution
  - LCDs for monitors & EWS laptops (1280x1024, 1024x768)
  - LCDs for notebooks (800x600, 640x480)
  - LCDs for PDAs (640x480, 320x240 and << 8" diagonal)
- Color palette
  - 256K color palette (LCDs for notebooks)
  - 16.7M color palette (LCDs for monitors and EWS laptops)
- Minimal EMI generation
  - Clock rates
  - Control and data signal voltage levels

Key issues for Color TFT LCD

- Display quality
  - Color uniformity
    - » Equal steps in perceived brightness (particularly in darker shades)
    - » Desired Gamma correction
    - » Elimination of flicker and other display artifacts
  - Color consistency
    - » Across a single LCD
    - » Among same model of LCDs
  - Color matching capability
  - RGB color correction

Key issues for Color TFT LCD

- Module form factor
  - Thickness
  - Weight
  - Maximized display area (minimum bezel widths)
- Minimal power consumption
  - Display data voltage levels
  - Vertical refresh rate
- Minimal cost

CIRRUS LOGIC

Panel interface goals

- Minimal EMI generation
- Minimal number of data lines from the graphics controller to the panel
- Upward/Downward expandability of panel interfaces
- Minimized power dissipation
- Ability to drive panels over cabling lengths > 3ft
- Multi Media hooks

CIRRUS LOGIC

Future expandability

CIRRUS LOGIC

Multi Media Considerations

- Ability to support full motion video
- Ability to support existing video standards
- Maintain minimal bezel widths
- Panel cost impact

CIRRUS LOGIC

Interface options

- CRT like panel interface
  - Consists of analog RGB, HSYNC & VSYNC
  - Requires on board PLL to generate dot clock
  - Gamma correction performed in the analog domain
  - Display quality optimization requires multiple external devices to condition data to provide opposite output voltage polarity on each adjacent pixels
- Disadvantages
  - High frequency PLL operation is a technical challenge
  - High cost and power dissipation
  - Large number of ICs/board space and cost

CIRRUS LOGIC

Interface options

- Analog Interface
  - Consists of analog RGB, HSYNC, VSYNC & DCLK
  - High speed A/D converters are used to convert data to digital domain
  - Gamma correction performed by control ASIC with look-up tables
  - Data is converted back into analog domain with high speed D/A converters
  - Data inverting circuit used to optimize display quality
- Disadvantages are a large number of ICs/board space, very high cost, high power consumption

Extension of existing interface

- Digital interface
  - Consists of 24 data lines (1 pel/clk), HSYNC, VSYNC, DCLK & DE
  - Existing interfaces are 5V and rapidly moving to 3.3 V or lower voltages
  - Existing base of graphics controllers supporting this interface
- Disadvantages
  - High speed digital interface is required from the graphics controller to the panel
  - High number of data lines required to support lower operating frequencies

Compatibility requirements

- VESA monitor timing compatibility
- Ability to support 60 Hz, 72Hz and 75Hz vertical refresh requirements
- Software driver compatibility for different resolutions and different vertical refresh rates

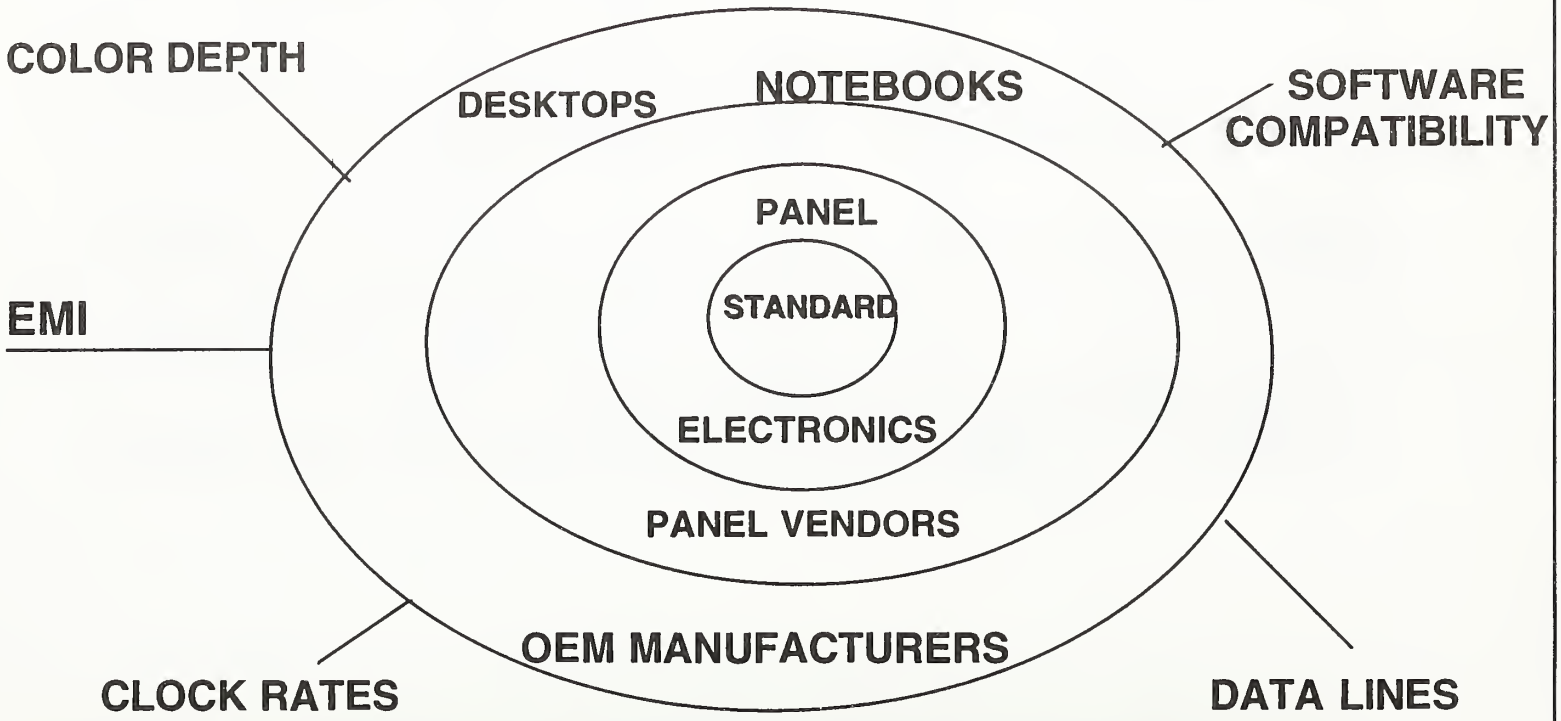
CIRRUS LOGIC

VESA compatible timing

Panel Size	Pel/clk	Clock rate	No. of Colors and data lines required				Refresh
		(MHz)	512 colors	4096 colors	256K colors	16.7 M colors	rate (Hz)
1280x1024	1	135	9	12	18	24	75
	2	67.5	18	24	36	48	
	4	33.75	36	48	72	96	
1024x768	1	78.75	9	12	18	24	75
	2	39.375	18	24	36	48	
	4	19.688	36	48	72	96	
1024x768	1	65	9	12	18	24	60
	2	32.5	18	24	36	48	
	4	16.25	36	48	72	96	

CIRRUS LOGIC

Decision making process



CIRRUS LOGIC

13

The Voluntary Standards Process

Mr. William Burr, NIST

The Voluntary Standards Process

W. E. Burr
January 13, 1993

NIST
UNITED STATES
DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS
AND TECHNOLOGY

"Voluntary Standards"

- formal, written standards
- not developed by the government
  - may participate in development
- voluntary participation in development
- use is voluntary, but
  - may be incorporated by reference in various codes
  - may be used in purchase specifications
  - may have effect on marketability of products
  - not observing some "voluntary" safety standards may increase liability exposure

Voluntary Standards Processes

- characterized by formal processes
  - written procedures
  - checks and balances
- motivated by concern for
  - fairness
  - antitrust liability (at least in the U.S.)

Antitrust Liability & Standards

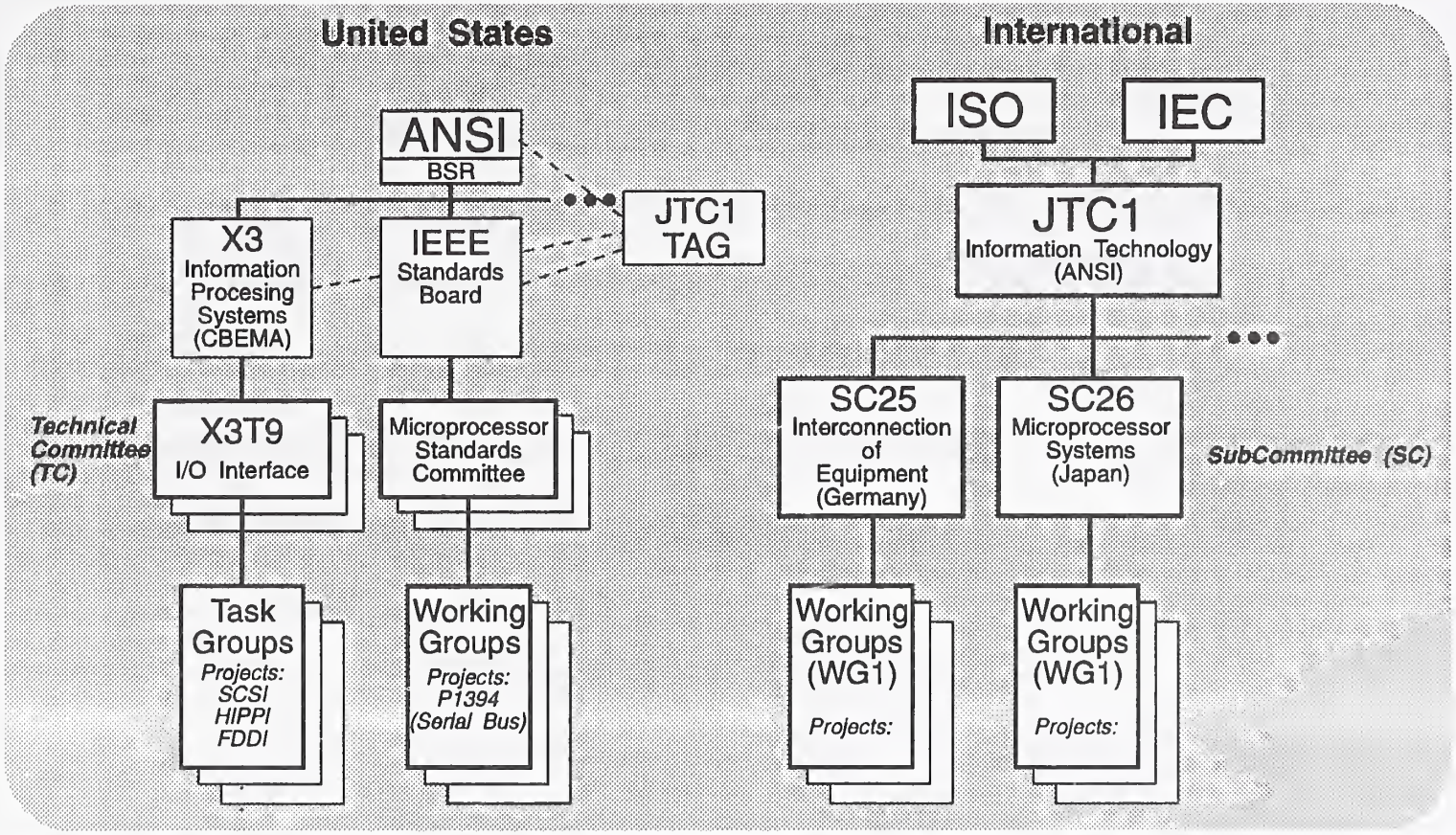
- triple damages
- Hydrolevel case
  - US Supreme held that a standards organization (American Society of Mechanical Engineers) could be held liable for the anticompetitive actions of standards committee officers acting with the "apparent authority" of the ASME
- Allied Tube case
  - US supreme court held that standards participants could be held liable for their anticompetive actions even when those actions followed all the rules and procedures of the standards-setting organization (National Fire Protection Association)

Standards Conspiracy Alleged

"I was directed to, and I did, conspire with my Bellcore management, and conspire jointly also with members of each of the RBOCs, to provide technical means necessary to leverage monopoly voice telecommunications access to create monopoly local access to ISDN."

From statement of Richard Taylor to Judge Harold Greene in a deposition given on Nov. 19, 1992 as reported in "ISDN standards scandal alleged" in the October 25, 1993 issue of *Network World*. According to this article, Mr. Taylor alleges that Bellcore and the RBOCs conspired to ensure that, "ANSI T1.602 is written to make 'unfair and unnecessary,' demands of the service providers, ensuring that only carriers with the resources of Bell operating companies can offer ISDN access."

Voluntary Standards Bodies



American National Standards Institute (ANSI)

- does not develop standards
- accredits standards developers
- approves & publishes standards
- U.S. member of international voluntary standards bodies
  - International Standards Organization (ISO)
  - International Electrotechnical Commission (IEC)

ANSI

- no special U.S. legal status
  - no law or treaty
- U.S. standards developers not all accredited by ANSI
  - QIC
  - VESA
  - ATM Forum
- ANSI is widely recognised for IT standards
  - X3, IEEE and EIA-TIA are accredited
  - ANSI is US member of ISO & IEC
    - » ANSI standards often become ISO/IEC standards

ANSI Accreditation

- accredited organization
  - IEEE is an accredited standards organization
- accredited standards committee
  - X3 is an accredited standards committee
- accredited sponsor using canvass method
  - NIST is an accredited canvass sponsor

Reasons for ANSI Accreditation

- requires a fair process
- process reduces risk of antitrust liability
- recognition
- consensus
- paves the way for an international standard

ANSI Accreditation Disadvantages

- takes time & effort to get accredited
  - get procedures approved
- more emphasis on process than results
- development process takes time
  - can't limit participation to like-minded parties
  - can't arbitrarily limit discussion
  - can't just ignore contrary views
  - market can pass you by while you follow process
- standards politics
  - with contending factions in your group
  - with other groups

ANSI Due Process

- written procedures
  - membership & voting
  - approval
  - appeals
- consideration of views & objections
  - must consider & attempt to resolve all objections
  - keep record of objections & their resolution
- consideration of standards proposals
  - prompt consideration of proposals to develop or revise standards
- records
  - minutes, etc.

ANSI Due Process

- written procedures
  - membership & voting
  - approval
  - appeals
- consideration of views & objections
  - must consider & attempt to resolve all objections
  - keep record of objections & their resolution
- consideration of standards proposals
  - prompt consideration of proposals to develop or revise standards
- records
  - minutes, etc.

Canvass Method

- proposed standard is developed
- sponsor develops canvass list
  - interested orgs, agencies, companies, individuals, etc.
  - not dominated by any interest category
  - announced in *Standards Actions* & reviewed by Executive Standards Council
- proposed standard balloted by canvass list
  - 3 month ballot (with 3 month extensions)
  - objections
    - » must state reason
    - » must be considered
    - » unresolved objections must be reported

Canvass Method

- works well for noncontroversial standards
  - specialised applications
- voted on by a potentially large list
  - How will objections be considered and resolved?
- may not naturally lead to ISO/IEC standard
  - may not be an established relationship with a JTC1 SC

ANSI Standards Approval

- Board of Standards Review (BSR) determines
  - due process followed
  - standard within scope
  - other known standards examined
  - patent policy met
  - appeals completed
  - consensus achieved
    - » more than majority, less than unanimity

Joint Technical Commission 1 (JTC1)

- International Standards Organization (ISO)
- International Electrotechnical Commission (IEC)
- voluntary standards (no treaty)
  - recognised by GATT
  - accepted international body for IT standards
- ANSI is U.S. Member of ISO & IEC
- ANSI is JTC1 Secretariat
- JTC1 Technical Advisory Group (JTC1 TAG) determines US policy
  - separate TAGS for each ISO SC

International Standards

- procedure in JTC1 SC
  - actual development work may be done in SC
    - » various OSI standards
  - or most work may take place elsewhere, then be taken to ISO SC
    - » SCSI
    - » FDDI
    - » IEEE 802 LANs
- "Fast Track" procedure
  - for approved National Standards
  - also "Fast Track" ECMA standards

One Option

- form industry group
- forget accreditation or recognition by standards bodies
- develop a standard
- push for acceptance in the marketplace

Paths to a "Recognized" FP Std.

(There's more than one road to Rome)

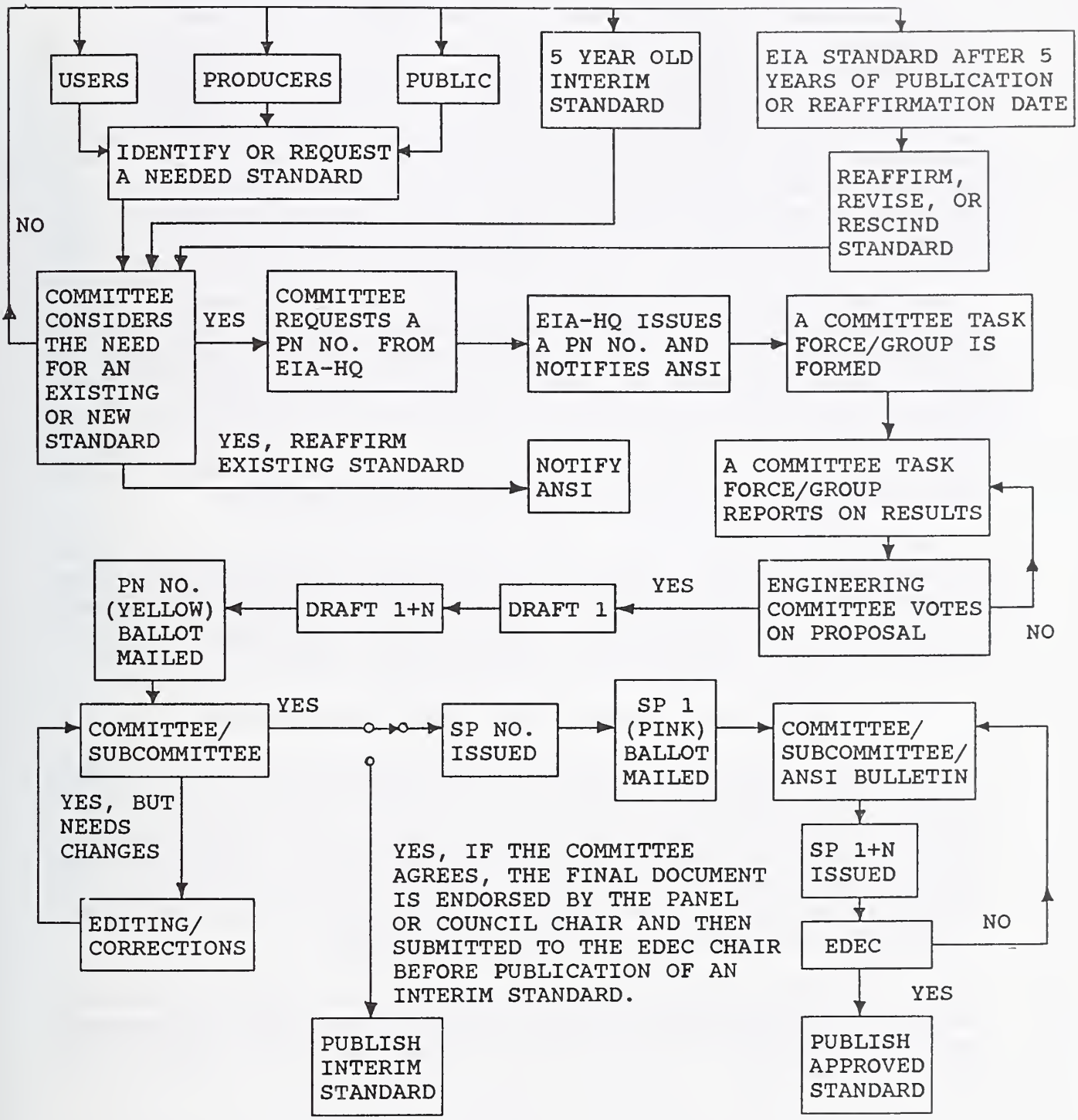
- get industry body accredited & develop there
- develop initial draft in industry group then
  - take draft to accredited committee
  - NIST sponsored canvas
  - submit to ECMA through an ECMA member company
    - » path to ISO via fast track
  - submit directly to ISO through JTC1 TAG
    - » might be possible, NIST is exploring
- start IEEE standards project
- interest existing X3 Technical Committee
- start a new X3 Technical Committee

14

Electronic Industries Association (EIA)

Mr. Thomas Mock, EIA

EXISTING EIA STANDARDS SETTING PROCESS



PN = Project Number
SP = Standards Proposal
EDEC = Engineering Department Executive Committee
ANSI = American National Standards Institute

REV. E

Reference to Patented or Patentable Products in EIA Standards

Requirements in EIA standards that call for the use of patented items should be considered with great care. While there is no objection in principle to drafting a proposed Standard in terms that include the use of an existing or pending patented item, if it is considered that technical reasons justify this approach, committees should ensure that no program of standardization shall refer to a product on which there is a known patent unless all the relevant technical information covered by the patent is known to the formulating committee, subcommittee, or working group. If the committee determines that the standard may require the use of patented or patentable item(s), then the committee chairperson must also receive a written assurance from the organization holding rights to such patents or patentable item(s) that a license will be made available without compensation to applicants desiring to use the license to implement the standard or a written assurance that a license will be made available to all applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination. Additionally, when a known patented or patentable item is referred to in an EIA standard, a Caution Notice, as outlined in this document, shall appear in the EIA standard. The term "patented", as used in this policy, also includes pending patents on items and processes under consideration by a committee, subcommittee, or working group.

All correspondence between the patent holder or applicant and the formulating committee, subcommittee, or working group, including a copy of the written expression from the patent holder as mentioned above, shall be transmitted to the EIA Engineering Department at the earliest possible time, but not later than the point in time when the standards is ready for subcommittee or committee ballot circulation.

Committee Chairpersons Responsibility Concerning IPR

The Chairperson must call to the attention of the members present the requirements contained in EIA Legal Guides, and call attention to the obligation of all participants to inform the Committee of any knowledge they may have of any patents, or pending patents that might be involved in the work they are undertaking. Appendix E - Legal Guides Summary provides viewgraphs that should be used at the beginning of the meeting to satisfy this requirement. Additionally, all participants must be asked to read the statement on the back of EIA Sign-in/Attendance Rosters.

When a formulating committee has determined through its balloting process that a patented or patentable item or process is included in the proposed EIA Standard, the following notice shall be included in the inside front cover in addition to that given in Appendix D:

Committee Chairpersons Responsibility Concerning IPR (continued)

"The user's attention is called to the possibility that compliance with this standard may require use of an invention covered by patent rights.

By publication of this standard, no position is taken with respect to the validity of this claim or of any patent rights in connection therewith. The patent holder has, however, filed a statement of willingness to grant a license under these rights on reasonable and nondiscriminatory terms and conditions to applicants desiring to obtain such a license. Details may be obtained from the publisher."

In addition, a footnote should be included on each page that has a reference to patented item(s) as follows: "Compliance with this section of the standard requires the use of patent No. XXXXXXX, XXXX." or "The formulating committee has determined that a patent has been applied for elements involved in this Section. The applicant, XYZ Company has agreed to [license without royalty] [license under reasonable terms demonstrably free of discrimination.]"

Policy Statements on EIA Sign-in/Attendance Rosters

The policy statements reproduced on the reverse side of EIA Sign-in/Rosters shall become an integral part of all Committee and Working Group meeting's minutes and a statement shall be included in the minutes indicating that the foregoing policy was complied with.

Commonality between EIA and International Standards

It is the policy of the of the U.S. National Committee of the International Electrotechnical Commission (USNC/IEC) to work toward commonality between IEC Standards and U.S. National Standards. Commonality between IEC Standards and U.S. National Standards shall also be an objective of EIA Committees. During the development of an EIA or JEDEC standards proposal, the formulating committee, subcommittee, or working group shall conduct a review and compare the standards proposal with any similar IEC or ISO standard. Where similar IEC or ISO standards exist, a determination shall be made regarding the extent to which the EIA standards proposal is based on an existing international standard.

Where similar IEC or ISO standards do not exist, it shall be recognized during the development of the EIA standards proposal that the resulting standard will represent a basis for a U.S. position in the development of an international standard. EIA is currently responsible for supporting the International Secretariat activities of eight IEC TC's and SC's for which the U.S. holds the secretariat and serves as TAG Administrator for approximately 40 U.S. TAGS for IEC and ISO TC's and SC's. The EIA Engineering Staff can provide information to committee chairpersons or secretaries on how an EIA committee draft-standards-proposal may be reviewed by the Technical Advisor of one of these groups to obtain assistance in following the above policy and in development of the IEC or ISO similarity statement.

Statement Outlining Similarities with Non-EIA Standards

During development of a standard, the formulating committee or working group shall conduct a review and compare the standard with any similar non-EIA standards such as those from the International Electrotechnical Commission (IEC), International Organization for Standardization (ISO), Electronic Industries Association of Japan (EIAJ), etc. EIA standards should agree technically with these non-EIA standards, especially international standards, unless there are valid technical reasons why this is not possible. Once this review has been completed, the chairman should select the one paragraph of the following five that most nearly expresses the extent to which the standard agrees with a similar non-EIA standard. The wording may be modified if necessary to achieve an accurate statement. This information is useful to U.S. users of EIA standards as well as to the cognizant U.S. Technical Advisory Group for international standards. The paragraph selected will appear on the inside front cover of the completed EIA standard.

(1) "This standard is based upon the major technical content of [International Electrotechnical Commission] [or International Organization for Standardization] [or Electronic Industries Association of Japan] Standard [number], [title], [date]. It conforms in all essential respects with this [IEC] [or ISO] [or EIAJ] Standard."

Statement Outlining Similarities with Non-EIA Standards (continued)

(2) "This standard contains the major technical contents of [International Electrotechnical Commission] [or International Organization for Standardization] [or Electronic Industries Association of Japan] Standard [number], [title], [date]. It differs from [IEC] [or ISO] [or EIAJ] Standard [number] in certain important respects, as given in Appendix ___. These differences have been called to the attention of the U.S. National Committee of the [IEC] [or ISO] [or EIAJ] Technical Committee [number], [title], [date], and resolution of these differences will be sought in future meetings of [TC number] [or EIA number]."

(3) "This standard was developed by EIA Committee [number] after consideration of the contents of the latest draft of the [International Electrotechnical Commission] [or International Organization for Standardization] [or Electronics Industries Association of Japan] [Document] [or Standard] [number], [title], [date] covering this subject. This standard does not agree with [IEC] [or ISO] [or EIAJ] [Document] [or Standard] [number]. The important differences that made reconciliation of the two documents impossible are given in Appendix ___. These differences have been called to the attention of the U.S. National Committee of the [IEC] [or ISO] [or EIAJ]."

(4) "This EIA standard is considered to have international standardization implication, but the [International Electrotechnical Commission] [or International Organization for Standardization] [or Electronic Industries Association of Japan] activity has not progressed to the point where a valid comparison between the EIA standard and the [IEC] [or ISO] [or EIAJ] document can be made."

(5) "This EIA standard is considered by the formulating committee not to have international standards implications or interest."

APPENDIX
PATENT POLICY GUIDELINES

- Committee discussion of pending or existing patents is a permissible activity and is encouraged when the Committee feels that the subject pending, or existing patent represents the best technical practice for a given standardization.

- Discussion of a pending or existing patent does not constitute an acknowledgement of the validity of the patent since validity is based on prior art and determination of who first (made application) (discovered the technique or process). The Committee or Working Groups concern is with its technical content and whether that content is suitable for standardization.

- By its terms, the Patent Policy applies with equal force to situations involving 1) the discovery of patents that may be required for use of a standard subsequent to its adoption and 2) the initial issuance of a patent after adoption. Once disclosure is made, the holder is obligated to provide the same assurances to EIA as are required in situations where patents exist or are known prior to approval of a proposed standard as an EIA Standard.

Thus, if notice is given of a patent that may be required for use of an already approved EIA Standard, a standard developer may wish to make it clear to its participants that the EIA Procedures require the patent holder to provide the assurances contained in the Patent Policy or suffer the withdrawal of EIA's approval of the standard as an EIA Standard and ultimately as an American National Standard.

BRIEF SUMMARY

IMPROPER ACTIVITIES AND PROGRAMS

- PRICES AND PRICING, POLICY
- TERMS AND CONDITIONS OF PURCHASE AND SALE
- COSTS PERTAINING TO INDIVIDUAL COMPANIES
- FUTURE PLANS OF INDIVIDUAL COMPANIES
- BOYCOTTING CUSTOMERS OR PRODUCTS

CONDUCTING ACTIVITIES

- NOTICES AND AGENDAS
- CONDUCT OF MEETINGS
  - OPENNESS
  - DUE PROCESS
  - VOTING
- MINUTES

BRIEF SUMMARY

EIA/JEDEC PATENT POLICY SUMMARY

- Requirements in Standards that call for use of a patented item or process may not be considered by formulating Committees unless all of the relevant technical information covered by the patent or pending patent is known to the formulating committee or working group, and the committee Chairman has received written expression from the patent applicant or holder that one of the following condition prevails:

(1) a license shall be made available without charge to applicants desiring to utilize the patent for the purpose of implementing the standard(s), or

(2) a license shall be made available to applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination

- In either event, the terms and conditions of the license must be submitted to the EIA General Counsel for review.

- An appropriate footnote shall be included in the standard identifying the patented item and describing the conditions under which the patent holder will grant a patent

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Video Electronics Standards Association (VESA)

Mr. Scott Vouri, Binar Graphics, Inc.

Video Electronics Standards Association (VESA)

Scott Vouri
Chairman

VESA is.....

- The international standards organization that sets and supports industry-wide video graphics and related standards for the benefit of the end user

VESA's Role in the Industry Today

- **Set and Support Industry Standards that:**
  - **Benefit the end user**
  - **Create a level playing field**
  - **Grow the market!**

VESA Sets Standards for:

- Computer Displays
- Graphics Contollers and Adapters
- Computer Busses
- Software

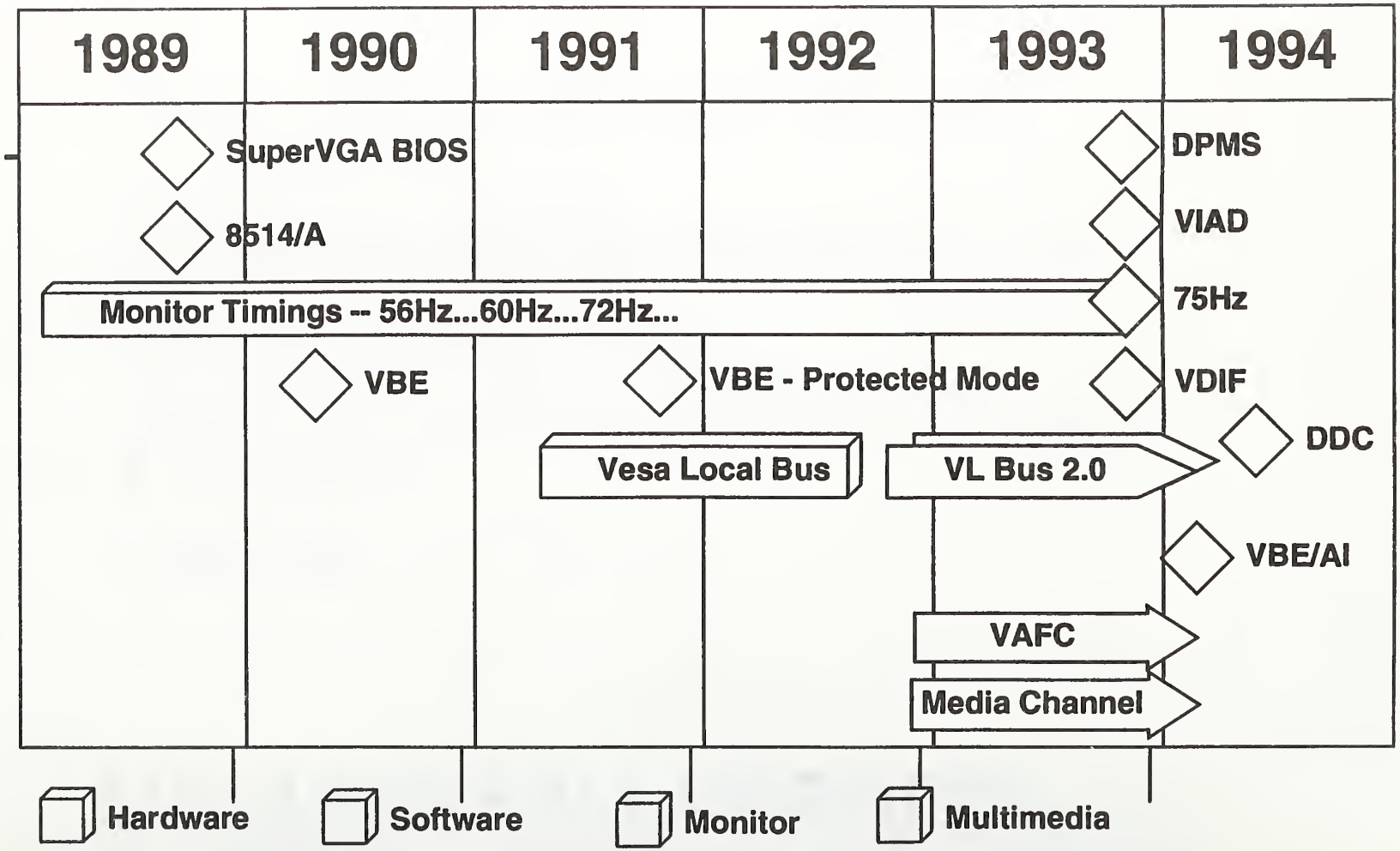
Most Major Manufacturers are VESA Members

- Apple, IBM, Compaq, Dell, Gateway
- Intel, AMD, Cypress
- ATI, Cirrus Logic, S3, Tseng Labs, WD
- NEC, Mitsubishi, Phillips
- Media Vision, PictureTel, Creative Labs

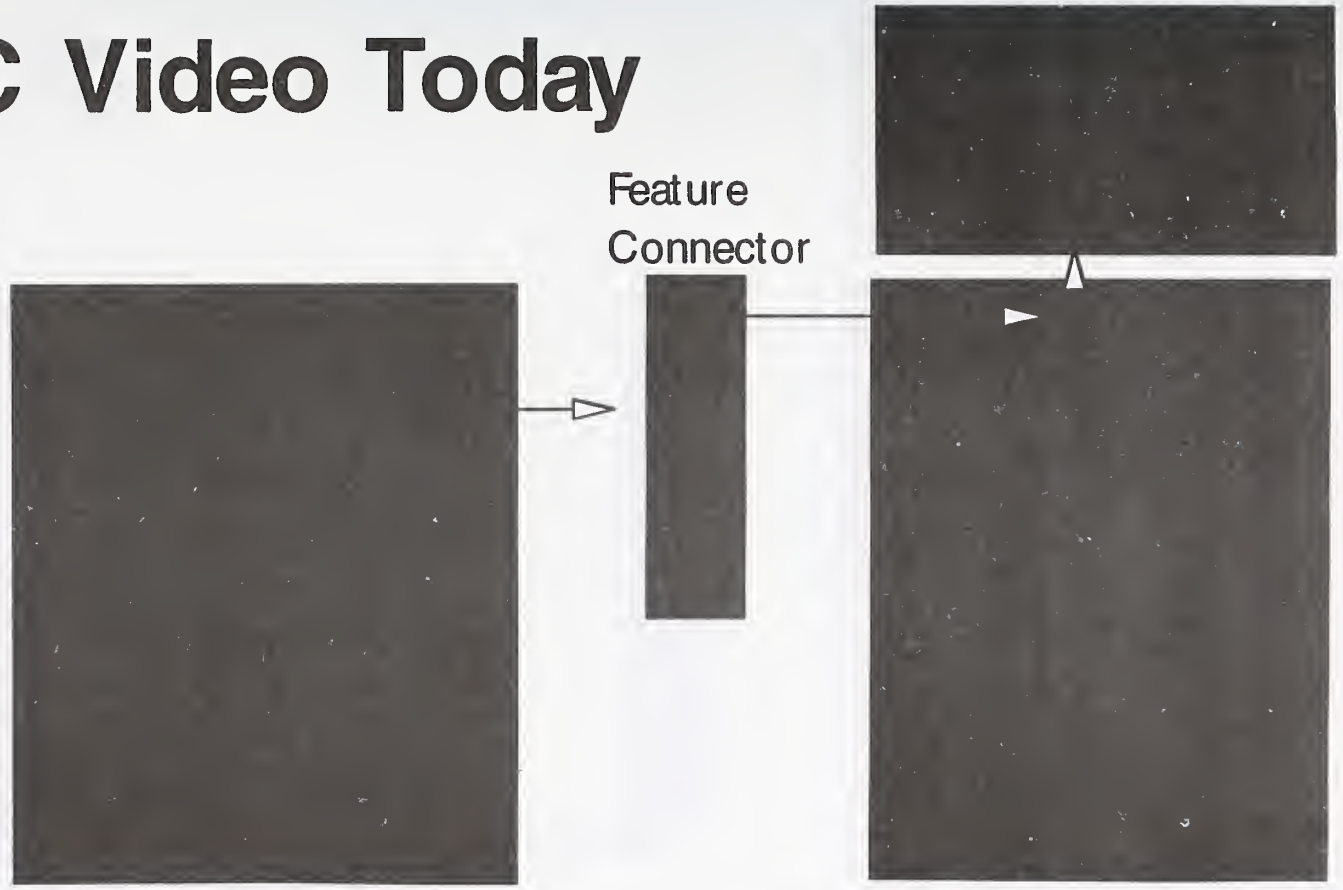
Five Technical Committees

- Monitor
- Local Bus
- Advanced Video Interface
- Software Standards
- Advanced Graphics Interface

VESA Standards



PC Video Today

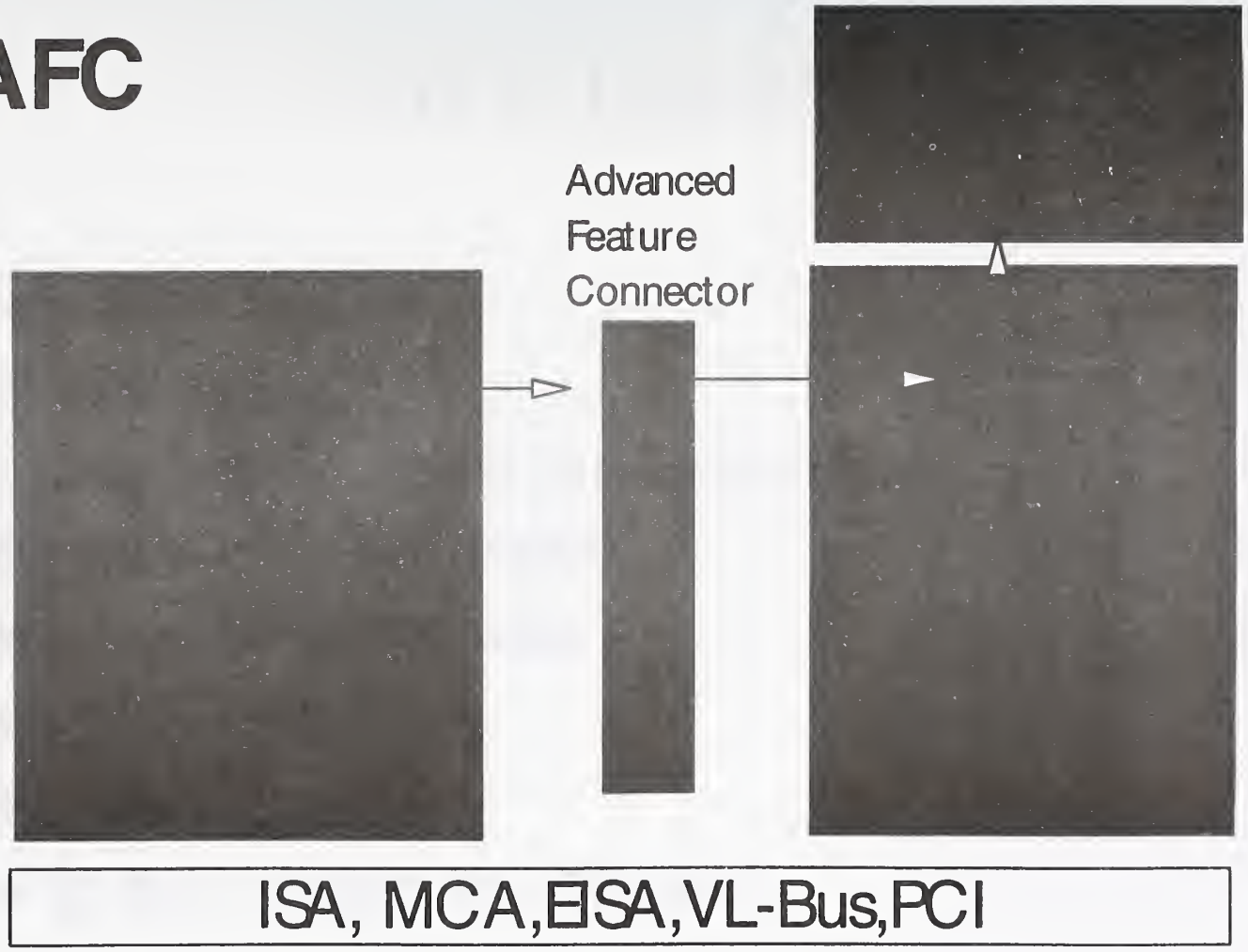


ISA, MCA, EISA, VL-Bus, PCI

Two New Approaches

- VESA Advanced Feature Connector
- VESA Media Channel

VAFC



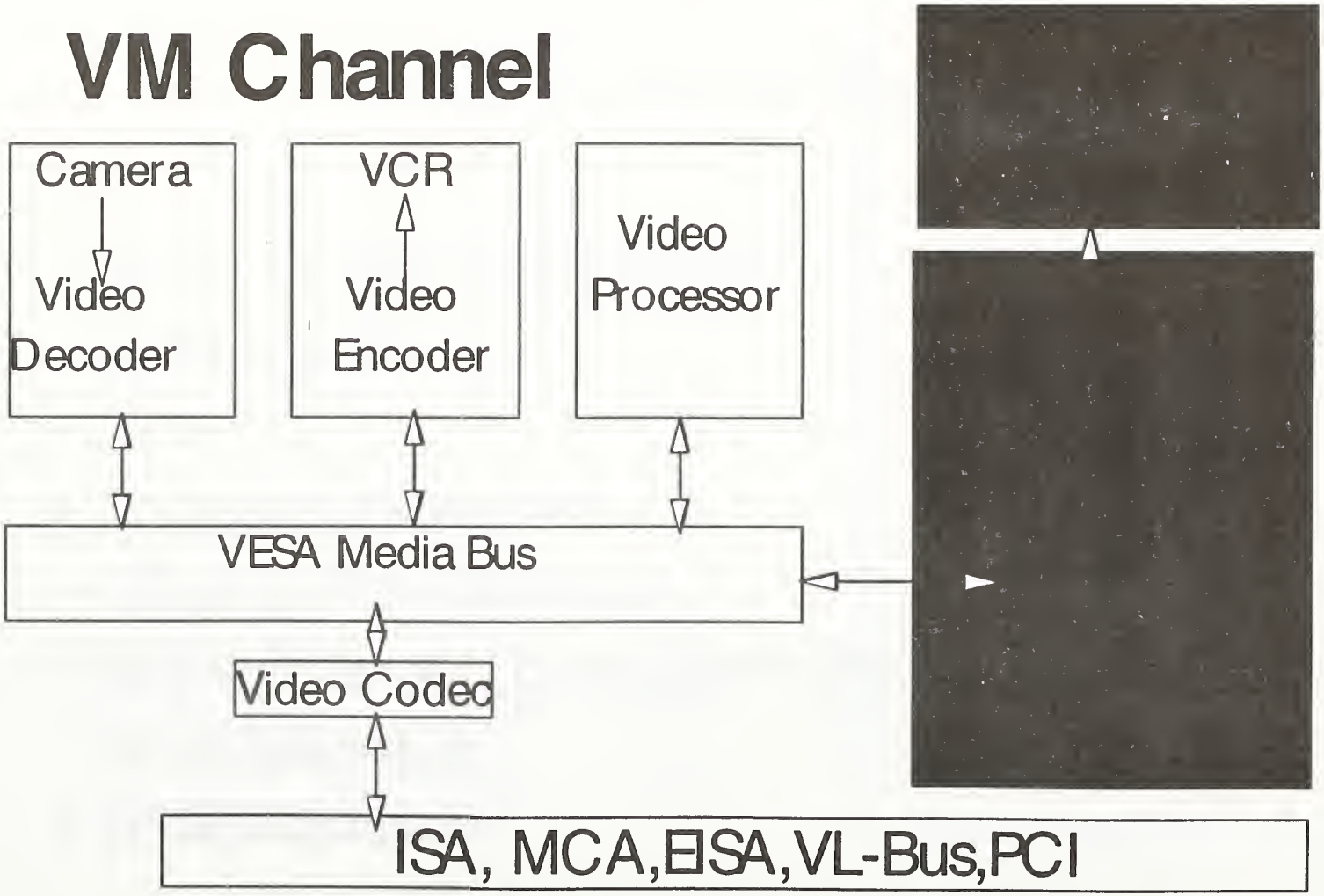
VAFC Advantages

- 32 bit / 150Mb per second
- 1280 x 1024
- RGB, YUV
- Implementable now
- Some cost reduction

VAFC Limitations

- Single Source
- Unidirectional
- Not Significant Cost Reduction

VM Channel

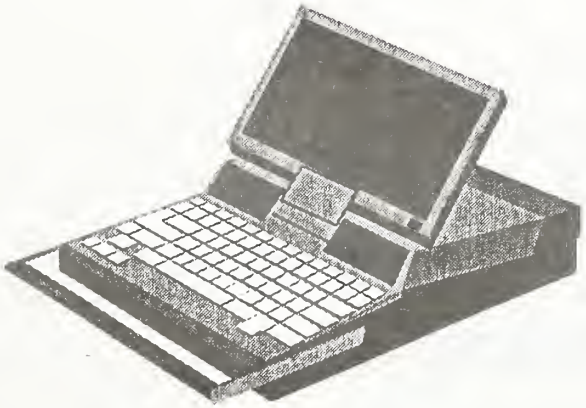

Camera
Video Decoder
VCR
Video Encoder
Video Processor
VESA Media Bus
Video Codec
ISA, MCA, EISA, VL-Bus, PCI

VM Channel Advantages

- Bi-directional
- Multi-Master
- 32 Bit Bus
- 16 Bit Per Pixel
- Excellent Cost Reduction

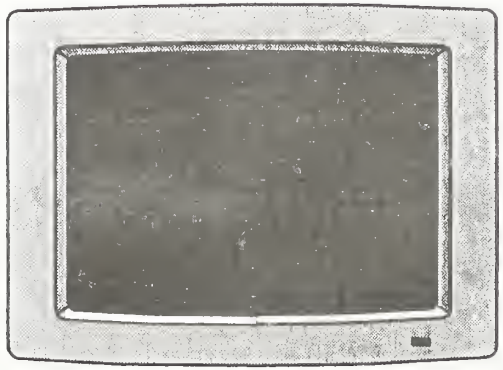
What Needs To Be Standardized

Old Issues



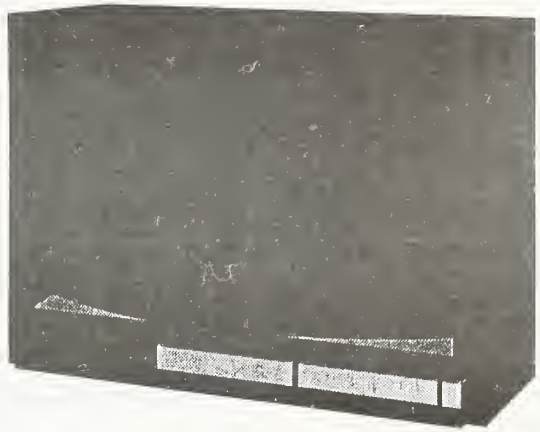
Laptops

New Issues



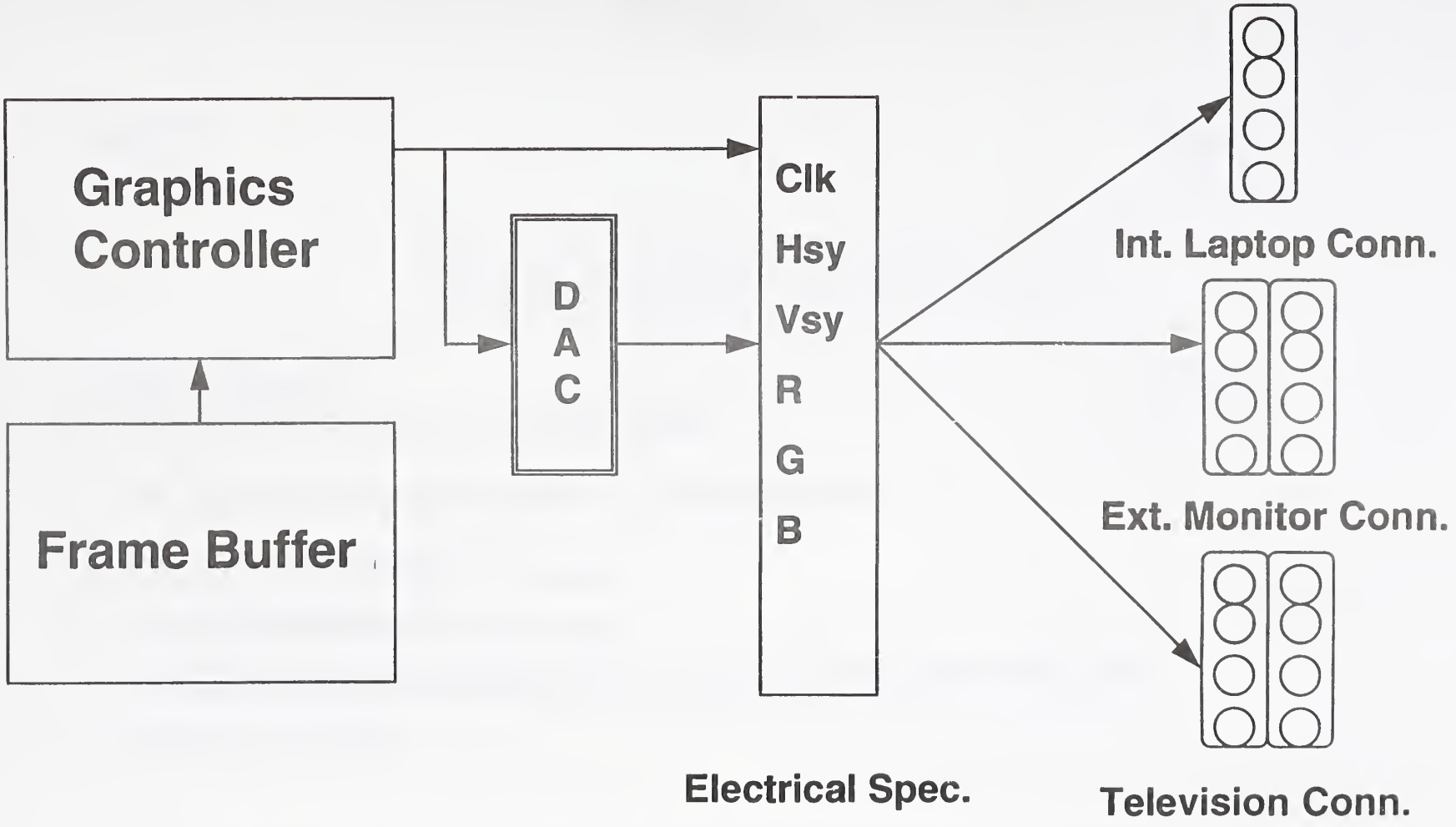
Monitors

Future Issues



Televisions

What Needs To Be Standardized



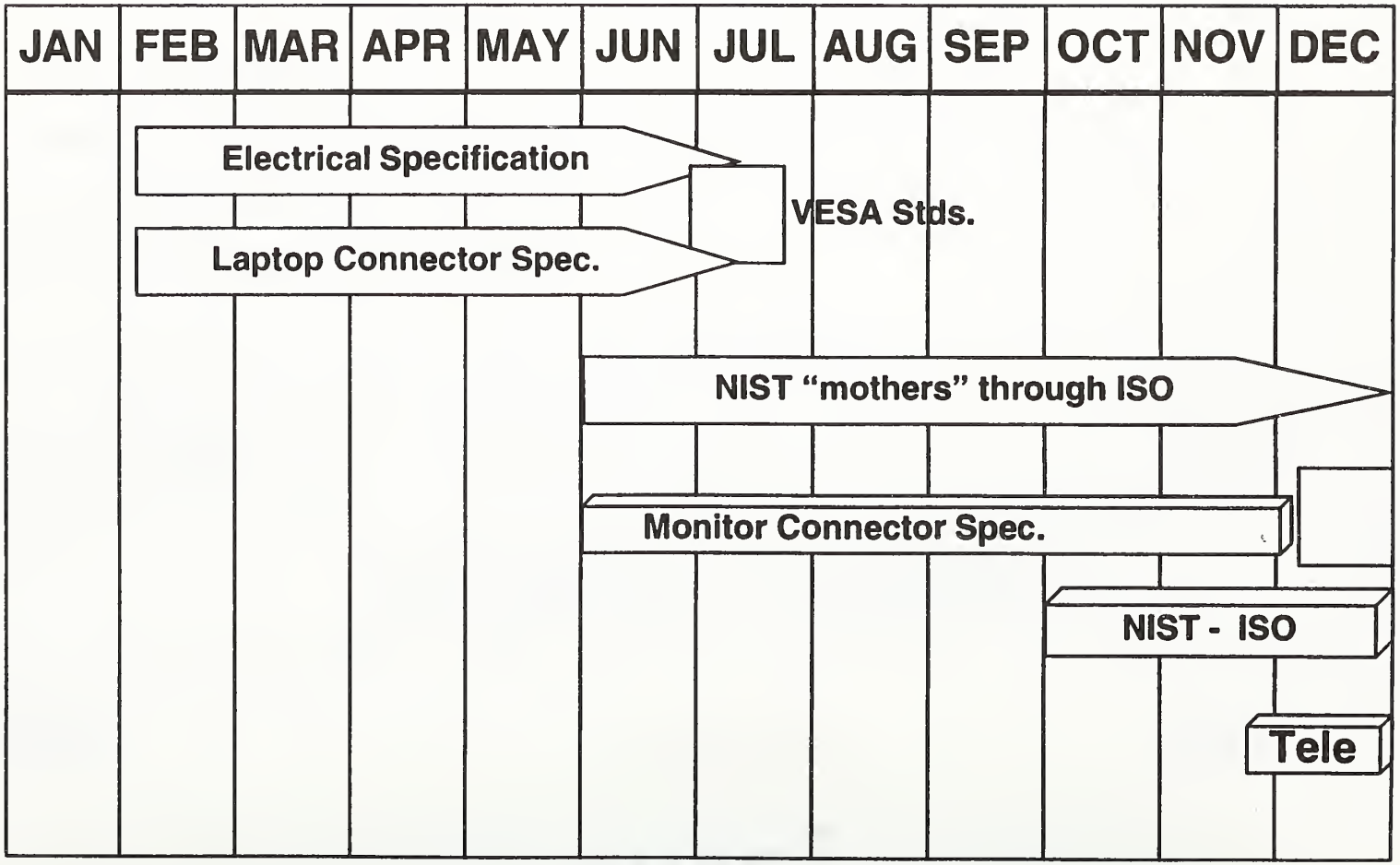
What Needs To Be Standardized

- Electrical Interface and Internal Laptop Connector
  - In Parallel
- External Monitor Connector
- Television Connector

Who...

- Correct mix of participants
- DDC, Universal Connector
- Silicon Valley location
- Time to market

Standardization Timeline



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