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Description of a CMOS Test Chip, NBS-39

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

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Description of a CMOS Test Chip, NBS-39

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Abstract

Test chip NBS-39 was designed to analyze the scaling properties of short-channel metal-oxide-semiconductor field effect transistors(MOSFETs). This report is a guide for identifying and locating each test structure included on the test chip. There is a table with each test structure identified by name, number, parameter measured, and a reference of how to perform the measurement when appropriate. The test chip can be fabricated by a junction-isolated(JI) silicon complementary metal-oxide semiconductor(CMOS) *p*-well process and by a local oxidation of silicon(LOCOS) CMOS *p*-well process. The modifications required to go from a JI-CMOS fabrication process to a LOCOS-CMOS are discussed.

Key words: CMOS; MOSFETs; p-well junction-isolated (JI) CMOS process; p-well local oxidation of silicon (LOCOS) CMOS process; scaling; short-channel; test chip; test structure.

Description

CMOS test chip NBS-39 was designed to analyze the scaling properties of short-channel MOSFETs. The test chip is shown in figure 1. The chip is divided into six subsections. Subsections labeled N-1, N-2, P-1, and P-2 contain arrrays of $n-$ and $p-$channel MOSFETS with different gate lengths and the same gate width. In addition, there are n^+ and p^+ doped polysilicon cross-bridge sheet resistor test structures with design bridge width equal to the adjacent transistor design gate length. Each structure contains probe pads in 2 x N array for electrical testing utilizing a manual probe station or a computer-controlled wafer prober. Selected transistors in each subsection are connected to the bonding pads around the periphery of the test chip. The chips can be packaged and the transistors bonded out for experiments which require that the transistor be under bias during test. Subsections labeled PP-1 and PP-2 contain process parameter test structures which can be used to characterize the process used to fabricate the transistors.

The design rules used for the layout of the test structures on the test chip had a minimum feature size of 5 μm. In selected cases, the gate length of some transistors and the bridge width of some of the cross-bridge sheet resistor test structures were smaller than the minimum feature.

The test chip can be fabricated by a junction-isolated(JI) p-well CMOS fabrication process or by a p-well LOCOS-CMOS fabrication process. Both processes use a p-well for the n-channel transistors, self-aligned polysilicon gates, and single-level metallization. The changes, although minor, apply to a particular JI process and

a particular LOCOS process and may not be applicable to other JI and LOCOS processes. The level-by-level design file for a JI-CMOS process is as follows:

1. p-well
2. p^+ guard band
3. Thick oxide opening
4. Polysilicon
5. n^+ source-drain
6. p^+ source-drain
7. Contact opening
8. Metal
9. Protective oxide overcoat.

The design file used for the JI process was converted into a CalTech Intermediate Form(CIF) file[1] with design rules compatible with a p-well LOCOS silicon foundry[2]. A list of the levels including changes to the corresponding JI levels listed in parentheses follows:

1. Active area(level 5 and 6, n^+ and p^+ source and drain implants)
2. p-well(level 1 and 2, p-well and p^+ guard band)
3. No equivalent level

4. Polysilicon

5. p^+ source-drain(level 6, p^+ source-drain)

6. The logical NOT of level 5 is used to define the n^+ source-drain regions

7. Contact opening(no change)

8. Metal(no change)

9. Passivation(no change).

Table 1 is a list of each test structure included on the test chip NBS-39. Each structure is identified by name, number, critical dimension, and the parameter measured. Test structures are identified by N followed by a number and P followed by a number according to their use to measure n-type or p-type parametrics, respectively. References to appropriate measurement techniques are provided for selected structures. For example, there is reference to the measurement of the misalignment between two conducting layers using an electrical alignment test structure[3], but there is no reference to the measurement of transistor characteristics.

Figure 2 is the key to the shading for the JI-CMOS process structures shown in the figures. Subsections N-1,N-2, P-1, and P-2 are shown in figures 3, 4, 5, and 6, respectively. An $n-$ and a $p-$channel transistor are shown in figures 7 and 8, respectively. The transistors are representative of the other transistors in the N- and P- subsections. The differences are only in the polysilicon gate length noted in Table 1. From left to right in subsection N-1, transistors with gate lengths of 8, 4,

and 1.25 μm and in subsection N-2 transistors with gate lengths of 3.5, 3.0, and 1.0 μm are connected to the bonding pads around the periphery of the test chip. From right to left in the P-1 and P-2 subsections, transistors with gate lengths of 8, 4, and 1.25 μm and 3.5, 3.0, and 1.0 μm, respectively, are connected to the bonding pads around the periphery.

In subsections N-1 and N-2, the polysilicon cross-bridge sheet resistor test structures are doped with the n^+ source-drain implant n^+ doped and in P-1 and P-2 subsections they are doped with the p^+ source drain implant. Representative n^+ and p^+ doped polysilicon cross-bridge sheet resistor test structures are shown in figures 9 and 10. The width of the bridge of the sheet resistor is designed to be equal to the gate length of the adjacent MOSFET. The gate dimensions are found in Table 1.

Process parameter test structures which address properties of n −channel devices are labeled N59-N69 and those that address properties of p −channel devices are labeled P57-P68. These structures are grouped into subsections PP-1 and PP-2 and are shown in figures 11 and 12. In subsections PP-1 and PP-2, there are test structures to be used to measure contact resistance[4] (fig. 13); MOS capacitors (fig. 14) to be used to measure gate oxide properties and interface trapped charge(ITC); cross-bridge sheet resistors[5] (fig. 9) to be used to measure the sheet resistance of the various conducting layers used to fabricate devices and circuits; and electrical alignment resistors[8] to be used to measure the misalignment between a contact window and a conducting layer (fig. 15). There are metal gate $n-$ and p −channel transistors to be used for characterizing the field oxide (fig. 16) and the intermediate field oxide (fig. 17). The large area structures N61 (fig. 18), and P61 are for secondary

ion mass spectroscopy(SIMS) profiling of the sources and drains in the $p-$ and $n-$ channel transistors. A NAND, a NOR, and four experimental structures, dual-gated diodes and split cross-bridge sheet resistors are included, but are not illustrated or discussed.

Acknowledgments

The author would like to acknowledge all of the members of the staff of the Semiconductor Devices and Circuits Division for their contributions to the design of the CMOS Test Chip NBS-39. In particular, the author would like to thank C. L. Wilson, K. F. Galloway and L. W. Linholm for their reading of the manuscript and their useful suggestions and E. J. Walters for preparing the manuscript.

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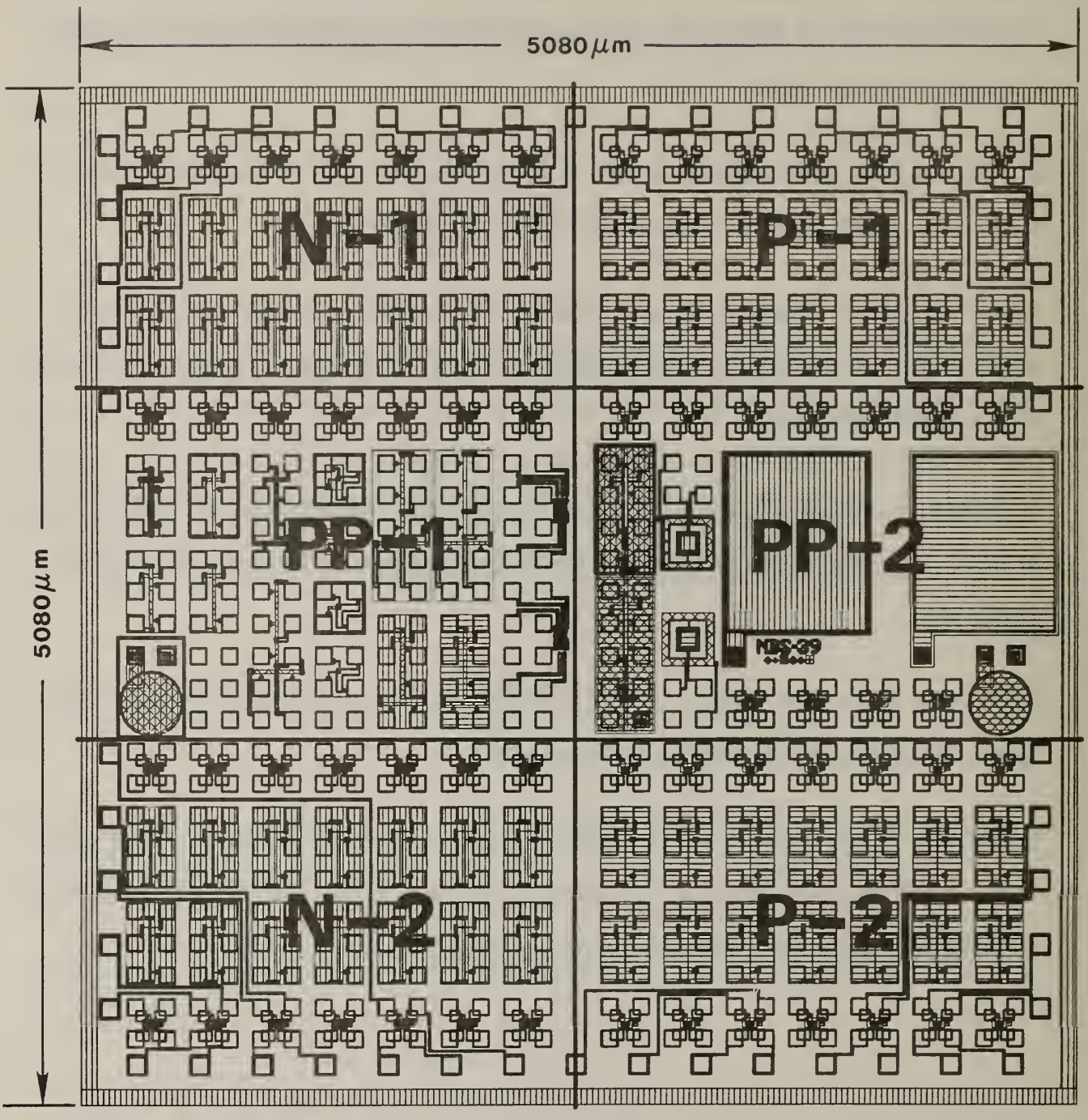

Figure 1. The CMOS Test Chip NBS-39 is shown with its six subsections labeled N-1, N-2, P-1, P-2, PP-1, and PP-2.

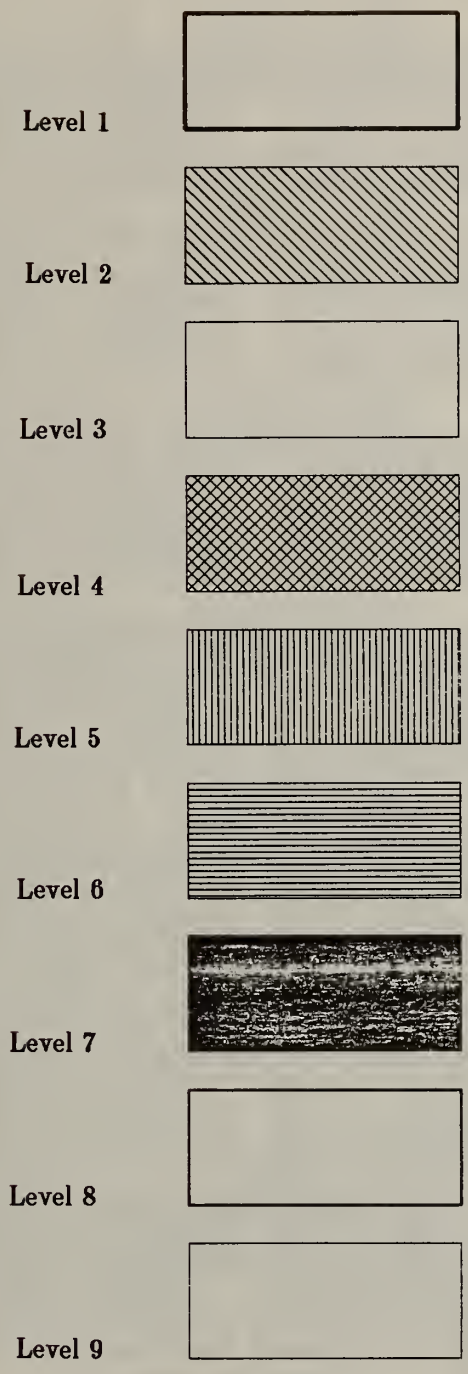

Figure 2. The key to the shading in figures for the JI-CMOS process.

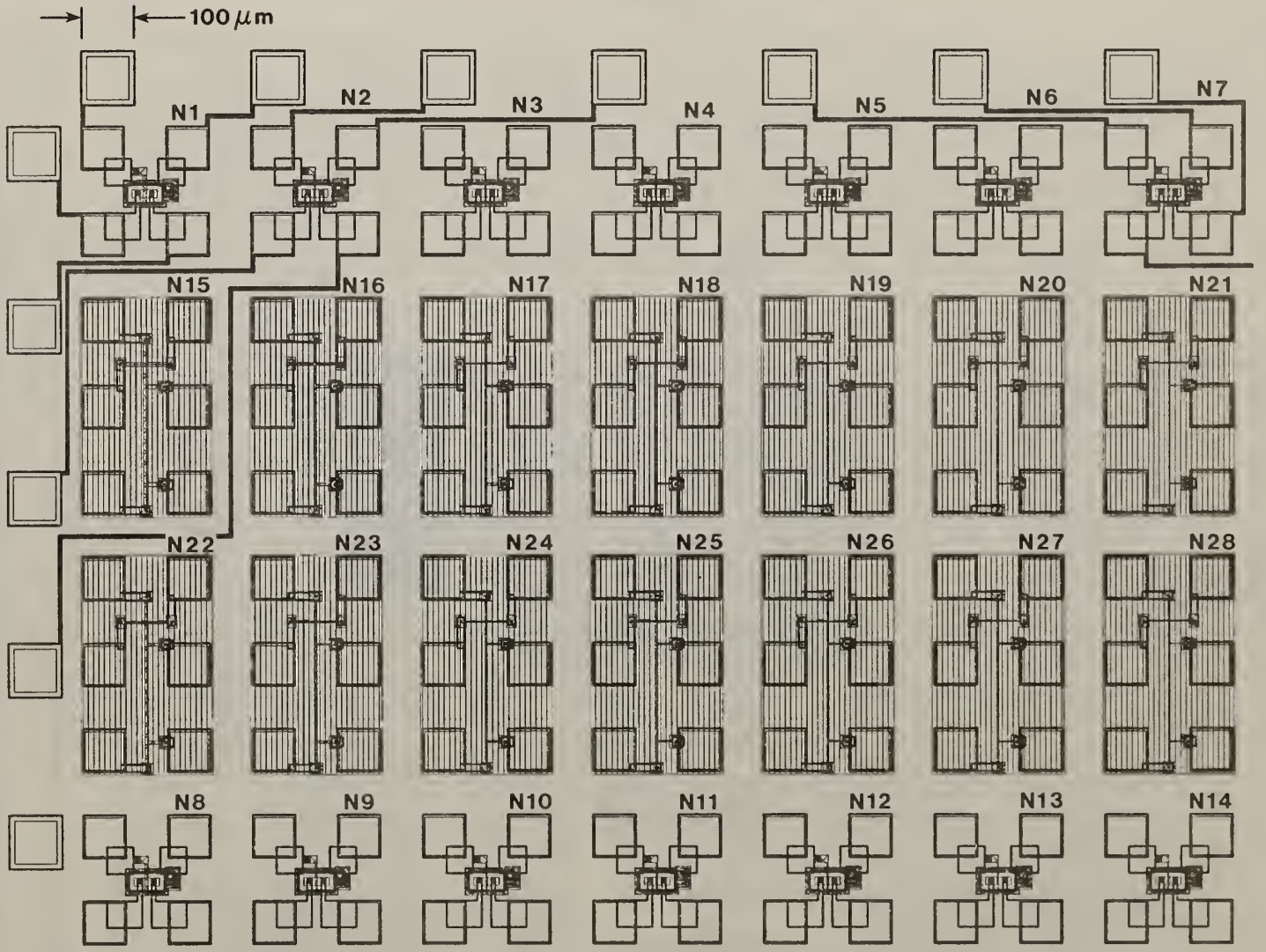

Figure 3. Subsection N-1 contains arrays of n –channel MOSFETs and n^+ doped polysilicon cross-bridge sheet resistors. The test structures are numbered and critical dimensions noted in Table 1.

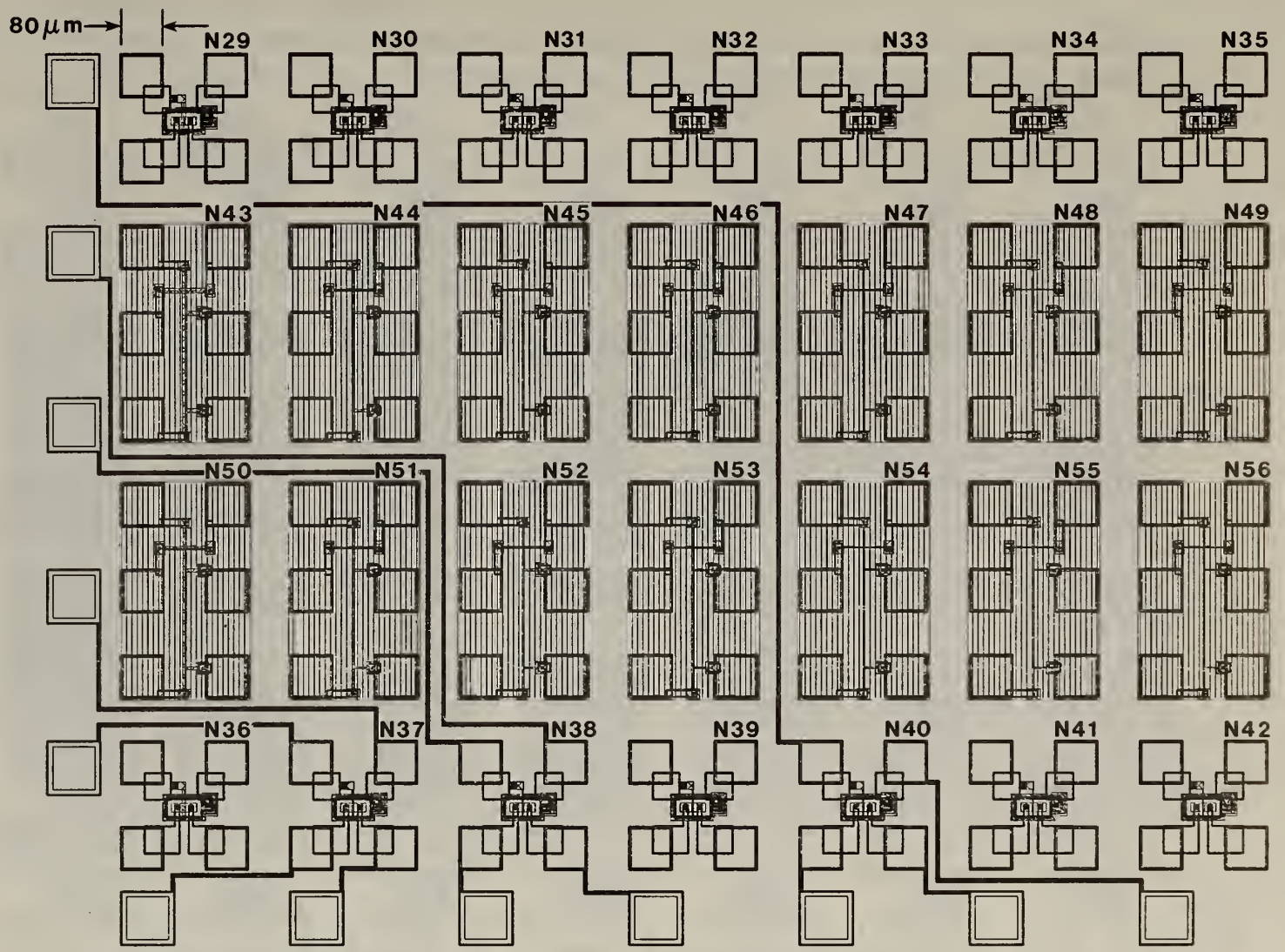

Figure 4. Subsection N-2 contains arrays of n –channel MOSFETs and n^+ doped polysilicon cross-bridge sheet resistors. The test structures are numbered and critical dimensions noted in Table 1.

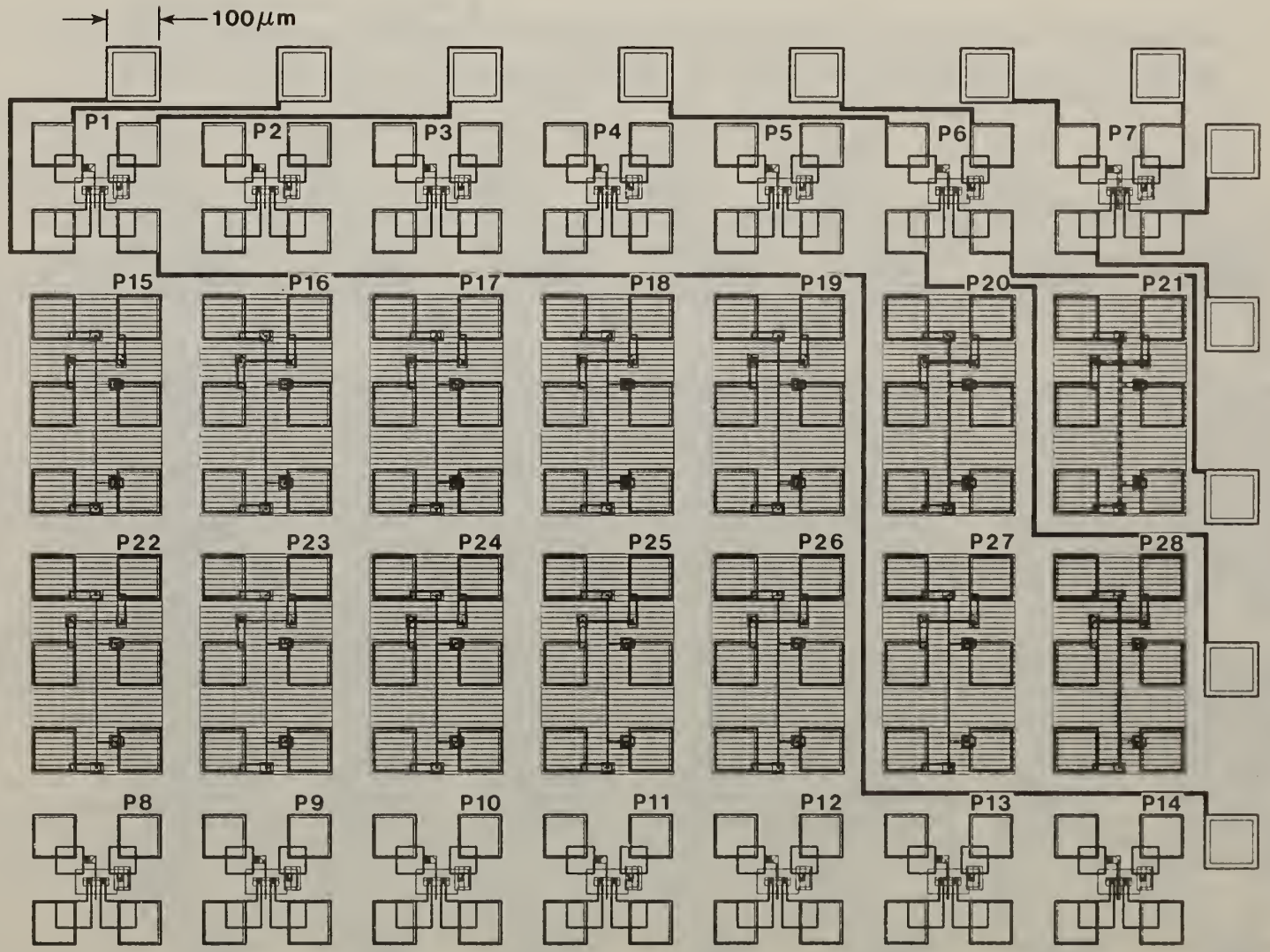

Figure 5. Subsection P-1 contains arrays of p −channel MOSFETs and p^+ doped polysilicon cross-bridge sheet resistors. The test structures are numbered and critical dimensions noted in Table 1.

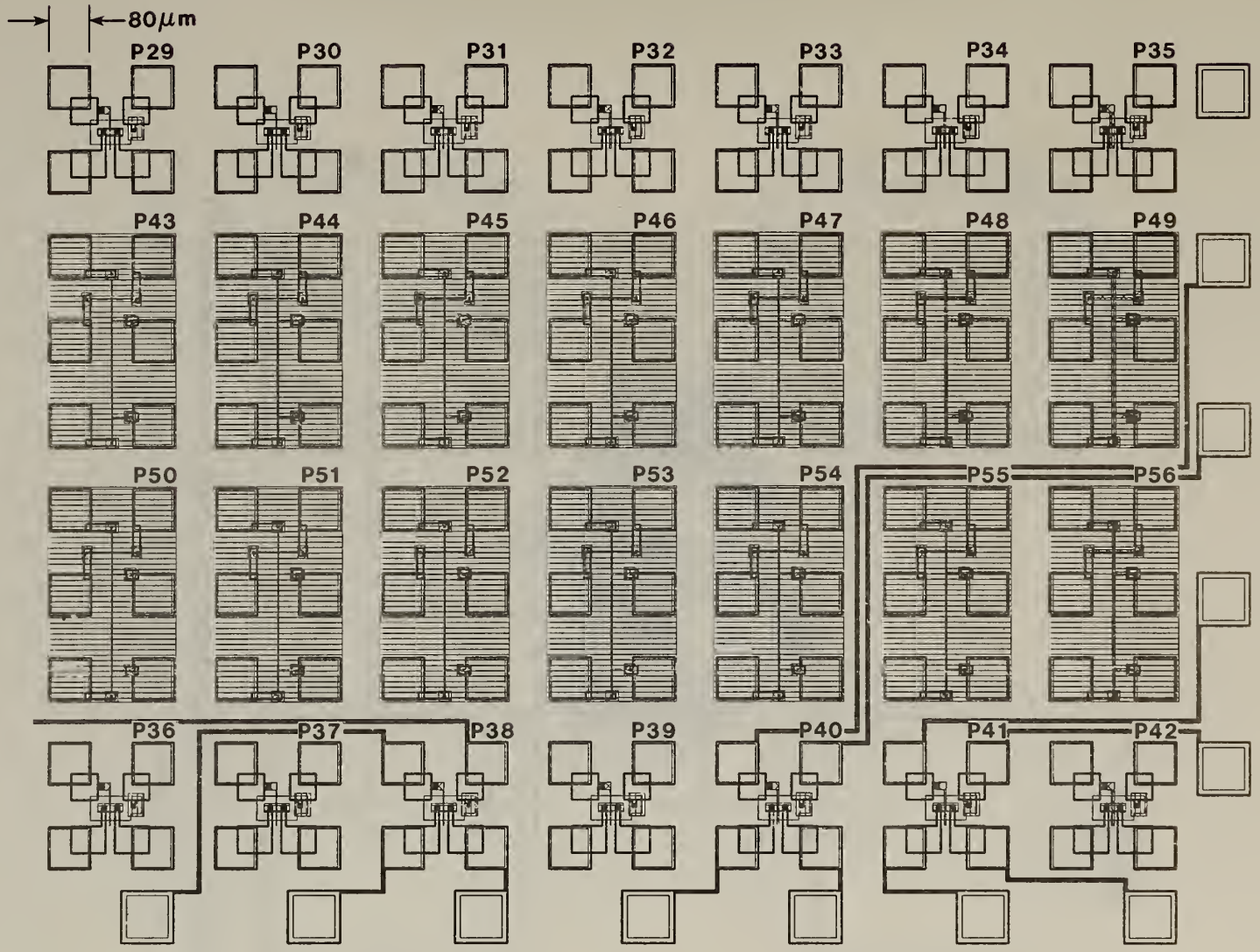

Figure 6. Subsection P-2 contains arrays of p −channel MOSFETs and p^+ doped polysilicon cross-bridge sheet resistors. The test structures are numbered and critical dimensions noted in Table 1.

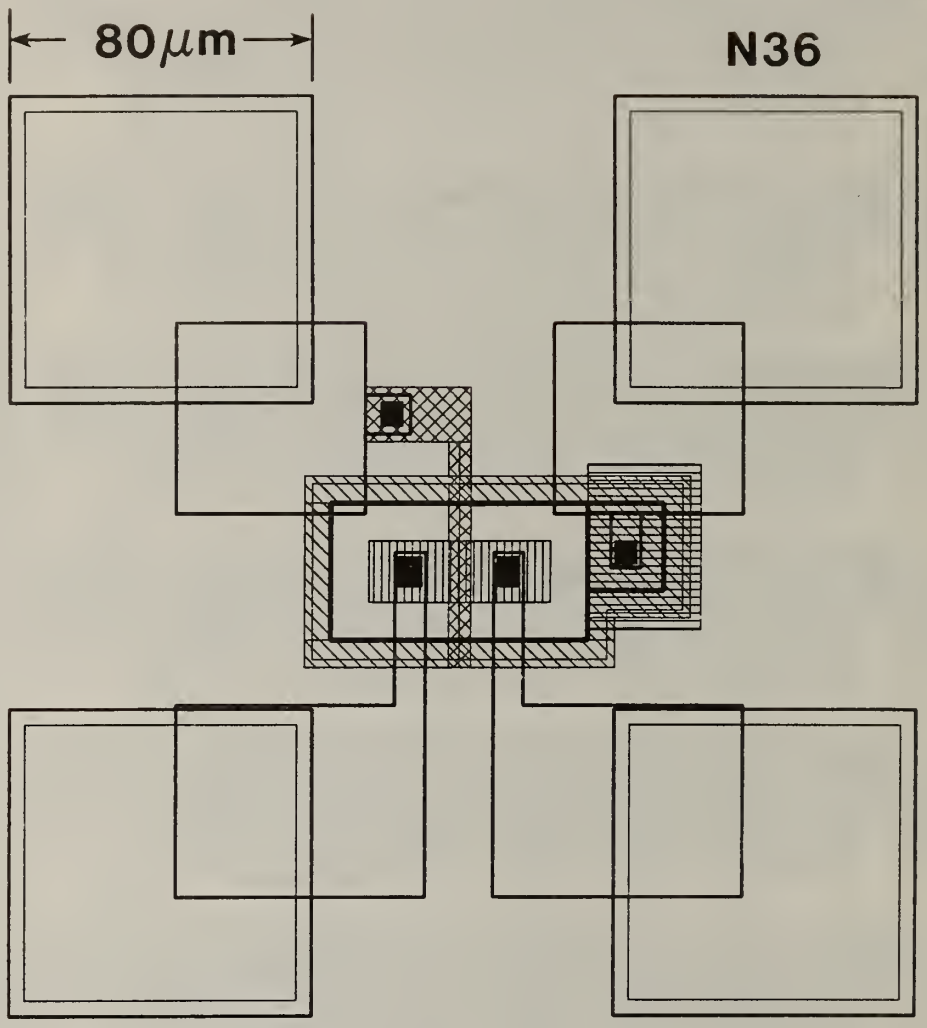

Figure 7. An n—channel MOSFET, N36, from subsection N-1.

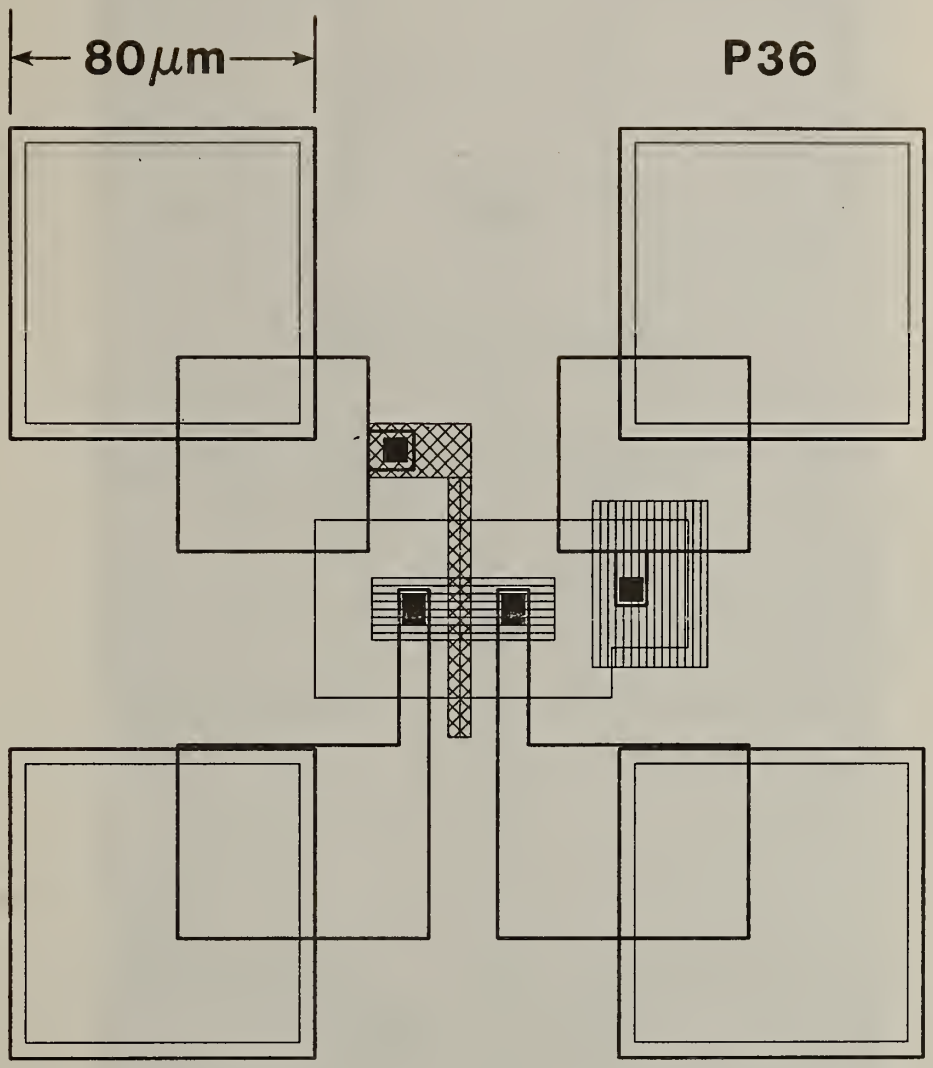

Figure 8. A *p*—channel MOSFET, P36, from subsection P-1.

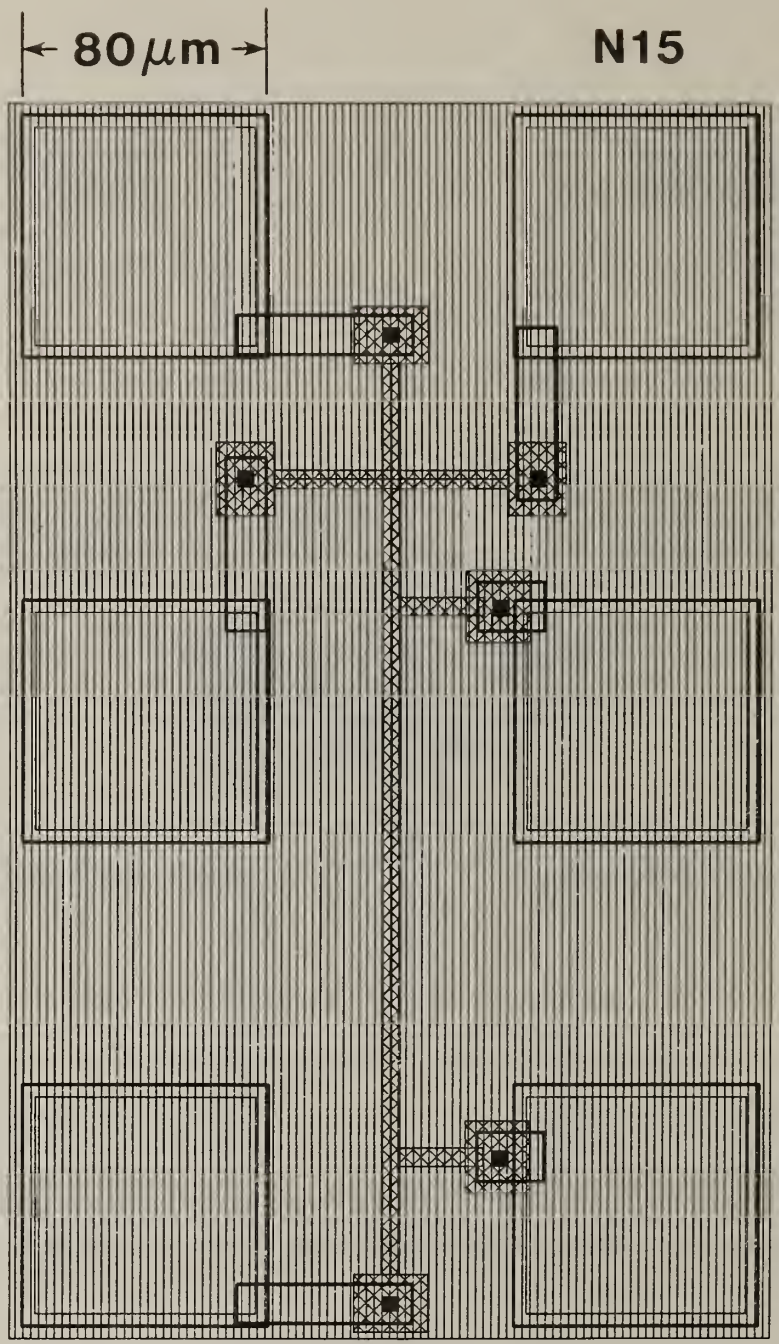

Figure 9. An n^+ doped polysilicon cross-bridge sheet resistor test structure, N15, from subsection N-1.

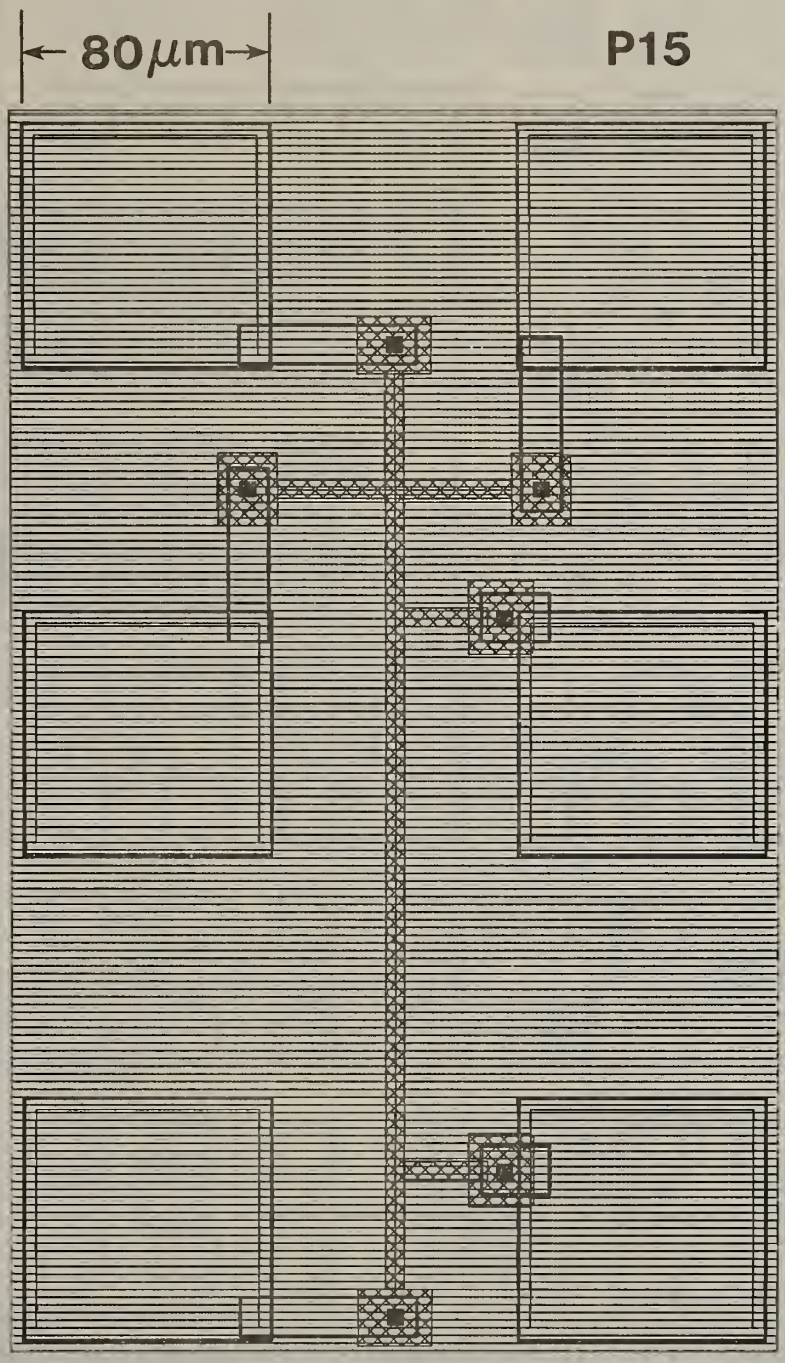

Figure 10. A p^+ doped polysilicon cross-bridge sheet resistor test structure, P15, from subsection P-1.

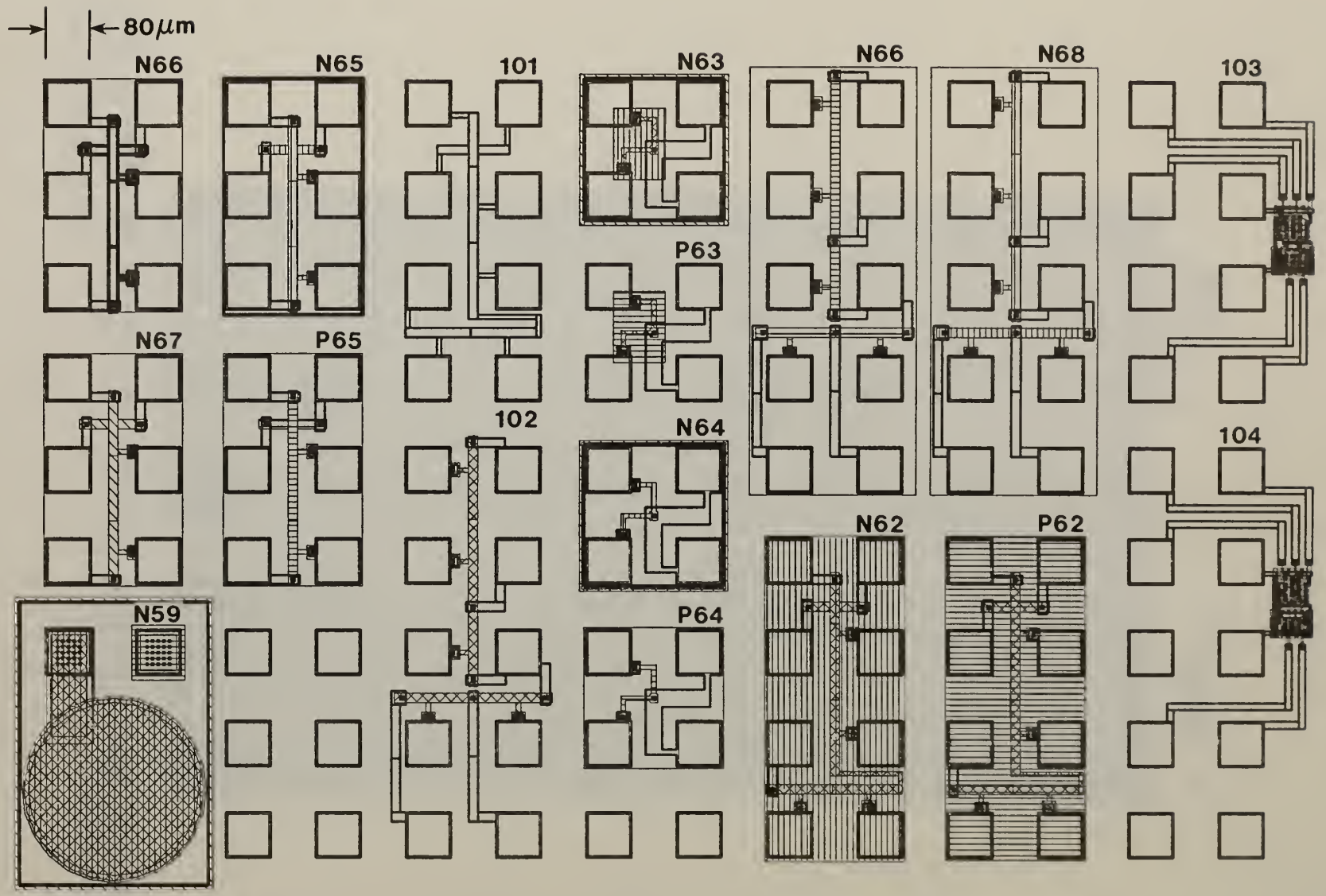

Figure 11. The subsection PP-1 contains process parameter test structures. The test structures are numbered and described in Table 1.

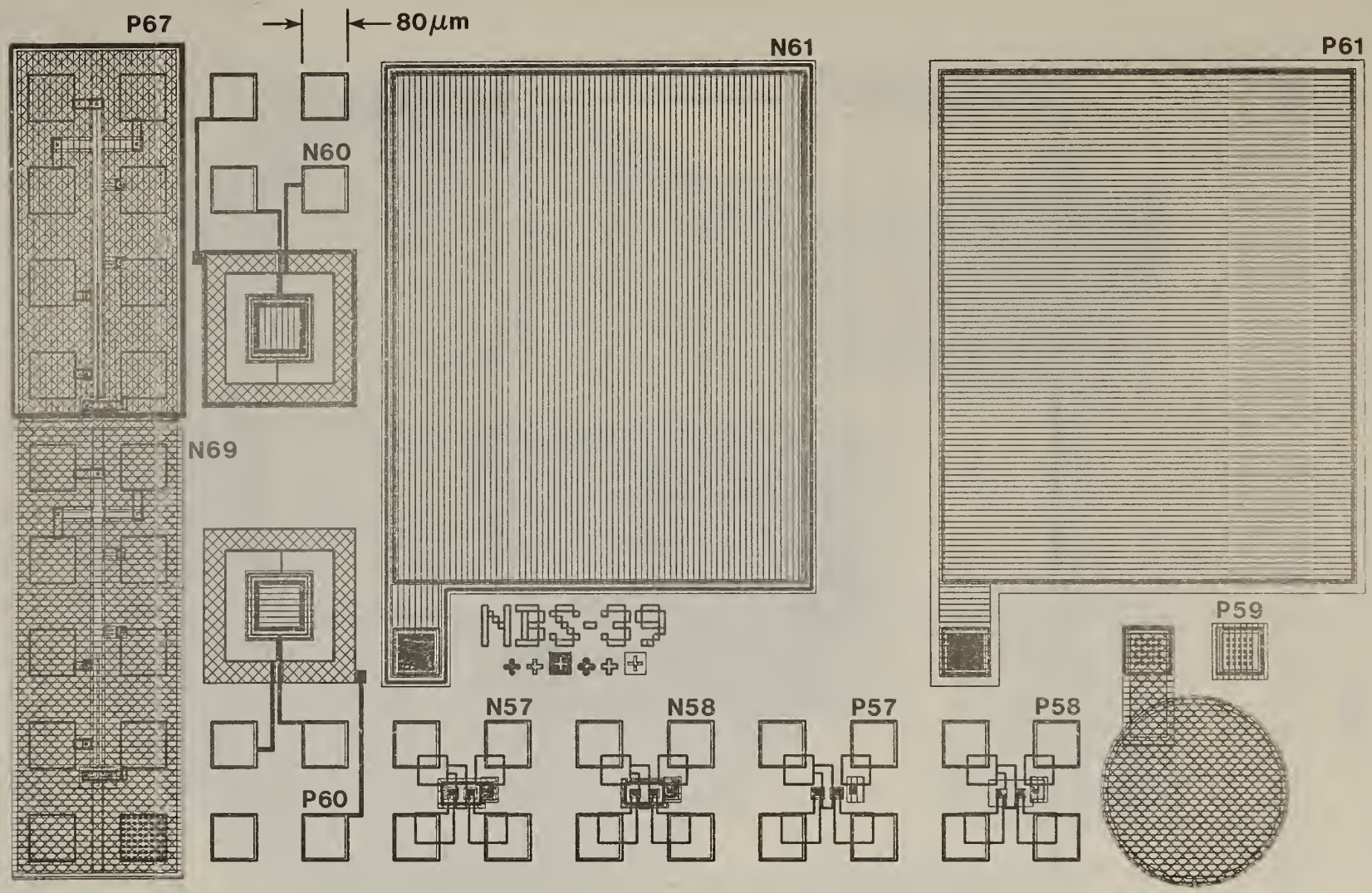

Figure 12. The subsection PP-2 contains process parameter test structures. The test structures are numbered and described in Table 1.

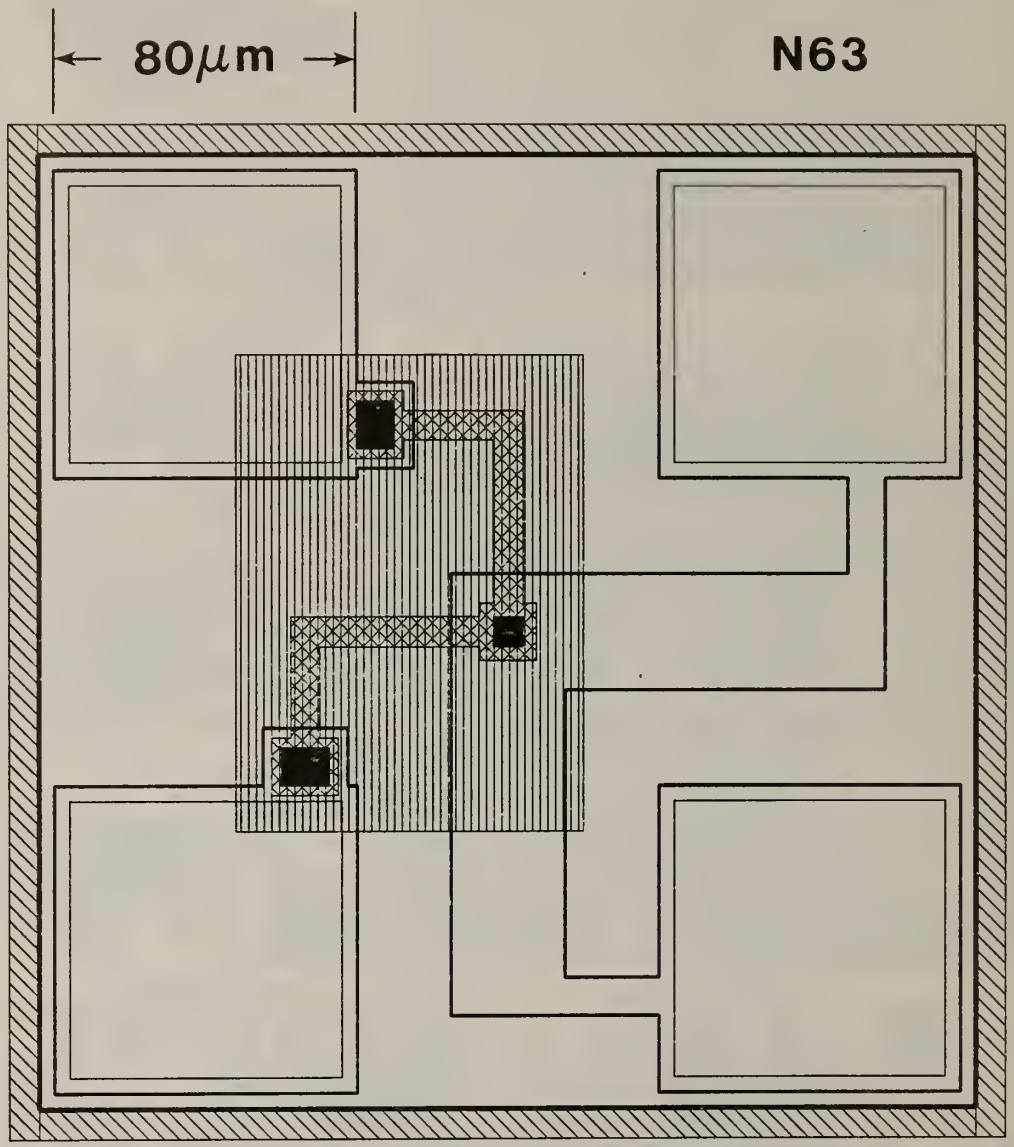

Figure 13. A contact resistor test structure, N63, from subsection PP-1.

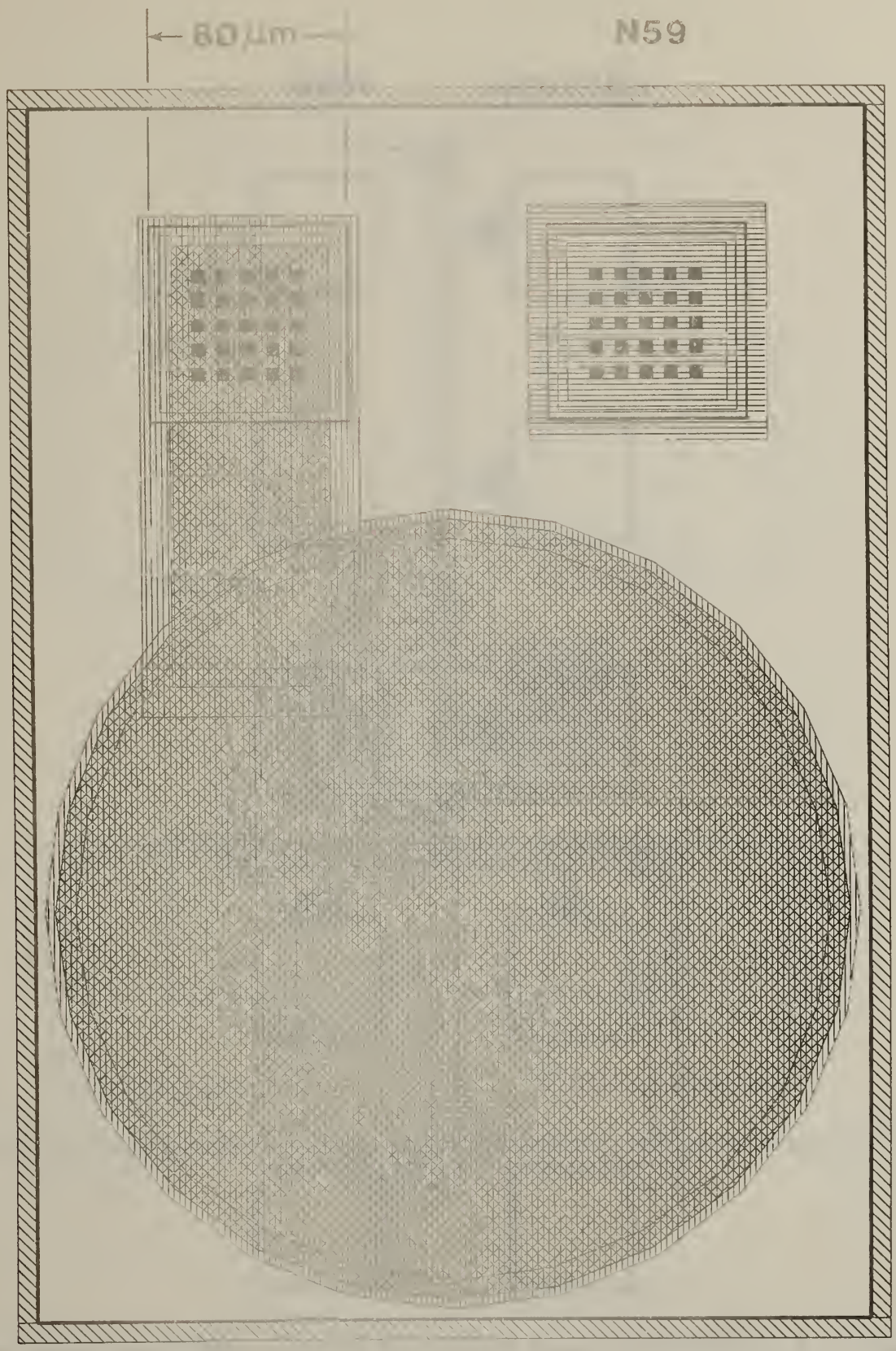

Figure 14. An MOS capacitor test structure, N59, from subsection PP-1.

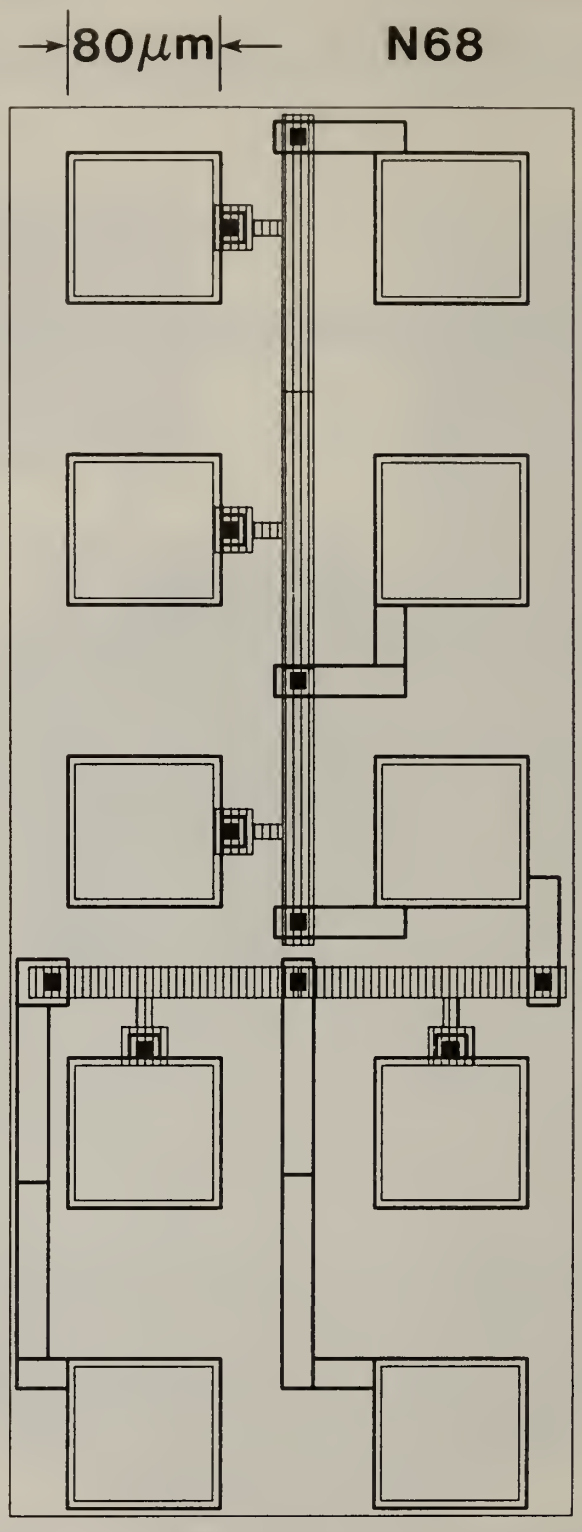

Figure 15. An electrical alignment resistor test structure, N68, from subsection PP-1.

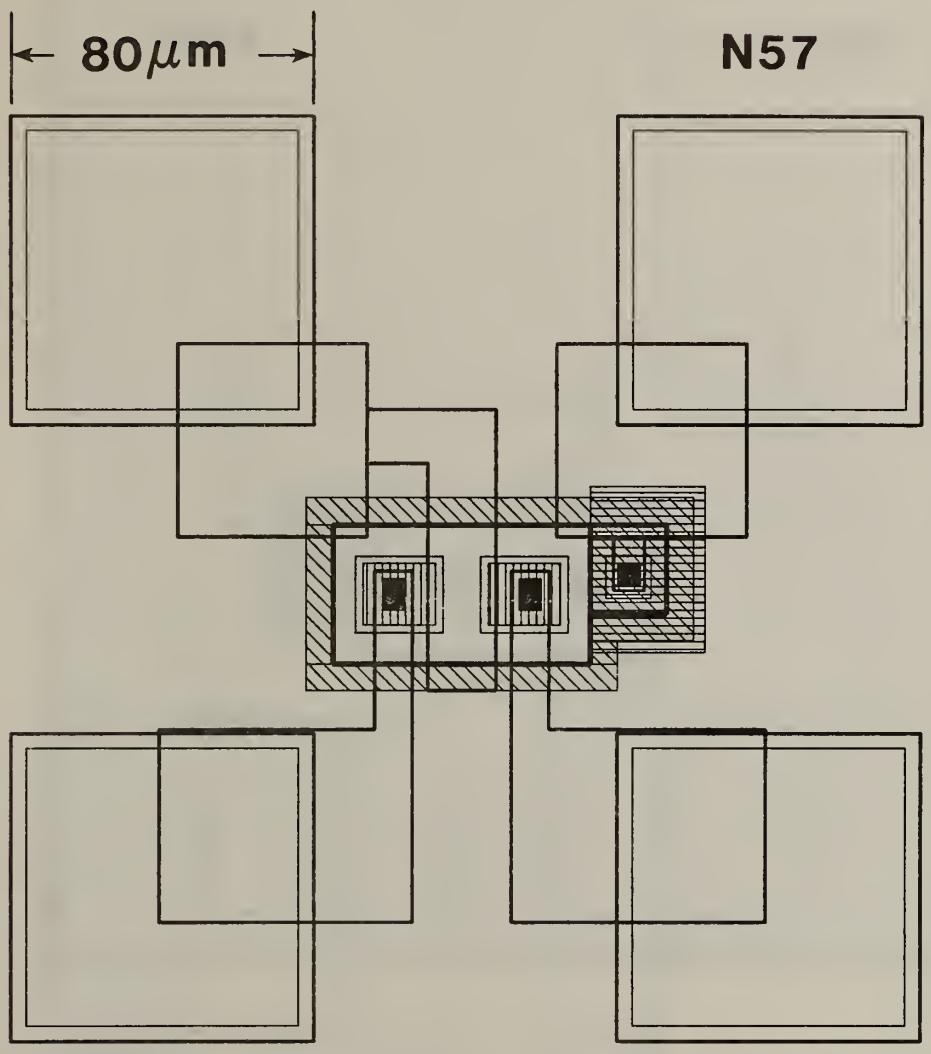

Figure 16. A metal gate field oxide n—channel MOSFET, N57, from subsection PP-2.

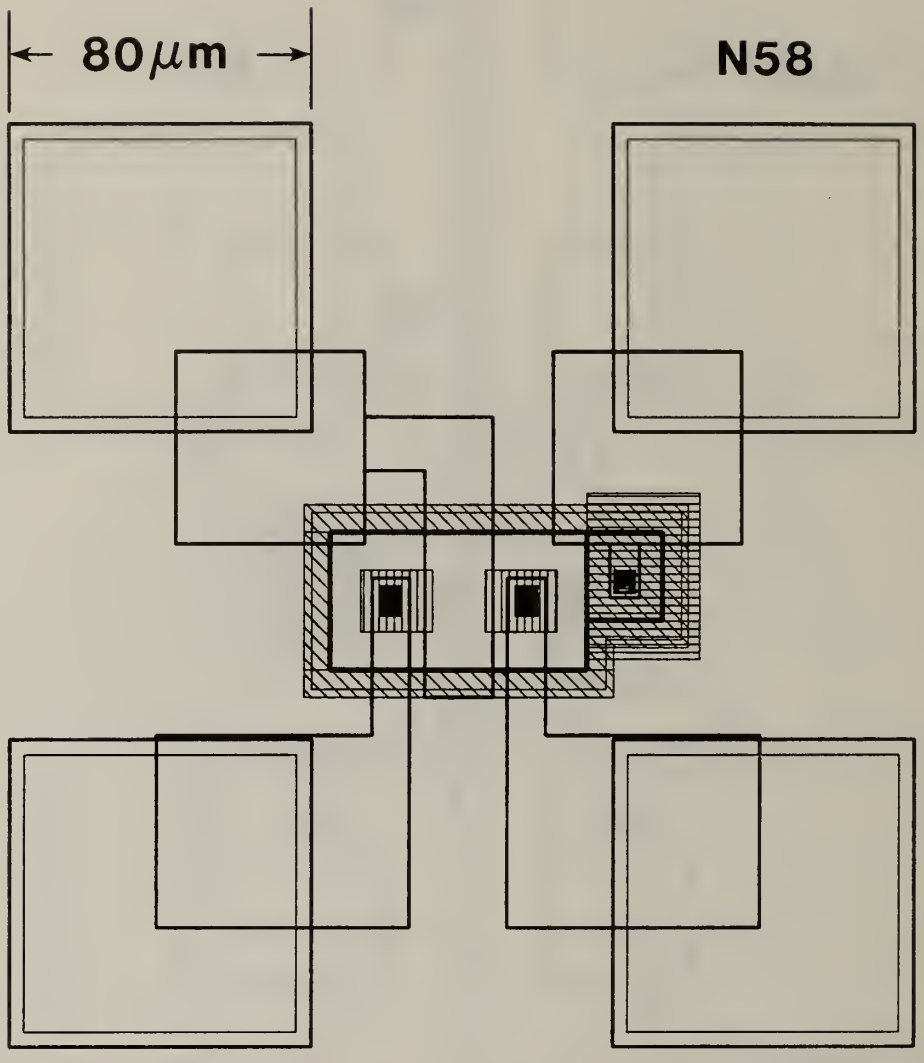

Figure 17. A metal gate intermediate oxide n—channel MOSFET, N58, from subsection PP-2.

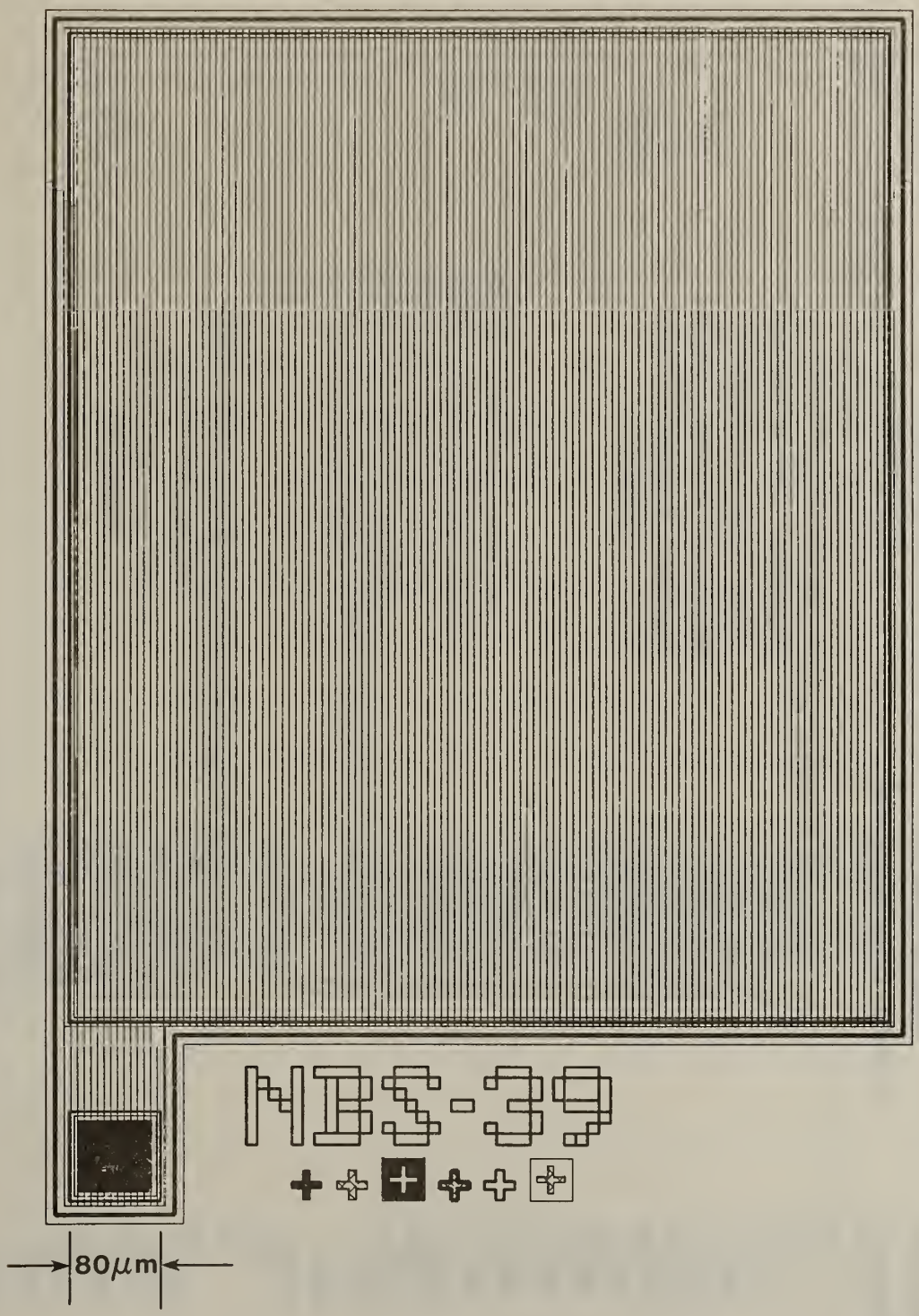

Figure 18. An n^+ secondary ion mass spectroscopy(SIMS) profiling target, N61, from subsection PP-2.

Table 1. Test Structure List for CMOS Test Chip NBS-39

Structure Number	Test Structure Critical Dimension(μm)	Parameter Measured	Reference
	n −Channel Polysilicon Gate MOSFETs(W=16)		
N1	(L=8.00)	Transistor Characteristics,	
N2	(L=4.00)	Gate Oxide Parameters,	
N3	(L=3.25)	Electrical Channel Length,	[6]
N4	(L=2.75)	Interface Trapped Charge	
N5	(L=2.25)	Density	[7,8]
N6	(L=1.75)		
N7	(L=1.25)		
N8	(L=6.00)		
N9	(L=3.50)		
N10	(L=3.00)		
N11	(L=2.50)		
N12	(L=2.00)		
N13	(L=1.50)		
N14	(L=1.00)		
	n^+ −Polysilicon Cross-Bridge Sheet Resistors(L=182)		
N15	(W=8.00)	Polysilicon Sheet	
N16	(W=4.00)	Resistance and Bridge	
N17	(W=3.25)	Width,W	[5]
N18	(W=2.75)		
N19	(W=2.25)		
N20	(W=1.75)		
N21	(W=1.25)		

Structure Number	Test Structure Critical Dimension(μm)	Parameter Measured	Reference
N22	(W=6.00)		
N23	(W=3.50)		
N24	(W=3.00)		
N25	(W=2.50)		
N26	(W=2.00)		
N27	(W=1.50)		
N28	(W=1.00)		
	n –Channel Polysilicon Gate MOSFETs(W=16)		
N29	(L=8.00)	Transistor Characteristics	
N30	(L=4.00)	Gate Oxide Parameters,	
N31	(L=3.25)	Electrical Channel Length,	[6]
N32	(L=2.75)	Interface Trapped Charge	
N33	(L=2.25)	Density	[7,8]
N34	(L=1.75)		
N35	(L=1.25)		
N36	(L=6.00)		
N37	(L=3.50)		
N38	(L=3.00)		
N39	(L=2.50)		
N40	(L=2.00)		
N41	(L=1.50)		
N42	(L=1.00)		
	n^+ –Polysilicon Cross-Bridge Sheet Resistors(L=182)		
N43	(W=8.00)	Polysilicon Sheet	

Structure Number	Test Structure Critical Dimension(μm)	Parameter Measured	Reference
N44	(W=4.00)	Resistance and Bridge	
N45	(W=3.25)	Width,W	[5]
N46	(W=2.75)		
N47	(W=2.25)		
N48	(W=1.75)		
N49	(W=1.25)		
N50	(W=6.00)		
N51	(W=3.50)		
N52	(W=3.00)		
N53	(W=2.50)		
N54	(W=2.00)		
N55	(W=1.50)		
N56	(W=1.00)		
	n −Channel Metal Gate MOSFETs(W=16)		
N57	(L=18)	Field Oxide	
N58	(L=18)	Intermediate Oxide	
	Process Parameters		
N59	MOS Capacitor(p−Well, Gate Oxide)		
N60	Dual Gate-Gated Diode		
N61	n^+ SIMS Target		
N62	Polysilicon Cross-Orthogonal Bridge Resistor(W=16, L_y=176, L_x=122)		[5]
N63	n^+ Polysilicon-to-Metal Contact Resistor(8x8)		[4]
N64	Metal-to-p^+ Contact Resistor(8x8)		[4]
N65	n^+ Source/Drain Cross-Bridge Sheet Resistor(W=16, L=176)		[5]

Structure Number	Test Structure Critical Dimension(μm)	Parameter Measured	Reference
N66	p-Well Cross-Bridge Sheet Resistor(W=16, L=176)		[5]
N67	p^{++} Guard-Band Cross-Bridge Sheet Resistor(W=16, L=176)		[5]
N68	Contact-n^+ Source/Drain Alignment Resistor(L=160)		[3]
N69	Cross-Split Bridge Sheet Resistor		
	p −Channel Polysilicon Gate MOSFETs(W=16)		
P1	(L=8.00)	Transistor Characteristics,	
P2	(L=4.00)	Gate Oxide Parameters,	
P3	(L=3.25)	Electrical Channel Length,	[6]
P4	(L=2.75)	Interface Trapped Charge	
P5	(L=2.25)	Density	[7,8]
P6	(L=1.75)		
P7	(L=1.25)		
P8	(L=6.00)		
P9	(L=3.50)		
P10	(L=3.00)		
P11	(L=2.50)		
P12	(L=2.00)		
P13	(L=1.50)		
P14	(L=1.00)		
	p^+ −Polysilicon Cross-Bridge Sheet Resistors(L=182)		
P15	(W=8.00)	Polysilicon Sheet	
P16	(W=4.00)	Resistance and Bridge	
P17	(W=3.25)	Width,W	[5]
P18	(W=2.75)		
P19	(W=2.25)		

Structure Number	Test Structure Critical Dimension(μm)	Parameter Measured	Reference
P20	(W=1.75)		
P21	(W=1.25)		
P22	(W=6.00)		
P23	(W=3.50)		
P24	(W=3.00)		
P25	(W=2.50)		
P26	(W=2.00)		
	p −Channel Polysilicon Gate MOSFETs(W=16)		
P27	(W=1.50)		
P28	(W=1.00)		
P29	(L=8.00)	Transistor Characteristics	
P30	(L=4.00)	Gate Oxide Parameters,	
P31	(L=3.25)	Electrical Channel Length,	[6]
P32	(L=2.75)	Interface Trapped Charge	
P33	(L=2.25)	Density	[7,8]
P34	(L=1.75)		
P35	(L=1.25)		
P36	(L=6.00)		
P37	(L=3.50)		
P38	(L=3.00)		
P39	(L=2.50)		
P40	(L=2.00)		
P41	(L=1.50)		
P42	(L=1.00)		

Structure Number	Test Structure Critical Dimension(μm)	Parameter Measured	Reference
	p^+ –Polysilicon Cross-Bridge Sheet Resistors(L=182)		
P43	(W=8.00)	Polysilicon Sheet	
P44	(W=4.00)	Resistance and Bridge	
P45	(W=3.25)	Width,W	[5]
P46	(W=2.75)		
P47	(W=2.25)		
P48	(W=1.75)		
P49	(W=1.25)		
P50	(W=6.00)		
P51	(W=3.50)		
P52	(W=3.00)		
P53	(W=2.50)		
P54	(W=2.00)		
P55	(W=1.50)		
P56	(W=1.00)		
	p –Channel Metal Gate MOSFETs(W=16)		
P57	(L=18)	Field Oxide	
P58	(L=18)	Intermediate Oxide	
	Process Parameters		
P59	MOS Capacitor(n–Substrate, Gate Oxide)		
P60	Dual Gate-Gated Diode		
P61	p^+ SIMS Target		
P62	Polysilicon Cross-Orthogonal Bridge Resistor(W=16, L_y=176, L_x=122)		[5]
P63	p^+ Polysilicon-to-Metal Contact Resistor(8x8)		[4]

Structure Number	Test Structure Critical Dimension(μm)	Parameter Measured	Reference
P64	Metal-to-p^+ Source/Drain Contact Resistor(8x8)		[4]
P65	p^+ Source/Drain Cross-Bridge Sheet Resistor(W=16, L=176)		[5]
P66	p-Well Cross-Bridge Sheet Resistor(W=16, L=176)		[5]
P67	Contact-p^+ Source/Drain Alignment Resistor(L=160)		[3]
P68	Cross-Split Bridge Sheet Resistor		
101	Metal Cross-Orthogonal Bridge Sheet Resistor(W=16, L_y=L_x=120)		[5]
102	Metal-to-Polysilicon Alignment Resistor(L=160)		[3]
103	NAND Gate		
104	NOR Gate		

NBS-114A (REV. 2-8C)

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T. J. Russell

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)*

Test chip NBS-39 was designed to analyze the scaling properties of short-channel metal-oxide-semiconductor field effect transistors (MOSFETs). This report is a guide for identifying and locating each test structure included on the test chip. There is a table with each test structure identified by name, number, parameter measured, and a reference of how to perform the measurement when appropriate. The test chip can be fabricated by a junction-isolated (JI) silicon complementary metal-oxide semiconductor (CMOS) p-well process and by a local oxidation of silicon (LOCOS) CMOS p-well process. The modifications required to go from a JI-CMOS fabrication process to a LOCOS-CMOS are discussed.

12. KEY WORDS *(Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)*

CMOS; MOSFETs; p-well junction-isolated (JI) CMOS process; p-well local oxidation of silicon (LOCOS) CMOS process; scaling; short-channel; test chip; test structure.

13. AVAILABILITY

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