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Semiconductor Measurement Technology

Thermal Resistance Measurements on Power Transistors

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Semiconductor Measurement Technology:

Thermal Resistance Measurements on Power Transistors

Sherwin Rubin and Frank F. Oettinger

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, DC 20234

U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, Secretary

Jordan J. Baruch, Assistant Secretary for Science and Technology

NATIONAL BUREAU OF STANDARDS, Ernest Ambler, Director

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PREFACE

This study, which resulted in a recommended procedure for measuring the thermal resistance of power transistors, was conducted as part of the Semiconductor Technology Program in the Electron Devices Division of the National Bureau of Standards (NBS). This Program serves to focus NBS research to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. This research leads to the development of carefully evaluated and well-documented test procedures and associated technology. Special emphasis is placed on the dissemination of the results of the research to the electronics community. Application of these results by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. Improved measurement technology provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement and, in addition, provides a basis for controlled improvements in fabrication processes and in essential device characteristics. The Semiconductor Technology Program is carried out with funds from a multiplicity of sponsoring agencies; the specific work reported herein was funded by NBS.

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DISCLAIMER

Certain commercial equipment, instruments, or materials are identified in this report in order to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Semiconductor Measurement Technology:

Thermal Resistance Measurements on Power Transistors

by

Sherwin Rubin and Frank F. Oettinger

Abstract: A brief description of the idealized concept of thermal resistance is given along with the problems and pitfalls encountered in applying the concept to power transistors. In addition, the advantages and disadvantages of various electrical techniques for measuring junction temperature (thermal resistance) are described, and a preferred, standard technique is discussed in detail. This preferred technique, in which the forward-biased emitter-base junction is used as the temperature-sensitive parameter, is usable on all types of bipolar transistors. The measurement procedure is relatively simple and lends itself to industrial measurements as well as for referee purposes. The power interruption circuitry is also relatively fast and simple since only one device terminal is switched. The preferred technique that was developed for measuring the thermal resistance of power transistors has been adopted as EIA Recommended Standard RS-313-B on Thermal Resistance Measurements of Conduction Cooled Power Transistors, dated October 1975.

Key Words: Current crowding; die attachment evaluation; junction temperature; measurement technology; power transistors; semiconductor devices; thermal characterization; thermal resistance; transistors.

1. Introduction

The thermal characterization of power semiconductor devices is important for predicting the reliability and performance of these devices and for ensuring their safe operation. Manufacturers usually specify a thermal resistance, R_θ, and a maximum safe junction temperature, $T_{J(max)}$. The specified thermal resistance is assumed to be constant for each device and is used to calculate the device junction temperature as a function of power dissipation for a given mounting arrangement and case or ambient temperature. Ultimately, R_θ is used to ensure that $T_{J(max)}$ is not exceeded during operation. The effect of exceeding the rated maximum safe junction temperature can range from a change in the electrical characteristics of the device to catastrophic failure. Thus, a knowledge of the operating junction temperature is critical for predicting device quality, reliability, and performance. For speed and simplicity of production line screening and to enable device users to duplicate the measurements, electrical measurement methods are usually used for determining device thermal resistance. However, there are problems with this ap-

proach that had been brought to our attention by industrial standards organizations, manufacturers and users of devices, and military and space agencies. Measurements were not repeatable within the desired precision due to the use of different test procedures and device operating conditions. The effect of current crowding on the accuracy of the electrical measurement of thermal resistance was not widely understood. This led to buyer-seller disagreements and in some cases to failure through misuse.

On the recommendation of these semiconductor manufacturers and users and of other government agencies, the National Bureau of Standards initiated a study of methods for nondestructively measuring the thermal resistance of power transistors in order to develop a satisfactory referee test method. Based on the criteria that the method must be easy to perform, precise, nondestructive, as accurate as possible, and usable at the working level, the emitter-only switching technique (in which the forward-biased emitter-base junction is used as the temperature-sensitive parameter) was found to be the preferred procedure for measuring the thermal resistance of power transistors.

This paper discusses the concept of thermal resistance, its shortcomings, and the care that must be exercised when it is used for specifying or checking the thermal characteristics of a device. Electrical techniques for measuring junction temperature (thermal resistance) of power transistors are discussed in some detail with the emphasis on the preferred method, now adopted as a standard technique [1] (reprinted with permission of EIA in Appendix I).

2. The Concept of Thermal Resistance

Thermal resistance has been used over the years as an aid to device manufacturers and users for calculating the junction temperature of operating devices. The concept of thermal resistance is based upon an analogy between the electrical and thermal properties of materials, with temperature, power dissipation, and thermal resistance being analogous to voltage, current, and electrical resistance, respectively. The thermal resistance ($R_{\theta JR}$) is defined as follows:

$$R_{\theta JR} \equiv \frac{T_J - T_R}{P} \tag{1}$$

where:

$R_{\theta JR}$ = thermal resistance between the junction and the reference point, in degrees Celsius/watt,

T_J, T_R = temperatures of the junction and the reference point, respectively, in degrees Celsius, and

P = power dissipated in the device, in watts.

In applying the electrical analogy to the thermal problem and in using eq (1), it is implicitly assumed that uniform current and temperature distributions exist across the junction of the device under test and that one-dimensional heat flow occurs from a planar heat source. These assumptions imply a unique value of thermal resistance for devices of a given design and construction. Since these assumptions are not completely valid for actual power transistors, care is needed in applying the results of eq (1) to real devices [2].

3. Electrical Measurement of Thermal Resistance

Because a power transistor cannot always be characterized by a unique value of thermal resistance for all operating conditions due to such effects as current crowding, it is very important to be able to measure the critical junction temperature for a variety of operating conditions. Ideally, the measurement method chosen should 1) yield a temperature as close to the peak junction temperature as possible, 2) be easy to perform, 3) be precise, and 4) be nondestructive. The most commonly used methods for measuring the junction temperature of a semiconductor device utilize a temperature-sensitive electrical parameter (TSP) of the device as the temperature indicator. Although electrical techniques do not always directly yield the peak junction temperature, they are nondestructive, are generally simple to perform, and can be precise.

A number of electrical parameters, such as the forward-biased collector-base voltage (V_{CB}), the d-c forward current gain (h_{FE}), the collector-base leakage current (I_{CBO}), and the forward-biased emitter-base voltage (V_{EB}) have been used as temperature indicators. In addition, various techniques have been used for monitoring each of these parameters; all these techniques can generally be put into one of two generic classes: 1) continuous methods and 2) switched or pulsed methods. Each of the techniques relies on the ability to simply and uniquely relate the TSP to junction temperature. The degree that this is possible is a major factor in assessing the worth of a particular technique. A brief description of the use of the various electrical parameters as TSPs is given below followed by a detailed description of a preferred technique which most closely meets the requirements of the ideal measurement method. With minor modifications, the circuit used for the preferred method for measuring thermal resistance can also be used to measure the transient thermal response of devices [3], the thermal resistance of integrated Darlington power transistors [4], and the quality of the die attach of devices (using the transient thermal response) [5].

3.1 Continuous Electrical Methods

In these methods, the TSP is monitored while the device is operating in an active, power-dissipating mode. In one version [6], the case, ambient, or other reference point is elevated to a high temperature (T_2), not exceeding the maximum junction temperature. The collector current (I_C) is set and a collector-base voltage (V_2) applied to the

device. The TSP is measured under these conditions and then the reference temperature is reduced to a lower temperature (T_1) and the collector-base voltage increased to a value V_1 until the same value of the TSP is measured as was measured above. The thermal resistance is then

$$R_\theta = \frac{T_2 - T_1}{I_C(V_1 - V_2)} . \tag{2}$$

The dc current gain (h_{FE}) [6] and the base-emitter voltage (V_{BE}) [7] have been used as transistor TSPs for measuring temperature by the continuous method.

It is generally assumed with continuous methods that the TSP (h_{FE} or V_{BE}) varies monotonically with temperature and that variations in the TSP as a result of the changes in the temperature are much greater than variations as a result of changes in the collector-base voltage (V_{CB}).* Unfortunately, both h_{FE} and V_{BE} may be strong functions of V_{CB}, and it is often difficult to separate these electrical effects from the desired thermal effects. For example, in the continuous V_{BE} method, a correction for the Early effect [8] may have to be included [9]. The added complexity required for this correction negates the apparent simplicity of the continuous V_{BE} method. In addition, it has been found that h_{FE} may not vary monotonically with V_{CB} because of changes in the device current density as the collector voltage is varied [10]. Thus, although the continuous methods appear at first glance to be simple, they are not recommended for use in making temperature measurements of semiconductor devices because of the difficulties mentioned.

3.2 Switched or Pulsed Methods

Switched or pulsed electrical methods require that the device be rapidly switched between a condition of high power dissipation and a condition of very low or zero power dissipation. In switched methods, the TSP is monitored during the low power dissipation condition immediately after the removal of a high power dissipation d-c operating condition. The calibration of the TSP against junction temperature is performed at the low power condition. In pulsed methods, the TSP is monitored during the high power dissipation d-c condition, while calibration of the TSP against junction temperature is performed by monitoring the TSP during a very short pulse at the same high power level. In both techniques, it is assumed that the junction temperature rise above the reference is negligible during the calibration procedure. The switched methods achieve this by a very low power dissipation, while the pulsed methods achieve this by a very short pulse of high power. Thus, the ref-

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* An example of the use of this assumption can be found in Method 3132, Thermal Resistance (DC Forward Voltage Drop, Emitter Base, Continuous Method) of MIL-STD-750B, February 27, 1970.

erence point temperature is indicative of the junction temperature under these conditions. The transistor TSPs that have been used in measuring thermal resistance by switched or pulsed methods are the collector-base current (I_{CBO}) [11], the d-c forward current gain (h_{FE}) [12], the collector-base forward voltage (V_{CB}) [13], and the emitter-base forward voltage (V_{EB}) [14].

Since h_{FE} can be a double-valued function of temperature, it is not recommended for use as the TSP. The switched method using I_{CBO} as the TSP is generally limited to measurements on germanium devices having relatively large bulk leakage currents and is of no real interest for the majority of modern silicon devices where surface and bulk leakage current effects may be of the same order.

The switched methods which use V_{EB} or V_{CB} as the TSP are generally equally precise. However, it has been found that V_{EB} when used as the TSP tends to indicate a junction temperature nearer the peak temperature than does V_{CB}, and, in addition, the switching techniques are simpler for the V_{EB} methods. In contrast to the other methods discussed, the circuit variations used to implement the switched V_{EB} techniques are numerous [14,15,16]. It can also be shown that switched V_{EB} methods are simpler to perform than the pulsed V_{EB} methods and under conditions of current crowding tend to indicate a junction temperature nearer to the peak temperature due to differences in calibration operating conditions. The switched V_{EB} technique that has been found to be the easiest to perform and to generally yield a temperature closest to the peak junction temperature is one in which the device under test operates as a transistor both during the heating and TSP monitoring or calibration procedures. This approach has come to be known as the V_{EB} emitter-only switching technique and is the preferred method for measuring the junction-to-case thermal resistance ($R_{\theta JC}$).

Table 1 presents a comparison of measurements of $R_{\theta JC}$ using the preferred V_{EB} emitter-only switching technique with other switching techniques. The data were extracted from measurements made by the National Bureau of Standards for use in a preliminary round-robin experiment on thermal resistance conducted in cooperation with EIA-JEDEC Committee JC-25 on Power Transistors.* These data illustrate the apparent differences in thermal resistance when measured using a variety of electrical techniques. Eleven devices were measured. Three were encased in TO-66 cans and eight in TO-3 cans. As expected, the V_{CB} technique gave lower values of thermal resistance than the V_{BE} base-and-collector switching technique, which in turn was lower than the V_{EB} emitter-only switching technique. It is this latter method that has been adopted as a standard technique for measuring the junction temperature of power transistors [1].

---

* This round robin was conducted under the auspices of Committee JC-25 on Power Transistors of the Solid State Products Division, Joint Electron Devices Engineering Council, Electronic Industries Association.

Table 1

Comparison of Different Electrical Techniques for Measuring the Thermal Resistance of Power Transistors

Device Number	Case Type	Measured Thermal Resistance (°C/W)		
		V_{CB} as TSP	V_{BE}† as TSP	V_{EB}* as TSP
A-2	TO-3	1.00	1.09	1.41
B-1	TO-3	0.74	0.90	1.06
B-2	TO-3	0.96	0.99	1.24
B-41	TO-3	0.48	0.53	0.71
B-42	TO-3	0.46	0.50	0.71
D-2	TO-3	0.41	0.48	0.56
D-3	TO-3	0.41	0.46	0.55
W-2	TO-3	0.38	0.40	0.61
W-3	TO-66	1.69	1.79	2.34
W-4	TO-66	1.69	1.79	2.40
D-4	TO-66	1.47	1.52	1.74

†Base and collector switching (device under test is operated as a diode during TSP monitoring or calibration).

*Emitter-only switching.

4. Preferred Electrical Measurement Method

The emitter-only switching technique in which the forward-biased emitter-base junction is used as the temperature-sensitive parameter is usable on all types of bipolar power transistors. The measurement procedure is relatively simple and lends itself to industrial measurements as well as for referee purposes. The power interruption circuitry is also relatively fast and simple since only one device terminal is switched. The technique also gives unambiguous results when current crowding occurs.

4.1 Measurement Procedure

In this method the emitter-base forward voltage (V_{EB}) is used as the TSP to indicate the junction temperature. The test procedure involves the measurement of the TSP as part of two steps, the power application and the calibration steps. In the power application step, V_{EB} is measured to determine the increase in the junction temperature due to power dissipation in the device under test. During the calibration step, V_{EB} is measured to determine the temperature coefficient of the device under test. A more detailed description of the measurement procedure is given in Appendix I where EIA Recommended Standard RS-313-B on Thermal Resistance of Conduction Cooled Power Transistors is reproduced by permission of the EIA. In this standard, the thermal resistance is given as:

$$R_{\theta JR} = \frac{T_J - T_R}{P_{(AVG)}} = \frac{V_{M2} - V_{MC} \text{ (for } T_{MC} = T_R)}{DP_2} \cdot \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{Calibration}} \tag{3}$$

where:

$R_{\theta JR}$ = thermal resistance, junction-to-reference point, in degrees Celsius/watt,

T_J = junction temperature, in degrees Celsius,

T_R = reference point temperature, in degrees Celsius,

$P_{(AVG)}$ = average heating power applied to transistor causing temperature difference $T_J - T_R$, in watts,

P_2 = magnitude of heating power applied to transistor, in watts,

V_{M2} = value of TSP corresponding to the temperature of the junction heated by P_2 and measured at the measuring current (I_M), in millivolts,

D = heating power duty factor (≈ 1),

$(\Delta V_{MC}/\Delta T_{MC})$ = TSP temperature coefficient measured at I_M, in millivolts/degrees Celsius,

T_{MC} = calibration temperature measured at reference point, in degrees Celsius, and

V_{MC} = values of TSP during calibration at I_M and specific values of T_{MC} in millivolts.

4.2 Test Circuit Description

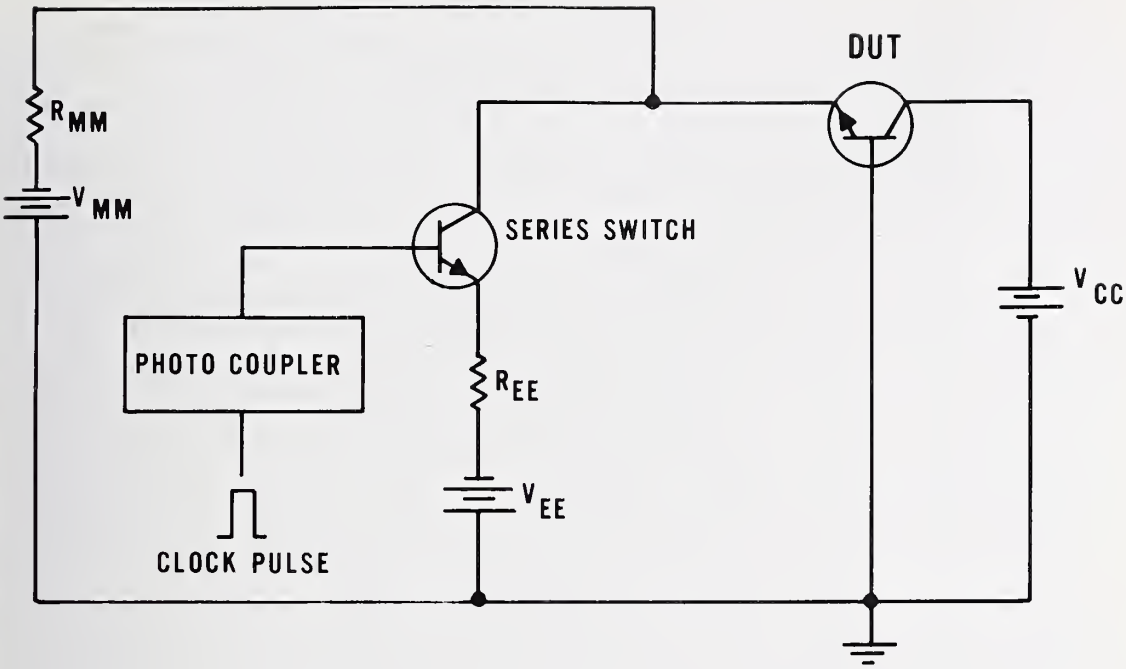
There are two basic test circuits used for the emitter-only thermal resistance measuring procedure. As can be seen in figure 1, the emitter has two current sources, one attached permanently which provides the constant measuring current and the other active only during the heating portion of the test cycle. The switching action is provided by a switch that either interrupts the emitter current by opening the line (series switching) or by shunting the emitter supply current to another path (parallel switching) as indicated in figure 1a and 1b, respectively.

The circuit in figure 1a offers no protection against reverse-biased emitter-base breakdown which can occur during switching. It was found that the process of rapidly reducing the emitter current from a very high value during heating to a very low value during measurement while the collector remained connected to its voltage supply could result in reverse-bias breakdown of the emitter-base junction of some transistors. Since the transistor may be damaged by reverse-biased breakdown of the emitter-base junction [17], fast switching circuits such as those needed for measurement of thermal resistance must be designed to avoid the possibility of such breakdown. A detailed explanation of the characteristics of the emitter-base voltage and current transients which occur when switching the emitter with a series transistor during measurement of thermal resistance is given in Appendix II together with a description of a proposed model.

Although the emitter-base voltage can be limited to a value below the breakdown voltage with a protective circuit based on the use of a regulator (zener) diode, a better solution is to use the parallel switching scheme. In this method, the emitter-base voltage is limited to the drop across the series diode D1 during switching. This method has the added advantage that parallel switching is a far superior procedure for high currents. For this reason, the preferred circuit for measuring the thermal resistance of power transistors utilizes parallel switching in the emitter lead to interrupt the heating current to the device under test (DUT).

The block diagram for the emitter-only switching circuit used to measure the thermal resistance of *npn* transistors, utilizing parallel switching in the emitter of the DUT, is given in figure 2.* The circuit is controlled by a clock pulse with a pulse width of approximately 300 μs and a repetition rate of approximately 4 Hz. When the voltage level of the clock pulse is zero, the transistor Q_1 is off and the current through the DUT is the sum of the heating current (switch S_1 closed) and

* This test method can also be applied to *pnp* devices by appropriate polarity charges in the test circuit elements.



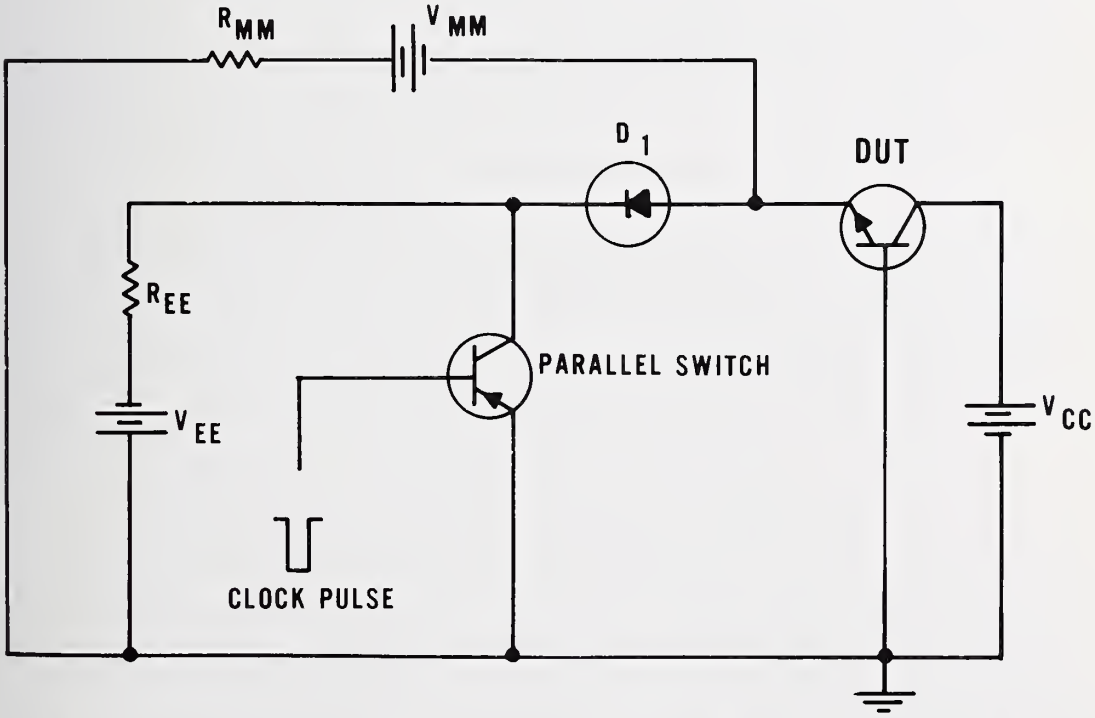


Figure 1. Basic circuits for measuring thermal resistance by the emitter-only switching technique. (a) series switching, (b) parallel switching.

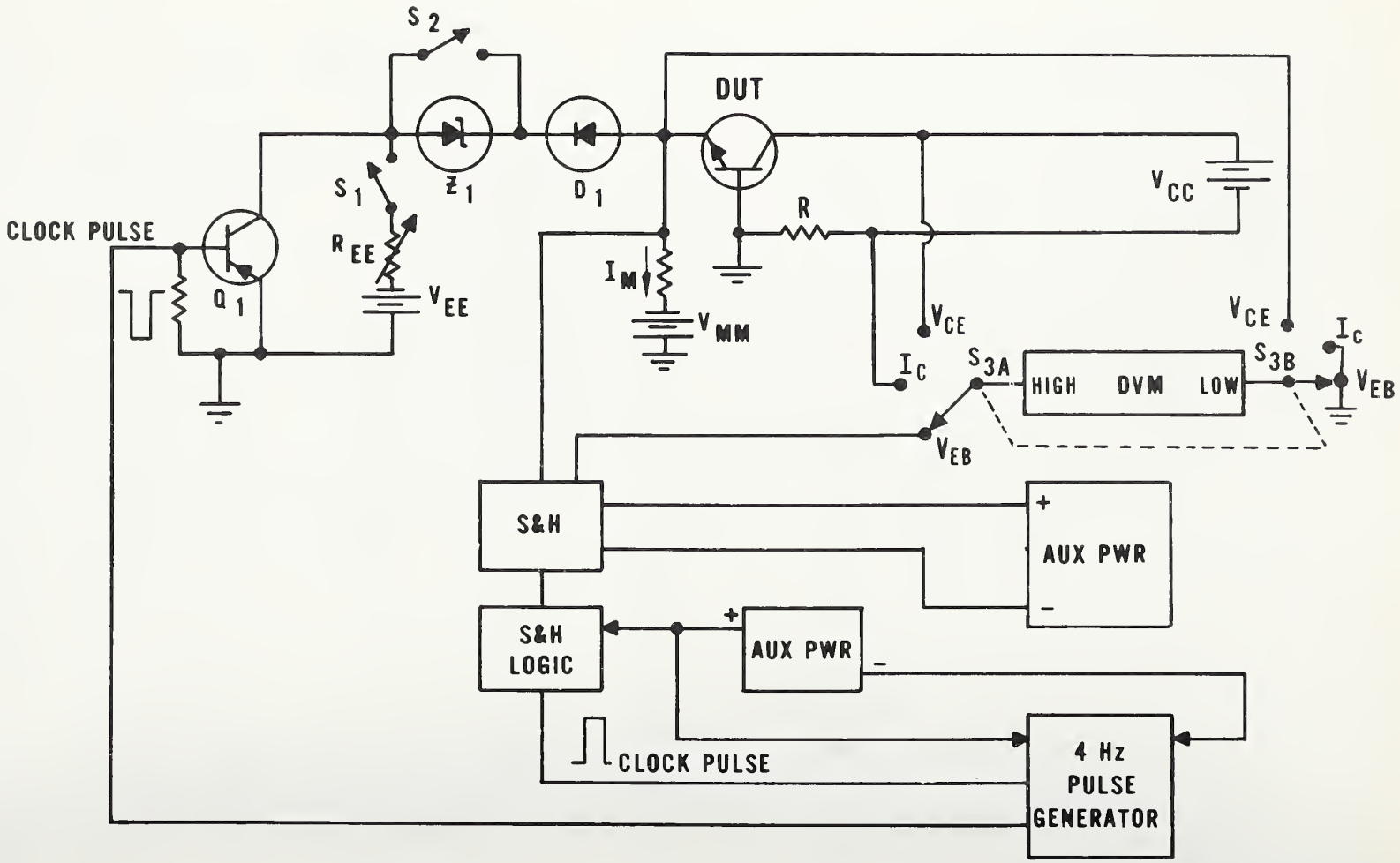


Figure 2. Block diagram for the emitter-only switching circuit used to measure *npn* transistor thermal resistance.

the measuring current I_M. The constant heating current is furnished by the V_{EE} supply, and the constant measuring current by the V_{MM} supply. At the end of each heating power pulse, the clock assumes a specified nonzero level for a period of time (∿300 μs) that is short compared with the heating interval (∿250 ms). This is sufficient to bias the transistor Q_1 on, which reverse biases the diode D1 so that the heating current no longer passes through the DUT. The function of the optional regulator (zener) diode Z_1 is to decrease the switching time of the DUT. The regulator voltage, V_Z, of the diode Z_1 should be equal to or less than the maximum rated V_{EBO} of the DUT. The sample-and-hold unit (S&H) is triggered when the heating current is removed and after a delay, usually 5 to 100 μs, senses the TSP, V_{M2}, for a 1.5-μs period and displays its value on the digital voltmeter (DVM). The temperature coefficient of the TSP and the calibration correlation voltage V_{MC} (for $T_{MC} = T_R$) are obtained by making the required measurements with the heating current supply disconnected (switch S_1 open). The digital voltmeter used to measure the TSP is also used to measure the power dissipation of the DUT as indicated by the DVM switch S_3. A noninductive current-sensing resistor R is used to measure the collector current I_C.

Details of the instrumentation to implement the V_{EB} emitter-only switching method for measuring the thermal resistance of power transistors are given in Appendix III. This appendix includes a description of the basic circuit itself as well as a description of the clock pulse generator, the sample-and-hold circuit, the temperature controller, and the temperature-controlled, water-cooled heat sink. Appendix IV describes the results of long-term, single-operator measurements to check the repeatability of the equipment for measuring thermal resistance described in Appendix III.

4.3 Special Precautions and Considerations

There are several special precautions and considerations that must be taken into account when measuring the thermal resistance of power transistors. They generally relate to the nonideal characteristics of semiconductor devices and interactions of the device under test with the measuring system. They range from such questions as to how to pick the measuring current to how to prevent oscillations in the device under test.

4.3.1 Measuring Current Considerations

As indicated previously, the measuring current is generally selected such that the TSP varies linearly with temperature over the range of interest and that negligible internal heating occurs during the calibration procedure and measuring interval. A measuring current equal to 0.1 percent of the maximum rated collector current ($I_{C(max)}$) of the device under test will generally meet this criterion. Generally, a measuring current of a few milliamperes is acceptable for the large majority of medium power transistors.

It has also been found that, for some devices, the calibration curve deviates from its normally linear slope for junction temperatures above 150 to 175°C due to high leakage current effects. When this happens, a best fit linear line to the actual curve, over the temperature range of interest, generally gives the required accuracy of measurement. If this is not the case for the particular temperature range of interest, the actual calibration curve should be plotted and the junction temperature due to internal power dissipation read off the curve.

4.3.2 Oscillations in the Device Under Test

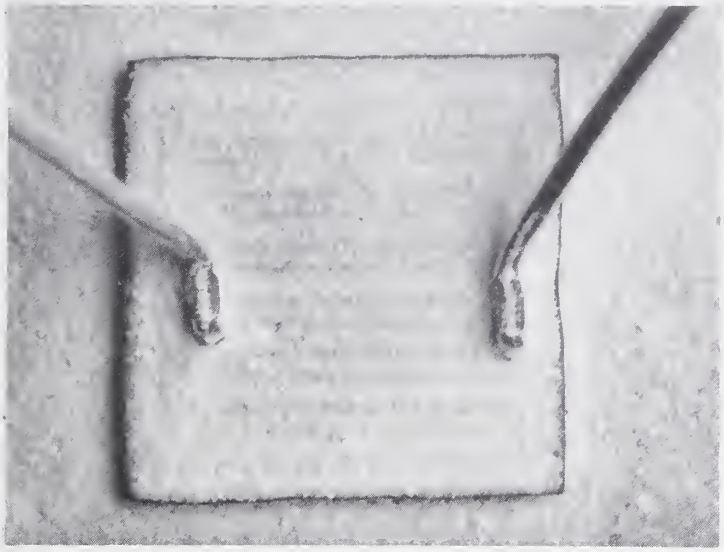
The occurrence of oscillations in the device under test can make it impossible to determine the actual power dissipation for calculations of thermal resistance. Also, the measurement of the TSP within the required time after the heating power is terminated becomes difficult, if not impossible, if oscillations occur.

The use of lossy ferrite beads on the emitter and base leads of the device under test has been found to be an effective means of attenuating unwanted high frequency oscillations. Lossy ferrite beads selectively absorb rf energy, being most effective at the higher frequencies where feedback energy causes oscillation. The effectiveness of the beads depends on the relative magnitude and frequency distribution of the source, the ferrite bead, and the load impedances.

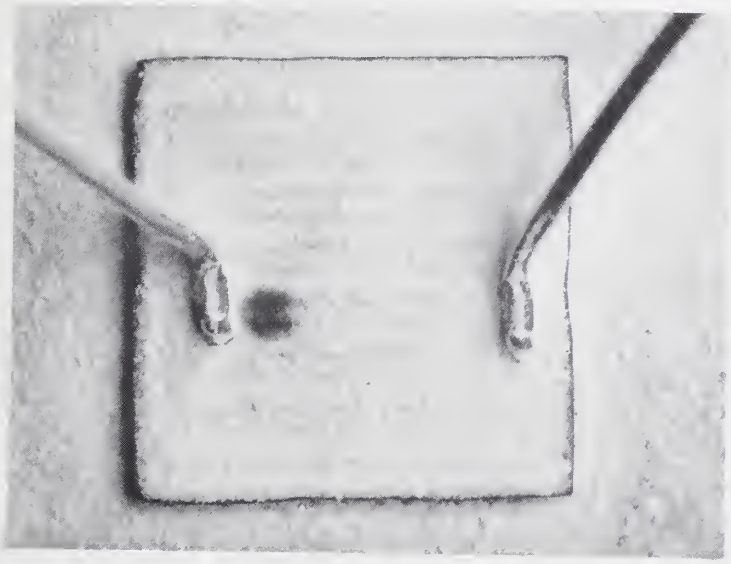
It has also been found that a capacitor may be required between the collector and base (ground) of the device under test to prevent oscillations. The value of the capacitor has to be large enough to damp the oscillations and may require parallel capacitors so as not to become series resonant within the frequency range of the test equipment.

4.3.3 Operating Conditions of the Device Under Test

The ability of the V_{EB} emitter-only technique to accurately measure the peak junction temperature is greatly dependent on the degree of heating current nonuniformity that exists within the active region of the semiconductor chip. The degree of current crowding is dependent on the device operating conditions even under constant heating power situations where $P_2 \approx I_C V_{CE}$ [10,18]. An example of this can be seen in figure 3 for a 125-W triple-diffused power transistor which is dissipating 50 W of power for two different operating conditions. The device is coated with a thermographic phosphor [19] which appears darkest at the hottest areas of the device in this figure. For the low-current, high-voltage condition (I_C = 0.25 A, V_{CE} = 200 V), the power density is much more localized (as evidenced by the very dark "hot spot") than for the other operating condition. Even though the power dissipation in the transistor was held constant, the peak junction temperatures are dramatically different. In this case, the difference is approximately 150°C.



(a)



(b)

Figure 3. A 125-W power transistor coated with a thermographic phosphor shown for two different operating conditions, each dissipating 50 W. The phosphor when illuminated with ultraviolet radiation as done here is brightest at the cooler areas and darkest at the hotter areas. (a) I_C = 1.0 A, V_{CE} = 50 V; (b) I_C = 0.25 A, V_{CE} = 200 V.

In general, for low-current, high-voltage operation, the measured thermal resistance is a strong function of operating conditions. At the other extreme, high current and low voltage, it is not as strong a function of the operating conditions. This can be seen in figure 4, which shows a plot of measured thermal resistance versus collector current at constant power for a 35-W power transistor. Data taken on three power transistors at various operating conditions, comparing indirect and direct measurements of thermal resistance, are summarized in table 2. It can be seen from the data that, as the degree of current crowding increases, the electrically measured thermal resistance deviates further from the actual peak thermal resistance as determined from direct measurements with an infrared microradiometer.

The reason for the large values of $R_{\theta JR}$ at low values of I_C is that the thermal-electrical feedback mechanisms that initiate current crowding and eventually second breakdown [20] are stronger at small values of I_C than at large values. Thus, the current tends to be more constricted and the peak temperature higher for these conditions.

The fact that for high-current, low-voltage operation the thermal resistance is generally not a strong function of device operating conditions does not mean that measurements at low collector voltage and high collector current are without difficulties. For example, the extremely long switching times of devices operating in the quasi-saturation region [21] make thermal resistance measurements using a switching technique in this region of operation essentially meaningless. This is because the part of the measured V_{EB} which arises from a long-lived nonthermal transient, which is due to the large density of stored charge, cannot be separated out from the desired thermal part. The problems encountered are illustrated in figure 5, which shows the measured thermal resistance of a 35-W power transistor plotted against the square root of the time after cessation of power for a transistor with collector current of 4 A and a range of values of collector-emitter voltage, V_{CE}.* The device is operating in the quasi-saturation mode at 5 and 7.5 V and is just beginning to come out at 10 V. Note that for 5, 7.5, and 10 V there is almost no linear portion of the curve as would be predicted by the extrapolation procedures based on one-dimensional cooling [3]; the nonlinearity indicates that nonthermal switching transients are present.

The thermal resistance at 5, 10, and 20 V as calculated from measurements of the peak junction temperature with an infrared microradiometer are also indicated in the figure at zero time. Because the electrical method is known to average the junction temperature, it should always indicate a temperature less than the peak temperature. Only at 20 V is this the case; at 5 V, the electrically measured temperature is greater than the peak temperature even after the device has cooled for 250 μs. This arises because the nonthermal switching transients completely obscure the temperature dependence of the junction voltage. Thus, operat-

*This extrapolation procedure is discussed in Appendix C of Appendix I of this report; also see 4.4.2.

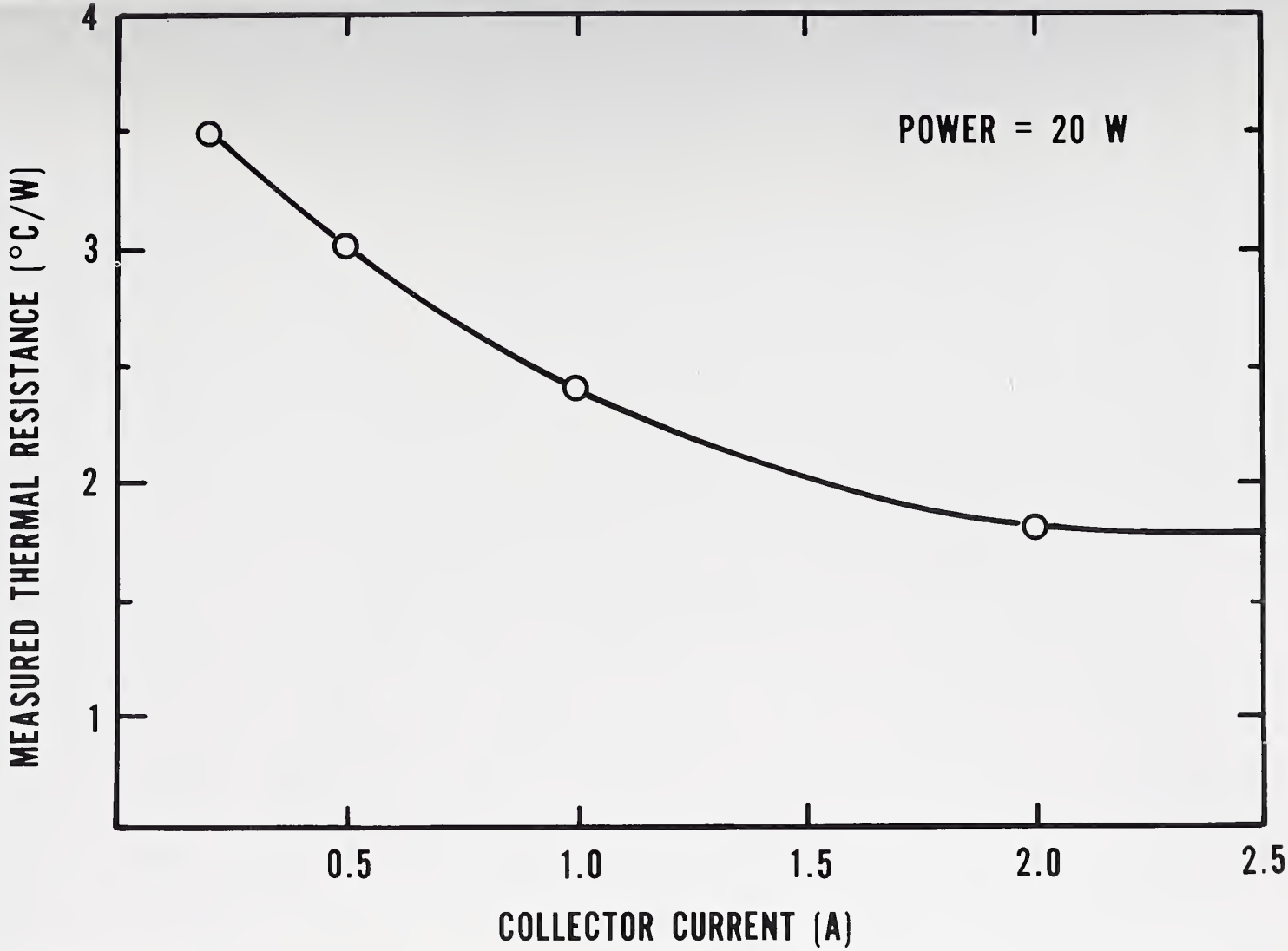


Figure 4. Measured thermal resistance as a function of collector current at a constant power of 20 W for a 35-W triple-diffused transistor.

Table 2

Comparison of Electrical and Infrared Techniques for Measuring the Thermal Resistance of Power Transistors under Various Device Operating Conditions

Device Number	Specified $R_{\theta JC}$ (°C/W)	Operating Condition I_C(A)/V_{CE}(V)	Power (W)	Measured Thermal Resistance (°C/W)	
				Standard Electrical	Infrared Microradiometer
1	5	0.1/170	17	8.5	14.6
		0.2/105	21	5.5	9.0
		0.4/80	32	4.2	5.5
		1.0/54	54	3.0	3.4
		2.0/33	66	2.5	2.7
2	1.5	0.2/140	28	2.9	4.6
		0.3/106	32	2.8	4.0
		1.0/44	44	2.4	2.9
		2.0/38	76	1.9	2.1
3	7	0.6/76	46	3.3	3.8
		1.0/50	50	3.0	3.4
		2.0/28	56	3.0	3.2
		3.0/20	60	2.8	2.9

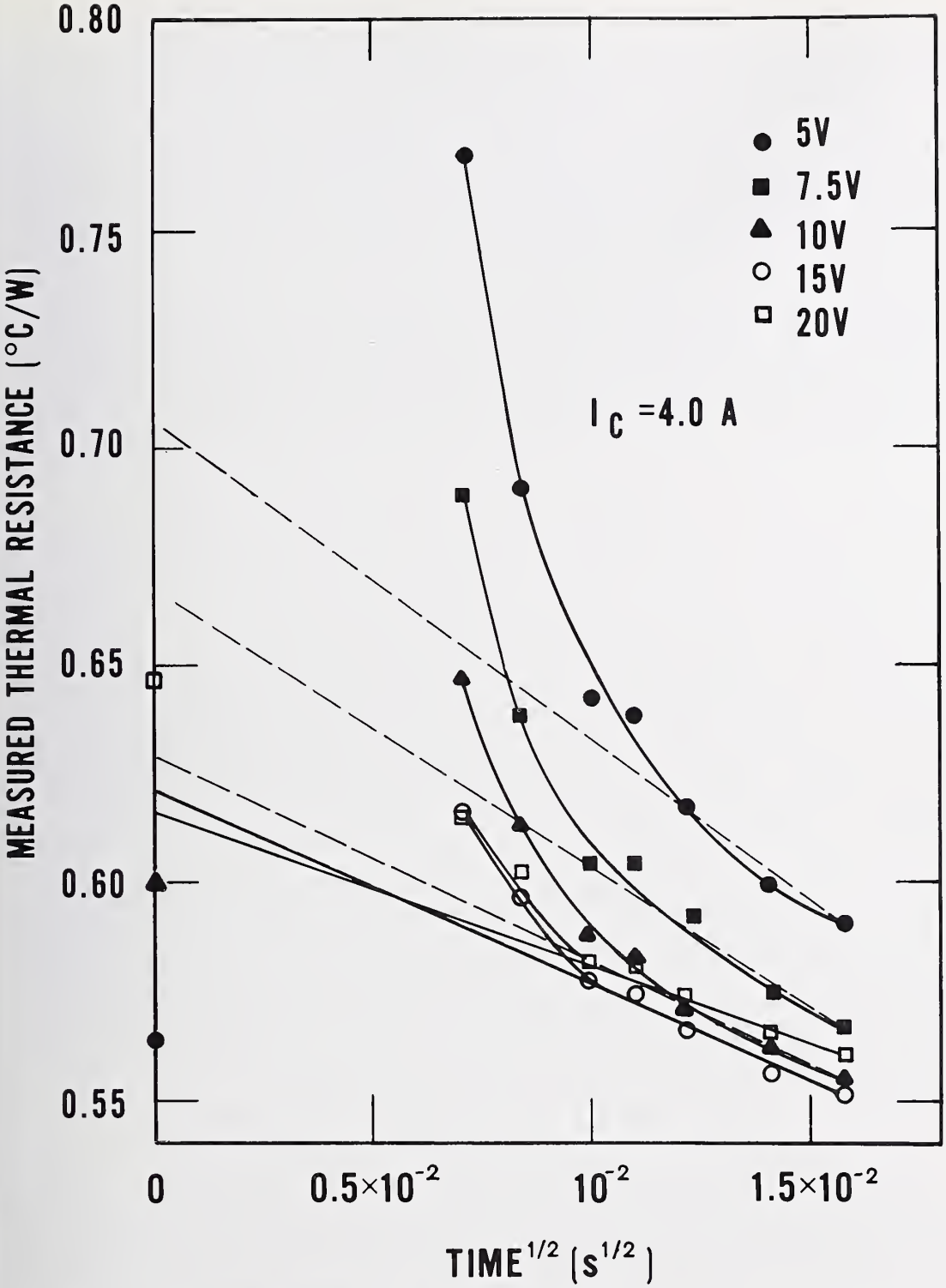


Figure 5. Cooling curves for a transistor operated with a collector current of 4 A and various emitter-collector voltages. Data points at zero time are derived from measurements of the peak junction temperature with an infrared microradiometer.

ing conditions that place the device under test in the quasi-saturation region should be avoided when making thermal resistance measurements.

4.4 Simplification of Measurement Procedure for Industrial Use

The basic procedure for measuring the thermal resistance of power transistors using the V_{EB} emitter-only switching technique was developed as a referee test method, although the ability to use the technique in the industrial environment was a major criterion involved in its selection. This section deals with modifications to the basic procedure to allow measurements to be made in an industrial environment with greater speed and without significant loss in precision and accuracy. Discussed are simplifications to the measurement procedure that allow testing of devices of a given design and construction to be accomplished without determining the calibration coefficient and extrapolated value of the TSP for each device being measured.

4.4.1 Simplified Calibration Procedure

When thermal resistance measurements are being made on a large number of devices of a given design and construction, the use of a simplified calibration procedure is often acceptable. It can generally be assumed that under these conditions the slope of the calibration curve (the temperature coefficient of the TSP) is relatively constant. Data, extracted from a study on the use of thermal response for die attachment evaluation [5] taken on 42 transistors mounted on TO-5 headers, indicated that the relative sample standard deviation of the calibration slope was 1.2 percent. Thus, if the processing for a particular device type does not change, then the slope of the calibration curve should not vary by more than a few percent.

The validity of the assumption that the temperature coefficient of the TSP is relatively constant can be verified in the following manner. The temperature coefficient should be measured on 10 devices of the same design and construction as those to be tested. If the relative sample standard deviation of these measurements is less than or equal to ±3 percent, the average of the measured temperature coefficients can be used in the calculation of thermal resistance for all other devices of that design and construction.*

4.4.2 Simplified Extrapolation Procedure

In measuring thermal resistance using the switched method, it would seem desirable to measure the TSP at the exact instant that the heating

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* This validation procedure was developed in conjunction with EIA-JEDEC Committee JC-13.1 on Government Liaison for Discrete Semiconductor Devices for use in a revision of Method 3131 on Thermal Resistance of MIL-STD-750. The revised test method for measuring the thermal resistance of transistors is designated Method 3131.1 and can be found in MIL-STD-750B, Notice 9, dated September 19, 1978.

power is removed, since the junction temperature is maximum at that time. However, this is not possible because 1) it takes a finite time for the transistor current to decay from the heating value to the measuring value and 2) transients exist in the measuring voltage waveform for some time after the measuring current value is reached due primarily to charge storage effects in the device under test (as discussed in 4.3.3). Because some semiconductor element cooling occurs during this delay period, the TSP may have to be extrapolated back to the time when the heating power was terminated (see Appendix C of Appendix I for details).

The extrapolation procedure is based on the assumption that the heat source thickness is small compared to the total chip thickness and that for approximately the first 250 μs of cooling one-dimensional heat flow occurs [3]. During this period, a proportionality factor, K, which relates the change in T_J during cooling to $t^{1/2}$ [see eq (1) of Appendix C of Appendix I] can be defined as follows:

$$K = \frac{T_{J2} - T_{J1}}{t_1^{1/2} - t_2^{1/2}} \tag{4}$$

where:

t = delay time after heating power is terminated, in microseconds,

T_{J1} = junction temperature at time $t = t_1$, in degrees Celsius, and

T_{J2} = junction temperature at time $t = t_2 < t_1$, in degrees Celsius.

When thermal resistance measurements are being made on a large number of devices of a given design and construction, the use of a simplified extrapolation procedure is often acceptable. Under these conditions and for a given set of device operating conditions (V_{CE}, I_C, and I_M), the proportionality factor, K, is relatively constant. It was also shown in section 4.4.1 that a single value of the temperature coefficient of the TSP is also appropriate for devices of a given design and construction. Then the extrapolation correction factor (K′) is given by:

$$K' = \frac{V_{M2(1)} - V_{M2(2)}}{t_1^{1/2} - t_2^{1/2}} = K \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]_{\text{Calibration}} \tag{5}$$

where K′ is the slope of the V_{M2} versus $t^{1/2}$ cooling curve for the first 250 μs of device cooling and $V_{M2(1)}$ and $V_{M2(2)}$ are measured at t_1 and t_2, respectively.

The basic relationship used to calculate the thermal resistance [see eq (3)] can be modified as follows to take into account the use of the constant extrapolation correction factor (K′):

$$R_{\theta JR} = \frac{V_{M2} - V_{MC} - K't^{1/2}}{DP_2} \cdot \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{Calibration}} \tag{6}$$

where V_{M2} is measured at time t. (For greatest precision, t should be as small as possible, consistent with $t_2 \leq t \leq t_1$.)

To validate the assumption that a single extrapolation correction factor (K′) can be used, the extrapolated slope of the cooling curve should be measured for 10 devices of the same design, construction, and operating conditions as those to be tested. If the relative sample standard deviation of these measurements is less than or equal to ±3 percent, the average extrapolation correction factor can be used in the calculation of thermal resistance for all other devices of that design and construction.* Since the cooling curve during the first 250 μs of cooling is proportional to the area of conduction of the transistor, the use of this simplified extrapolation procedure is not recommended for operating conditions at which current crowding occurs.

5. Thermal Response Measurements for Die Attachment Evaluation**

Both the steady-state thermal response (or thermal resistance) and the transient thermal response of semiconductor devices are sensitive to the presence of voids in the die attachment material between the semiconductor chip and header since these voids impede the flow of heat from the chip to the case (header). Due to the difference in the thermal time constants of the chip and case, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the case. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-case interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant, but less than that of the case. Heating power pulse widths ranging from 5 to 10 ms have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with

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* This validation procedure was developed in conjunction with EIA-JEDEC Committee JC-13.1 on Government Liaison for Discrete Semiconductor Devices for use in a revision of Method 3131 on Thermal Resistance of MIL-STD-750. The revised test method for measuring the thermal resistance of transistors is designated Method 3131.1 and can be found in MIL-STD-750B, Notice 9, dated September 19, 1978. In Method 3131.1, the extrapolation correction factor, K′, is labeled K. [See Appendix V of this report for information on the equivalency of symbols used in the commercial and military thermal resistance test methods for transistors.]

** This procedure is incorporated in EIA Recommended Standard RS-313-B, Thermal Resistance of Conduction Cooled Power Transistors, dated October 1975 as Appendix A. (See Appendix I of this report).

the added advantage of not having to mount the device under test on a heat sink [5].

To compare relative quality of the die bond, it is assumed that the temperature coefficient of the TSP is the same for all members of a given group of devices of the same design and construction (see section 4.4.1). It is therefore necessary only to measure the TSP first under conditions of no internal power dissipation (V_{MC}) and then at some specified time after the termination of the constant heating power pulse (V_{M2}). A quantity proportional to the junction-to-reference point temperature difference is obtained by subtracting V_{M2} from V_{MC}. This allows the transient thermal response technique to be made less time-consuming for use as a manufacturing screen or process control measurement for die attachment evaluation.

A typical circuit for measuring V_{MC} and V_{M2} is shown in figure 6. It should be noted that the power interruption circuitry is similar to that used in the measurement of thermal resistance utilizing the emitter-only switching procedure, although for transient thermal response measurements, the power-off interval is long compared to the power-on interval.

The circuit is controlled by a clock pulse with adjustable width and repetition rate. When the voltage level of the clock pulse is zero, transistor Q_1 is off, and the current through the DUT is the sum of the heating current (switch S_1 closed) and I_M. The heating power pulse ends when the clock goes negative. This turns Q_1 on, causing the heating current from V_{EE} to now flow through Q_1 instead of the DUT. After a delay to allow electrical transients to subside (usually 10 to 50 μs), the sample-and-hold unit (S&H) senses V_{M2} and displays its value on the digital voltmeter (DVM) (switch S_3 as indicated). The voltage V_{MC} is obtained by making the measurement, with the heating current supply disconnected (switch S_1 open) or with transistor Q_1 turned on, prior to the application of the heating power pulse.

6. Conclusions

A brief description of the idealized concept of thermal resistance has been given along with the problems and pitfalls encountered in applying the concept to power transistors. It was shown that for high-current low-voltage operating conditions, a unique and meaningful thermal resistance based on the peak junction temperature can usually be defined, but for low-current, high-voltage conditions, no unique value, independent of operating conditions, can be defined.

In addition, the advantages and disadvantages of various electrical techniques for measuring thermal resistance were described, and a preferred standard technique was discussed in detail. This preferred technique, in which the forward-biased emitter-base junction is used as the temperature-sensitive parameter, is usable on all types of bipolar transistors. The measurement procedure is relatively simple and, because the temperature-sensitive parameter is sensed under conditions that simulate normal device operation, it is relatively accurate. The power interrup-

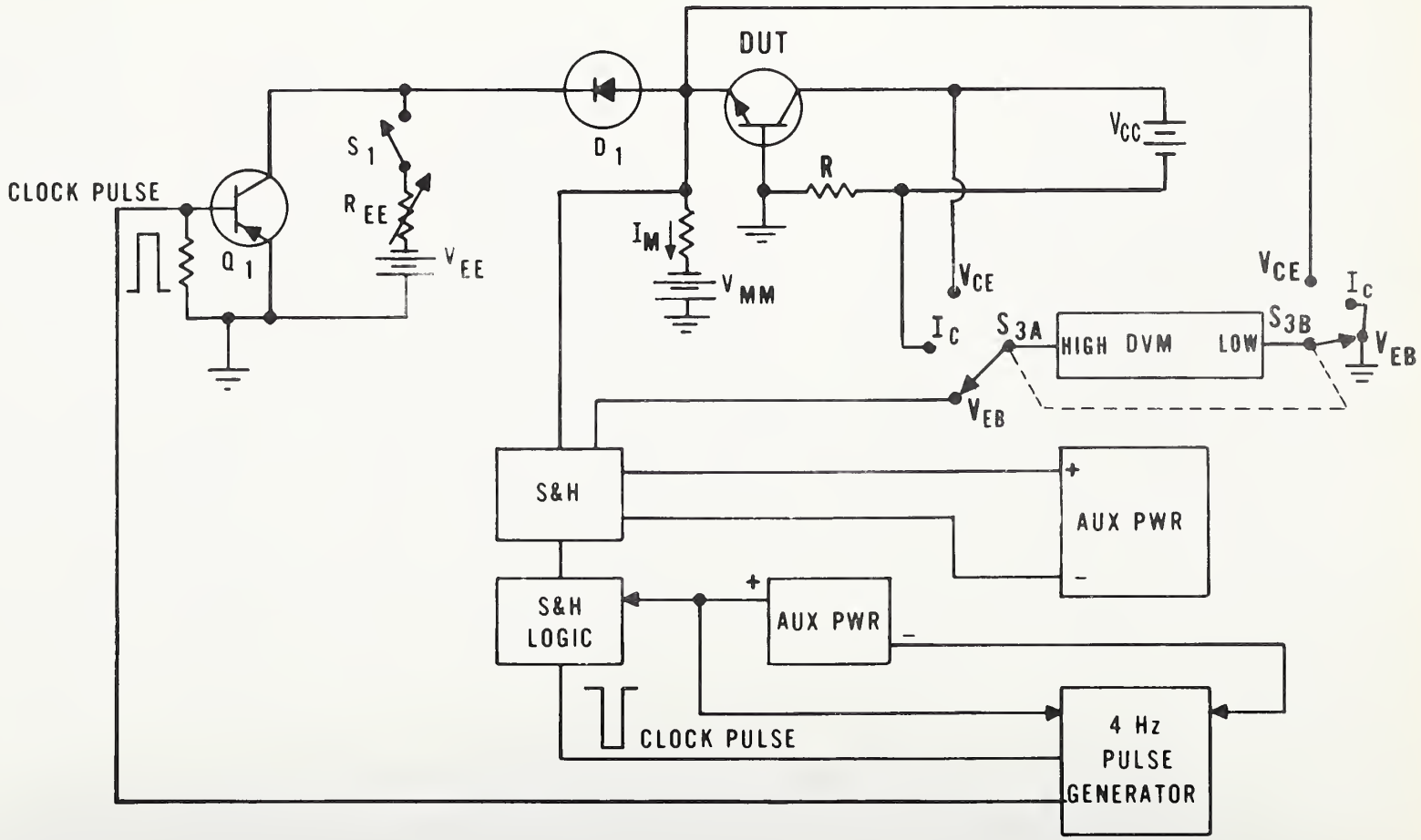

Figure 6. Block diagram for thermal response measuring system for *npn* transistors.

tion circuitry is also relatively fast and simple since only the emitter terminal of the device under test is switched. Detailed circuit diagrams and mounting and cooling arrangements to enable the building of a completed test system for measuring the thermal resistance of power transistors using the V_{EB} emitter-only switching technique are also presented. Simplifications in the temperature-sensitive parameter calibration and extrapolation procedures to make the technique usable in a production environment are valid under a variety of device operating conditions as long as the device design and construction is not changed. The basic approach and test circuitry is also usable for semiconductor device die attachment evaluation.

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THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS

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ELECTRONIC INDUSTRIES ASSOCIATION

RS-313-B
Revision of RS-313-A

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FOREWORD

This standard describes a recommended test method for measuring the thermal resistance of conduction-cooled power transistors. This method is offered as a replacement for that contained in EIA/NEMA Standard RS-313-A (March 1968) which has been found deficient in its test method detail. The present method is the emitter-base forward voltage method with emitter-base switching and treats the detail circuitry, test instruments, calibration and precautions to assure reliable and reproducible measurement. It generally conforms to the principle of MIL-STD-750 Method 3131 and to IEC Publication 147-C2 Method 12.3.1. However, experience has shown that the test performed under this Standard is applicable to all power transistors regardless of thermal response times.

This material was prepared by JEDEC Committee JC-25 on Power Transistors and approved for publication by the JEDEC Solid State Products Council.

(From Standards Proposal No. 1179, formulated under the cognizance of the JC-25 JEDEC Committee on Power Transistors.)

1. THERMAL RESISTANCE, JUNCTION to SPECIFIED REFERENCE POINT ($R_{\theta JR}$).

1.1 General Considerations. Of the thermal characteristics of a semiconductor device, the most frequently specified parameter is the thermal resistance between the chip and a reference point such as the device case or ambient.

The thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure (package) to provide for heat removal from the semiconductor junction. In most devices, the maximum junction temperature can't be measured directly since the area of interest is not accessible due to packaging considerations. Thus, indirect means are used to infer the temperature of a specific area on the chip. The thermal resistance of a semiconductor device is therefore determined by the measurement of a temperature-sensitive electrical parameter of a semiconductor junction within the device.

The measured thermal resistance of semiconductor elements (transistors) is not constant as frequently assumed, but depends on the device operating conditions, the junction and reference point temperatures, and the temperature-sensitive parameter chosen. When specifying thermal resistance, it is therefore important to indicate clearly the measuring conditions. The temperature sensitive device parameter is used as an indicator of an average (weighted) junction temperature of the semiconductor element for calculations of thermal resistance.

In measuring power transistor thermal resistance, either the emitter-base forward voltage or the collector-base forward voltage can be used as the temperature sensitive electrical parameter to indicate the junction temperature. Although equally precise, the Emitter-Base Voltage Technique has been found to be more accurate than the Collector-Base Voltage Technique, i.e., the Emitter-Base Voltage Technique gives a junction temperature closer to the actual peak temperature on the chip. The greater inaccuracy of the Collector-Base Voltage Technique is due to the greater deviation between the region of the collector junction traversed by the measuring current during calibration and the region traversed during test.

1.2 The Measurement of Thermal Resistance, Junction to Specified Reference Point ($R_{\theta JR}$), *using the emitter–base voltage of a transistor in the emitter-only switching mode as the temperature sensitive parameter.*

1.2.1 Purpose. The purpose of the test is to measure the junction to specified reference point thermal resistance of single element transistors by using the emitter-base junction to indicate the device junction temperature. This method is to be used as the standard

technique, i.e., referee method for the measurement of thermal resistance. However, the procedure is also adaptable to production testing, including die attachment screening (see Appendix A).

1.2.2 Procedure. In measuring transistor thermal resistance, the emitter-base forward voltage of the transistor is used as the temperature sensitive parameter (TSP) to indicate the junction temperature. The TSP is measured at a small fixed forward current. This low level current, at which the temperature sensitive parameter is measured, is called the measuring or calibration current (I_M). The magnitude of I_M is such that the TSP varies linearly with temperature and is stable. The TSP is measured under two general operating conditions. First, the measurements of the emitter-base forward voltage necessary to determine the changes in the TSP due to the dissipation of power are made. For these measurements the case temperature is kept at a constant preset value. After this is complete, the calibration curve is generated by measuring the TSP as a function of the case temperature starting at the lowest case temperature of interest. The information generated under these operating conditions is then used to calculate the junction-to-reference point thermal resistance in the following manner:

$$R_{\theta JR} = \frac{T_J - T_R}{P(AVG)} = \frac{V_{M2} - V_{M1}}{(P_2 - P_1)D} \times \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{Calibration}}$$

where:

$R_{\theta JR}$ = Thermal Resistance, junction to reference point, in degrees Celsius/watt.

T_J = Junction temperature in degrees Celsius.

T_R = Reference point temperature in degrees Celsius.

P(AVG) = Average heating power applied to transistor causing temperature difference $T_J - T_R$ in watts.

P_2 = Magnitude of higher heating power applied to transistor in watts.

P_1 = Magnitude of lower heating power applied to transistor in watts.

V_{M2} = Value of TSP corresponding to the temperature of the junction heated by P_2 and measured at I_M in millivolts.

V_{M1} = Value of TSP corresponding to the temperature of the junction heated by P_1 and measured at I_M in millivolts.

D = Heating power duty factor.

$(\Delta V_{MC}/\Delta T_{MC})$ = Temperature sensitive parameter temperature coefficient measured at I_M in millivolts/degree Celsius.

T_{MC} = Calibration temperature measured at reference point in degrees Celsius.

V_{MC} = Value of TSP during calibration at I_M and specific value of T_{MC} in millivolts.

If the lower heating power (P_1) applied to the transistor is equal to the power dissipation during calibration then $V_{M1} = V_{MC}$ (for $T_{MC} = T_R$). Also, if the power dissipation during calibration is negligible, then $P_1 \approx 0$. $R_{\theta JR}$ can then be simplified to:

$$R_{\theta JR} = \frac{V_{M2} - V_{MC}\ (\text{for } T_{MC} = T_R)}{P_2 D} \times \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{Calibration}}$$

Measurements of T_R and T_{MC} are made by means of a thermocouple attached to the reference point. See Appendix B for information on reference point temperature measurements of conduction cooled power transistors. The power dissipation in the device under test is calculated as follows:

$$P = I_C V_{CB} + I_E V_{BE}.$$

The measurement of thermal resistance is generally divided into two steps:

Step I - Power Application Test.

The power application test is performed in two parts. For both portions of the test, the reference point temperature is held constant at a preset value. The first measurement to be made is that of the temperature sensitive parameter, i.e., V_{MC}, under operating conditions with the measuring current (I_M) and the collector-emitter voltage (V_{CE}) used during the calibration procedure (see Step 2). If the power dissipation during this part of the test is not negligible, then power $P_1 = I_M V_{BE} + I_C V_{CB}$ should be subtracted from P_2 when calculating the thermal resistance.

The device under test is then operated with power (P_2) intermittently applied, but at a very high (greater than 99 percent) duty factor. The specified power level (P_2) is reached by varying the emitter current (I_E) to attain the required collector current (I_C); the collector-emitter voltage being equal to that value used during the calibration procedure. During the interval between heating pulses (generally less than or equal to 250 μs), and with the constant measuring current (I_M) and collector-emitter voltage (V_{CE}) applied, the value of the temperature sensitive parameter (V_{M2}) is measured. When measuring the thermal resistance of a transistor, only the emitter current is switched from the heating to measuring mode.

It would be desirable to measure the temperature sensitive parameter at the exact instant that the heating power removal is initiated since the junction temperature is maximum at that time. However, this is not possible for the following reasons:

1. It takes a finite time for the transistor current to decay from the heating value to the measuring value.

2. Transients exist in the measuring voltage waveform for some time after the measuring current value is reached due primarily to charge storage effects in the device under test.

The measuring voltage cannot be used as an indicator of junction temperature until after these transients subside. The delay time before the TSP can be measured ranges from 5 to 100 μs for most transistors. Since some semiconductor element cooling occurs between the time that the heating power is removed and the time that the TSP is measured, the junction temperature value determined from the TSP will be in error leading to a deceptively lower calculated thermal resistance. It may therefore be necessary to extrapolate the measured junction temperature back to the time where the heating power was terminated based on the shape of the cooling waveform beyond the measuring point (see Appendix C for details). The extrapolated value, either in terms of the TSP in millivolts or in terms of the actual calculated temperature in degrees celsius, should then be used in the calculation of thermal resistance.

It is recommended that the Power Application Test be performed so that the test device junction temperature is representative of worse case usage. Consistent with this, the reference point temperature should be such that the generated junction-to-case temperature difference is greater than or equal to 30°C. The type of heat dissipator used for the Power Application test must be chosen to accomplish this. The values of V_{M2}, V_{MC}, P_2, and D are recorded during the Power Application Test.

The same value of collector-emitter voltage used during the Power Application Test for internal device heating purposes is also applied during the Calibration Procedure (see Step 2).

Step 2 — Measurement of the Temperature Coefficient of the TSP.

The temperature coefficient of the temperature sensitive parameter is generated by measuring the TSP as a function of the reference point temperature, for a specified constant measuring or calibration current (I_M) and collector-emitter voltage (V_{CE}), by externally heating the device under test in an oven or on a temperature controlled heatsink. At small currents, the transistor emitter-base voltage decreases with increasing temperature. A measuring current ranging from 1.0 to 50 mA is generally used, depending on the rating and operating conditions of the device under test, for measuring the TSP. The measuring current is generally picked such that the TSP varies linearly with temperature over the range of interest and that negligible internal heating ($P_1 \approx 0$) occurs during the measuring interval. Therefore, the reference point temperature is approximately equal to the junction temperature during calibration. The value of the TSP temperature coefficient ($\Delta V_{MC}/\Delta T_{MC}$), for the particular measuring current and collector-emitter voltage used in the test, is calculated from the calibration curve.

1.2.3 Test Conditions to be Specified

1. Case Temperature range during calibration.
2. Measuring or calibration current.
3. Heating current magnitude.
4. Heating (collector) voltage magnitude.
5. Heating power duty factor.
6. Heating power repetition rate.
7. Delay time before measurement of TSP.
8. Total heating time duration.
9. Reference temperature measuring point.
10. Reference point temperature for heating power measurements.
11. Mounting torque.
12. Mounting arrangement.
13. Extrapolation procedure.

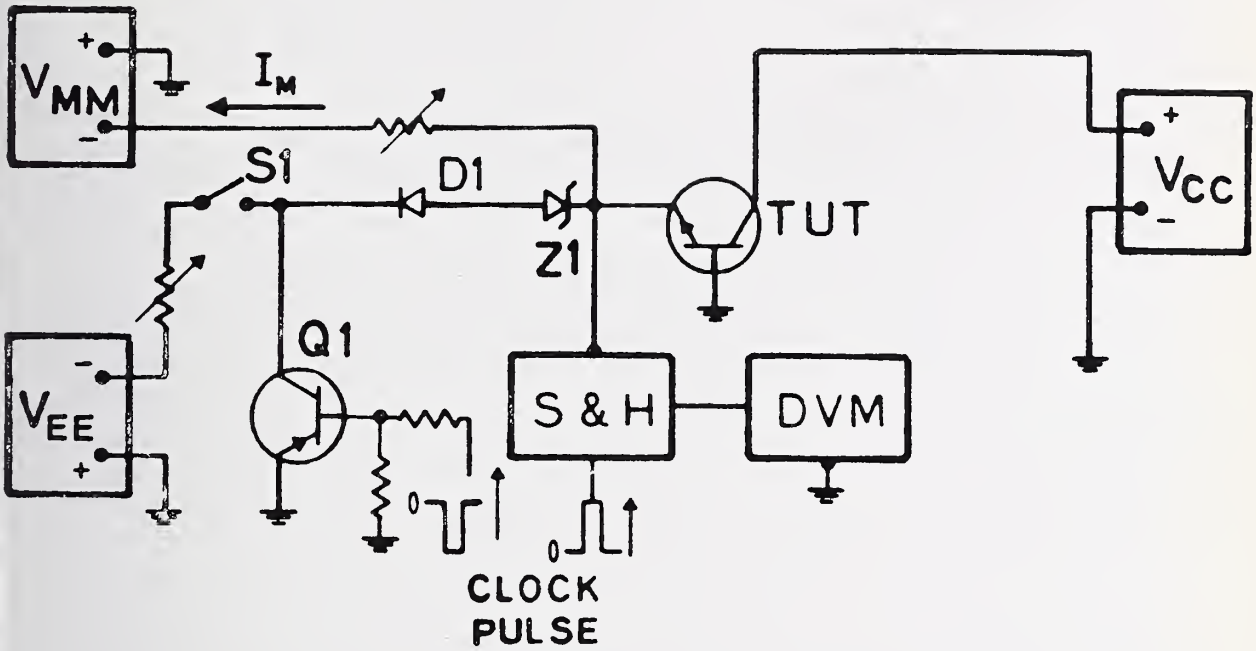
CHARACTERISTIC TO BE MEASURED

Thermal Resistance, Junction to Specified Reference Point ($R_{\theta JR}$). Two of the most common thermal resistance specifications are:

1. $R_{\theta JC}$ - Thermal resistance from junction to case.

2. $R_{\theta JM}$ - Thermal resistance from junction to mounting surface.

1.2.4 Test Circuit



Note: Lossy ferrite beads may be required on the emitter and base leads of the device under test to prevent oscillations. A capacitor may also be required between the collector and ground of the device under test to prevent oscillations.

The circuit is controlled by a clock pulse width of approximately 250 μs * and a repetition rate of approximately 4 Hz *. When the voltage level of the clock pulse is zero, the transistor Q1 is off and the current through the transistor under test (TUT) is the sum of the heating current (switch S1 closed) and the measuring current (I_M). The heating current is furnished by the V_{EE} supply, and the measuring current by the V_{MM} supply. At the end of each heating power pulse the clock assumes a specified non-zero level for a period of time that is short compared with the heating interval. This is sufficient to bias the transistor Q1 on, which reverse biases the diode D1 so that the heating current no longer passes through the device under test. The function of the regulator Zener) diode Z1 (optional) is to decrease the switching time of the device under test. The regulator voltage V_Z of the diode Z1 should be equal to or less than the maximum rated V_{EBO} of the transistor under test. After a delay, usually 5 to 100 μs, the sample-and-hold unit (S & H) senses the TSP, i.e., V_{M2}, for a 1.5 μs * period and displays its value on the digital voltmeter (DVM). The temperature coefficient of the TSP and the required voltage V_{MC} (for $T_{MC} = T_R$) are obtained by making the required measurements with the heating current supply disconnected (switch S1 open). The digital voltmeter used to measure the TSP can also be used to measure the power dissipation of the device under test by connecting it across the junction(s) to measure the voltage(s), and across a suitable non-inductive current sensing resistor(s) to measure the current(s).

* Typical Value

APPENDIX A

Thermal Response Measurements for Semiconductor Device Die Attachment Evaluation

A.1 General Considerations

Steady-state thermal response (or thermal resistance) and transient thermal response of semiconductor devices are sensitive to the presence of voids in the die attachment material between the semiconductor chip and header since these voids impede the flow of heat from the chip to the case (header). Due to the difference in the thermal time constants of the chip and case, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the case. Thus, the heating power pulse width can be selected so that only the chip, and the chip-to-case interface, are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the case. Heating power pulse widths ranging from 5 to 10 ms have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heatsink the device under test.

A.2 Procedure

To compare relative quality of the die bond, if it is assumed that the temperature coefficient of the TSP is the same for all members of a given group of devices of the same type or lot, it is possible to eliminate the conversion of the TSP to temperature in the calculations. This assumption is generally valid for semiconductor devices where the forward voltage of a p-n junction is used as the TSP. It is therefore necessary only to measure the TSP first under conditions of no internal power dissipation and then at some specified time after the termination of the heating power pulse. A quantity proportional to the junction-to-reference point temperature difference is obtained by subtracting the second voltage, V_{M2}, from the first, V_{M1}. This allows the transient thermal response technique to be made less time consuming for use as a manufacturing screen or process control measurement for die attachment evaluation.

APPENDIX B

Reference Point Temperature Measurements of Conduction Cooled Power Transistors.

B.1 Case Temperature (T_C)

The case temperature of a stud-mounted, hexagonal-base transistor is measured at the center of any flat on the hex. The case temperature of other base-mounted transistors is measured at a point specified by the manufacturer. The recommended procedure for measuring the case temperature of a transistor employs the use of a thermocouple and is defined as follows:

B.1.1 Type of Thermocouple – The thermocouple material shall be copper-constantan (Type T). Its useful temperature range for standard temperature measurements is -183 to +371°C. The wire size shall be no larger than #30 AWG. The junction of the thermocouple shall be welded together to form a bead rather than soldered or twisted. [See "1971 Annual Book of ASTM Standards-Part 30, Method E220 for Calibration of Thermocouples by Comparison Techniques" for information on construction and usage of thermocouples.]

B.1.2 Mounting Method – A small hole, just large enough to insert the thermocouple, shall be drilled approximately 0.762 mm (0.03 in) deep in the base plate of the semiconductor device at the point specified by the manufacturer. The edge of the hole should then be peened with a small center punch to form a rigid mechanical contact with the welded bead of the thermocouple. In the event that drilling into the base plate of the device case becomes impractical because of case material or case dimensions, the thermocouple wire may be welded or soldered directly to a specified point on the case.

B.1.3 Accuracy – An accuracy of ±0.5°C should be expected of the thermocouple and associated measuring system. Under load condition, slight variations in the temperature of different points on the case may reduce the accuracy to ±1.0°C for still-air cooling, and ±2.0°C for forced-air cooling.

B.1.4 Other Thermocouple Mounting Methods – Other methods of mounting thermocouples, with the possible exception of the thermocouple welded or soldered directly to the case, usually result in temperature readings lower than the actual temperature. Such deviations result from:

A. Inadequate contact with the case when using cemented thermocouples.
B. External heat dissipator in contact with the thermocouple when using pressure contacts.

B.2 Mounting Surface Temperature (T_M)

The mounting surface temperature for EIA Registered Power Transistor packages is measured using a thermocouple imbedded in a washer. The use of a washer, with a thermocouple imbedded, offers the best single method of non-destructive testing that is compatible with most package types. [The case and mounting surface temperatures are sometimes used interchangeably.]

B.2.1 Type of Thermocouple – The thermocouple material shall be copper-constantan (Type T). Its useful temperature range for standard temperature measurements is -183 to +371°C. The wire size shall be no larger than #30 AWG. The junction of the thermocouple shall be welded together to form a bead rather than soldered or twisted. [See "1971 Annual Book of ASTM Standards – Part 30, Method E220 for Calibration of Thermocouples by Comparison Techniques" for information on construction and usage of thermocouples.]

B.2.2 Mounting Washer Construction – For all registered T0 outlines the following general rules apply:

a. The base material of the washer shall be copper. (Preferred half hard or softer).
b. The thickness of the washer shall be 3.175 ± 0.127 mm(0.125 ± 0.005 in).
c. The outline of the washer shall be larger by 0.762 to 1.524 mm (0.03 to 0.06 in) than the outline of the seating surface of the package for which the washer is intended.
d. Clearance holes shall be 0.406 to 0.787 mm(0.016 to 0.031 in) larger than the maximum outside diameter of the studs or screws intended to pass through the holes.
e. Surfaces of the washer shall be flat within 25 μm per 25 mm(0.001 in per in) and parallel within 75 μm per 25 mm (0.003 in per in) and shall be nickel plated to a thickness of 1.27 to 2.54 μm (50 to 100 μin). [See "ANSI B46.1 – 1962, Surface Texture" for further details.]
f. The surface of the washer shall be free from burrs, but the maximum chamfering of edges or holes shall not exceed 0.406 mm(0.016 in) by 45 deg. so as not to effectively reduce the contact area of the washer.
g. Both surfaces of the washer shall have a 1.60 μm (63 μin) finish or better and be free of oxides. [See "ANSI B46.1 – 1962, Surface Texture" for further details.]
h. The thermocouple hole shall be drilled into the washer midway between and parallel to the top and bottom surfaces. The size of the thermocouple hole shall be no greater than 1.52 mm(0.06 in) in diam. but it is recommended that it be no larger than necessary to accept the thermocouple.
i. For flat type packages (such as T0-3) the bottom of the thermocouple hole shall extend approximately 0.76 mm(0.03 in) beyond the geometric center of the washer. Radial orientation of thermocouple hole is arbitrary.
j. For stud type packages (such as T0–61) the bottom of the thermocouple hole shall be approximately 0.76 mm(0.03 in) from the inside hole of the washer.
k. For tab type packages the bottom of the thermocouple hole shall extend approximately 0.76 mm(0.03 in) beyond the geometric center of the seating surface.
l. It is recommended that the thermocouple be secured into the washer with a thermal conducting adhesive and that particular attention be paid to minimizing air voids around the ball of the thermocouple. (The thermocouple bead should be in direct contact with the copper washer.)
m. Clearance holes for device leads should allow suitable clearance to prevent electrical shorting to the washer. It is recommended that this clearance hole be approximately 1.52 mm (0.06 in) larger in diameter than the lead to allow clearance for insulating sleeving to be used on the leads.

n. Device mounting torque should comply with the manufacturer's recommendations.
o. A thermal conducting compound at the interface of the washer and device should be used.
p. Special precautions must be taken so that only the bead of the thermocouple is allowed to come in mechanical contact with the washer.

Extrapolation Procedure for Power Transistors

C.1 Extrapolation Procedure

This extrapolation proeedure is based on the assumption that the heat source thickness is small compared to the total chip thickness and that for approximately the first 200 or 250 μs of cooling, one dimensional heat flow occurs. Therefore, the first 200 or 250 microseconds of cooling can be represented by

$$T_{J\,(Cooling)}(t) = T_{J\,(S.S.)} - Kt^{1/2} \tag{1}$$

where K is approximately eonstant and $T_{J(S.S.)}$ is the steady state junction temperature.

If, for equation (1), $T_{J(Cooling)}(t)$ versus $t^{1/2}$ is plotted on linear graph paper, the generated curve will be a straight line with $T_{J(S.S.)}$ as the Y – intercept, i.e., at $t^{1/2} = 0$. Plotting this curve for an actual device also provides a means for determining when non-thermal switching transients are significant since the curve, as plotted, will be non-linear under this eondition.

Using equation (1), a mathematieal expression which can be used to generate the extrapolated valu $T_{J(S.S.)}$ (t = 0) is a follows:

$$T_{J(S.S.)}(t = 0) = T_{J1} + \frac{T_{J2} - T_{J1}}{t_1^{1/2} - t_2^{1/2}}\, t_1^{1/2}$$

where:

$T_{J(S.S.)}(t = 0)$	=	Junction temperature, extrapolated to the time at which the heating power is terminated.
t	=	Delay time after heating power is terminated.
T_{J1}	=	Junction temperature at time t_1, e.g., t_1 = 200 μs.
T_{J2}	=	Junction temperature at time t_2, e.g., t_2 = 100 μs.

APPENDIX II

SWITCHING TRANSIENTS IN TRANSISTORS*

The turn-off transient which occurs when the emitter of a transistor is opened rapidly while the base and collector remain connected can result in emitter-base junction breakdown. This breakdown may cause deterioration [1] or catastrophic failure of the transistors. The breakdown occurs even though the emitter current is in the direction appropriate to a forward-biased emitter-base junction. It arises because of a potential drop along the emitter-base junction induced by the flow of majority carriers out of the base as required to bring the base region back to equilibrium following reduction of electron injection from the emitter. Breakdown can be avoided if the emitter is opened slowly enough that the base can remain in a near neutral condition without rapid flow of charge and the resulting potential build-up. Alternatively, the emitter-base voltage can be limited to a value below the breakdown voltage with a protective circuit based on the use of a zener diode. The charge flow in the base during the turn-on and turn-off transients and of the operation of the protective circuit are described in detail below.

To elucidate the details of the charge flow during switching an extensive series of experiments was conducted. In these experiments, the current in various branches of the circuit was measured with a current probe and the voltage across the appropriate transistor terminals was measured with an oscilloscope. The circuit used for these measurements is shown in figure II-1. This circuit also contains a protective zener diode circuit which can be incorporated by the switch S_1.

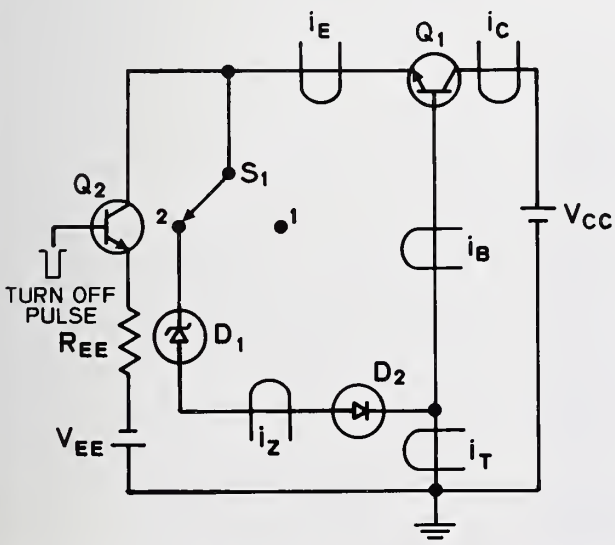


Figure II-1. Test circuit. (Current is measured by means of a probe at the loops marked i_X.)

* Extracted from Methods of Measurement for Semiconductor Materials, Process Control, and Devices (Quarterly Report for Period January 1 to March 31, 1973), NBS Tech. Note 788, W. M. Bullis, Ed, pp. 65-70.

The low-level emitter current supply, usually included when measuring thermal resistance, was omitted during this series of experiments; no significant differences, except one which will be noted subsequently, were observed when the low-level emitter current was included.

Turn-on Transient — Consider first the conditions in the on state which are set up during turn on. For explicitness the argument is developed for an *n-p-n* transistor, but it can easily be extended to a *p-n-p* transistor. In the quiescent state the base is grounded and the collector-base junction is reverse biased (collector positive). At a time t = 0, the emitter supply is connected to the emitter contact to foward bias the emitter-base junction (emitter negative) which results in electrons being injected into the base. The injected electrons are minority carriers in the base. They diffuse toward the collector-base junction with a time constant that can be the order of microseconds, but as soon as they enter the base they upset the charge neutrality in the base. To maintain charge neutrality, majority holes flow rapidly into the base from the base contact. The return to neutrality in the base occurs with a time constant determined by the dielectric relaxation time in the base. This time constant is the order of 10^{-12} to 10^{-13} s. Thus, as soon as an electron is injected into the base a hole is created to neutralize it. This process results in a build up of the electron-hole pair density in the base and continues until equilibrium is reached. The turn-on current transients for a 35-W, single diffused transistor with a 1.5 mil (60 μm) wide base are shown in figure II-2. During the period of charge build-up, the electron current into the base from the emitter is much larger than the electron current leaving the base for the collector, and holes flow into the active region of the base, under the emitter-base junction. Outside the active region the base is thin and long relative to its width. The charge flow across the extrinsic base

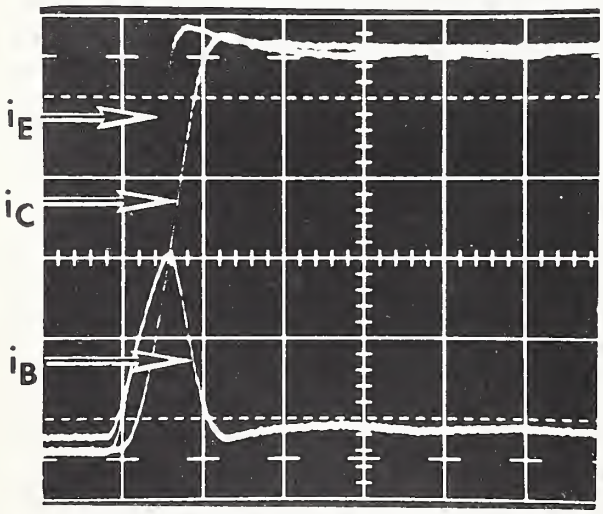


Figure II-2. Turn-on base, emitter, and collector current transients. (Horizontal scale: 1 μs/div. Vertical scale: 200 mA/div.)

resistance associated with this region results in a potential drop such that the edge of the active region of the transistor is negative with respect to the base contact. Lateral hole flow across the intrinsic base resistance within the active region, causes an additional potential drop across the emitter-base junction; this potential drop is, of course, in the same direction. It acts to debias the center of the junction and causes the familiar current crowding phenomenon which forces the emitter current to the outer periphery of the junction.

Equilibrium is established when the excess hole-electron pair density in the base region reaches the value appropriate to the injected electron current from the emitter. In equilibrium, holes still flow from the base contact to the active region in order to supply holes for recombination with electrons in the base (base transport losses) and for injection into the emitter (injection efficiency losses). The current associated with these losses is much smaller than either the peak base current during turn-on or the steady-state emitter current. In the example shown in figure II-2, the equilibrium base current is 15 mA while the peak base current is approximately 450 mA and the steady-state emitter and collector currents are about 1 A.

Turn-off Transient — When the transistor emitter circuit is opened, electron injection into the base from the emitter decreases. However, the excess carrier density which causes the concentration gradient associated with the diffusion of electrons toward the collector does not change instantaneously; hence, electrons continue diffusing toward the collector-base junction where they are swept out of the base region. This results in a reduction of the electron density in the base which must be accompanied by a reduction of the hole density in order to maintain charge neutrality. Consequently, holes must flow out from the active region of the transistor to the base contact. This flow is in the opposite direction to the flow during the turn-on transient and sets up a potential gradient across the extrinsic base resistance such that the active region of the transistor is positive with respect to the contact. The most positive portion of the base can approach the potential of the collector region.

The simplest turn-off transient occurs for collector-base voltage well below the breakdown voltage of the emitter base junction. To illustrate this case, the current and base emitter voltage turn-off transients are shown for a collector voltage of about 10 V in figure II-3. The switch S_1 in the test circuit (figure II-1) was set to position 1 so that the protective circuit is not connected. When turn-off begins, as evidenced by a decrease in i_E, v_{EB} begins to rise toward zero from a small negative potential. At the same time, i_B decreases from a small positive value to zero and then increases to a negative value of approximately 165 mA. During this same period i_E begins to decrease rather rapidly, but the collector current does not begin to decrease rapidly until about 0.2 μs after i_E starts to decrease. During this 0.2-μs period, i_B increases in the reverse direction in such a way as to be always equal to

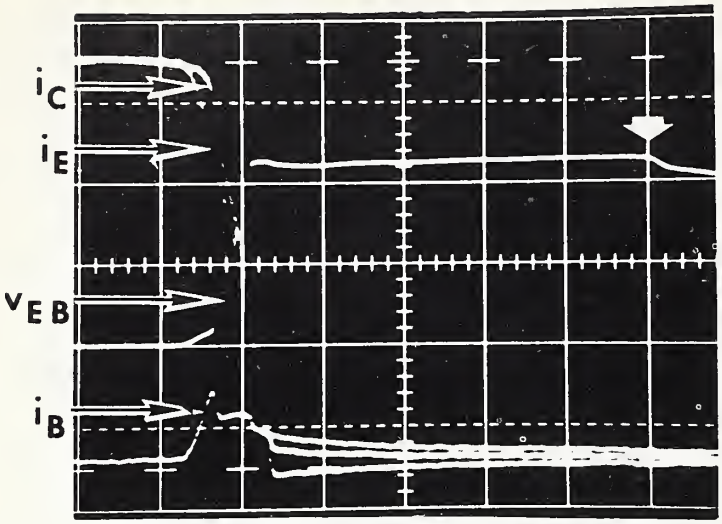


Figure II-3. Turn-off emitter-base voltage and base, emitter, and collector current transients for collector-base voltage less than emitter-base junction breakdown voltage. ($V_{CC} \approx 10$ V. Horizontal scale: 1 μs/div. Vertical scales: 5 V/div (v_{EB}); 200 mA/div (i).)

the difference between the magnitudes of i_C and i_E. The action of the currents and the reverse-biased emitter-base voltage during this time period can be explained as follows. Since the injection rate of electrons from the emitter is being reduced while for a time the extraction rate of electrons at the collector remains unchanged, holes must flow out of the active region of the device toward the base contact through the extrinsic base resistance. Since both i_B and v_{EB} increase linearly during this period, it appears that the extrinsic base resistance is constant as one would expect.

About the time i_C begins to decrease significantly, i_B also begins to decrease. Since v_{EB} continues to increase even more rapidly, this suggests that the base resistance is increasing. This could occur if the active area of the emitter changed from the periphery to the central core. Such a change is in accord with the direction of hole flow; in contrast to the situation encountered during turn-on the outer regions of the emitter tend to be debiased. Next i_B stabilizes for a time while v_{EB} continues to increase; then when v_{EB} reaches its maximum value (limited by the collector voltage), i_B decreases toward its new steady-state value (in the present case, zero). At long times, after i_B, i_E, and i_C reach their new steady-state values, v_{EB} begins to decrease to zero or, if $i_E \neq 0$, a small value of forward bias. This is also illustrated in figure II-3 (see arrow).

If a higher value of collector voltage is applied, again with the protective circuit not connected, the turn-off transients begin in the same fashion, but when v_{EB} reaches a value near the breakdown voltage of the emitter-base junction it ceases to rise significantly and i_B increases abruptly as illustrated in figure II-4. This abrupt increase in i_B is due to the onset of breakdown at the periphery of the emitter-base junction. The active region of the transistor has been pinched in toward the center of the emitter area by virtue of the hole flow out to the base lead as discussed

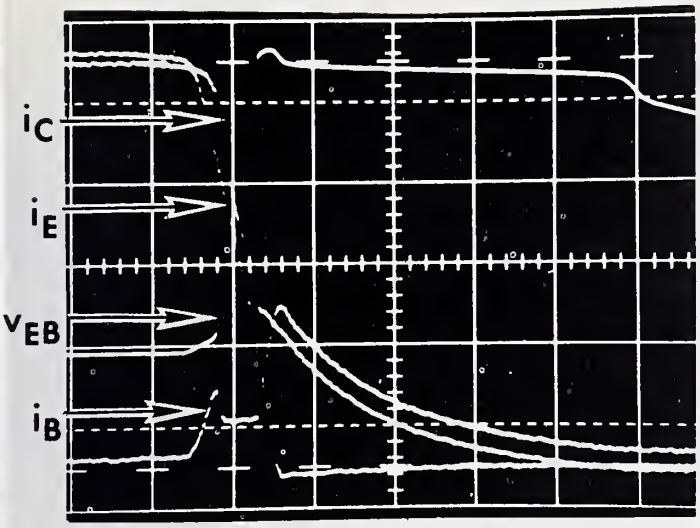


Figure II-4. Turn-off emitter-base voltage and base, emitter, and collector current transients for collector-base voltage greater than emitter-base junction breakdown voltage, without protective circuit. ($V_{CC} \approx 20$ V. Horizontal scale: 1 μs/div. Vertical scales: 5 V/div (v_{EB}); 200 mA/div (i).)

above. In this central region the emitter-base junction is forward biased so the emitter potential is only a fraction of a volt more negative than the potential in the central base region. Since the emitter is a low-resistance element the entire emitter is at approximately the same potential. However, the base contact is much more negative than the central region of the base because of the resistive drop associated with the lateral hole flow through the base. As a result, except for the central active area, the emitter-bias junction is reverse biased; this bias can increase until its value at the periphery reaches the limit imposed by the collector voltage or the junction breakdown voltage, whichever is lower. In the latter case, there is a substantial flow of electrons from the base contact, laterally across the extrinsic base resistance, into the emitter across the reverse-biased junction at the periphery, through the emitter layer, to the central region of the emitter where they join the injected electrons from the emitter circuit in crossing the forward-biased portion of the junction, through the base, and into the collector. These electrons serve to retard the rate of decrease of the collector current as can be seen in figure II-4.

This model can be verified by considering the transients in the case where the zener diode protective circuit is included and the collector voltage is greater than the zener voltage. In this case as illustrated in figure II-5 it is possible to separate the current through the base region and the current through the zener diode which breaks down in much the same way as the peripheral region of the emitter-base junction in the previous case. The i_B transient, which consists of holes leaving the active region of the base, is very similar to the i_B transient when breakdown of the emitter-base junction does not occur (figure II-3), while the i_T transient, which is the sum of the base and zener currents, is very similar to the i_B transient when breakdown occurs (figure II-4). Note that in this case, the zener current also influences i_E in

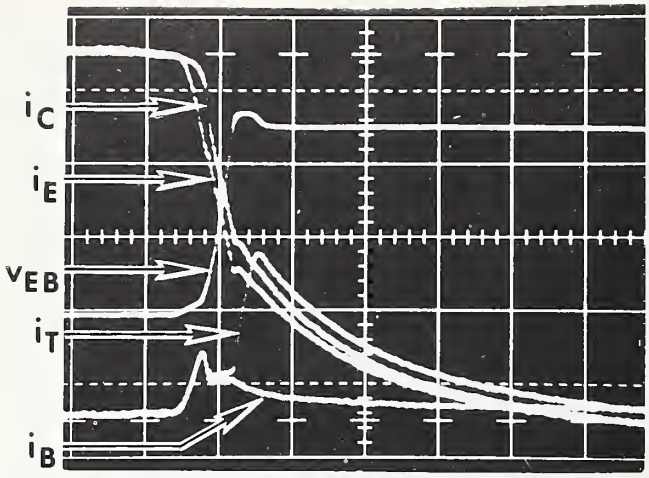


Figure II-5. Turn-off emitter base voltage and base, emitter, and collector current transients for collector-base voltage greater than emitter-base junction breakdown voltage with a 12-V zener diode protective circuit. ($V_{CC} \approx 20$ V. Horizontal scale: 1 μs/div. Vertical scales: 5 V/div (v_{EB}); 200 mA/div (i).)

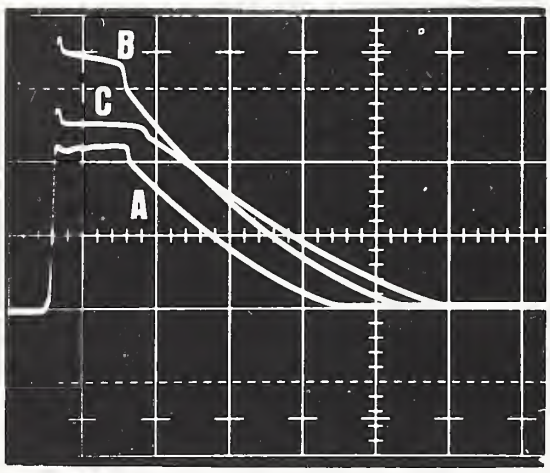


Figure II-6. Turn-off emitter-base voltage transients. (A: $V_{CC} \approx 10$ V, no protective circuit. B: $V_{CC} \approx 20$ V, no protective circuit. C: $V_{CC} \approx 20$ V, 12-V zener diode protective circuit. Horizontal scale: 5 μs/div. Vertical scale: 5 V/div.)

contrast to the previous case. With the protective circuit, the fall of v_{EB} is somewhat delayed. This can be seen more clearly in the traces presented in figure II-6 which cover a longer time period.

As a final observation, it should be noted that the rate of decay of the v_{EB} transient depends primarily on the nature of the external circuit and not on the device properties. In particular, inclusion of the low-level emitter current supply used for thermal resistance measurements substantially increases the rate of decay.

REFERENCE

1. Verway, J. F., On the Mechanism of h_{FE} Degradation by Emitter-Base Reverse Current Stress, *Microelectronics and Reliability* 9, 425-432 (1970).

APPENDIX III

Detailed Description of Test Circuitry

The instrumentation to implement the measurement of transistor thermal resistance using the emitter-only switching technique, in which the forward-biased emitter-base junction is used as the TSP, is described in this section. This includes a description of the basic test circuit itself as well as a description of the clock pulse generator, the sample-and-hold circuit, the temperature controller, and the temperature-controlled water-cooled heat sink. The description which follows is for the purpose of presenting an operating system in sufficient detail to allow duplication. However, it should be emphasized that the instrumentation being described may not represent an optimized system.

III.1 Basic Circuit for Thermal Resistance Measurements

The complete circuit diagram of the thermal resistance test system used for measuring the thermal resistance of *npn* transistors with the exception of the heat-sink temperature controller is given in figure III-1. A floating constant-voltage power supply V_{CC} is connected between collector and ground via a precision power resistor R_C, which is used to monitor the collector current. The parallel capacitor C_C serves to absorb the switching transient which occurs when the collector current drops from the heating value to the measuring value. The lossy torroid on the emitter lead is an oscillation suppressor. The speedup diode D_1 and the diode switch D_2 should be placed close to the emitter of the DUT. The ground connections for the DUT and associated equipment should all have a common ground on a low impedance copper strap placed close to the base lead of the DUT. The problem of switching transients in the V_{EE} supply is not as serious as those in the collector supply, since V_{EE} is disconnected during the measuring interval. Further, the low (4-Hz) repetition rate allows leeway in the recovery time of V_{EE} because the transients occur for such a small portion of the heating time of the DUT. The recovery time transients are not important because no measurements are made while they exist.

The parallel emitter switch (transistors Q_1 and Q_2), which can handle 4A of emitter current, is shown in detail. For higher currents, more transistors can be paralleled or, preferably, higher current transistors should be used. Mechanically, the two transistors are mounted on a heat sink cooled by tap water. The water cooling is used to reduce the size of the heat sink so that the switch can be placed in reasonable proximity to the DUT. A single high current Darlington could be used where higher currents create the need for a preamplifier to drive the emitter switching transistor, since the use of two diodes in series (the series switch D_2 and the speedup diode D_1) ensures emitter current cutoff even though the saturation voltage of a Darlington is greater than that of a single transistor stage. As discussed in Appendix II, the turnoff speed of the DUT is proportional to the forward drop of the series combination of D_1

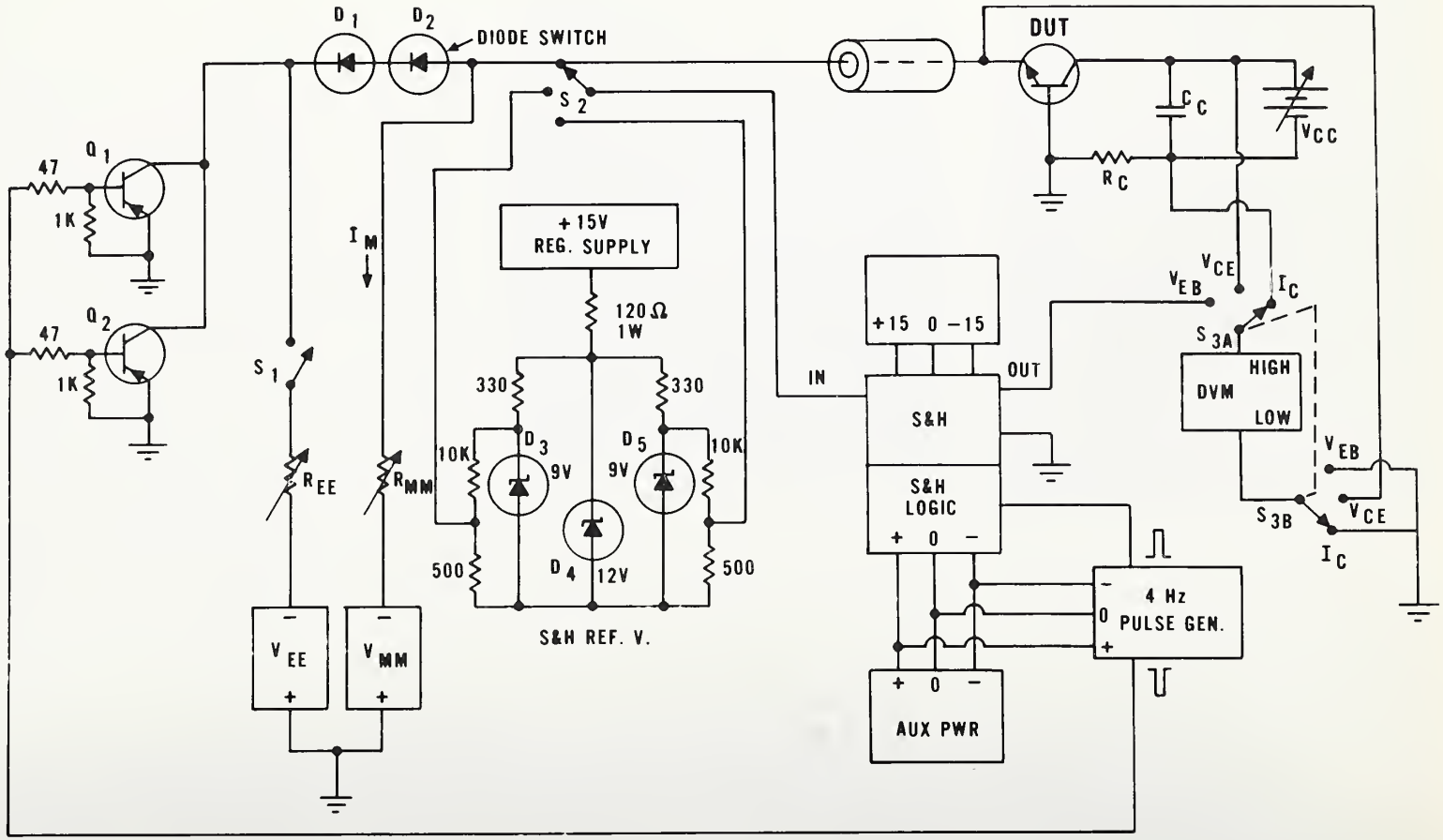


Figure III-1. Basic test circuit for measuring the thermal resistance of *npn* transistors.

and D_2. This switching speed can be increased if D_1 is a regulator (zener) diode with a breakdown voltage less than the reverse-biased breakdown voltage of the emitter-base junction of the DUT. However, if the extrapolation procedure for measuring the thermal resistance is used, the high power regulator diode is not needed and a single forward-biased diode can be used as the speedup diode D_1. The use of a water-cooled heat sink may still be desirable to minimize changes in the diode electrical characteristics. The variable emitter-resistor R_{EE}, composed of a group of parallel resistors, is mounted on a separate tap-water-cooled heat sink. This is done for economy of space since the physical size of the resistors would be much greater if they were not cooled. Both V_{EE} and V_{MM} along with their associated variable resistors function as constant current supplies.

III.2 Clock Pulse Generator

The 4-Hz pulse generator circuit is shown in detail in figure III-2. Commercial generators have also been used and are quite satisfactory, but they included a great deal of versatility which is not required in this operation. Further, the use of common power sources for the pulse generator and other devices simplified the overall test unit construction. A unijunction relaxation oscillator Q_1 generates a 4-Hz pulse which is amplified by Q_2, fed to the one shot 74121 whose pulse width is governed by the time constant of R_7C_3. The negative going output pulse is fed from pin one of 74121 to amplifier inverter Q_4 whose positive pulse is fed to the test unit via emitter follower Q_6. The output of Q_4 is also fed to amplifier inverter Q_3 which drives amplifier Q_5. Because Q_5 is a *pnp* transistor, a positive going input signal will turn the transistor off and give a negative going output signal which is amplified by the emitter-follower Q_7 and fed to the test unit. Capacitors C_4 and C_5 provide the energy storage needed by Q_6 and Q_7 to drive the test circuit of figure III-1 and should be 1 μF or larger. In particular, this energy storage is required to provide the charge needed to rapidly turn on the parallel emitter switching transistors. The positive supply is 7 V and the diodes D_1,D_2 and the regulator diode-resistor combination D_3,R_6 are used to prevent overvoltage damage to the one shot. Switch S_1 disconnects the unijunction relaxation oxcillator, while switch S_2 in conjunction with resistor R_4 provides a means for single pulse operation. This operation is helpful in making some experimental measurements and in troubleshooting the equipment.

III.3 Sample-and-Hold Unit

The sample-and-hold (S&H) circuit diagram is shown in figure III-3. The sample-and-hold unit and its logic are placed in an aluminum case and the case is connected to the common ground of the ±15 V supply. It differs from most commercially available units in that it uses a large integrating capacitor and is therefore basically slow. It therefore tends to average out the noise in the sampled signal and gives excellent repeatability. Since the thermal measurements being made are inherently

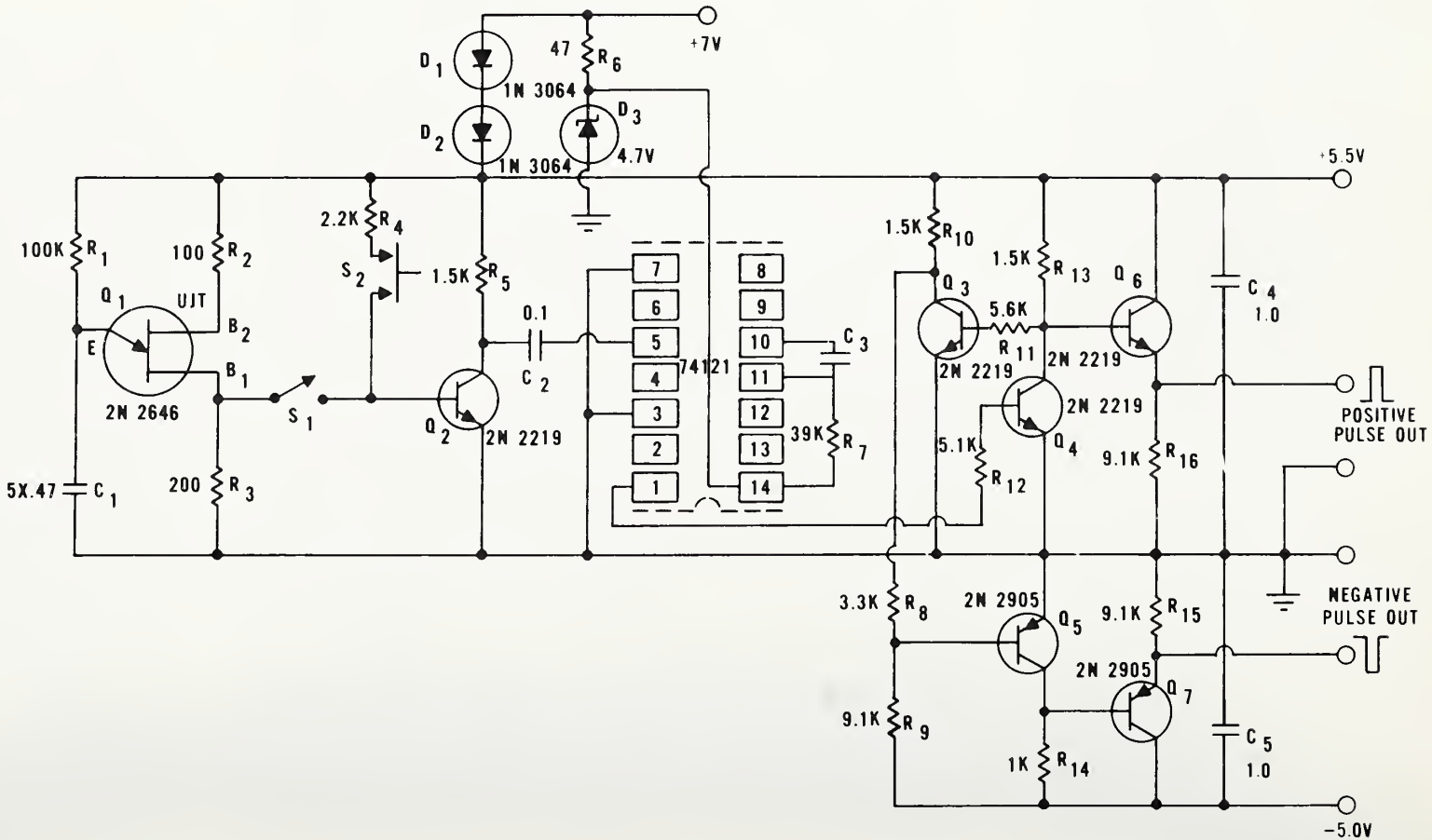


Figure III-2. Clock pulse generator.

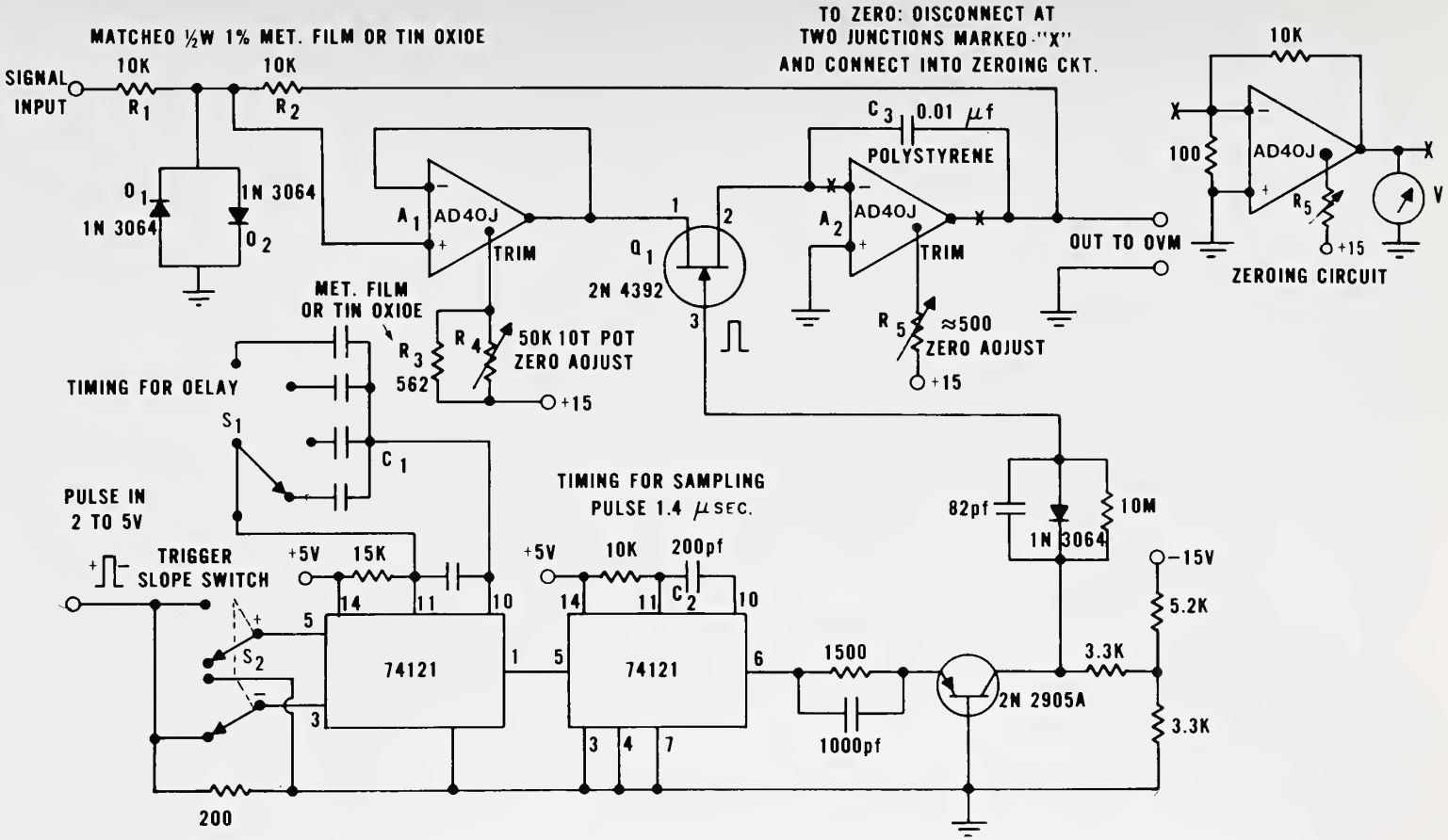


Figure III-3. Sample-and-hold unit.

slow (it is necessary to wait for thermal stabilization of the DUT whenever the dissipation is changed or whenever the DUT is replaced), the settling time of the S&H (of the order of seconds) is not detrimental. For a test method designed exclusively for rapid production line testing, an S&H with a fast acquisition time would be required.

The S&H as now constituted uses low-cost operational amplifiers which take considerable time to stabilize when first activated. Further, they are subject to some drift with time. To provide some method of monitoring the condition of the S&H unit, a separate reference voltage circuit (fig. III-1) consisting of regulator diode D_4 and two separate reference diodes D_3 and D_5 was added to the original test unit. These two reference sources provide a measurement of the degree of equilibrium and drift of the S&H. Two diodes were used so that a malfunction in one would not indicate a malfunction in the S&H.

The logic for the S&H unit consists of two 74121 one shots in tandem. The first one shot sets the delay time and the second one shot, triggered by the trailing edge of the output pulse of the first one shot, operates the FET gate Q_1. The S&H consists of two operational amplifiers. The input amplifier A_1 is a voltage follower which drives the integrating amplifier A_2. This allows the use of a large integrating capacitor C_3. The input resistors R_1 and R_2 set the gain and should be stable (temperature coefficient of 100 ppm/°C or less). Metal film or tin oxide resistors are recommended.

It is necessary to adjust the S&H for unity gain by trimming one of the input resistors with a parallel resistor if the utmost accuracy is desired. The two amplifiers used (A_1 and A_2) have to be zeroed prior to use of the circuit. The integrating amplifier A_2 is zeroed by opening the input and output, replacing the integrating capacitor C_3 by a 10-kΩ resistor, putting a 100-Ω resistor between the input terminals, and monitoring the output terminals while the trimming resistor is adjusted for minimum output. Once adjusted, further zeroing of A_2 is unnecessary and the variable resistor can be replaced by a fixed resistor of equal magnitude. A useful procedure for accomplishing this consists of installing a 50-kΩ potentiometer in parallel with a 562-Ω resistor; after the potentiometer is adjusted to determine the proper value, a fixed trimming resistor of this value is substituted for it. After A_2 is zeroed, it is reconnected and then A_1 is zeroed by shorting its input and monitoring the S&H output using the DVM. This latter zeroing process is not permanent, and thus an arrangement should be provided for rezeroing the 50-kΩ potentiometer, R_4, whenever necessary. It is best to check the zero before each run. Amplifiers with improved temperature coefficients and offset characteristics would reduce the need for rezeroing.

III.4 Temperature Controller

The temperature controller is shown in simplified form in figure III-4 and in detail in figure III-5. Referring to the simplified diagram of figure III-4, one sees a reference voltage on the left picked

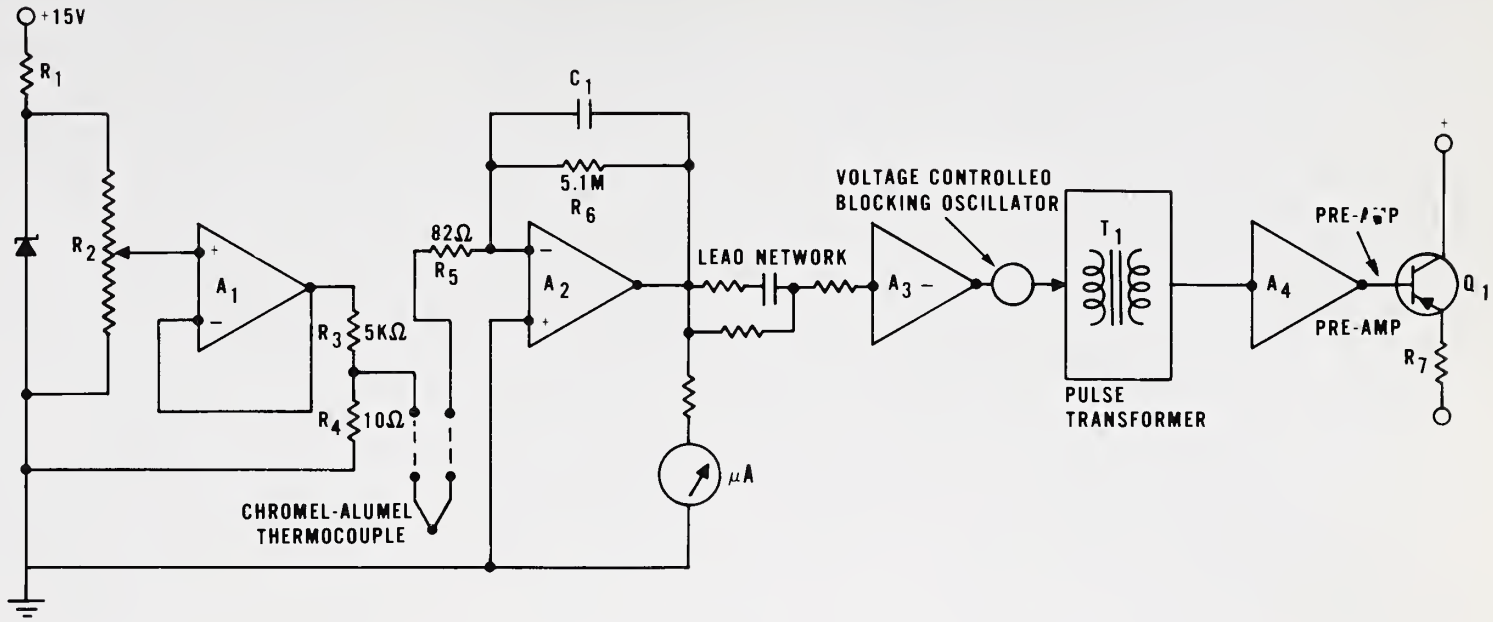


Figure III-4. Simplified diagram of temperature controller.

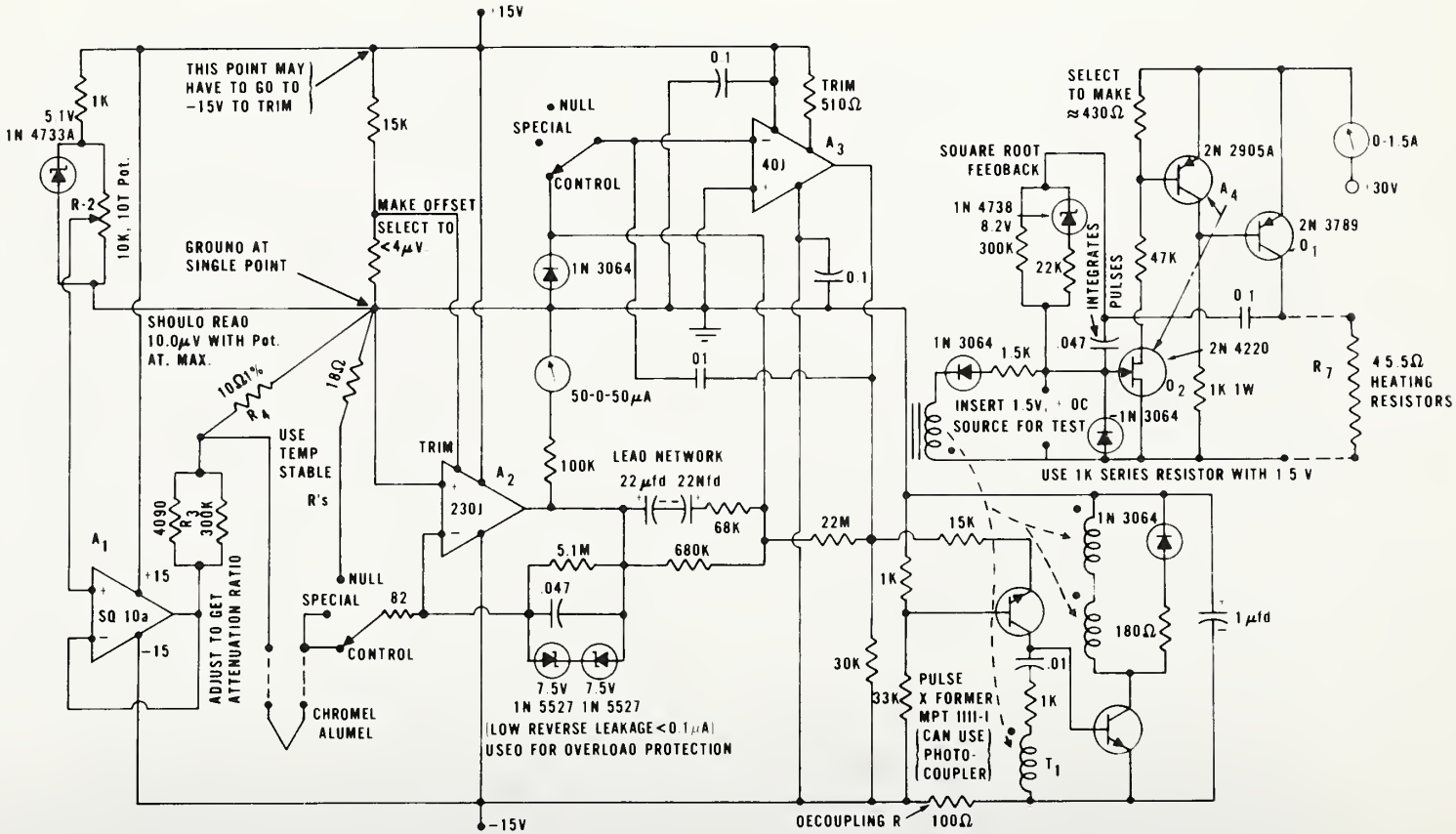


Figure III-5. Complete circuit diagram of the temperature controller.

off in part by the potentiometer R_2 which is isolated from its load by voltage follower A_1 which drives voltage divider R_3,R_4. The low voltage across R_4, which is set by potentiometer R_2, is bucked against the thermal emf generated by the chromel-alumel thermocouple. The difference voltage is amplified by the chopper-stabilized operational amplifier A_2, whose output controls the repetition rate of a blocking oscillator via a lead network and amplifier A_3. The blocking oscillator operates together with pulse transformer T_1 to isolate the temperature sensing from the power circuits of the heat-sink temperature regulator. This allows the thermocouple to be soldered directly to the copper washer or to a transistor case despite elevated voltage. The output amplifier A_4, consisting of two discrete transistors, drives transistor Q_1 which in turn controls the heating power for the heat-sink resistors, R_7. In the circuit shown, the resistor R_7 consists of two parallel 5-W, 91-Ω ceramic-insulated wire-wound resistors. The blocking oscillator output consists of 15-μs pulses. Networks in A_4 integrate the pulses to provide a drive for Q_1. Now Q_1 drives R_7 according to a square law since, if the output is doubled, both the current and voltage double so that the resistor dissipation is quadrupled. To linearize this characteristic to provide smoother control, a feedback circuit consisting of two resistors and a regulator diode was used to approximate a square root function so as to provide linear control. This network is shown between the collector of output transistor Q_1 and the gate of FET transistor Q_2 in figure III-5.

The complete schematic of figure III-5 has notations helpful to those who desire to duplicate it. As noted on the schematic, several simplifying construction techniques can be applied. The distinguishing features of this controller lie in the floating input which can be duplicated by using commercially available isolation amplifiers and the feedback network around A_2 which has to be adjusted for optimum response for each heat-sink configuration. In general, the time required to ensure DUT stabilization was such that a single feedback network sufficed.

III.5 Hydraulic System

The temperature-controlled heat sink and associated apparatus are shown in figure III-6. Tap water is used to fill an elevated container which acts as a constant pressure source. This simple device eliminates the effects of the varying pressure experienced with most tap water sources. The water from the constant pressure tank flows through a chilled-water heat exchanger via a pressure monitor to the heat sink and out to the tap water sink. Tap water is also used to cool the heat sinks on which the emitter resistors, the speedup diode, and the emitter parallel switches are mounted. This tap water is not regulated in pressure because the heat-sink temperature in these cases is not critical.

The chilled water in the heat exchanger is used to allow measurements with a heat-sink temperature of 25°C since this is specified in most military and commercial documents.

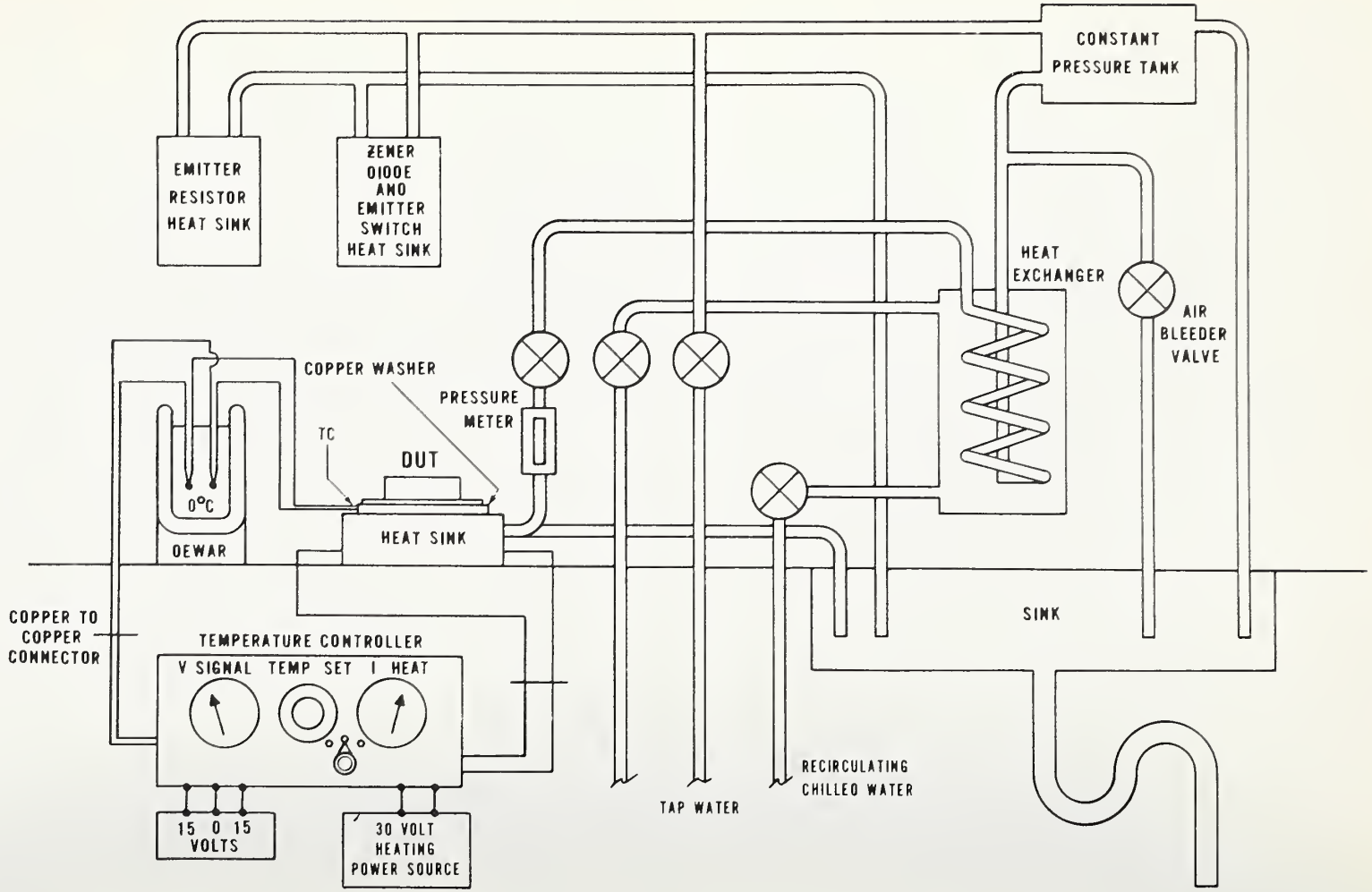


Figure III-6. Water flow diagram for the temperature-controlled heat sink and associated cooling functions.

III.6 Temperature-Controlled Heat Sink

The temperature-controlled heat sink includes resistance heaters which work in conjunction with continuously running coolant water to keep the heat sink temperature constant. The sensing thermocouple is placed in the upper side of a standard copper washer used to monitor the case temperature of the DUT. This mounting surface technique for measuring the case temperature is nondestructive and is generally as repeatable as sensing a point directly on the device case. It should be noted that case temperature and mounting surface temperature are sometimes used interchangeably.

A typical heat sink with its associated copper washer is shown in figures III-7 and III-8, respectively. The copper washer shown is used for a TO-3 transistor case outline and is constructed according to EIA recommended practices [1]. The heat sink itself has a two-level cooling-water path, two servo-controlled, 5-W heating resistors, and a third line-operated, 50-W resistor which is included for manual operation when fast heating is desired for a temperature calibration run. The 50-W resistor is operated from a 115-V adjustable-output-voltage transformer.

The three drawings on the left side of figure III-7 are simplified representations which do not include the details of the resistor cavities. The center left drawing is a top view of the heat sink while the top and bottom drawings are sections through the top and bottom water channel levels, respectively. The center-of-page drawing is an end view showing the entrance to the servo-controlled resistor cavities in addition to the water channel plugs and openings. The top right drawing shows the water channels and an end view of the 50-W resistor cavity including a small air hole which eases the insertion of the resistor when it has been coated with a thermal heat-sinking compound. The right center and bottom drawings are a bottom and side view of the heat sink. The bottom view drawing includes complete details of the heat sink with the servo-controlled heater cavities and their connector wire lead openings shown dotted along with the 50-W resistor cavity and the cooling water channels. The right bottom drawing shows how the servo-controlled resistor lead wires angle out the bottom of the heat sink. The three 6-32 tapped holes on the right center drawing are used for mounting the heat sink to insulated ceramic standoffs. The plugs used in the fabrication of the water channels are silver soldered to allow high temperature operation during calibration runs. Gold-plated phosphor-bronze contact pins are held in place by glass-filled, free flowing, non-copper-corrosive silicone rubber. The copper washer can be attached directly to the heat sink surface with silicone rubber, after applying a thin coating of zinc-oxide-loaded silicone thermal grease to the heat sink and the washer contacting surfaces. In instances where it is desired to keep the collector potential off the heat sink, a beryllium oxide washer can be placed (after coating both sides with thermal grease) between the heat sink and the copper washer. For this case the mounting screws for the transistor must be insulated with a high-temperature-compatible spaghetti, and an insulated bottom plate containing captive nuts must be

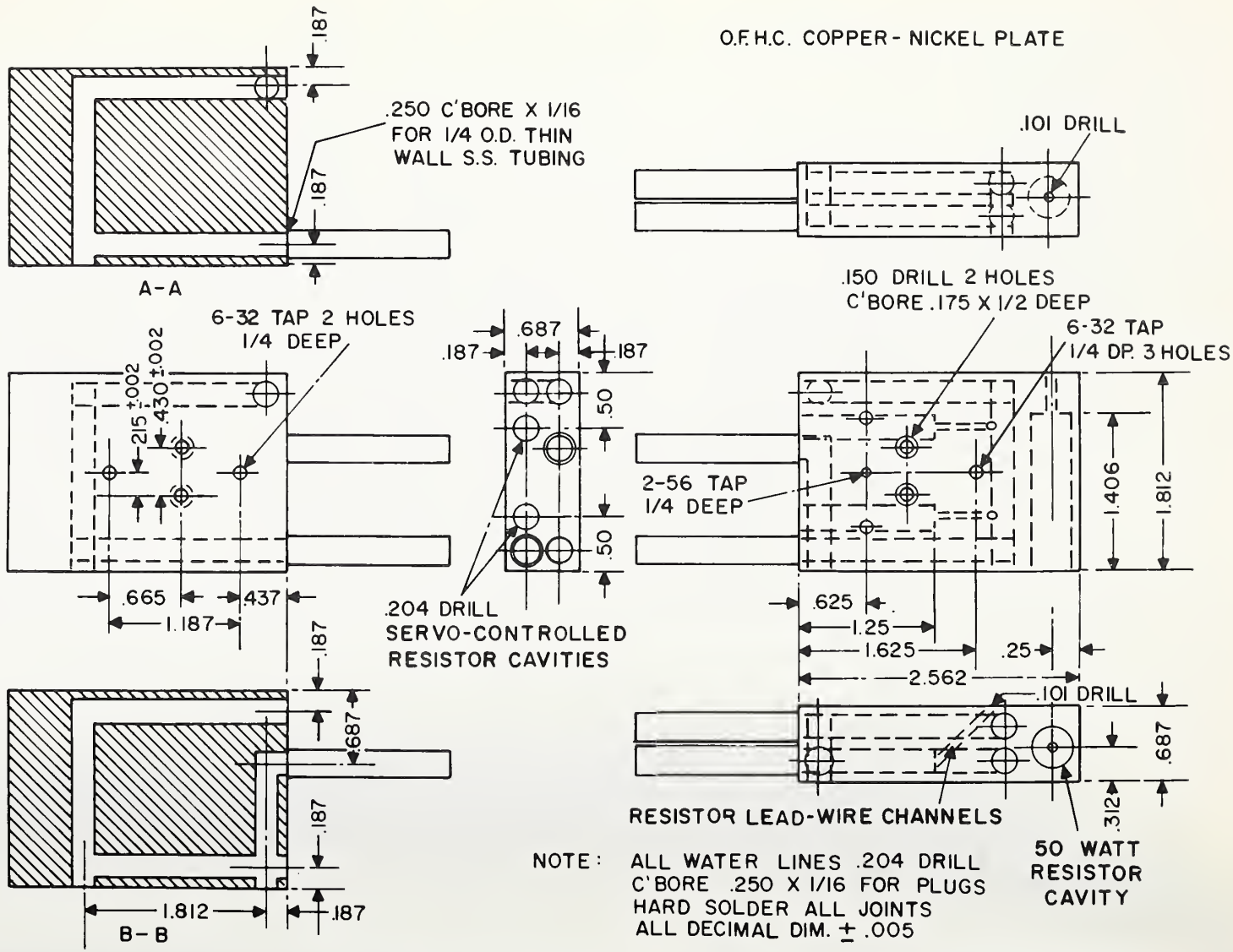


Figure III-7. Construction of a temperature-controlled heat sink. (All dimensions in inches)

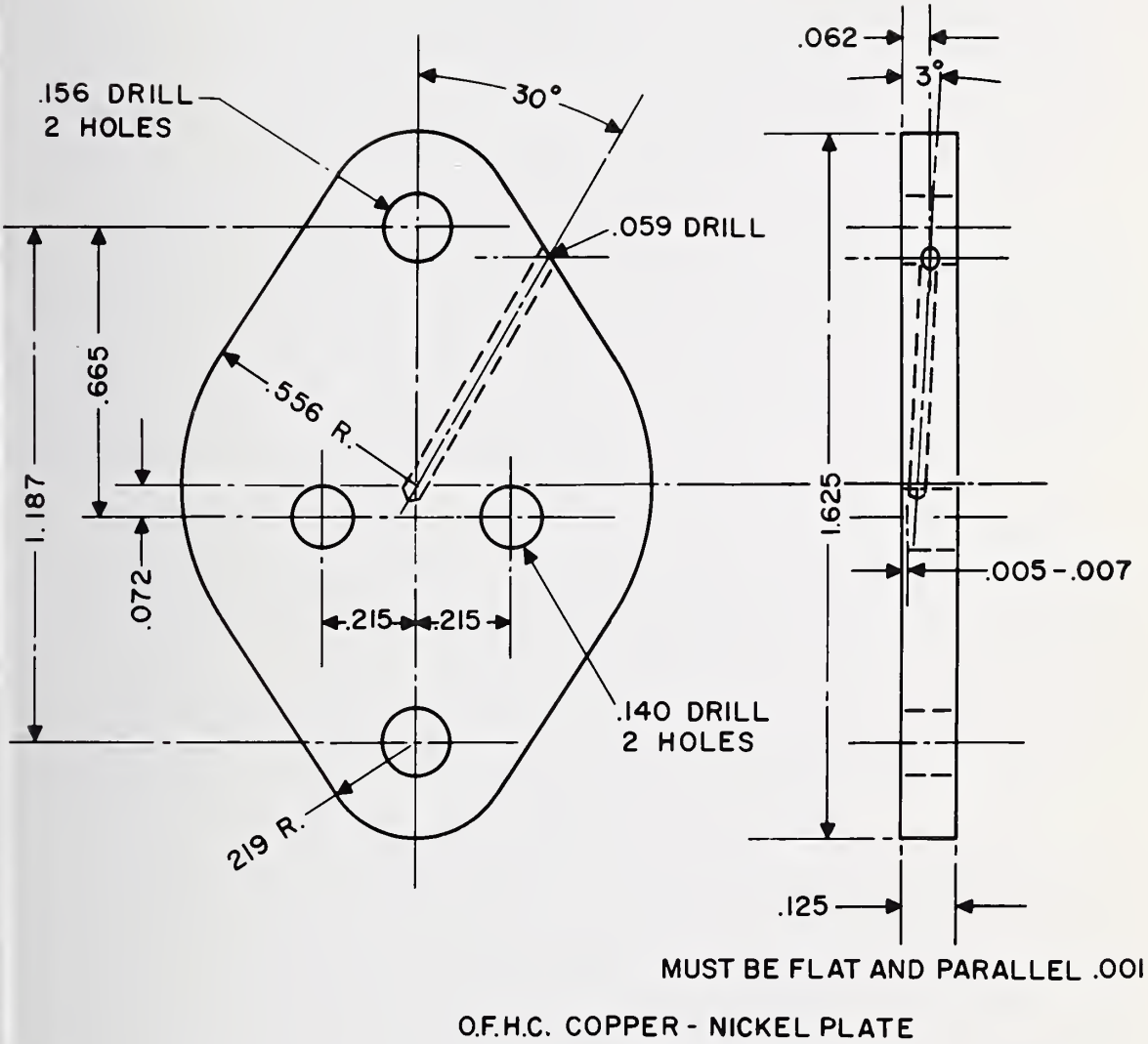


Figure III-8. Typical mounting washer for a TO-3 encased transistor. (All dimensions in inches)

provided for tightening the mounting screws. This necessitates larger holes in the heat sink for the mounting screws.

Reference

1. Thermal Resistance Measurements of Conduction Cooled Power Transistors, EIA Recommended Standard RS-313-B (Revision of RS-313-A), October 1975 (Electronics Industries Association, 2001 Eye Street, N.W., Washington, D. C. 20006). [This reference can be found in Appendix I of this report.]

APPENDIX IV

Single-Operator, Single-Laboratory Repeatability Measurements*

Long-term single-operator measurements were undertaken to check the repeatability of the equipment for measuring thermal resistance of transistors by the emitter-only switching technique. During a ten-week period, 12 to 15 sets of measurements were made on seven test devices at a case temperature of 25°C and 22 sets of measurements on three test devices at a case temperature of 60°C. Two devices (lot A) were single-diffused transistors in TO-66 cases, two devices (lot NM) were epitaxial transistors in TO-66 cases, and three devices (lot AA) were single-diffused transistors in TO-3 cases.

The test conditions were chosen to provide sufficient power dissipation to ensure a reasonable rise in junction temperature but not enough power or voltage to cause significant current crowding. Heating current was 1 A for the devices in TO-66 cases (lots NM and A) and 2 A for the devices in TO-3 cases (lot AA). In both instances, the collector-emitter voltage was 20 V. A measuring current, I_M, of 6 mA was used. Measurements were made with the circuit shown in figure 1b of section 4.2 which utilizes parallel-switching techniques.

The case temperature was measured using the washer technique in which a thermocouple is embedded in the nickel-plated copper washer at a location underneath the chip approximately 50 μm below the case-washer interface. All devices were tested with a case temperature of 25°C while the TO-3 encased devices were also tested with a case temperature of 60°C.

The results of the measurements obtained for a delay time of 10 μs for the lots NM and AA devices and 20 μs for the lot A devices are listed in table IV-1. Since more than one device of each type was measured, the results for the individual device types are pooled.

The data also indicate that for the TO-66 encased devices the sample standard deviation was nearly constant even though the thermal resistance varied from 2.5 to 5.6°C/W. For the TO-3 encased devices, even though the thermal resistance was measured at case temperatures of 25 and 60°C, the sample standard deviation was also constant. If the measured thermal resistance is multiplied by the heating power, the sample standard deviation of the resulting junction-to-case temperature difference ranges from 0.4 to 0.6°C for the parallel emitter switching technique. Thus, these measurements indicate that the repeatability is nearly independent of the magnitude of the measured thermal resistance but is limited by a minimum resolvable junction-to-case temperature difference.

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* Extracted from Methods of Measurement for Semiconductor Materials, Process Control, and Devices (Quarterly Report for Period April 1 to June 30, 1973), NBS Tech. Note 806, W. M. Bullis, Ed, pp. 51-53.

Table IV-1

Pooled Results of Thermal Resistance
Repeatability Experiment

Lot Number	Case Temperature (°C)	Thermal Resistance (°C/W)
NM	25	5.57 ± 0.03
A	25	2.53 ± 0.03
AA	25	0.75 ± 0.01
AA	60	0.78 ± 0.01

APPENDIX V

Equivalency of Symbols in Commercial and Military Thermal Resistance Test Methods

In EIA RS-313-B [1], the junction-to-reference point thermal resistance is given as:

$$R_{\theta JR} = \frac{V_{M2} - V_{MC} \text{ (for } T_{MC} = T_R)}{DP_2} \cdot \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{Calibration}}, \qquad \text{(V-1)}$$

while in MIL-STD-750B, Notice 9, Method 3131.1 [2], the junction-to-reference point thermal resistance is given as:

$$R_{\theta JR} = \frac{V_{MH} - V_{MC} \text{ (for } T_{MC} = T_R)}{DP_H} \cdot \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{Calibration}}. \qquad \text{(V-2)}$$

A list of equivalent symbols used in the two test methods as they refer to eqs (V-1) and (V-2) is given in table V-1.

References

1. Thermal Resistance Measurements of Conduction Cooled Power Transistors, EIA Recommended Standard RS-313-B (Revision of RS-313-A), October 1975 (Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20006). [This reference can be found in Appendix I of this report.]

2. Method 3131.1, Thermal Resistance, Test Methods for Semiconductor Devices, MIL-STD-750B, Notice 9, dated September 19, 1978 (Department of Defense, Washington, DC 20301).

Table V-1

Equivalency of Symbols Used in the Measurement of Thermal Resistance Using Various Standard Techniques

EIA RS-313-B	MIL-STD-750B, Method 3131.1
V_{M2}	V_{MH}
P_2	P_H
P_1[a]	P_C
V_{M1}	V_{MC}
$K \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]_{\text{Calibration}}$[b]	K

[a] If P_1 is equal to the power dissipation during calibration, then P_1 equals P_C in Method 3131.1.

[b] In the text of this report, $K \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]_{\text{Calibration}}$ is denoted K'.

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