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Semiconductor Measurement Technology:

Thermal Resistance Measurements

F. F. Oettinger and D. L. Blackburn

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Semiconductor Measurement Technology:

Thermal Resistance Measurements

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Semiconductor Measurement Technology:
THERMAL RESISTANCE MEASUREMENTS

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Semiconductor Measurement Technology:
THERMAL RESISTANCE MEASUREMENTS

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Abstract

This Special Publication reviews the thermal properties of power transistors and integrated circuits and discusses methods for characterizing these properties. The discrete devices discussed include bipolar transistors and metal-oxide-semiconductor field-effect-transistors. Measurement problems common to these devices, such as deciding the reason for requiring a particular measurement, adequate reference temperature control, selection of a temperature-sensitive electrical parameter, and separation of electrical and thermal effects during measurement are addressed. Due to the inherent difficulties in measuring and analyzing the thermal properties of active integrated circuits, an approach using specifically designed thermal test chips for evaluation of new die-attachment and packaging schemes is finding wide acceptance in the industry. In this Special Publication, indirect (i.e., electrical) measurements, direct (e.g., infrared) measurements, and computer simulation techniques for thermally characterizing integrated circuits are discussed in terms of their usefulness in characterizing VLSI packages.

Key words: integrated circuits; junction temperature; power transistors; safe-operating-area limits; temperature-sensitive electrical parameter; thermal measurements; thermal resistance; thermal test chips.

Disclaimer: Certain commercial equipment, instruments, or materials are identified in this paper in order to specify adequately the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

I. POWER TRANSISTORS [1,2]

Introduction

Accurate characterization of the thermal properties of power transistors is critical to the reliability of the systems using these devices. Failure of a single power device can shut down a computer, bring to a halt a motor-driven system, or stop a vehicle dead in its tracks. Power devices are often expected to run hotter than other components, but the excessive temperature rise of an inherently "bad" device that "slipped through" screening will lead to early, often catastrophic failure. Likewise, the absence of adequate thermal characterization information may cause an otherwise "good" device to be used in a circuit

that stresses it beyond its thermal limits.

The purpose of this section is to review the thermal properties of power transistors and to discuss methods for characterizing these properties. The devices discussed include bipolar transistors and metal-oxide-semiconductor field-effect-transistors (MOSFETs). Measurement problems common to these devices, such as deciding the reason for requiring a particular measurement, adequate reference temperature control, selection of a temperature-sensitive electrical parameter (TSEP), and separation of electrical and thermal effects during measurement are addressed. Finally, the needs for thermal characterization of evolving devices such as high voltage and power integrated circuits and merged bipolar/MOSFET devices are mentioned.

The Concept of Thermal Resistance

The concept of thermal resistance has been developed over the years as an aid to device manufacturers and users for calculating the junction temperature of operating devices. The concept is based upon an analogy between the electrical and thermal properties of materials, with temperature, heat flow, and thermal resistance being analogous to voltage, current, and electrical resistance, respectively. Thus, the equation

$$R_{\theta JR} \equiv \frac{T_J - T_R}{P} \tag{1}$$

where

$R_{\theta JR}$ = thermal resistance between the junction and the reference point (°C/W),

T_J, T_R = temperatures of the junction and the reference point, respectively, (°C), and

P = power dissipated (W),

are used to define the device thermal resistance.

In applying the electrical analogy to the thermal problem and in using eq (1), it is implicitly assumed that

1) the junction temperature is spatially uniform, and

2) $R_{\theta JR}$ is independent of the device operating conditions, i.e., independent of the values of collector current I_C and collector-emitter voltage V_{CE} used to obtain the power $P(P \approx I_C \times V_{CE})$.

Neither of these assumptions is valid for actual power transistors though, and care is needed in applying the results of eq (1) to real devices. The effect of these invalid assumptions on the defined and measured $R_{\theta JR}$ is discussed in the remainder of this section.

The Effect of Nonuniform Junction Temperature on the Definition of $R_{\theta JR}$ – The idealized isothermal temperature distribution upon which eq (1) is based is shown superposed upon a

more realistic nonisothermal temperature distribution in figure 1. The calculation of $R_{\theta JR}$ using eq (1) is straightforward for the isothermal case, but it is not immediately obvious how to apply the equation, or even if it is applicable, for the nonisothermal real-world case. This is because T_J is not well defined for the latter case in that it takes on a continuum of values between the peak junction temperature and the minimum junction temperature. For the concept of thermal resistance to be applicable to the real-world situation, some unique and meaningful value for T_J must be defined.

Because it is the peak junction temperature $T_{J(peak)}$ that is most important for predicting the reliability and safe operation of a device, $T_{J(peak)}$ is the most logical choice for use in place of T_J in eq (1) [3]. Thus, if eq (1) is rewritten as

$$R_{\theta JR(peak)} \equiv \frac{T_J(peak) - T_R}{P} \tag{2}$$

where $R_{\theta JR(peak)}$, the peak-junction-to-reference-point thermal resistance (°C/W), a unique and meaningful value of thermal resistance for any junction temperature distribution is defined. Unfortunately, all of the commonly used electrical methods for measuring junction temperature indicate some average temperature which is less than $T_{J(peak)}$ by an unknown amount. Thus, if $R_{\theta JR(peak)}$ is to be specified, some arbitrary correction factor usually must be applied to the measured value of $R_{\theta JR}$ to account for the difference between the measured junction temperature and the peak junction temperature. There appears to be no consistency in the application of the arbitrary correction factor in common practice, and the factor is often insufficient to ensure safe device operation.

The peak junction temperature of power transistors can be estimated using a modification of the standard electrical measurement method in conjunction with some simple mathematical procedures [4]. Thus, realistic values for $R_{\theta JR(peak)}$ can be determined without the need for arbitrary correction factors. A comparison of the actual peak thermal resistance as determined using an infrared microradiometer, that determined using the methods described in reference [4], and the average thermal resistance determined using the standard electrical technique is shown in table 1 for a number of devices and for a number of operating conditions. As can be seen in the table, a considerable difference may exist between the measured average thermal resistance and the peak thermal resistance.

Unfortunately, as also can be seen in table 1, the value of $R_{\theta JR(peak)}$ depends upon the device operating conditions. This is true even for different values of I_C and V_{CE} which give nearly the same (or even the same) value of power ($I_C \times V_{CE}$). Thus, even though a unique value of thermal resistance can be defined for a given set of operating conditions, it is unique only to those specific operating conditions.

The Variation of $R_{\theta JR}$ with Device Operating Conditions (I_C, V_{CE}) – The value of $R_{\theta JR(peak)}$ depends upon I_C and V_{CE} because the distribution of I_C throughout the device, and therefore the distribution of the power density, depends upon the device operating conditions [5,6]. An example of this can be seen in figure 2 for a 20-W planar power transistor which is dissipating 16 W of power for three different operating conditions. The device is coated

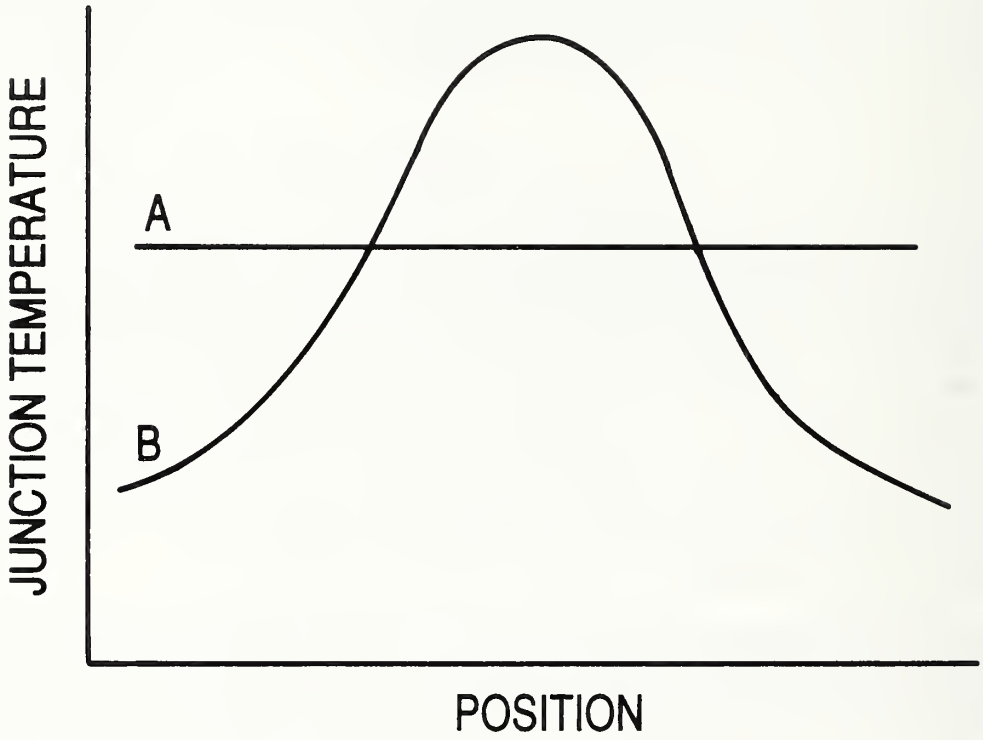


Figure 1. Idealized versus real-world temperature distribution for a power transistor. (A) idealized isothermal temperature distribution upon which the concept of thermal resistance is based; (B) more representative of the real-world temperature distribution for a power transistor.

TABLE 1

Comparison of Thermal Resistance
Measurement Techniques for a Bipolar Transistor

Device Number	Specified $R_{\theta JR}$ (°C/W)	Operating Condition $I_C(A)/V_{CE}(V)$	Power (W)	Measured Thermal Resistance (°C/W)		
				Standard Electrical	Electrical Peak Technique	Infrared Microradiometer
		0.1/170	17	8.5	12.5	14.6
		0.2/105	21	5.5	7.8	9.0
1	5	0.4/80	32	4.2	5.5	5.5
		1.0/54	54	3.0	3.5	3.4
		2.0/33	66	2.5	2.7	2.7
		0.2/140	28	2.9	4.1	4.6
		0.3/106	32	2.8	3.7	4.0
2	1.5	1.0/44	44	2.4	2.8	2.9
		2.0/38	76	1.9	2.1	2.1
		0.6/76	46	3.3	3.6	3.8
		1.0/50	50	3.0	3.3	3.4
3	7	2.0/28	56	3.0	3.4	3.2
		3.0/20	60	2.8	3.0	2.9

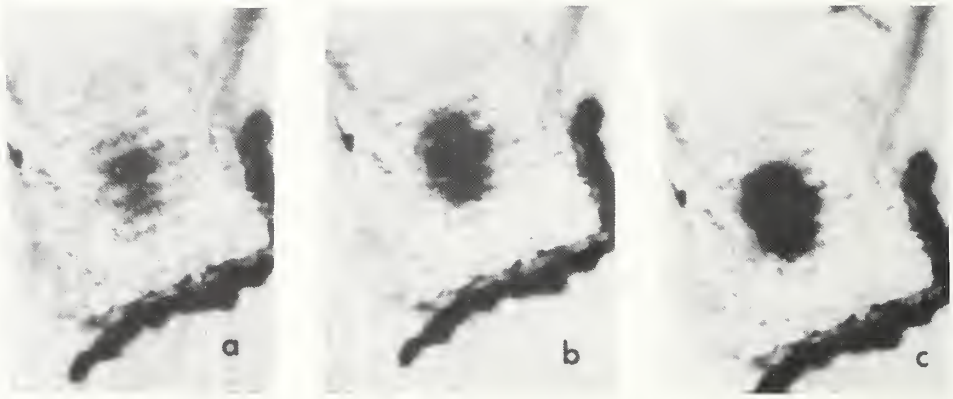


Figure 2. A 20-W power transistor coated with a thermographic phosphor shown for three different operating conditions, each dissipating 16 W. The phosphor when illuminated with ultraviolet radiation as done here is brightest at the cooler areas and darkest at the hotter areas. (a) $I_C = 0.8$ A, $V_{CE} = 20$ V; (b) $I_C = 0.4$ A, $V_{CE} = 40$ V; (c)$I_C = 267$ mA, $V_{CE} = 60$ V.

with a thermographic phosphor [7] which appears darkest at the hottest areas of the device in this figure. For the low-current, high-voltage conditions (I_C = 267 mA, V_{CE} = 60 V), the power density is much more localized (as evidenced by the very dark "hot-spot") than for either of the other two operating conditions. This is despite the fact that the same power is being dissipated for each condition. The peak thermal resistance for the operating condition depicted in figure 2(c) is about 9.7 °C/W and for the condition depicted in figure 2(a) is about 9.1 °C/W. Although the $R_{\theta JR(peak)}$ in this instance varies by only a few percent, variations as a function of operating conditions of several hundred percent are not uncommon for other devices [5].

In general, for low-current, high-voltage operation, the thermal resistance is a strong function of operating conditions. At the other extreme, high current and low voltage, it is not as strong a function of operating conditions, but it still may depend upon I_C and V_{CE}. This can be seen in figure 3, which shows a plot of thermal resistance versus I_C at constant power for a bipolar power transistor. The reason for the large values of $R_{\theta JR}$ at low values of I_C is that the thermal-electrical feedback mechanisms that initiate current crowding and eventually second breakdown [8] are stronger at small values of I_C than at large values. Thus, the current tends to be more constricted and the peak temperature higher for these conditions. It is shown later that the presence of current crowding and the associated large $R_{\theta JR(peak)}$ at low values of I_C should be taken into account when generating SOA limits.

General Methods for Measuring Device Temperature

There are two sets of "generic" methods in general use for measuring the operating temperature of a semiconductor device. One set requires that the semiconductor chip be exposed for viewing and in some instances that a foreign substance be placed on the surface of the chip. Examples are infrared microradiometry [9] and the use of liquid crystals [10,11] and thermographic phosphors [7]. These methods allow one to create a map of the temperature distribution on the chip surface. The infrared method is of most interest here for mapping purposes because it can be used to quantitatively map the surface temperature, whereas the other methods, although extremely valuable, are more qualitative in nature. The other set of "generic" methods uses a temperature-sensitive electrical parameter (TSEP) of the device as a thermometer. These methods can be performed on fully packaged devices but give a single, average temperature value for the chip.

The infrared methods are the most useful methods for accurately determining the distribution of temperature on the device surface. Because the surface temperature is never uniform, a single temperature value cannot fully characterize the temperature of the device, and large-temperature nonuniformities can be mapped using the infrared techniques. An example of the value of this is shown in figure 4, in which the temperature distribution for a power Darlington chip, measured using an automated infrared microradiometer, is displayed. From this display, it is clear that one area of the chip (the hottest area) is dissipating most of the power. Much of the chip is apparently dissipating little or no power. Only from such a temperature map can one establish the nonuniformity of the temperature and the area of the chip that is dissipating most of the power. The impact that this has on chip reliability is demonstrated by the picture in figure 5 of the same

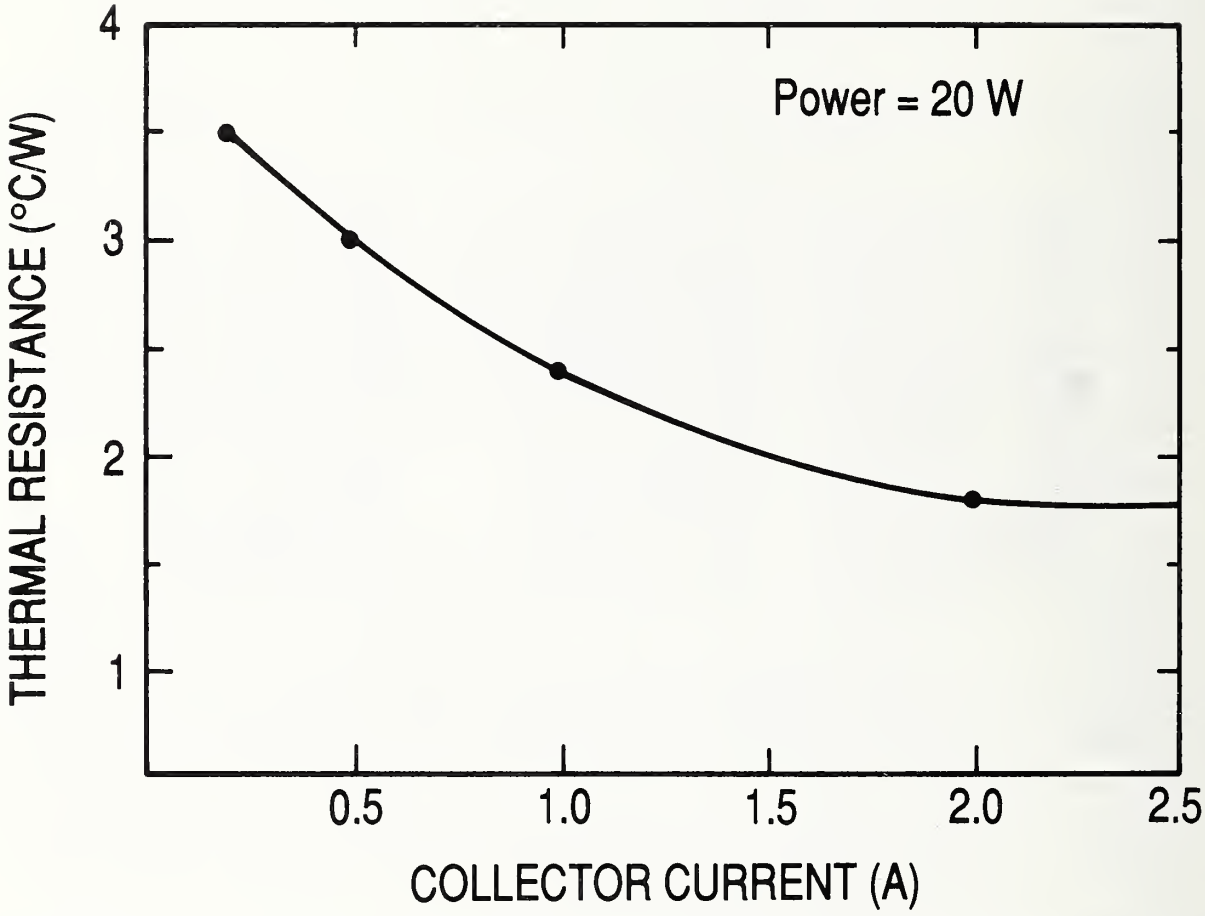


Figure 3. Measured thermal resistance as a function of collector current at a constant power of 20 W for a 35-W triple-diffused transistor.

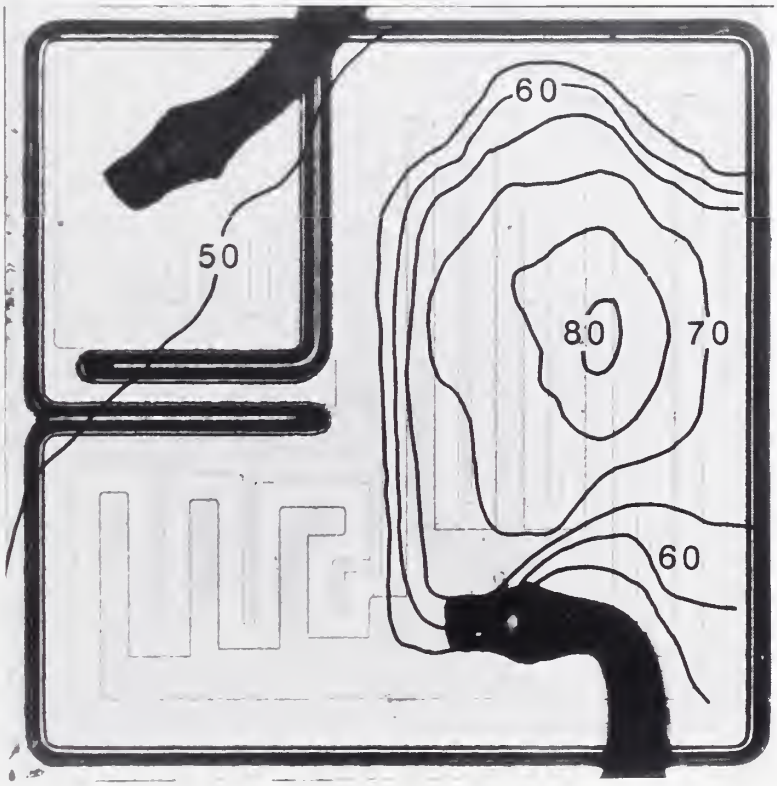


Figure 4. Temperature distribution of a Darlington power transistor measured with an automated infrared microradiometer.

Figure 5. Photomicrograph of a Darlington transistor in previous figure after experiencing a high power pulse. Dark area leading from bond wire at bottom center of figure is melted emitter metallization.

chip after it experienced a brief high power pulse. The darkened area is melted aluminum, leading from the emitter bond wire to the spot on the chip that was hottest during the temperature scan.

The major problem with infrared methods is that they require that the device being studied be "decapped" and visible to the infrared. In addition, the methods are time-consuming, they are quantitatively practical only for steady-state measurements, they require extensive temperature control equipment for controlling the thermal environment of the device being studied, and they require expensive infrared measuring equipment. For these reasons, such measurements are often only made to diagnose problems, such as the one demonstrated by figures 4 and 5.

Temperature measurement methods that use TSEPs are the most often-used methods. They have the advantage that they can be performed on fully packaged devices, oftentimes may be done quickly and are easy to perform, can be quantitatively accurate for steady-state or transient conditions, can often be done with relatively inexpensive electrical equipment, and in certain special circumstances may be done with minimal heat sinking or thermal environment control. The typical "electrical" measurement of temperature is done in two phases, the calibration phase and the measurement phase. In the calibration phase, the value of the particular TSEP chosen is calibrated versus temperature. For instance, if the emitter-base voltage of a bipolar transistor is selected as the TSEP, the value of the emitter-base voltage is determined at various chip temperatures. This is accomplished by externally heating the device, such as in an oven or by a temperature-controlled hot plate or heat sink, and then measuring the emitter-base voltage with a constant current passing through the device. The constant current must be very small as it is assumed that the device is at the same temperature as the oven environment or hot plate which requires that no power (or at least minimum power) be dissipated in the device. In the measurement phase, the device is self-heated by dissipating at a much larger power than that at which the calibration was done. To measure the temperature, the device must be switched from the heating condition (high power) to the measurement condition (the same low current and power at which the calibration was performed) with a heating power duty factor of approximately unity. An example of the heating and measurement waveforms for measuring the temperature of a bipolar transistor is shown in figure 6.

In calculating the power transistor junction-to-reference-point thermal resistance and assuming the previously stated approximations, i.e., 1) the power dissipation during calibration is negligible and 2) the heating power duty factor is approximately unity, the following equation is used [12]:

$$R_{\theta JR} = \frac{T_J - T_R}{P(Avg)} = \frac{V_{MH} - V_{MC}}{P_H} \left(\left. \frac{\Delta V_{MC}}{\Delta T_{MC}} \right|_{I_M} \right)^{-1} \tag{3}$$

where

$R_{\theta JR}$ = thermal resistance, junction to reference point (°C/W),

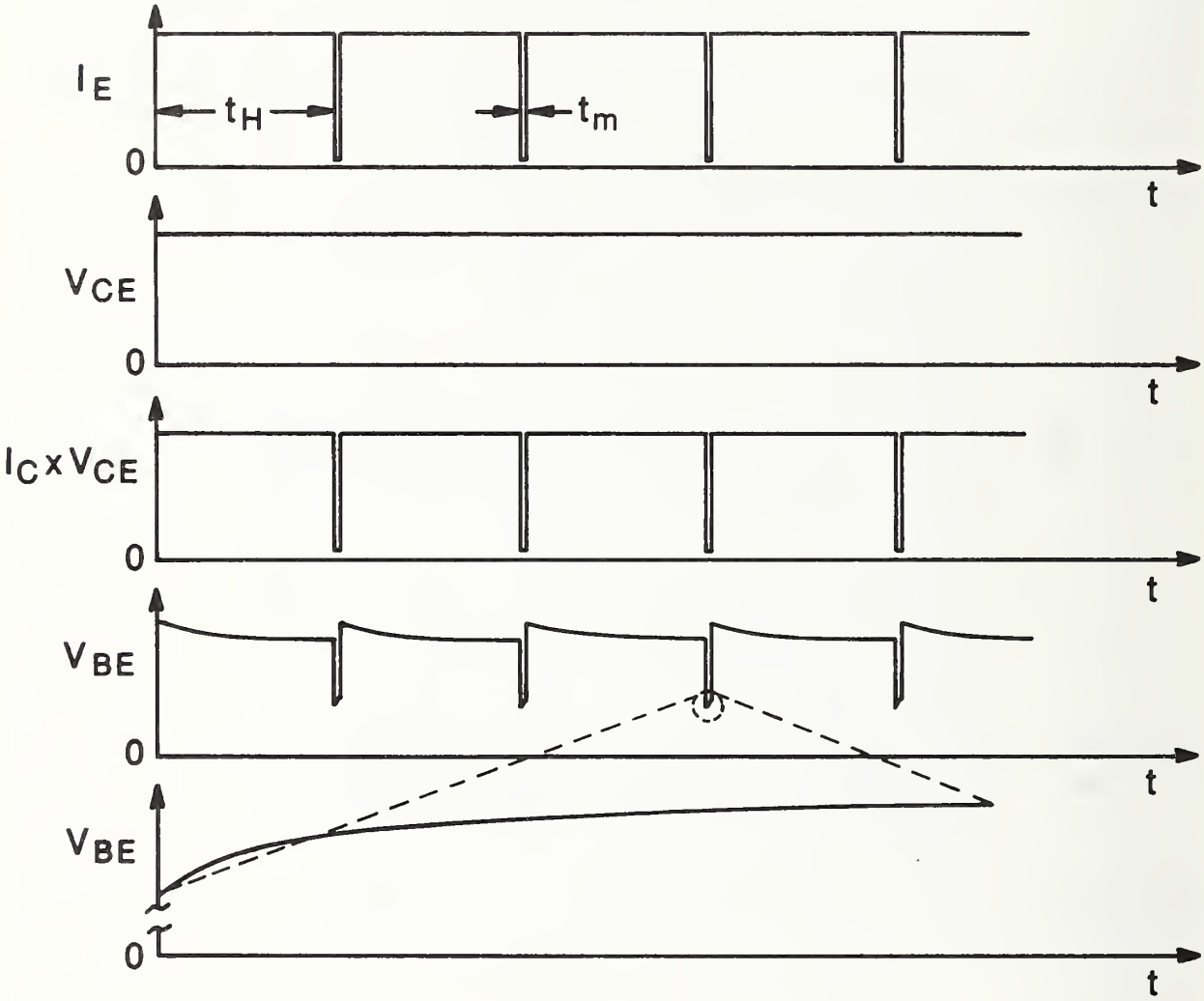


Figure 6. Heating and measurement waveforms as they appear at device terminals. This is a specific example for a bipolar transistor.

T_J = junction temperature (°C),

T_R = reference point temperature (°C),

I_M = measuring/calibration current (mA),

$P(Avg)$ = average heating power applied to transistor causing temperature difference $T_J - T_R$ (W),

P_H = magnitude of heating power applied to transistor (W),

V_{MH} = value of TSEP corresponding to the temperature of the junction heated by P_H and measured at I_M (mV),

V_{MC} = value of TSEP during calibration at I_M and specific value of T_{MC} (mV),

T_{MC} = calibration temperature measured at reference point (°C), and

$\Delta V_{MC}/\Delta T_{MC}$ = TSEP temperature coefficient measured at I_M (mV/°C).

There are some subtle but potentially major difficulties with the switching requirements of the electrical methods. One is that the device is cooling during the actual measurement because the heating power has been removed. For an accurate measurement to be made, this cooling must be considered and taken into account. Second, the device cannot change electrical states instantaneously. It takes a finite time for the device to switch fully from the heating state to the measurement state. If a measurement is made before the electrical switching is completed, large errors can result in the measured temperature. Finally, as figure 4 demonstrates, the device has some distribution of temperature, but the electrical methods indicate a single device temperature that is some average of this temperature distribution. Methods have been developed to overcome some of the limitations of the electrical measurement procedures. They are discussed in later sections of this publication.

Control of the Thermal Environment

If one is to measure accurately the thermal characteristics of a device, the thermal environment of the device during measurement must be known and controlled. This environment will typically not be the environment experienced by the device in its application, but it must be known and controlled for one to relate the measured characteristics to the application characteristics.

Knowledge and control of the thermal environment usually means knowledge and control of the temperature at a specified point on the device or its package. To "know" the temperature at the reference point means that a thermocouple, thermistor, or thermometer of some other type be attached to or in some way determine the temperature at the point. It is usually not satisfactory to know only the temperature of the surrounding gas or fluid because in most instances the reference temperature and the fluid or gas temperature will be different.

For steady-state, multiple-pulse, or single-pulse heating conditions greater than about

300 ms in length, it is usually not sufficient to use a heat sink that is not temperature controlled, such as merely a large copper block. The problem is that the uncontrolled heat sink begins to rise in temperature, heated by the device under test, making it impossible to maintain a controlled reference point temperature. Control and measurement of the reference point temperature is usually difficult and requires ancillary equipment such as temperature sense and control units and methods of heating and cooling the heat sink. A schematic of a temperature-controlled heat sink and temperature control system used at the National Institute of Standards and Technology for many years is shown in figure 7. The copper heat sink is continuously cooled by the chilled water and intermittently heated by the heating resistors as required. The temperature control unit senses the temperature with a thermocouple and commands the power supply to supply heating current to the resistors to maintain the preset temperature. With the system shown in the figure, the reference point temperature can be controlled to within about 0.1 °C.

For some important measurements, a heating pulse of less than 300 ms is desirable. Such a case is for die-attach evaluation [13-18]. In this instance, one wants to make the die-attach portion of the thermal resistance to be as large a portion as possible of the measured thermal resistance. This is accomplished with a short heating pulse of the appropriate length. More will be said about this later, but for this type of measurement, close control of the thermal environment is not critical because the thermal resistance between the device package and the environment does not enter into the measurement.

Selection of Temperature-Sensitive Electrical Parameters

Although a variety of factors enter into the selection of a TSEP for measuring the temperature of a particular device, the two most important factors are the accuracy with which the TSEP can determine the device temperature and the convenience or ease of use of the particular parameter. The particular parameter chosen may also depend upon the reason for performing the thermal characterization. If the purpose is to qualify a device to some particular rating or limit, the most accurate parameter should be used. If the purpose is to screen devices quickly or as an outgoing or incoming inspection, then an easier, more convenient parameter may be chosen, provided good correlation between the actual temperature and the parameter being measured has been established.

It has been well established that the most accurate and the easiest TSEP to use for bipolar devices is the emitter-base voltage measured at a small, constant current. In addition, it has been found that the preferred technique to use is the "emitter-only switching" method for which the collector voltage is not switched between the heating conditions and the measurement conditions [12,19-20]. A schematic of the measurement circuit is shown in figure 8 and the various waveforms at the terminals of the device under test are those shown in figure 6.

The situation for power MOSFETs is more complicated than for the bipolar transistor. It has been shown that the most accurate TSEP for the MOSFET is the threshold voltage, i.e., the source-gate voltage measured at a small drain current [21]. Although the procedure developed for using the source-gate voltage as the TSEP is nearly identical to that used

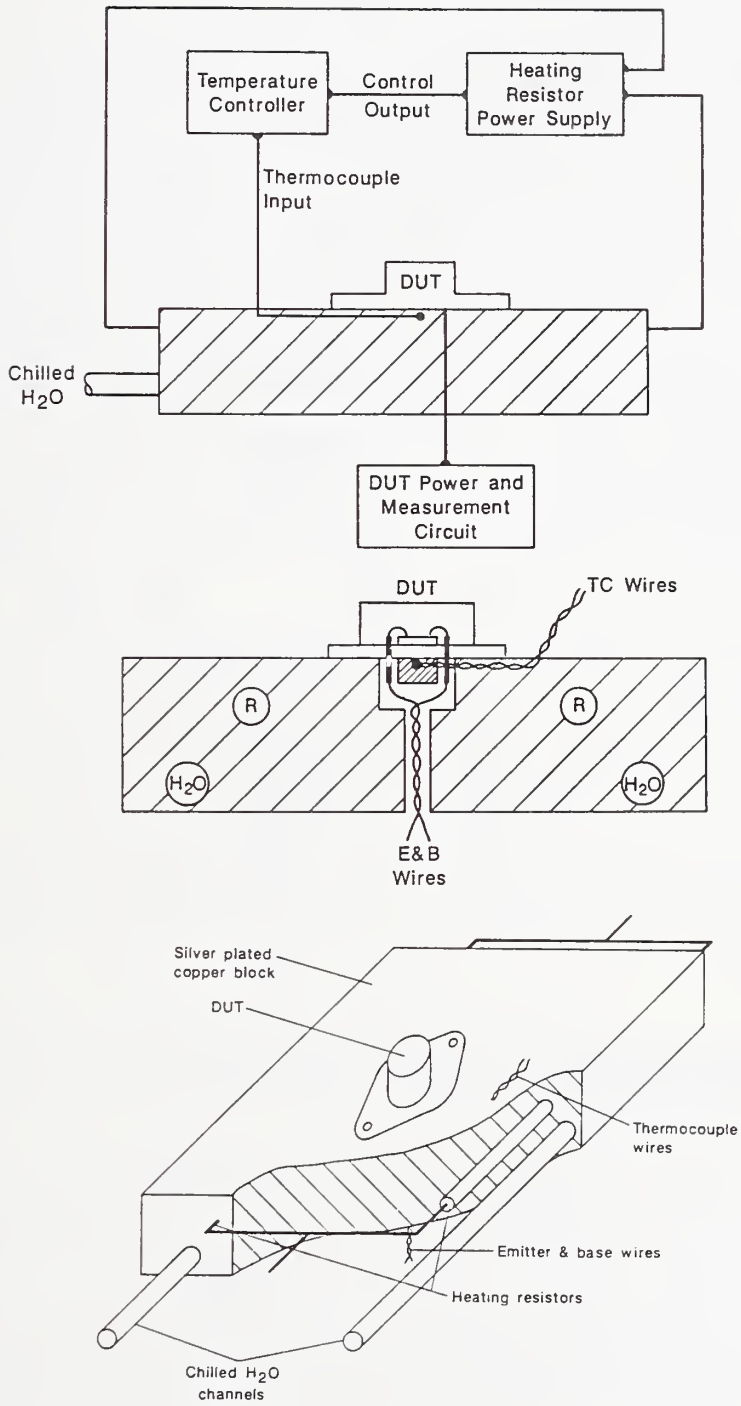


Figure 7. Schematic of the temperature control system (a) and temperature-controlled heat sink (b,c) used at the National Institute of Standards and Technology.

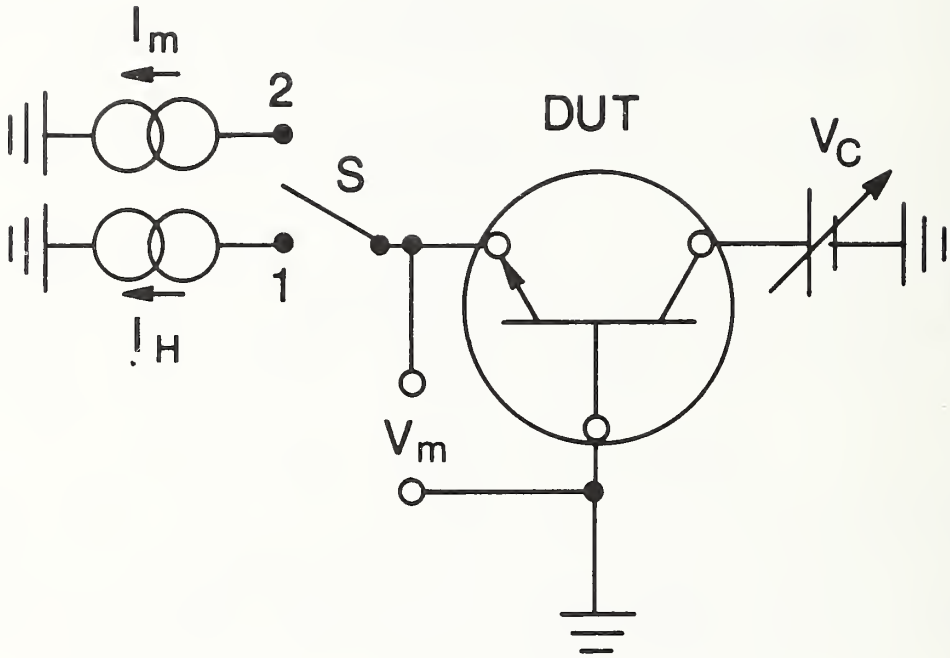


Figure 8. Schematic of measurement circuit for using standard method for measuring temperature of a bipolar transistor.

for the emitter-only switching method used for bipolar transistors, and is equally as easy, a different method has been standardized and is therefore most often used [22]. This second method uses the forward voltage of the intrinsic drain-body diode present in all power MOSFETs as measured using the drain-source voltage as the TSEP. Examples of a calibration curve for each of these TSEPs are shown in figure 9. Schematics of the measurement circuits for these two techniques are shown in figure 10 with a comparison of the extrapolated TSEP temperatures to that of infrared measurements of the peak chip surface temperature given in table 2. This method has been selected as the standard because it was in popular use for several years before the threshold voltage method was developed and also because the calibration of the diode forward voltage is somewhat simpler than that of the threshold voltage. This latter condition is related to the fact that the variation in dV_{ds}/dT for a group of "identical" diodes is usually less than the variation in dV_{th}/dT for MOSFETs. Thus, rather than generating a single calibration curve valid for all MOSFETs of a single type, as is done for diodes, the threshold voltage method could require calibration for each device. Fortunately, because power MOSFETs usually have a comparatively uniform chip temperature distribution, the standard method is usually satisfactory.

The situation for merged bipolar/MOSFET devices is not well defined. The only commercially relevant device in this category today is the Insulated Gate Bipolar Transistor (IGBT). One difficulty with this device is that there is no intrinsic diode available as there is for the power MOSFET. It is possible that the threshold voltage of this device will yield similarly accurate temperature measurements as for the power MOSFET and be equally as easy to use. The other possible candidate as a TSEP is the forward voltage drop, or saturation voltage, of the device measured at a low forward current. Little reported work has been done on comparing the various TSEPs for temperature measurements of the IGBT, although the threshold voltage has been proposed as the TSEP in a military standard.

Measurement of Temperature-Sensitive Electrical Parameters

The method chosen to measure the TSEP is critical to determining the accuracy and repeatability with which the TSEP indicates the actual device temperature. Because the measurement procedure nearly always requires the device under test to be switched from a high-power, heating condition to a low-power, measuring condition, the presence, control, and identification of "nonthermal" switching transients are problems for all device types. Nonthermal switching transients are defined as electrical transients that mask the temperature variations of the TSEP that one is attempting to measure. Often, these nonthermal effects are inseparable from the desired thermal effects without some "post-data collection" processing. Ignoring nonthermal switching transients probably is second only to lack of reference temperature control in contributing to temperature measurement errors.

Typically, the TSEP has a variation with temperature of a few millivolts per degrees Celsius. Thus, for an accurate and reliable measurement of temperature, a few millivolts error in the TSEP translates into a few degrees Celsius error in temperature. For instance, the emitter-base voltage at a low emitter current typically has a temperature variation

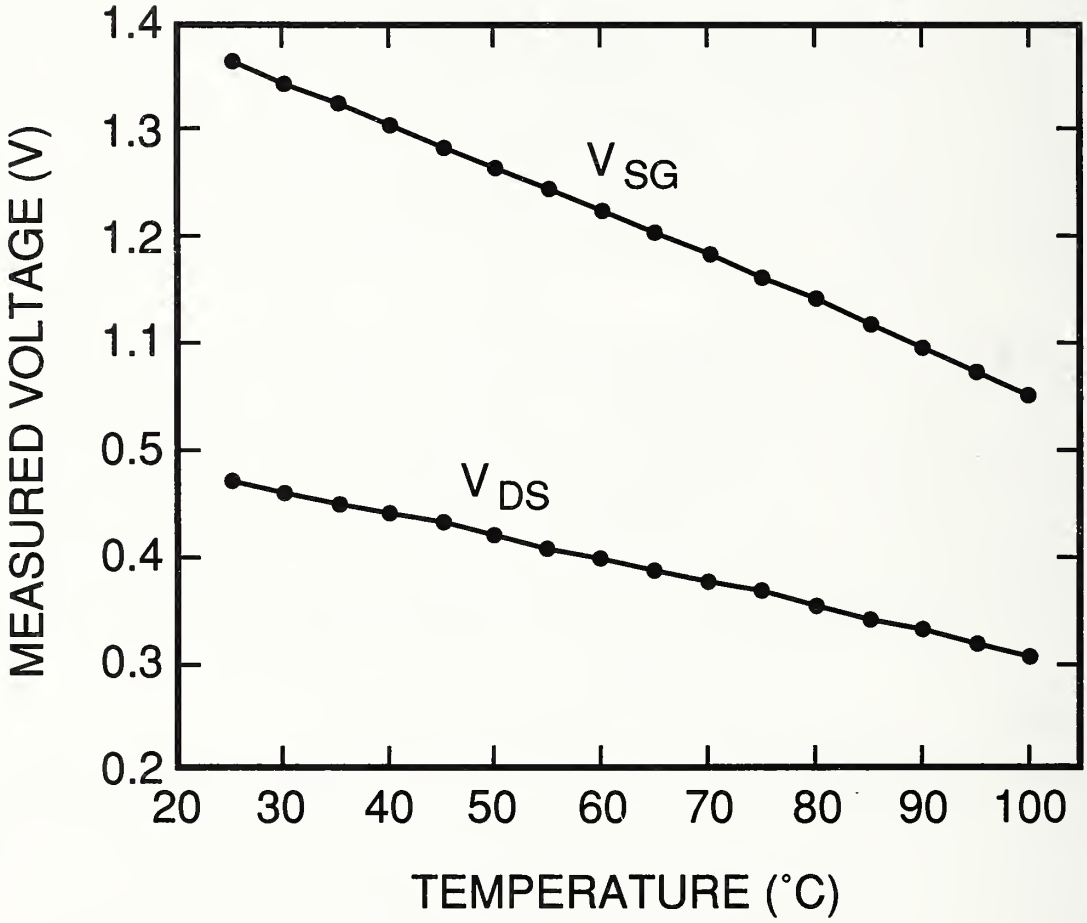
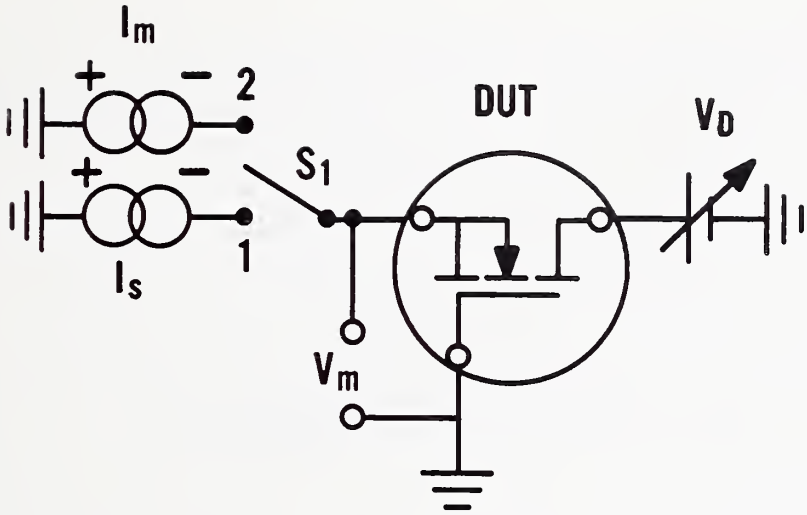


Figure 9. Examples of calibration curves for each of the power MOSFET TSEPs.



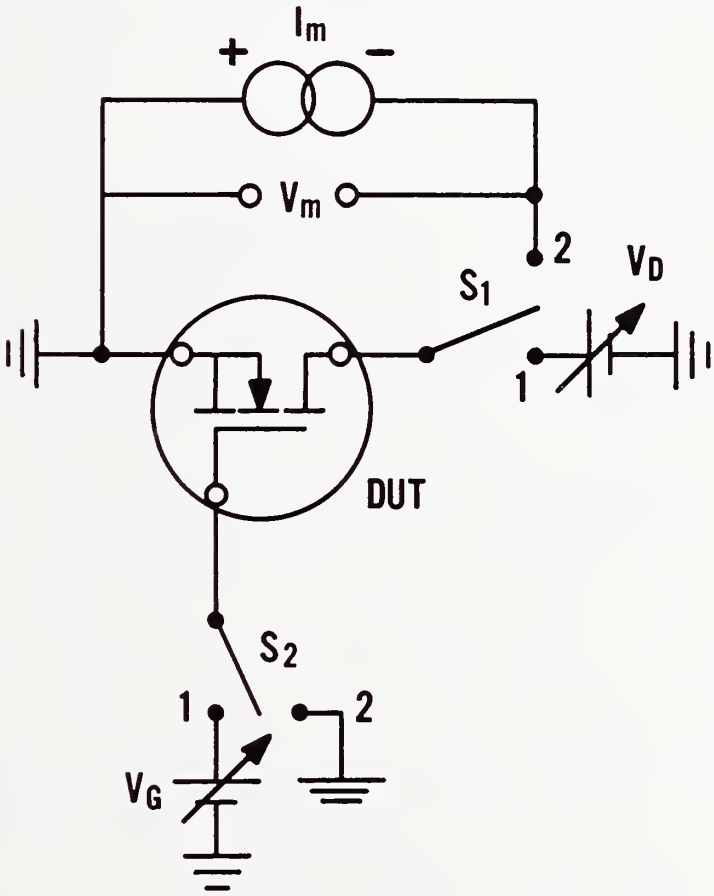


Figure 10. Schematics of measurement circuits for each TSEP. Source-gate voltage (top); drain-source voltage (bottom).

TABLE 2

Comparison of Thermal Resistance
Measurement Techniques for a MOSFET

Device Number	Operating Conditions $I_D(A)/V_{DS}(V)$	Temperature Rise Above Case (°C) IRM	V_{SG}	V_{DS}
	0.5/60	33.5	31.0	28.8
1	1.0/30	33.5	31.0	28.8
	1.5/20	33.5	31.0	27.8
	0.5/60	38.0	35.0	36.5
2	1.0/30	38.0	35.0	36.1
	1.5/20	38.0	35.0	36.1
3	1.0/60	80.0	80.3	70.7
	1.5/40	80.0	80.3	70.4
	0.5/60	37.0	36.8	36.1
4	1.0/30	37.0	36.8	36.1
	1.5/20	37.0	36.8	35.0
5	1.5/40	73.0	69.0	62.0
6	1.0/20	34.3	31.4	28.1

of about −2 mV/°C. In the usual switching application, if the emitter base voltage has settled to within a few tens of millivolts of its final value, the device has for all intents and purposes finished switching. It may take less than a microsecond for the voltage to settle to within a few tens of a millivolt of its final value, but it typically takes more than 10 μs for the voltage to settle to within a millivolt of the final value. It has even been shown that the metallic leads of a typical power device package contribute to these nonthermal switching transients [23]. An example of this is shown in figure 11. The net result of all this is that to measure the temperature accurately using a TSEP, one must wait until the nonthermal switching transients have subsided. This will nearly always require a delay of at least 20 μs after switching to the low-level measurement condition from the high-level heating condition. Usually, the delay is longer, sometimes being 100 μs or longer. A method has been developed for detecting the presence of nonthermal switching transients and for extrapolating the temperature measured after a delay time to the temperature of the device at the moment that the device was switched [24]. The procedure used is based upon one-dimensional cooling theory and is summarized in table 3. An example of the measured temperature, with and without consideration of nonthermal switching transients, and the extrapolated temperature are shown in figure 12.

Safe-Operating-Area Limits

Device manufacturers publish safe-operating-area (SOA) limits for nearly all of their power transistors. The limits define an area on an $I_C - V_{CE}$ plane within which safe operation is guaranteed and within which the peak junction temperature is guaranteed not to exceed the specified safe maximum temperature, $T_{J(max)}$. These limits are set for both dc and pulsed operation, but the limits of the SOA of concern here are the dc thermal limit and the dc second breakdown limit denoted by the line segments 1 and 2, respectively, in figure 13. The discussion is also limited to forward-bias SOA limits. A comparison of the techniques generally used for determining the pulsed thermal limits has been published [24].

DC Thermal Limit – The dc thermal limit of the SOA is in reality determined from the thermal resistance of the device. Because the thermal limit defines the limit along which $T_{J(peak)} = T_{J(max)}$, one finds from eq (2)

$$R_{\theta JR(peak)} = \frac{T_{J(max)} - T_R}{(I_C \times V_{CE})_{LIMIT}} \tag{4}$$

where $(I_C \times V_{CE})_{LIMIT}$ defines the locus of points along which $T_{J(peak)} = T_{J(max)}$. If $R_{\theta JR(peak)}$ is assumed constant, as are $T_{J(max)}$ and T_R,

$$(I_C \times V_{CE})_{LIMIT} = C, \tag{5}$$

where C is constant (i.e., constant power), or,

$$ln[I_C] = -ln[V_{CE}] + C'. \tag{6}$$

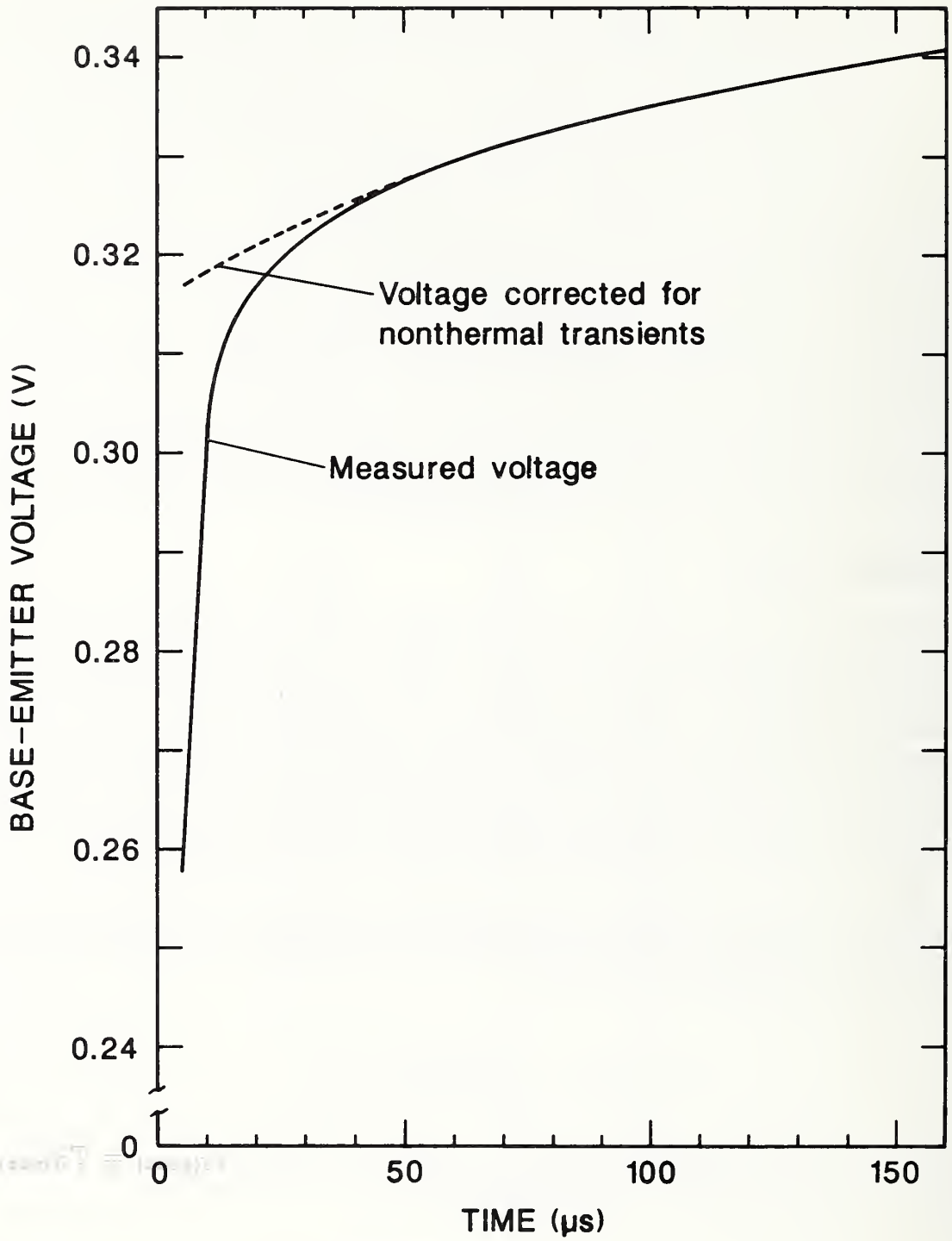


Figure 11. Measured and corrected (for nonthermal switching transients) emitter-base voltage waveform during measurement of the temperature for a bipolar transistor.

TABLE 3

Procedure for Detecting Nonthermal Switching Transients and Extrapolating Temperature to Instant of Switching

1. Measure temperature in normal manner but as a function of time after switching. A series of measurements between 10 μs and 250 μs after switching is satisfactory.

2. Plot measured temperature, T, versus the square root of time after switching, $\sqrt{t}$.

3. Nonthermal switching transients have subsided at the time the plot of T versus $\sqrt{t}$ becomes linear.

4. Draw a straight line through the linear portion of the T versus $\sqrt{t}$ plot and extend the line to $t = 0$. The intercept with the $t = 0$ axis is the extrapolated temperature at the instant of switching.

An example of the results of this procedure is shown in figure 12.

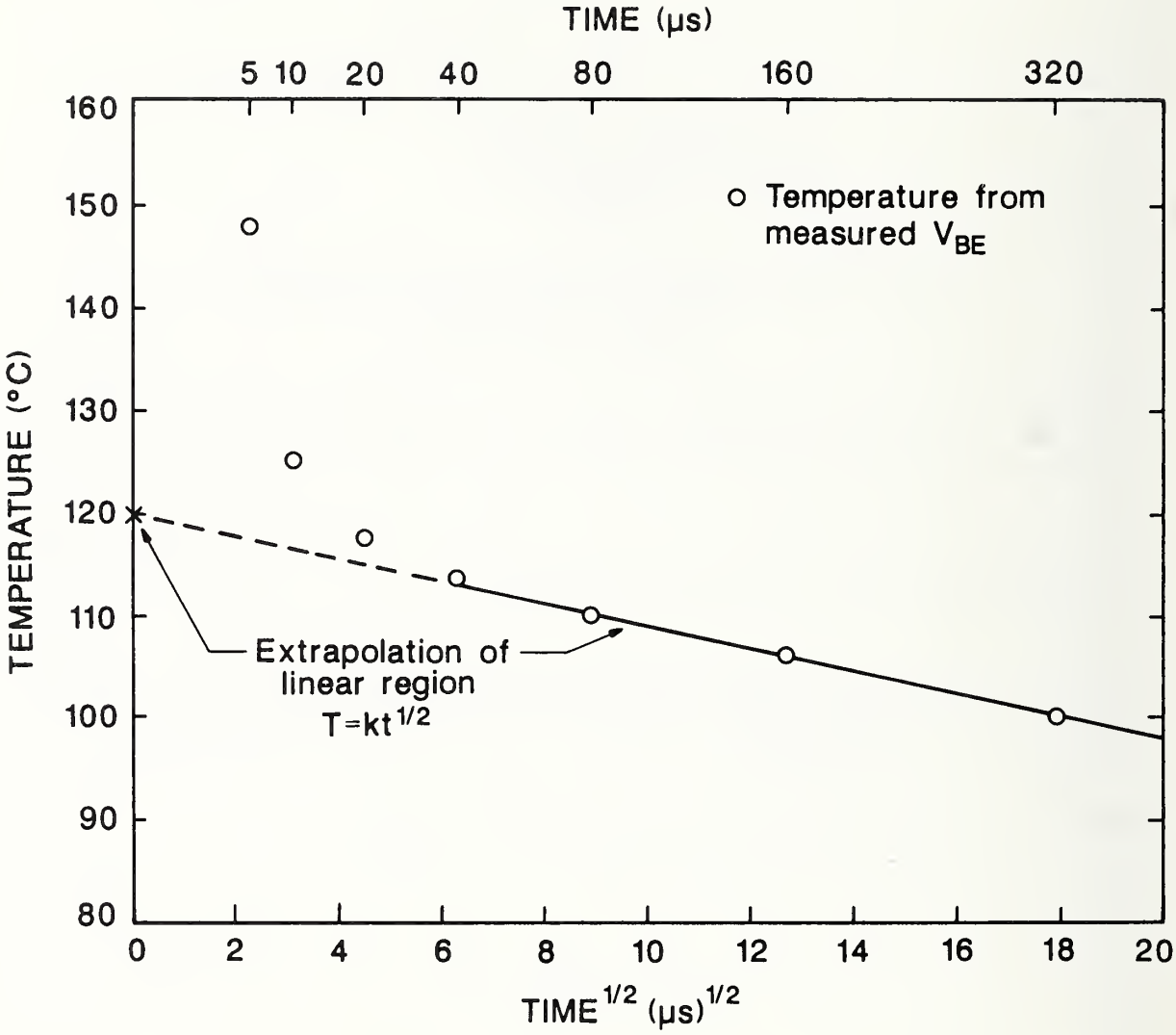


Figure 12. Measured T versus $\sqrt{t}$ and extrapolated temperature for a bipolar transistor. The time after switching for each measured temperature is noted on the top scale.

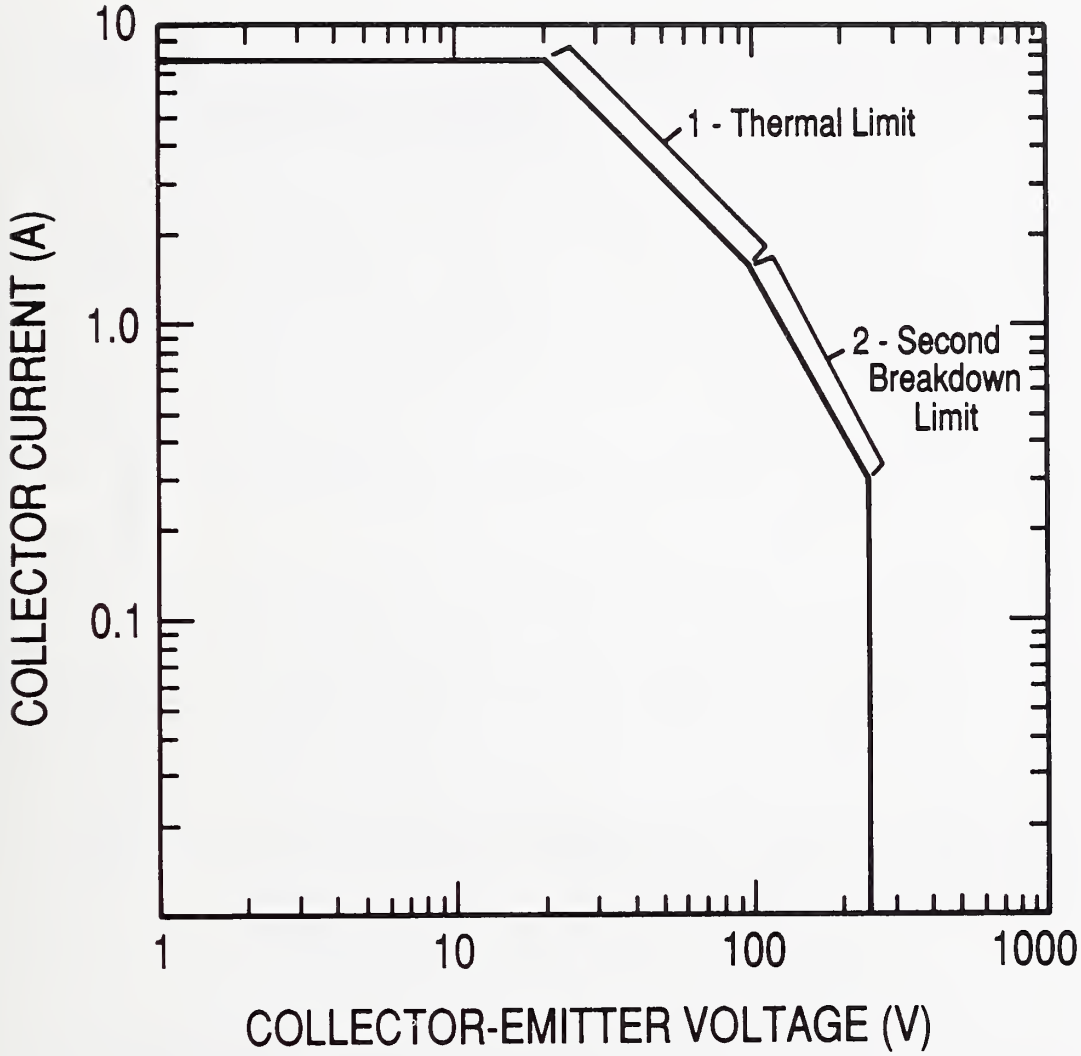


Figure 13. A representative example of a manufacturer's published safe-operating-area (SOA) limits for a power transistor.

Thus, a straight-line relation with a slope of −1 exists between $ln[I_C]$ and $ln[V_{CE}]$ if $R_{\theta JR(peak)}$ is constant. This can be seen in figure 13, where line segment 1 has a slope of −1. The specified thermal limit of the SOA will usually run from the maximum safe value of collector current, $I_{C(max)}$, to some lower value of I_C at which point a limit of slope less than −1, the second breakdown limit, commences.

As has been shown previously, $R_{\theta JR(peak)}$ cannot be considered a constant for all device operating conditions. However, in the high-current, low-voltage operating region (near the $I_{C(max)}$ limit), the assumption of a constant $R_{\theta JR(peak)}$ is usually reasonable. An indication of this can be seen in figure 14 where the manufacturer's published SOA (solid line) as well as the SOA determined from the actual peak junction temperature measured with an infrared microradiometer (dashed line) are shown for a device with no specified second breakdown limit. Within the specified thermal limit, this device can operate quite safely with $T_{J(peak)}$ significantly below $T_{J(max)}$. In addition, the thermal limit as determined by the infrared microradiometer has a slope of approximately −1, which indicates a constant $R_{\theta JR(peak)}$. For this device then, the safe operating area is conservatively limited by the specified $T_{J(max)}$. It has also been observed that for most devices operating at or near $I_{C(max)}$ (and thus limited by the −1 slope of the safe operating curve), $T_{JR(peak)} \approx T_{JR(Avg)}$, where $T_{JR(Avg)}$ is measured using the V_{EB} emitter-only switching technique. This is because of the more uniform temperature distribution at high currents.

Second Breakdown Limit – The second breakdown limit of the SOA is usually determined by actually permitting a number of devices to enter second breakdown. The limit is usually set at values of I_C and V_{CE} somewhat less than those for which second breakdown occurs in the sample to add a margin of safety. Often, however, the thermal resistance of the device is not measured over this region because it is assumed that the thermal limit must continue with a slope of −1 and would thus be outside the second breakdown limit. As has been described, the low-current, high-voltage operating conditions, for which the published SOA is usually second-breakdown-limited, $R_{\theta JR(peak)}$ is usually a strong function of operating conditions. This means that the published high-current, low-voltage thermal limit probably cannot be linearly extrapolated to the low-current, high-voltage operating region. In fact, the low-current, high-voltage conditions, $R_{\theta JR(peak)}$ can be so large that the junction temperature exceeds the published safe maximum temperature well within the second-breakdown-limited safe-operating area. Thus, though the device may be protected from second breakdown in this region, it is not thermally protected.

An indication of the way variations in $R_{\theta JR(peak)}$ can affect the actual SOA limits of a device that is severely second-breakdown-limited can be seen in figure 15. This figure shows the manufacturer's published SOA (solid line) as well as the experimentally determined SOA (dashed line) which was determined by using an infrared microradiometer to estimate the actual peak junction temperature. Within most of the specified thermal limit (specified slope of −1), this device can operate quite safely with $T_{J(peak)}$ significantly below $T_{J(max)}$ even though the true slope deviates from −1. For the low-current, high-voltage conditions, though, the actual thermal limit falls well within even the specified second breakdown limit, and thus this device should be thermally limited over almost all of its operating

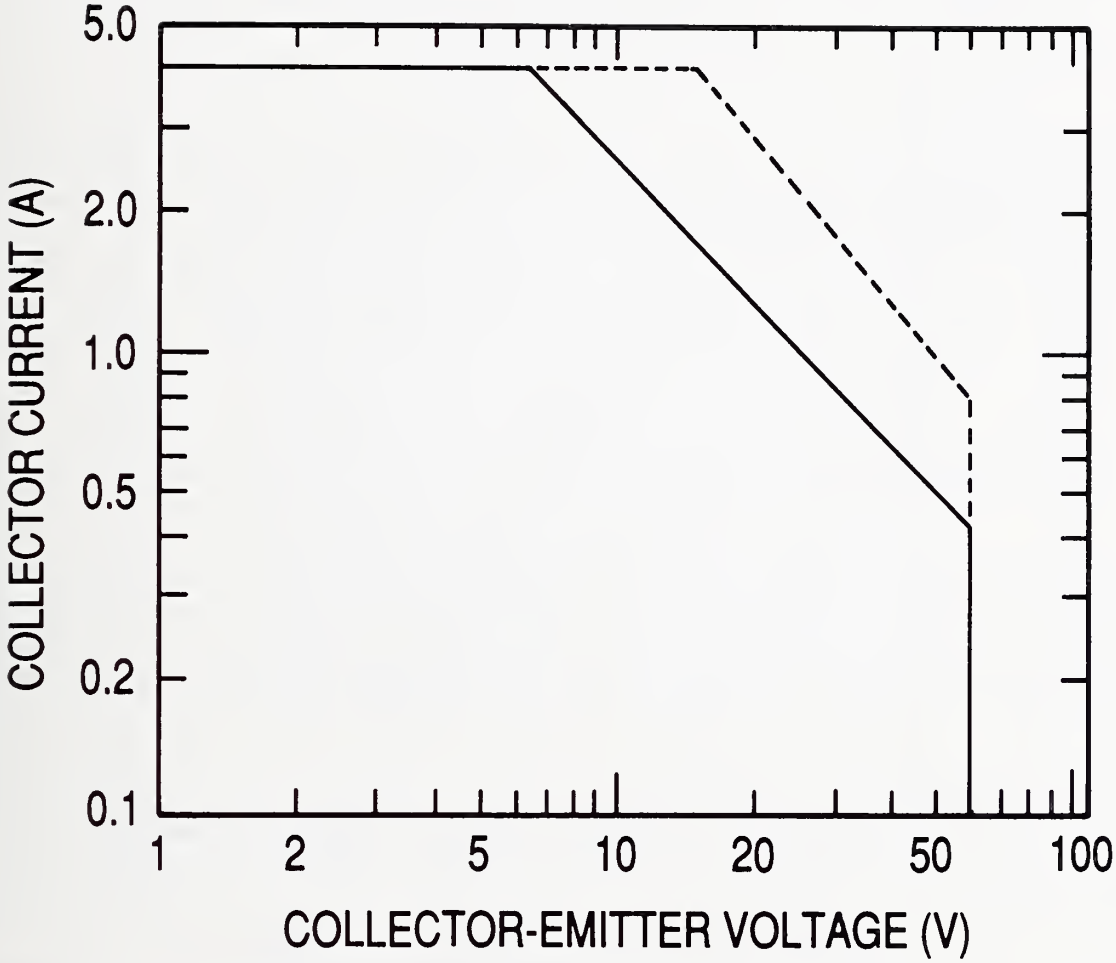


Figure 14. The manufacturer-specified SOA limits (solid line) and the actual SOA limits determined by an infrared microradiometer (dashed line) for a power transistor which has no specified second breakdown limit.

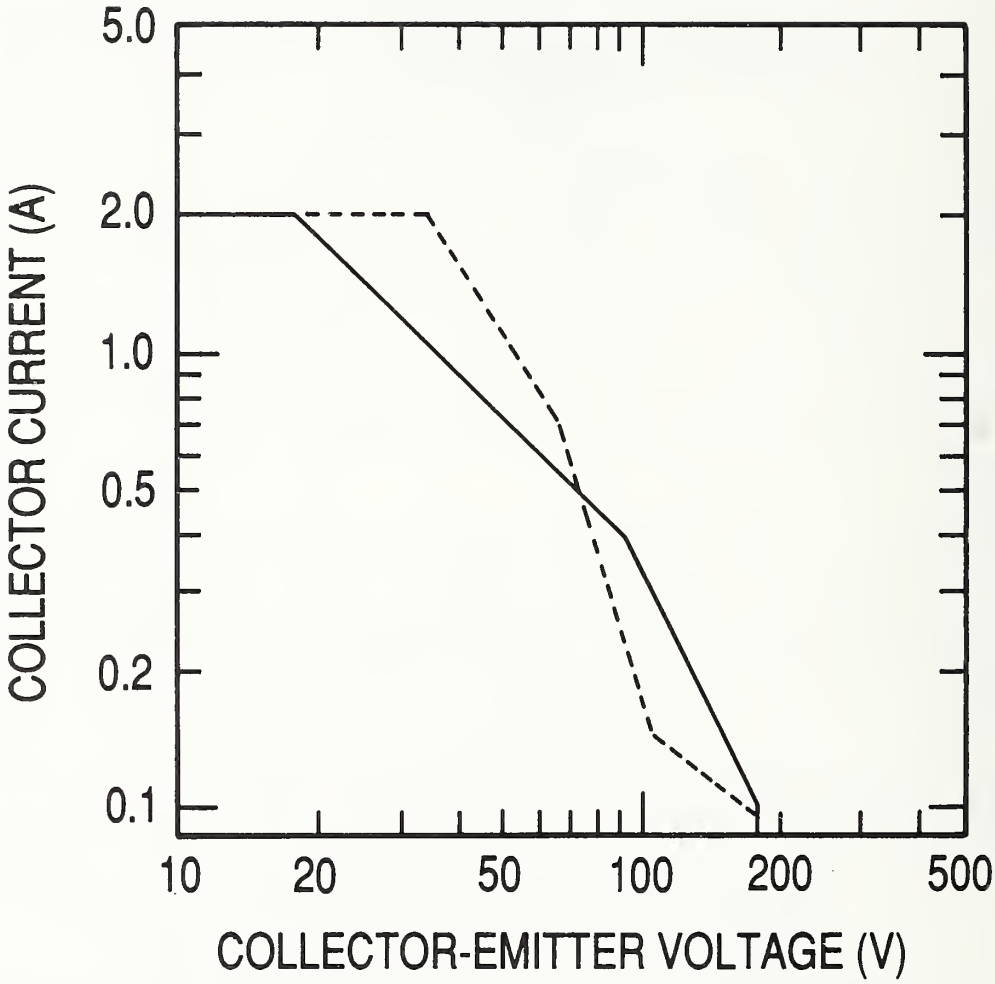


Figure 15. The manufacturer-specified SOA limits (solid line) and the actual SOA limits determined by an infrared microradiometer (dashed line) for a device that is inadequately rated in the second breakdown region by the manufacturer.

range.

There are a number of electrical measurement techniques that can possibly be used to determine better the SOA limits for power transistors. These techniques can be used by manufacturers in determining the original specified limits or by users to determine if a particular device in a particular application is operating with a safe peak temperature and safe temperature distribution. These techniques are discussed below along with their possible applications to the determination of SOA limits.

Relating the Chip Temperature to the Measured Temperature

The term "chip temperature" is ambiguous. The semiconductor chip does not have a single temperature, but has a distribution of temperature. An example of a relatively uniformly distributed surface temperature for a power MOSFET chip is shown in figure 16. An example of a nonuniform distribution for a power bipolar transistor is shown in figure 4. The surface temperature distributions of these two chips were measured with an infrared microradiometer. The electrically measured temperature for the uniform temperature MOSFET was 94 °C, only 4 °C below the actual peak temperature. The TSEP used for the MOSFET was the source-gate voltage at a low level current. The electrically measured temperature for the bipolar transistor of figure 4 was 64 °C, 16 °C below the peak temperature. For the bipolar transistor with a nonuniform temperature distribution, the electrically measured temperature is a poor representation of the actual peak temperature.

It is important to be able to estimate the peak junction temperature of a power transistor. It is equally important to be able to determine when the temperature distribution becomes nonuniform and thus when the standard electrically measured temperature is considerably below the peak temperature (electrical techniques typically average the temperature). In addition, the onset of temperature nonuniformity is usually a precursor to second breakdown and certainly enhances the possibility of premature device failure. One possible method of improving SOA limits would be to set the limit as determined either by the peak junction temperature or by the onset of temperature nonuniformity, whichever occurs first [25]. Because the onset of temperature nonuniformity will generally precede second breakdown, this SOA limit would generally fall within the usual second-breakdown limit.

Determination of Area of Power Generation and Peak Junction Temperature – It is possible to estimate the actual area of steady-state power dissipation for a power transistor [24] and thus determine the extent of current crowding in the device, because for at least the first 250 μs of cooling, power transistors cool from steady-state according to one-dimensional heat flow theory. That is,

$$T(t) - T(0) = Kt^{1/2}, \tag{7}$$

where

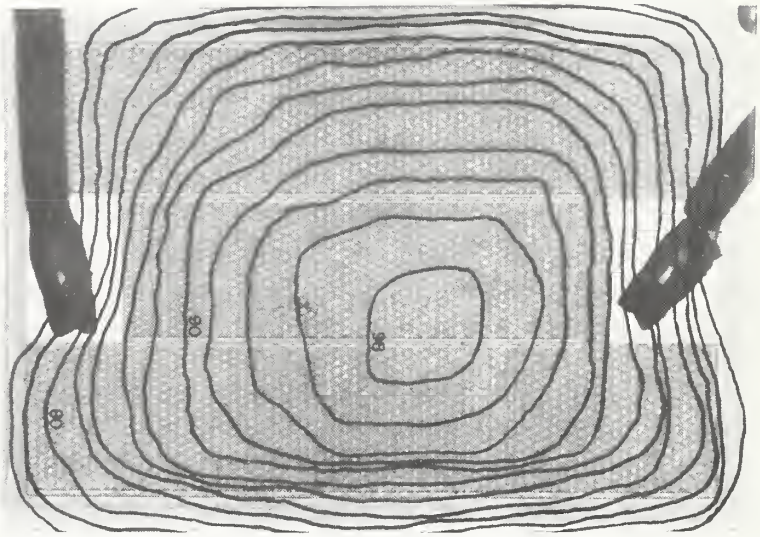


Figure 16. The temperature distribution of a power MOSFET measured with an automated infrared microradiometer.

$$K = \frac{2P}{\sqrt{\rho \pi k c}\, A_E}, \tag{8}$$

and

$T(t)$ = temperature at time t (°C),

$T(0)$ = temperature at instant of power removal (°C),

t = time after removal of power (s),

P = power dissipation (W),

ρ = density (g/mm^3),

k = thermal conductivity (W/mm·°C),

c = thermal capacity (W·s/g·°C), and

A_E = area of power generation or effective active area (mm^2).

A plot of temperature of the device as it is cooling versus $t^{1/2}$ results in a straight line, and the area of power generation A_E can be found from the slope of that line K. This is demonstrated in figure 17, where the cooling rate of a power transistor is shown for two different operating conditions, but each for the same power level. The slope of the curve I_C = 0.2 A gives an area of 0.72 mm^2 and the slope of the curve for I_C= 0.5 A gives A_E = 1.96 mm^2. The total chip area is about 6.46 mm^2. It is obvious that the junction temperature for the 0.2-A condition should be much hotter (same power, smaller area) than for the 0.5-A condition, and both the infrared and electrical measurements indicate this. It is important to note, though, that for the small-area case, the actual peak temperature (as indicated by an infrared microradiometer) is considerably higher than the electrical indication. The difference is not nearly so great for the large-area case, because, as has been mentioned, the electrical techniques for measuring temperature tend to average the junction temperature, and the more nonuniform the temperature, the more the electrically measured average temperature will deviate from the peak temperature.

Generally, it can be assumed that for chips of equal area, for the same power dissipation, the faster the rate of cooling during measurement, the more nonuniform is the chip temperature. Also, the more nonuniform the temperature, the less representative the electrically measured temperature is of the peak temperature.

It is possible to estimate better the peak temperature from the electrical measurement with some further data processing. It is necessary, though, to measure the cooling response of the device just as for extrapolating the temperature, as is shown in table 3. Because the semiconductor chip will cool one-dimensionally for the first 200 to 300 μs, a plot of temperature versus the square root of time will be linear during this time. The slope of the linear curve is inversely proportional to the area being heated. If it is assumed also that

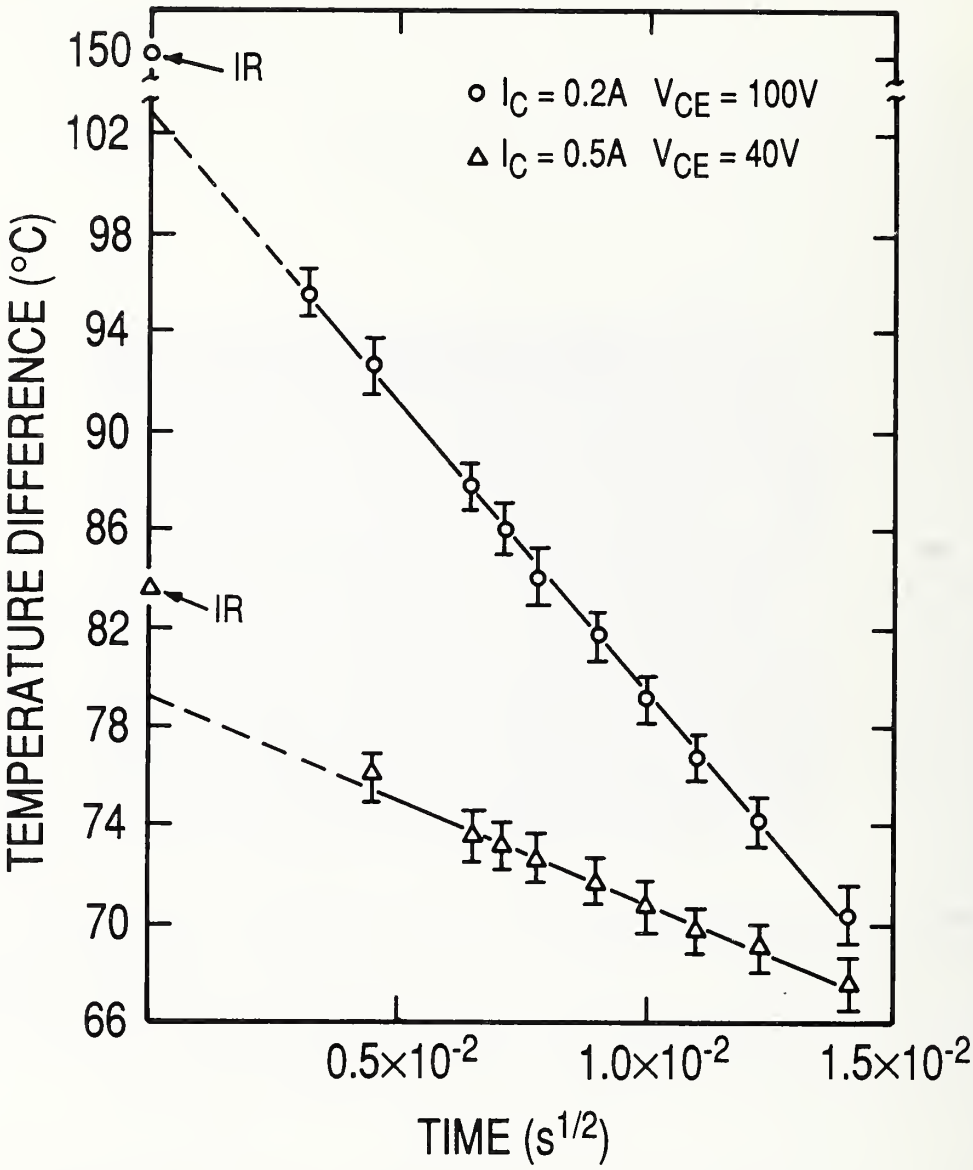


Figure 17. The electrically measured cooling response of a power transistor versus the square root of time for two different operating conditions for the same power (20 W). The infrared (IR) measured temperature is also noted for each operating condition. The ordinate is the junction temperature rise above the reference point (case) temperature.

the low-level measurement current takes on the same distribution within the chip during measurement that the heating current did during heating, then a simple relation can be developed between the calibration curve generated by externally heating the chip (with the measurement current uniformly distributed over the chip) and the measured TSEP during the actual measurement (with the measurement current nonuniformly distributed over the chip). The full procedure is described elsewhere [4].

An indication of the accuracy of this technique can be seen from figure 18 which shows the manufacturer-specified SOA, the SOA as determined using the modified electrical technique for determining the peak temperature, and the actual SOA determined using an infrared microradiometer for a 35-W triple-diffused transistor. Also shown is the SOA which would be determined using the standard electrical measurement technique. As has been discussed, for high current and low voltage, the specified SOA safely limits the junction temperature below $T_{J(max)}$ for this device. However, as the voltage increases and the current decreases, the current begins to constrict and the specified SOA, although derated for second breakdown, is not derated sufficiently to account for the increased current constriction. Both the infrared-determined limit and the electrical-peak junction temperature limit show this.

Detection of Onset of Current Constrictions – There are a number of rather simple techniques that detect when the junction temperature (or equivalently the power density distribution) begins to become nonuniform.

One possible method of detecting the onset of current nonuniformity is by monitoring V_{EB} at constant I_C as V_{CE} is increased [25]. The value of V_{EB} can be measured either near the end of a pulse (of 1-s duration, for instance) while the pulse is still on, or it can be measured after the pulse is removed from the device ($\sim$10 to 20 μs after removal of power) with a small sampling current present. The latter is more sensitive to the onset of the temperature nonuniformity, and the measurement technique is nearly the same as making an $R_{\theta JR}$ measurement using the emitter-only switching technique. A plot of V_{EB} versus V_{CE} for several values of I_C is shown in figure 19 for the same 35-W triple-diffused device shown previously. As the power is increased, V_{EB} initially falls linearly with V_{CE} because of a rather uniform increase in junction temperature. As the power density begins to be constricted, and the peak temperature begins to rise more rapidly, V_{EB} falls more rapidly. In each curve the break point from the initial linear region is the point where current crowding has begun to occur. This measurement is very easy to perform, and each datum point can be obtained with a single pulse of power applied to the device. An SOA curve based on the onset of current crowding can then be generated from these data.

Reasons for Measuring Temperature

There are many reasons why one desires to know the operating temperature of a power device. Oftentimes, the specific reason for wanting to know the temperature dictates the type of measurement to be made.

If one wants to know accurately the actual operating temperature of a device in operation,

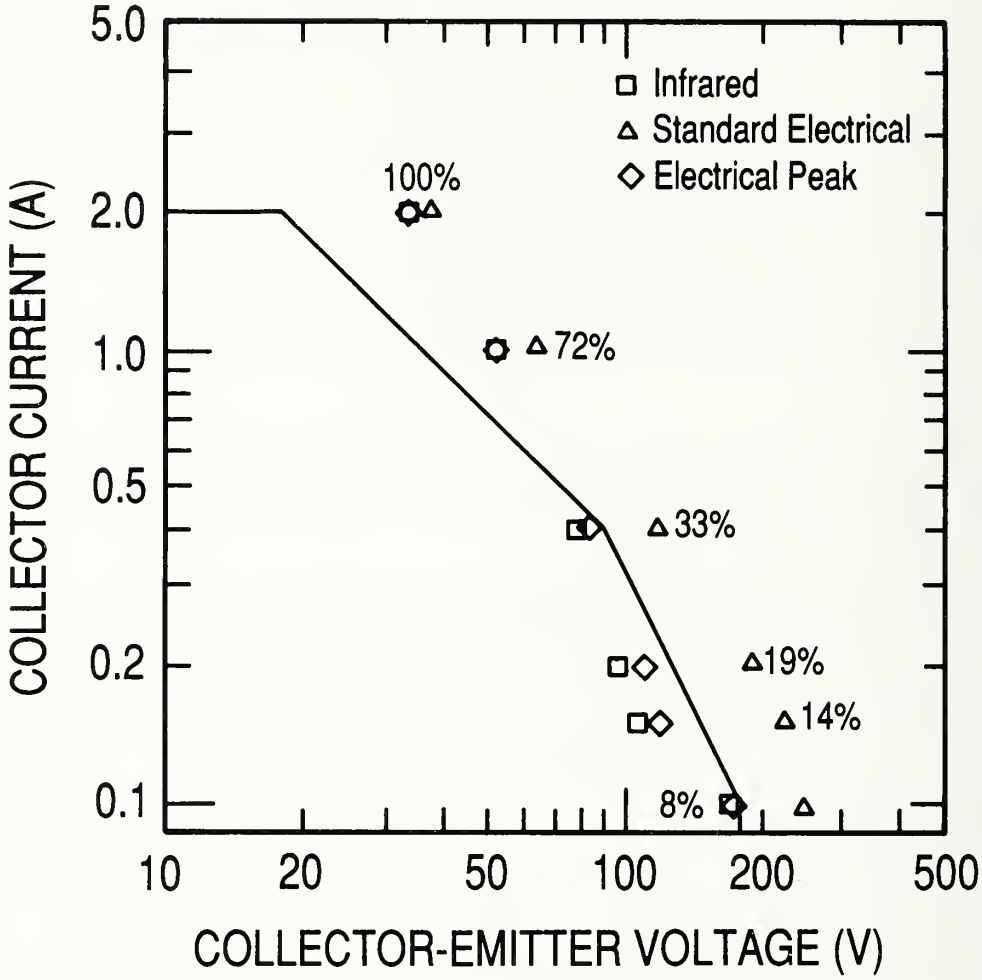


Figure 18. The manufacturer-specified SOA limits (solid line) and points along the measured SOA limits as determined by an infrared microradiometer, by the peak temperature electrical technique, and by the standard electrical technique. The number beside each standard electrical point is the percent of the total active area estimated to be dissipating power for each operating condition.

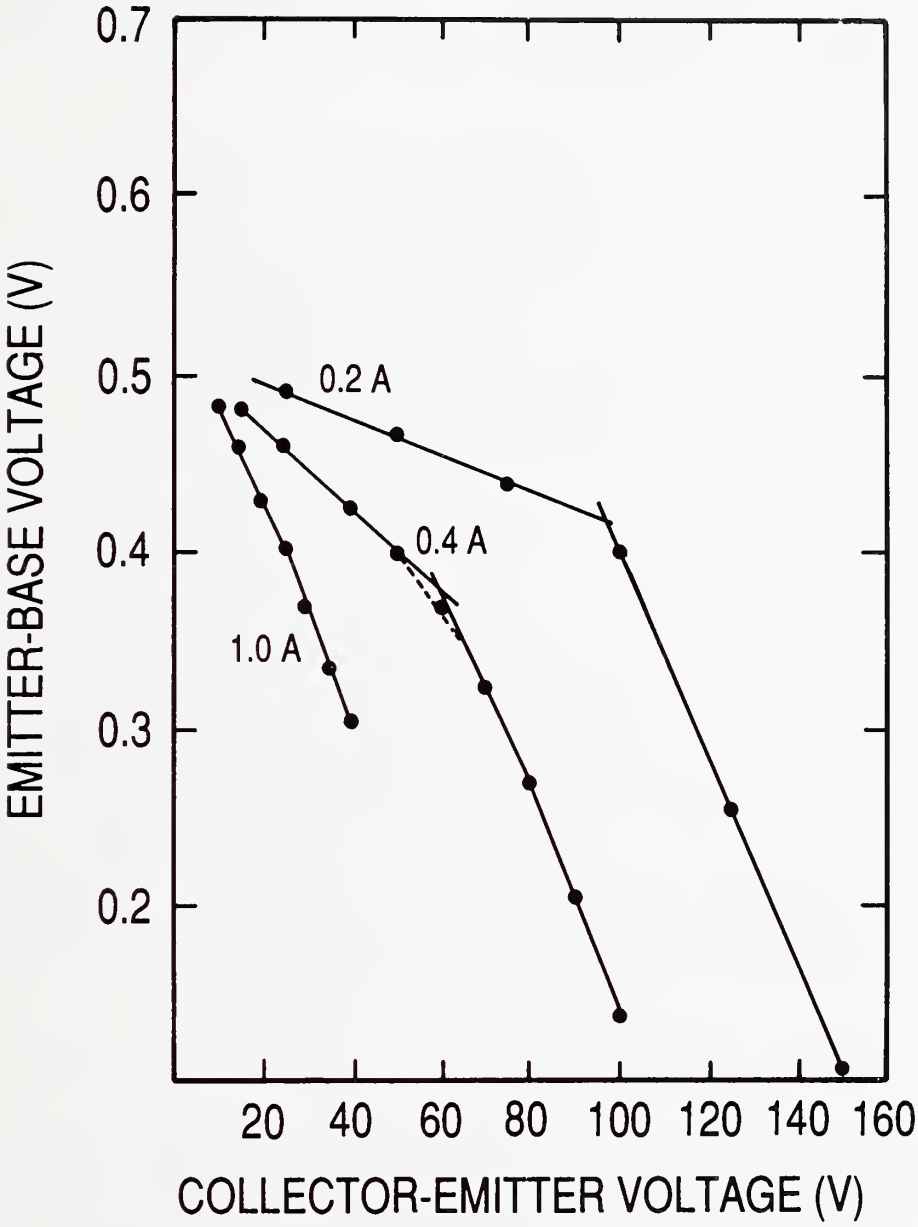


Figure 19. The measured V_{EB} at 20 μs after the removal of a 1-s power pulse versus V_{CE} for a number of values of I_C. The onset of current crowding is noted by the initial break in the linear relation of V_{BE} versus V_{CE} as V_{CE} is increased.

then a careful measurement of the thermal resistance is required. This requires that dc measurements for pulse lengths approximating many seconds be made. Also, careful heat sinking and reference temperature measurement are required. In all, such a measurement is long and difficult. If one truly wants to know the dc temperature, there are really no shortcuts. Fortunately, such measurements can be made on a sampling basis on a few devices from a lot.

Oftentimes, one wants to "compare" devices to one another. Such is the case in performing thermal measurements for die-attach evaluation. Usually, devices of the same type differ in thermal resistance because of differences in die-attach quality. Well-bonded chips have a lower thermal resistance than poorly bonded chips. One can screen out poorly attached dice by comparing the thermal response of the devices. Since it is mainly the die attach that causes differences in the thermal resistance, it is advantageous to make the die attach as large a part of the measurement as possible. Heat flows from the chip to the die attach, to the heat spreader, to the package, to the heat sink. The dc thermal resistance measurement adds all of these factors to one another. The die-attach portion is a small part. If only the die-attach portion differs between devices, then one is looking for a small change in a big number if the dc thermal resistance is used. It would be ideal if one could measure only the "thermal resistance" of the die attach. Closer to practicality, but still close to ideal, it would be satisfactory to include only the thermal resistance of a few of the other heat transfer regions (chip, die attach, heat spreader, package, heat sink). This can be accomplished by heating the device with a short pulse (ranging from 10 to 100 ms for most device types), short enough that the heat energy only has time to flow through the chip and into the die-attach area. The pulse is stopped before significant heat enters into the heat spreader. In this way, the measured temperature is a function of the chip and the die attach and does not depend upon the other transfer elements. It must be emphasized, though, that all one is testing here is the die attach. Usually, the dc thermal characteristics follow the die-attach characteristics, but not always. Nevertheless, a pulsed measurement used to detect the right parameter, i.e., die-attach quality, is certainly better and easier than performing a dc test [13]. The advantages of this technique are summarized in table 4.

A die-attach test, or a theoretical calculation, does not replace the need for accurate characterization of the transient and dc thermal resistance of a device. The measurements do not have to be made on every device, but they must be made on enough devices to assure the manufacturer and user that well-bonded devices will have a thermal resistance less than some agreed-upon value. A true-life example of the need to know the dc thermal resistance is in order. A device user was experiencing a high failure rate in one particular bipolar transistor in a motor drive system. The particular device had two Darlington chips paralleled in a single TO-3 package. An obvious question was, "How well are the chips sharing the workload?" If one chip is poorly die bonded compared to the other, then it may end up hogging all the current due to the positive thermal feedback effects for which bipolar transistors are well known. Pulsed tests were made out to pulses 1 s in length, and no particular differences were noticed between devices. Also, the 1-s measurements indicated that the dc thermal resistance was within specifications when using theoretical thermal response curves. Careful dc thermal resistance measurements, though, revealed

TABLE 4

Advantages of Thermal Response Testing
for Die Attachment

The technique is:

- SENSITIVE – It can be used to detect contiguous voids as small as 10 to 15% of the chip bonding area.
- CONVENIENT – It can be performed on finished devices and requires minimal, if any, heat sinking.
- FAST – It can be automated.
- ADAPTABLE – It can be used for testing a wide variety of device types and structures.

that there was in fact a very wide variation in the thermal resistance of different devices. Subsequent measurements made with an infrared microradiometer revealed that in fact, oftentimes, only one of the chips was dissipating power while its parallel mate was along just for the ride. Qualitative infrared measurements showed that the pulsed measurements were accurate; the chips shared power equally for single pulses at least as long as 1 s. The problem was that because of the relative locations in the package of the two chips and the asymmetry of the heat spreader in the TO-3 package, the thermal resistance of one of the chips to the heat sink (the one that failed 80 percent of the time) was greater than that of the other chip. Thus, even if each chip shared evenly in the workload, one would be hotter (and thus eventually could not share equally because of the positive thermal feedback of bipolar transistors). The temperature rise during a single pulse was not enough to cause the chips not to share the pulse.

Measurement of Integrated Power Devices

The measurement of integrated power structures presents special difficulties. The major problem is that a simple, well-defined and well-behaved TSEP often is not available at the device terminals. Even if a TSEP is easily available, it may not be sensing the temperature at the desired region of the chip.

For instance, consider perhaps the simplest integrated power circuit, the monolithic, bipolar Darlington transistor. A circuit schematic of a typical Darlington is shown in figure 20. The actual chip for this Darlington is shown in figures 4 and 5. The output transistor Q2 dissipates the large fraction of the power in this device and is expected to be the hottest area on the chip. The emitter-base voltage is typically used as a TSEP for bipolar transistors, but for the Darlington, the emitter-base voltage measured at the terminals of the device is the sum of the emitter-base voltage of the input transistor, Q1, and the output transistor, Q2. Under most circumstances, then, the temperature measured using the emitter-base terminal voltage of the Darlington is some average temperature of the input and output device. There are no readily available temperature-sensitive parameters that one can use that only senses the output transistor temperature. This example is perhaps the simplest example of the problems associated with measuring the temperature of integrated devices.

Although this measurement cannot be made directly, an indirect determination of the Darlington output transistor thermal resistance using the emitter-only switching technique and a simple equation has been developed [26]. The procedure employs two separate measurements, one of the average temperature of the input and output transistors and the other of the temperature of the input transistor only. The method relies upon the presence of the two resistors, R1 and R2, and upon the fact that for very small values of emitter-base current, only the input transistor is active. This is because the voltage drop across R2 for very small currents may be made less than a diode forward voltage drop. This keeps transistor Q2 off. The method is outlined in table 5.

The Darlington example is indicative that perhaps simple thermal resistance measurements may not suffice for complex integrated power circuits. Many such circuits do have isolation

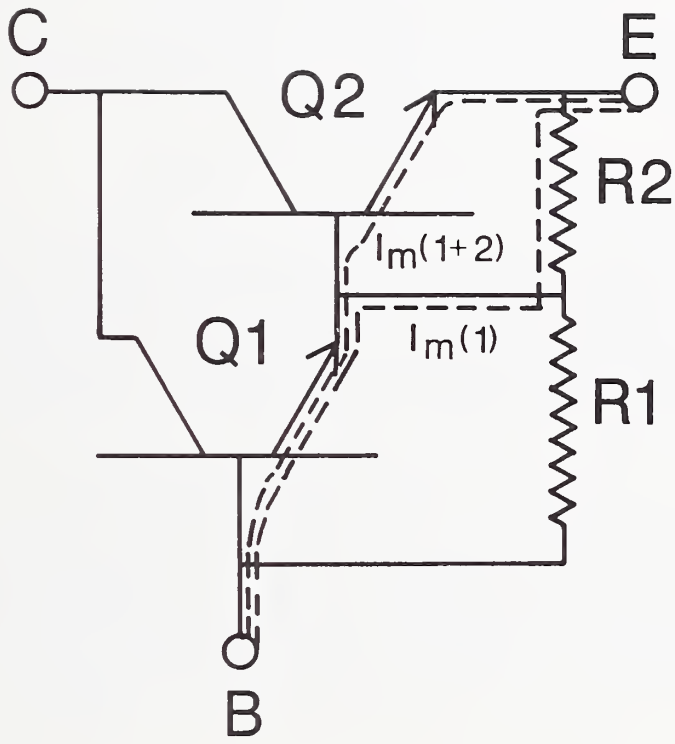


Figure 20. Schematic of Darlington transistor.

TABLE 5

Procedure for Measuring the Temperature
of Darlington Transistors
(see fig. 20 for Darlington details)

1. Using the emitter-base voltage of the Darlington as the TSEP, use the emitter-only switching method *and a measurement current small enough to only turn on the input transistor* (Q1) to measure the temperature of Q1. The measurement current is selected to be small enough that the potential drop across R2 is less than about 0.3 V. Call this temperature T(1).

2. Increase the measurement current such that both transistors Q1 and Q2 are turned on during measurement. The current should be large enough that the potential drop across R2 is greater than about 1.0 V. An average temperature of Q1 and Q2 is measured with this step. Call the temperature measured T(1+2).

3. The temperature T(2) of the output transistor Q2 is calculated as T(2) = 2T(1+2) – T(1).

diodes, but the diode is usually not sensing the temperature of the power elements, the temperature of most interest.

Power Transistor Thermal Standardization Activities

Presently active in the improvement and standardization of thermal characterization techniques for power transistors are the Electronic Industries Association's JEDEC JC-25, JC-50.1, and JC-13.1 Committees on Transistors, GaAs Reliability & Quality Standards, and Government Liaison for Discrete Devices, respectively, and the Department of Defense through the Defense Electronics Supply Center (see table 6 for details). Technical expertise and a willingness to participate actively in the development of standards are always welcomed by the various groups involved in these efforts.

II. INTEGRATED CIRCUITS [27]

Introduction

The thermal characterization of packaged integrated circuits generally takes one of three forms. They are computer simulations and both direct (infrared) and indirect (electrical) measurements of the integrated circuit chip surface/junction temperature [28]. Due to the inherent difficulties in analyzing and measuring the thermal properties of active integrated circuit chips, an approach using specifically designed thermal test chips for evaluating new packaging schemes is finding wide acceptance in the industry. The focus of this section is on the thermal characterization of single-chip ceramic packages, although there is some discussion pertaining to plastic packages and hybrids.

Thermal resistance has been used over the years as an aid to device manufacturers and users for calculating the junction temperature of operating devices. The concept of a unique value of thermal resistance is based upon an analogy between the electrical and thermal properties of materials, with temperature, power dissipation, and thermal resistance being analogous to voltage, current, and electrical resistance, respectively. The thermal resistance ($R_{\theta JR}$) is defined as follows:

$$R_{\theta JR} = \frac{(T_J - T_R)}{P_H} \tag{9}$$

where

$R_{\theta JR}$ = thermal resistance between the junction and the reference point (usually on the device case or in the surrounding ambient) (°C/W),

T_J, T_R = temperature of the junction and the reference point, respectively, (°C), and

P_H = power dissipation in the device (W).

In applying the electrical analogy to the thermal problem and in using eq (9), it is implicitly assumed that uniform electrical power and temperature distributions exist across

TABLE 6

Power Transistor Thermal
Test Method Standardization

1. "Thermal Resistance Measurements for Bipolar Transistors (Emitter-to-Base Forward Voltage, Emitter-Only Switching Method)," Method 3131.2, MIL-STD-750C Test Methods for Semiconductor Devices, Dept. of Defense, Washington, DC.

2. "Thermal Impedance Measurements for GaAs MESFETs (Constant Current Forward-Biased Gate Voltage Method)," Method 3104, MIL-STD-750C Test Methods for Semiconductor Devices, Dept. of Defense, Washington, DC.

3. "Thermal Impedance Measurements for Insulated Gate Bipolar Transistors (Gate-to-Emitter On-Voltage Method)," Method 3103, MIL-STD-750C Test Methods for Semiconductor Devices, Dept. of Defense, Washington, DC.

4. "Thermal Impedance Measurements for Vertical Power MOSFETs (Source-to-Drain Diode Voltage Method)," Method 3161, MIL-STD-750C Test Methods for Semiconductor Devices, Dept. of Defense, Washington, DC.

5. "Thermal Resistance Measurements of Conduction Cooled Power Transistors," EIA RS-313-B, Electronic Industries Association, Washington, DC.

6. "Low Frequency Power Transistors (Part 4 – Thermal Characteristics)," JEDEC Standard No. 10, Electronic Industries Association, Washington, DC.

7. "Power MOSFET's (Chapter 4 – Thermal Characteristics)," JEDEC Standard No. 4, Electronics Industry Association, Washington, DC.

the junction of the microelectronic device under study and that one-dimensional heat flow occurs from a planar heat source. The assumption is also made that the thermal properties of the materials involved are not dependent on temperature. These assumptions imply a unique value of thermal resistance for devices of a given design and construction. Since these assumptions are not completely valid for actual semiconductor devices, care is needed in applying the results of eq (9) to real devices. Because both monolithic and hybrid integrated circuits do not normally have uniform power dissipating sources, nor do the materials from which they are made have thermal conductivities that are independent of temperature, it is imperative that the conditions under which the device is thermally characterized are clearly described. If this is not done, it will be almost impossible to get accurate, reproducible, and correlatable results.

In this publication, the three techniques for thermally characterizing integrated circuits are discussed in terms of their usefulness in characterizing VLSI ceramic packages. A major problem, though, is that one is tempted to assume that one (or possibly all) of the techniques can be used as a standard in terms of accurately indicating the thermal properties of packages. There is no a-priori "right" technique. At best, operating and test conditions can be defined that bear some relationship to reality and that give reproducible results.

Design of Thermal Test Chips

A variety of thermal test chips is being used in the industry, with most companies using chips of their own design. Despite this general use of thermal test chips by the defense community, and semiconductor chip, package, computer, and automotive companies, these chips are still not readily available. Chips are circulated among users with little or no documentation. A chip that is suitable for die-attachment quality-control screening may not be usable for the thermal characterization of packages. Also, chips of the same physical size may have very different heat-source and temperature-sensing configurations. The implications of a particular chip design should be understood in order that the measured results might be rationally interpreted.

Thermal test chips currently used in the industry employ planar technology and have separate heating and temperature-sensing elements. Examples of pictorial representations of thermal test chips are given in figure 21; actual photographs are shown in figure 22. As can be seen, there is little commonality in layout and size. In all cases, p-n junctions are used as the temperature-sensing elements, although not all of the diode elements are independently accessible (see inserts in fig. 22). Heating elements are diffused resistors in a variety of series-parallel combinations in all but one of the examples shown in figure 21. The advantage of separate heating and sensing elements over the normal techniques for measuring the thermal resistance of discrete semiconductor devices [12], and operating integrated circuits [29], is that no electrical switching is involved. How then does one choose between the various thermal test chip designs either presently in use or being proposed for future production? One approach that has been shown to be feasible is that of using computer simulations of the chip-package configuration to gain insight into how best to design and utilize thermal test chips [27,30].

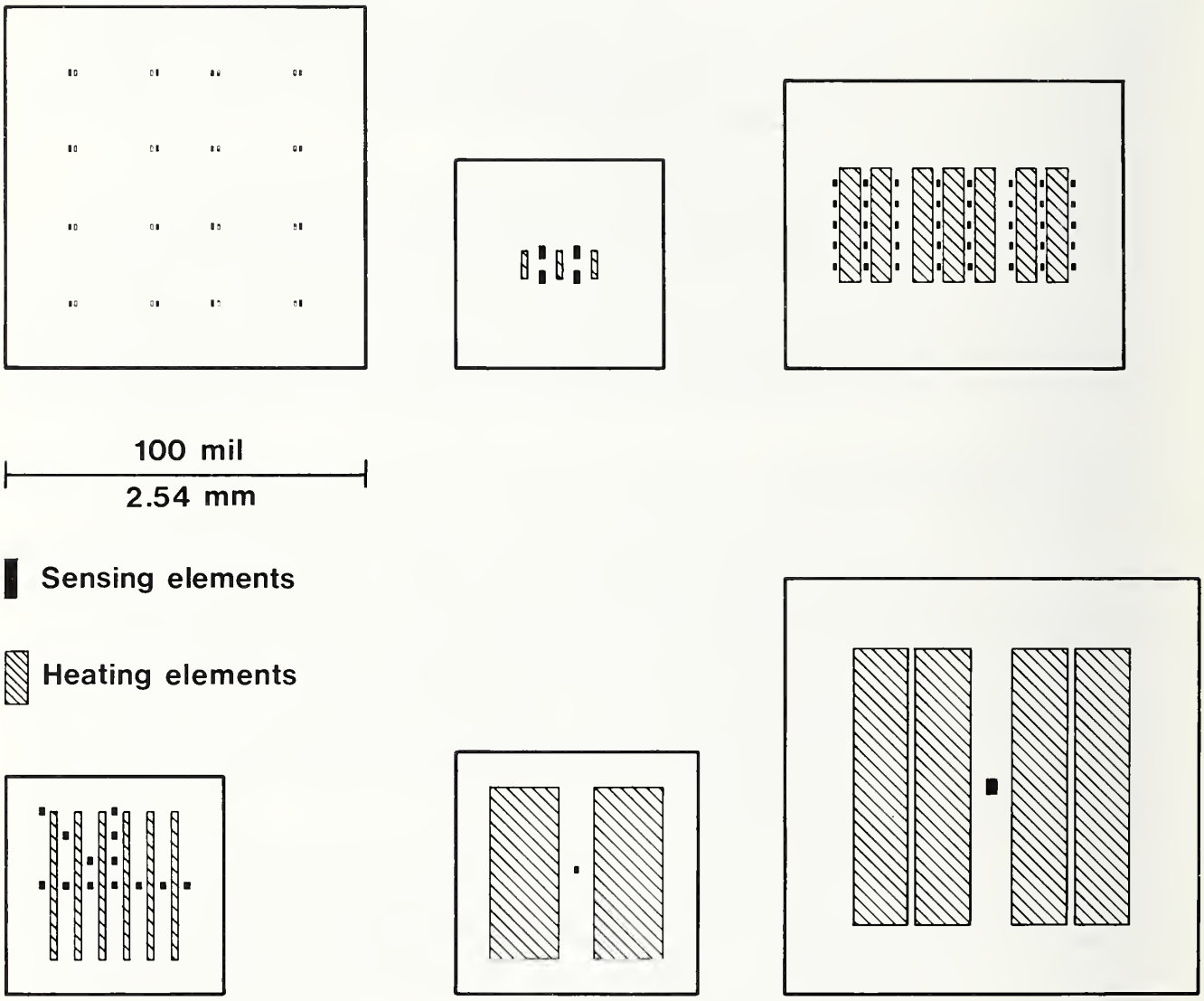


Figure 21. Pictorial representation of heating and sensing areas on thermal test chips.

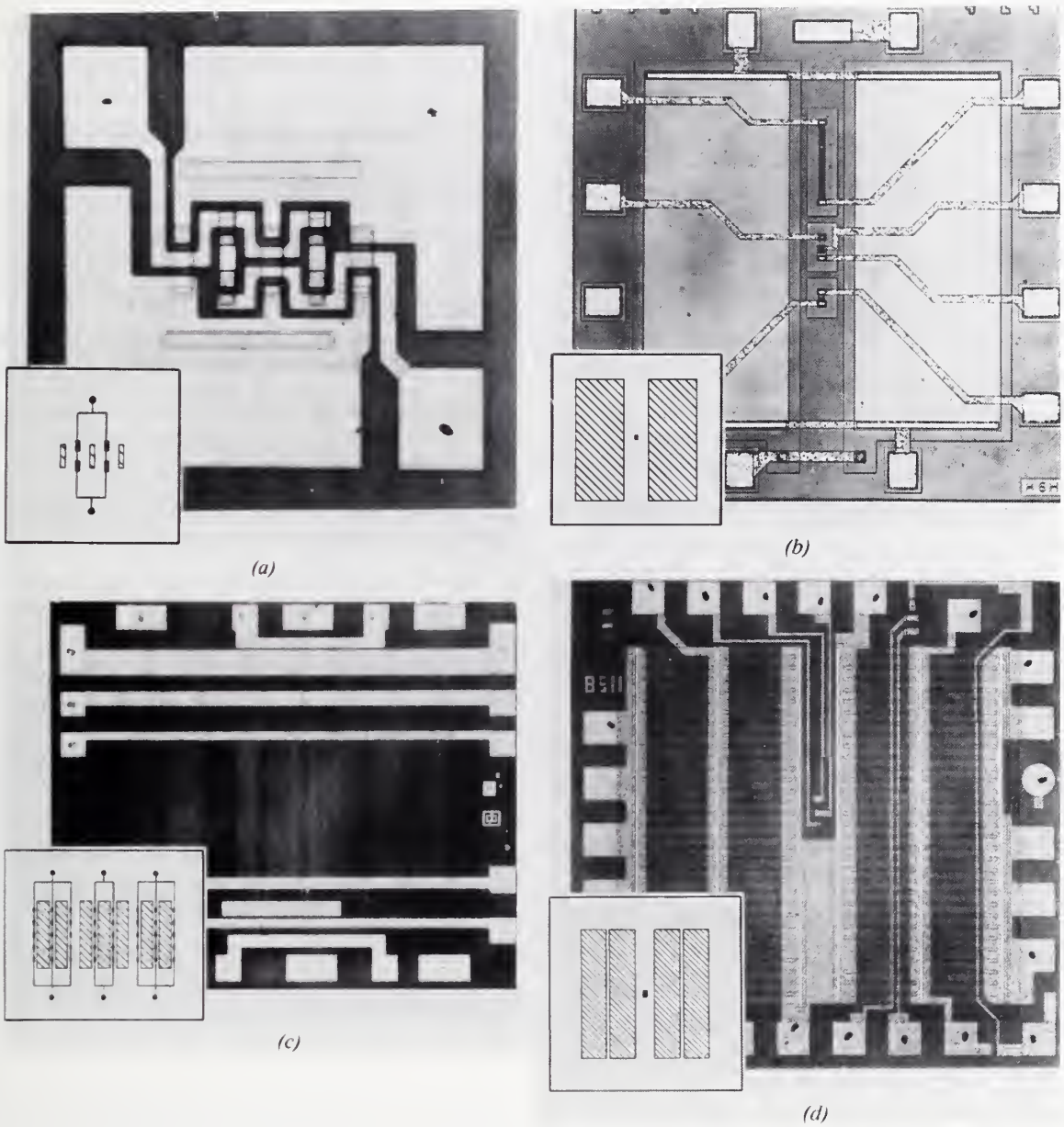


Figure 22. Photomicrographs of representative thermal test chips with inserts showing sensing diode circuit configuration. (a) Signetics; (b) Motorola; (c) Burroughs; (d) Texas Instruments.

Computer Simulations – Theoretical analysis for thermally characterizing semiconductor devices has taken many forms, from the simplistic to the complex. Computer simulations generally take one of the following forms: numerical analysis using finite element or finite difference codes [31,32], closed-form analytic solutions using Laplace and/or Fourier transforms, or Green's function methods for solving the heat flow equation [33-36]. It is the task of users of computer codes to ascertain which technique will do the required job adequately [36,37]. For example, in a study conducted by Oettinger [27] and Albers [30], the steady-state temperature distribution in thermal test chips bonded to various substrate layers was simulated using the model originally developed by Kokkas [34]. The structure modeled is depicted in figure 23 and consists of three layers with an arbitrary number of heat sources on the surface of the top (first) layer. The rectangular dimensions of the three layers are identical, although the thermal conductivity and thickness of each layer may differ. The bottom of the third layer is assumed to be in contact with an ideal heat sink and is held at a constant temperature. The model assumes only conductive heat transfer through the three layers and no heat transfer from or through interconnection leads. This assumption has been shown by Baxter to be valid for a wide variety of integrated circuit package configurations in which there is a preferred heat flow path, i.e., for most ceramic packages [28]. The simplicity of the model leads to a closed-form analytic solution which lends itself to the calculation of the temperature at any point, or points, on or inside the three-layer structure. The computer code to implement this solution, written in FORTRAN and designated TXYZ, has been documented by Albers [30].

Thermal Properties of Materials – One of the difficulties that occur when one attempts to model semiconductor structures is that accurate information on the thermophysical properties of the materials involved is not readily available. For steady-state thermal simulations, the thermal conductivity of the various materials is the property of particular interest. The thermal conductivity of silicon and of both alumina and beryllia are very temperature dependent [38,39]. Also, the thermal conductivity of ceramics is very dependent on the purity of the material [40]. Examples of these variations are shown in figure 24 for silicon, alumina, and beryllia. The situation is worse for die-attachment materials such as solders, eutectics, and conductive and nonconductive epoxies. For these materials, accurate values of thermal conductivities are hard to find. At the very least, a researcher should indicate what values of thermal conductivity are used, and the range of temperature and material purity for which they are valid.

Guidelines for Thermal Test Chip Design – In a study conducted by Oettinger [27] and Albers [30], thermal test chips representative of industrial practice were modeled to determine their efficiency in adequately characterizing the thermal properties of VLSI package structures. The structures modeled simulate a silicon chip 15 or 30 mil (0.38 or 0.76 mm) thick, bonded with a 1-mil- (0.025-mm-) thick layer of either gold-silicon eutectic or silver-filled epoxy, to a 30-mil- (0.76-mm-) thick substrate of either alumina or beryllia. The values of thermal conductivity for the various materials used in this study are given in table 7. Based on the results of the computer simulations of various chip-substrate configurations, the following recommendations are made for the design of thermal test chips for VLSI package characterization:

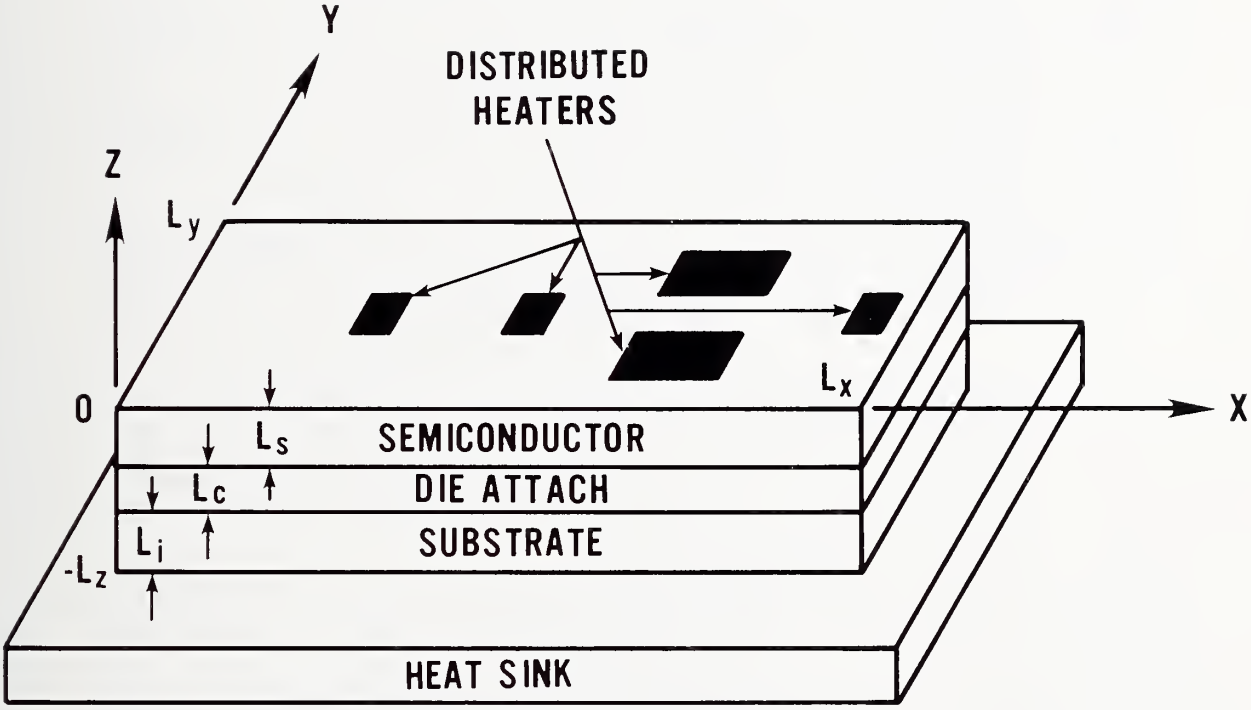


Figure 23. Three-layer structure modeled by computer code.

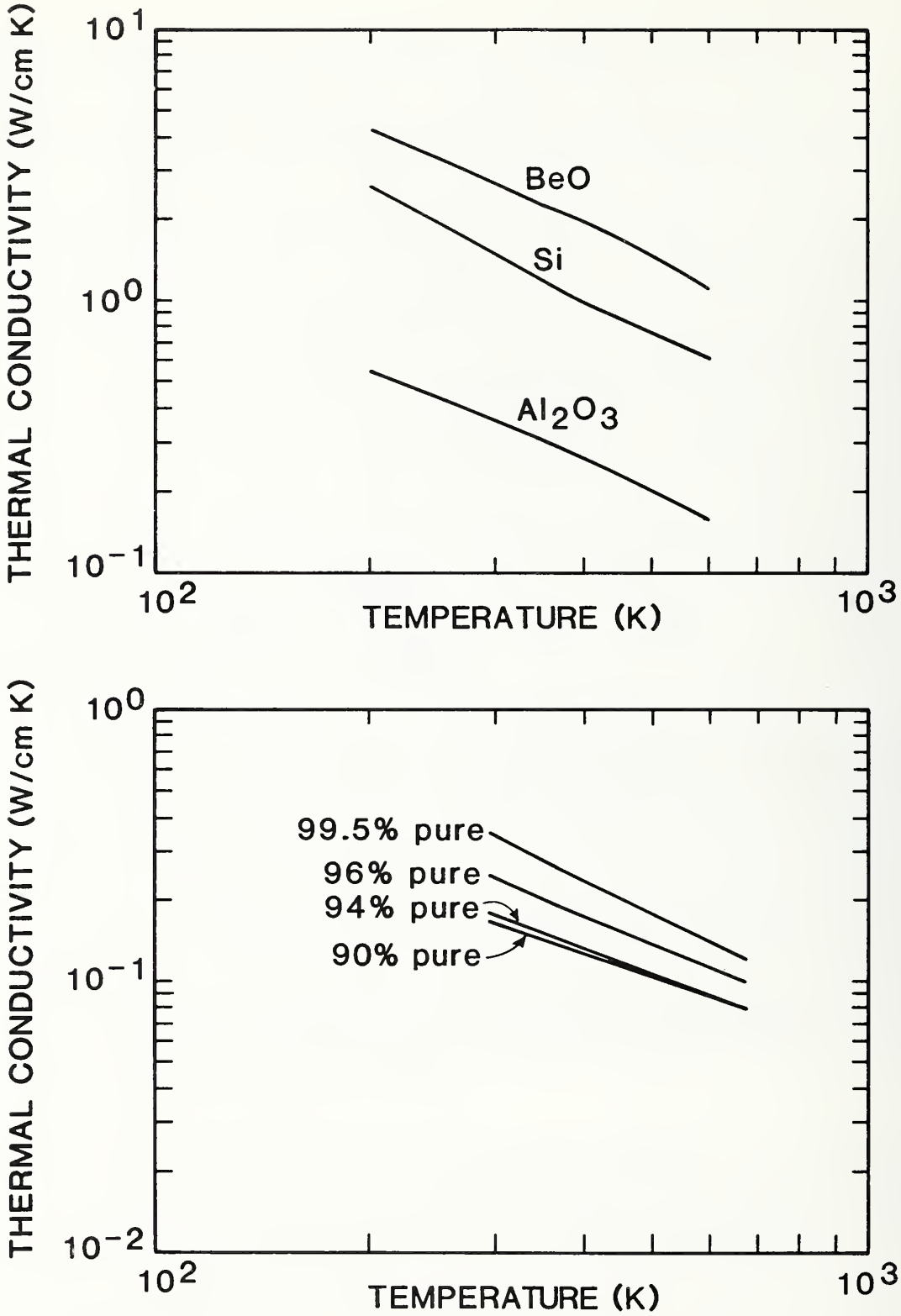


Figure 24. Influence of temperature on the thermal conductivity of integrated-circuit-related materials. Thermal conductivity of various materials (top); thermal conductivity of aluminum oxide for various purities (bottom).

TABLE 7

Thermal Conductivity of Materials

Conversion Factor: 1 cal/s = 4.184 W; k = Thermal Conductivity

Silicon

k(T) = 286/[T–100]	@T = 300–600 K
k = 1.05 W/cm °C	@T = 100°C [k = 0.00267 W/mil °C]
k = 0.976 W/cm °C	@T = 120°C [k = 0.00248 W/mil °C]

Copper

k = 3.93 W/cm °C	@T = 20–100°C [k = 0.00998 W/mil °C]

Kovar

k = 0.21 W/cm °C	@T = 20–100°C [k = 0.000533 W/mil °C]

Steel [1010]

k = 0.46 W/cm °C	@T = 20–100°C [k = 0.00117 W/mil °C]

Alumina (99–99.5%)

k = 0.25 W/cm °C	@T = 20°C [k = 0.00064 W/mil °C]

Gold-Silicon Eutectic

k = 2.95 W/cm °C [k = 0.0075 W/mil °C]

Solder

k = 0.35 W/cm °C [k = 0.0009 W/mil °C]

Epoxy (Electrically Conductive – Silver Filled)

k = 0.016 W/cm °C [k = 0.00004 W/mil °C] @120°C

Epoxy (Electrically Insulative – Alumina Filled)

k = 0.004 W/cm °C [k = 0.00001 W/mil °C] @120°C

Beryllia (98%)

k = 2.05 W/cm °C [k = 0.0052 W/mil °C] @20°C
k = 1.54 W/cm °C [k = 0.0039 W/mil °C] @100°C

Alumina (90–92%)

k = 0.17 W/cm °C [k = 0.00043 W/mil °C] @20°C
k = 0.15 W/cm °C [k = 0.00038 W/mil °C] @100°C

1. The heat sources, i.e., the resistor stripes or transistors, should utilize as much of the active chip area as possible so that the measured package thermal resistance is indicative of the chip size being used. A 10-mil- (0.25-mm-) parameter stripe should be sufficient for bonding pads, etc. Examples of the variation of chip surface-to-case thermal resistance with chip size, for a silicon chip eutectically bonded to either alumina or beryllia substrates, are given in figure 25. It is desirable to use a range of test chip sizes so that the package thermal resistance can be determined as a function of chip size. Arrays of test chips can be built up from, for example, a 100-mil- (2.54-mm-) square standard chip size.

2. Spacing between heat sources, which is needed to accommodate the temperature-sensing elements, i.e., diodes, should be minimized. The spacing should be less than or equal to 2 mil (0.051 mm). The sensing element should be located at the center of the chip surface and should be as large as possible, consistent with design rules. Examples of the temperature distribution of thermal test chips utilizing these design rules are depicted in figure 26 for silicon chips eutectically bonded to either alumina or beryllia substrates. The chips consist of nine 100-mil (2.54-mm) basic cells, a single 300-mil- (7.62-mm-) square chip cell, and a chip with uniform heat source coverage over the entire active area (an ideal case).

3. The thermal test chip should be designed such that its power dissipation limitations are consistent with the range of package thermal resistance encountered. The ability to cause a chip surface-to-case temperature difference of at least 20 °C is desirable. The heat source power dissipation needed to produce a chip surface-to-case temperature difference of 20 °C is presented in figure 27, for a silicon chip eutectically bonded to either alumina or beryllia substrates.

Following these recommendations, the computer simulations for these package configurations predict that the temperature sensor will measure a temperature that is at least 90 percent of the peak temperature on the chips. This was also found to be the case if the sensor temperature was compared to the peak temperature on the surface of an ideal thermal test chip where the total active chip surface area was covered by a uniform heat source. The chip surface-to-case temperature difference versus distance curves, depicted in figure 28 for various test chip designs, show the temperature variations that might be encountered. It should be noted that the heat source layout depicted in chip A does not adhere to the proposed guidelines. In general, even for chip designs that adhere to the indicated guidelines, the higher the substrate thermal conductivity, the worse the agreement.

A comparison was made between measured results using a thermal test chip and the TXYZ predictions for a ceramic leadless chip carrier package. The thermal resistance data, using an early Signetics thermal test chip design (see fig. 22(a)) [41] were supplied by Corman [42]. The measured junction-to-case thermal resistance obtained was not indicative of what one would expect for a chip of the particular size used. The chip heating and sensing element layout, the measured data, and curves of computed results for the actual (curve A), ideal (curve B), and proposed (curve C) thermal test chip designs for the 180-mil- (4.57-mm-) square chip used in the study are presented in figure 29. The data indicate that this

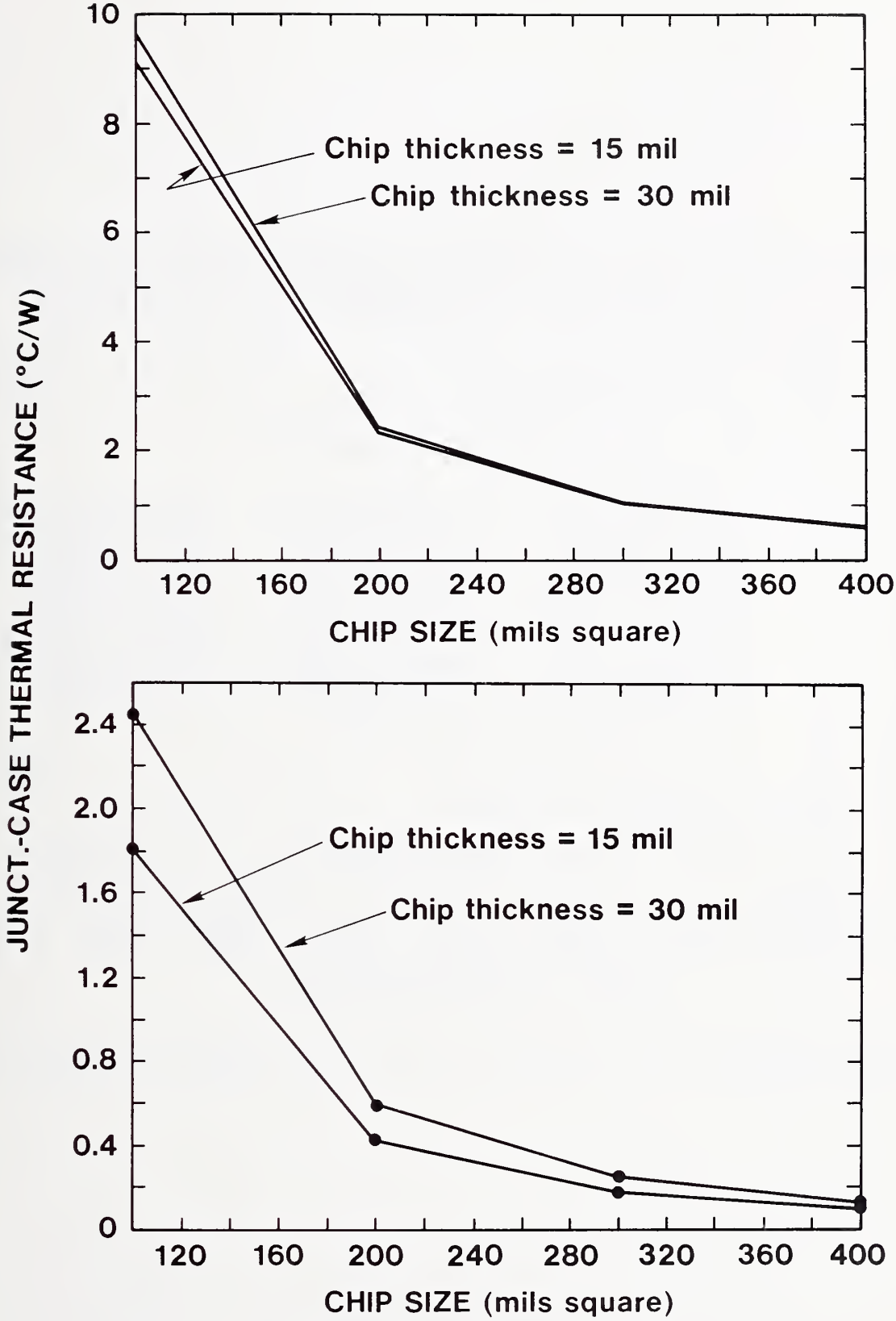


Figure 25. Influence of chip size on the junction-to-case thermal resistance of a three-layer package structure. Alumina substrate with thickness of 30 mils (top); beryllia substrate with thickness of 30 mils (bottom).

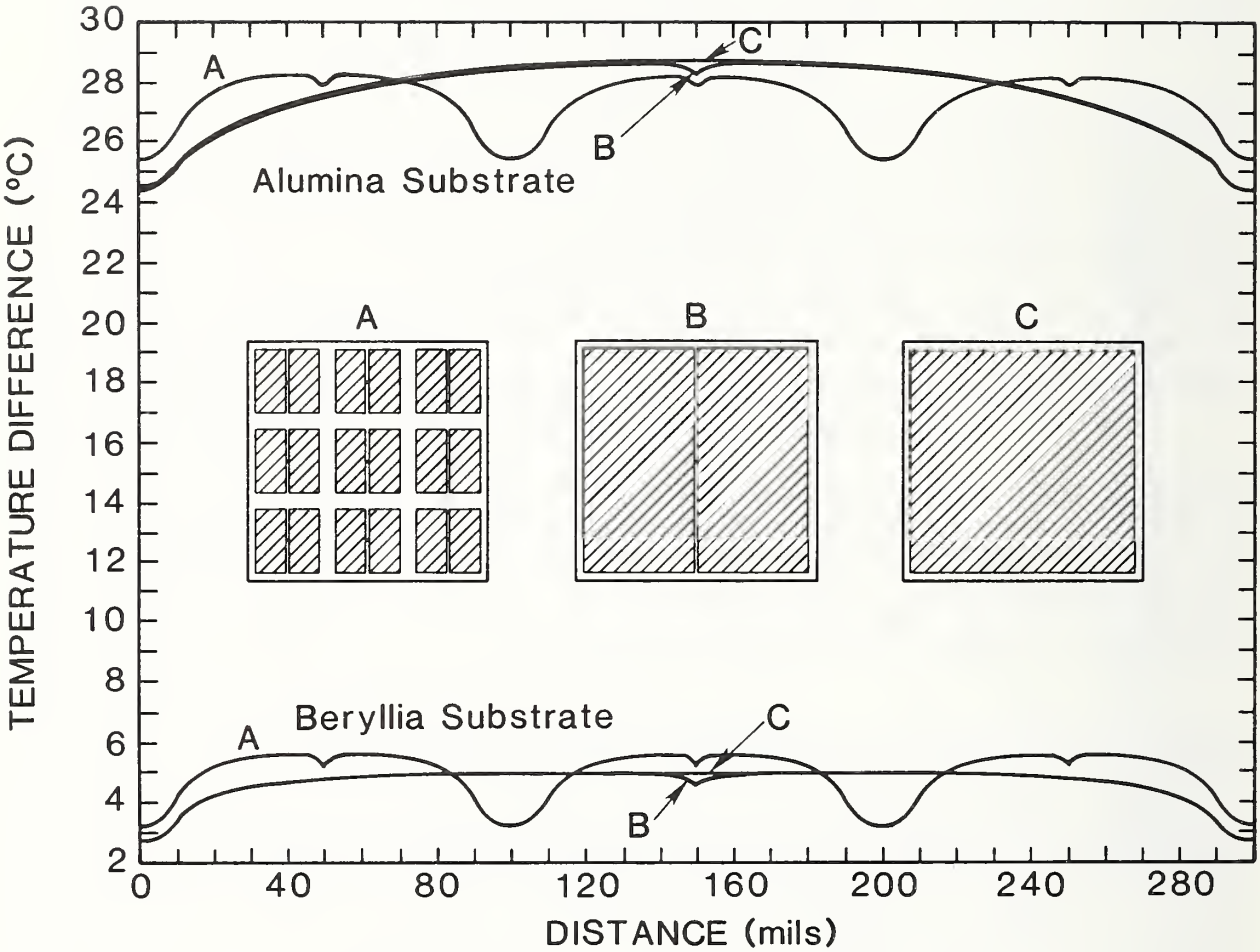


Figure 26. Influence of heat source layout on chip surface temperature for test chip arrays and single cell chips.

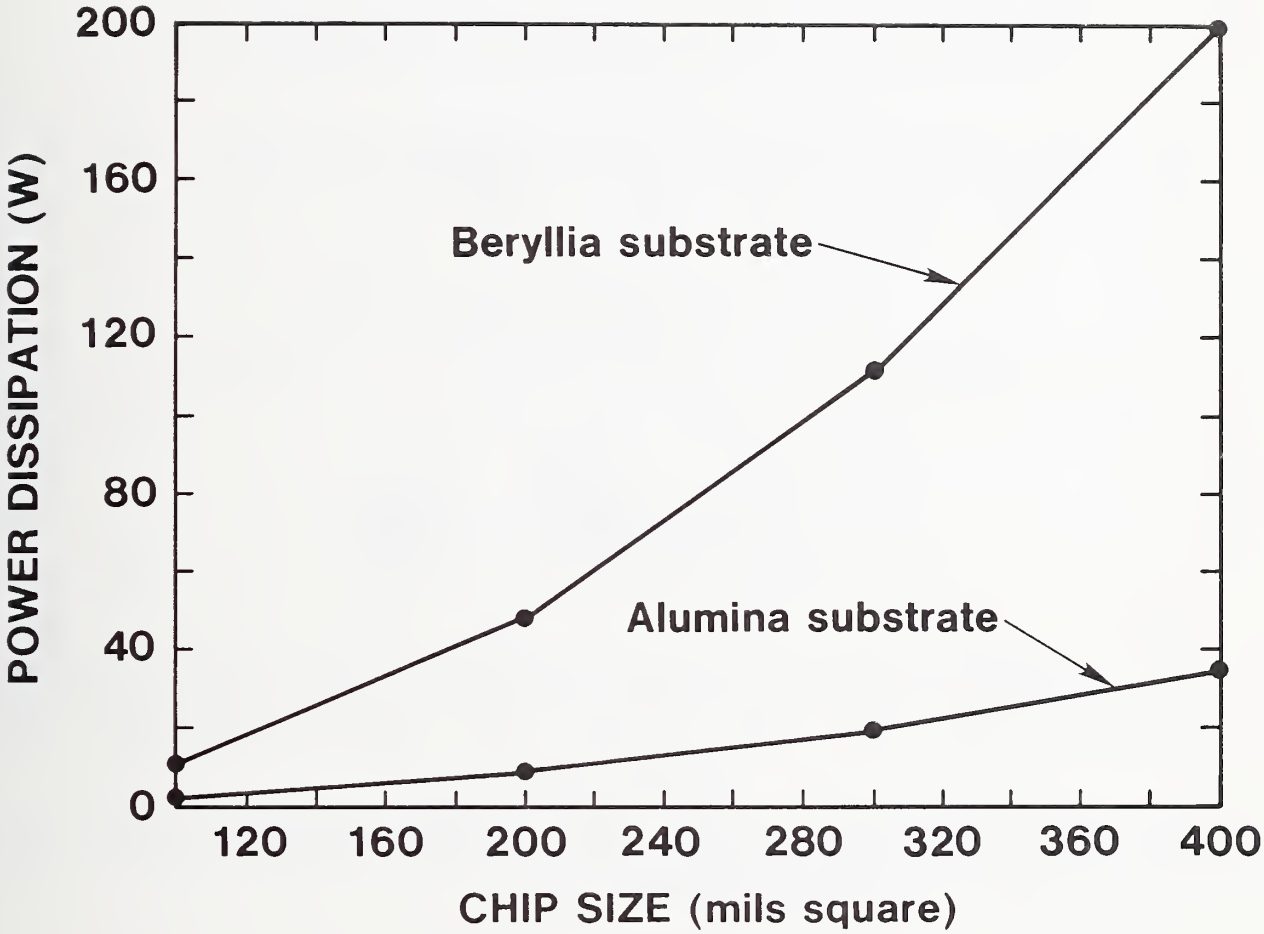


Figure 27. Influence of chip size on internal power dissipation for a junction-to-case temperature difference of 20 °C.

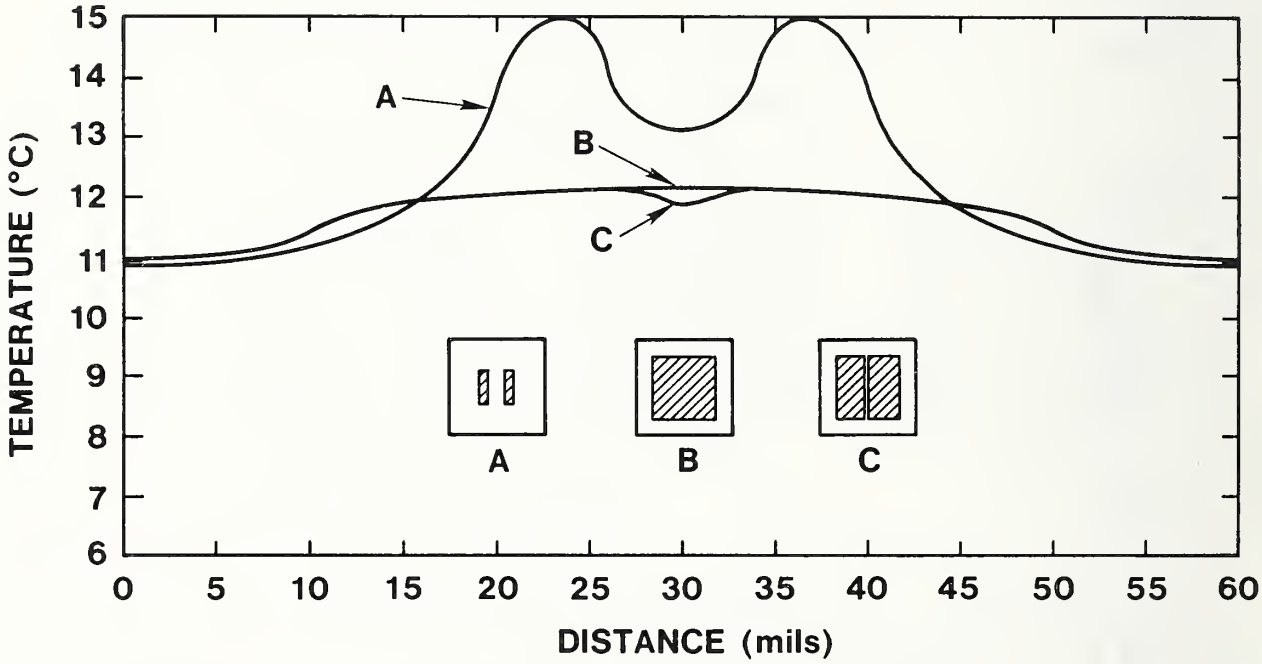


Figure 28. Influence of heat source layout on chip surface temperature for a silicon chip eutectically bonded to an alumina substrate.

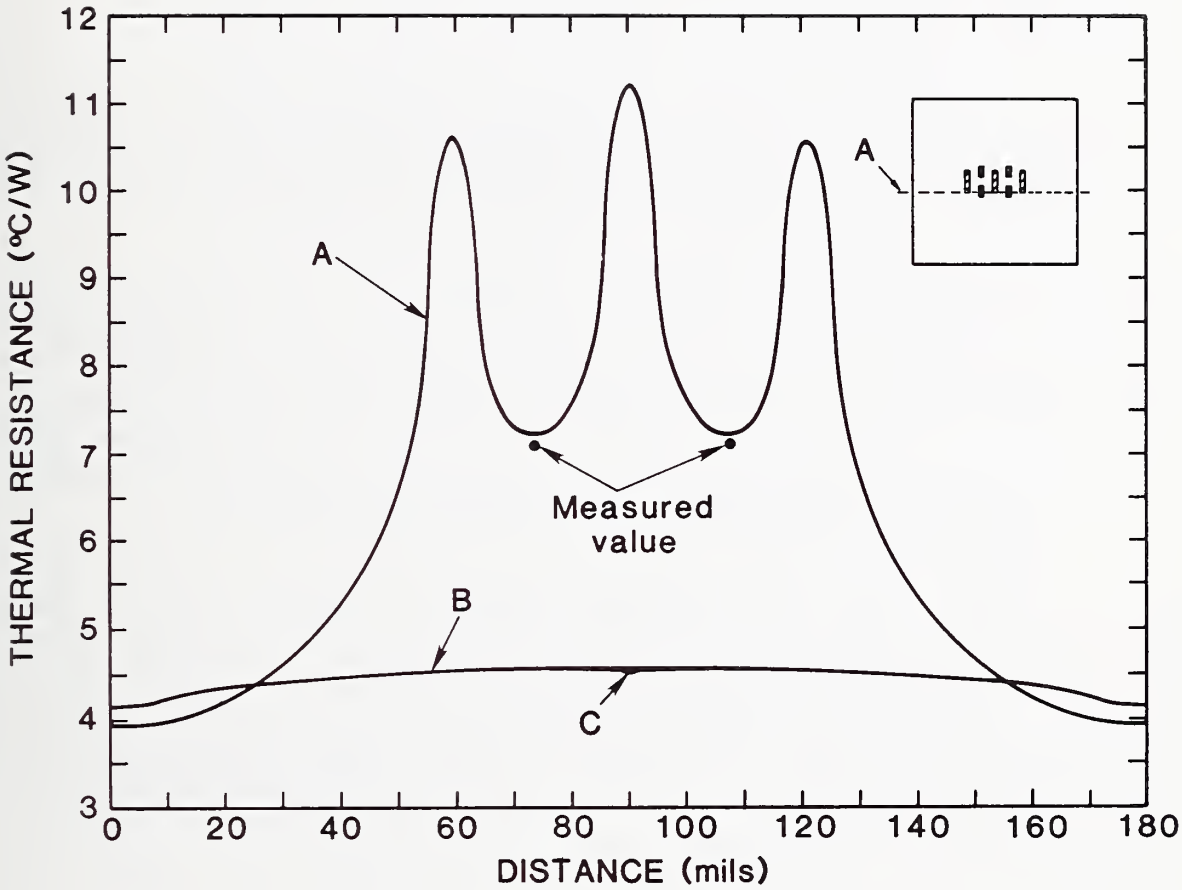


Figure 29. Comparison of computer-simulated and measured thermal resistance for a leadless ceramic chip carrier package.

particular thermal test chip design would give overly conservative results in characterizing the thermal properties of a similar package with the same size chip with uniform power dissipation. The quantitative nature of the TXYZ code is also demonstrated.

Fabrication techniques for implementing thermal test chips vary and are not limited to bipolar technologies. Table 8 lists a number of possible techniques for fabricating thermal test chips using both bipolar and MOS technologies. Most of these approaches have been utilized at one time or another.

Utilization of Thermal Test Chips

Assuming that one is satisfied with the design of a thermal test chip and is ready to measure the thermal characteristics of a particular chip package configuration, then both direct and indirect procedures, along with a variety of mounting arrangements, are available for measuring the chip-surface/junction temperature of the packaged device.

Mounting Considerations – At present, there is no consensus as to the preferred mounting arrangement for thermally characterizing VLSI packages. There is even difficulty in determining how to quantify what is "best." Also, when one discusses mounting arrangements, it becomes apparent that the point at which the reference temperature is measured is an important consideration. Should junction-to-case or junction-to-ambient temperature measurements be made? At what specific location on the device case or in the surrounding ambient environment should the reference point temperature be measured?

There are four basic mounting configurations used when thermally characterizing packaged microelectronic chips. These mounting methods, pictorially depicted in figure 30, potentially allow for measurements of both case and ambient environment temperatures. All of these mounting methods are presently being used to characterize thermally VLSI packages, although there appears to be little agreement between the various approaches. Baxter, in his studies to identify a preferred technique for thermally characterizing military grade integrated circuit packages [28], indicates that using a reference point on the package for junction-to-case thermal resistance measurements can lead to reproducible results that are independent of the type of package heat-sinking used. For packages with a preferred heat flow path, the recommended case reference point is the point of maximum temperature on the package. This reference point is determined with the device operated in free air and with no external heat-sinking. For ceramic and metal packages, this point is generally located on the package surface directly below the chip. It should not be assumed, though, that all devices have a preferred heat flow path. It is unclear at this time whether this concept can or should be applied, for example, to plastic-encapsulated devices. In fact, in a study conducted by Hannemann [43], in which plastic-encapsulated devices were included, an approach using the ambient as the reference point for microelectronic device thermal resistance measurements was advocated.

Computer simulations in support of the concept of a measured thermal resistance that is independent of heat-sinking were reported by Baxter et al. [44], and are shown in table 9 where computed junction-to-case thermal resistance ($R_{\theta JC}$) data are shown to be constant

TABLE 8

Fabrication Technologies for Thermal Chips

MOS Technology

- Polysilicon layer for heating and drain/source junctions for temperature sensing
- Transistors with the gate shorted to the drain for heating and p/n junctions for temperature sensing
- Discrete power transistor for heating and for temperature sensing
- Power transistors for heating and p/n junctions for temperature sensing

Bipolar Technology

- Diffused resistors for heating and p/n junctions for temperature sensing
- Discrete power transistor for heating and for temperature sensing
- Buried n^+ layer for heating and junction diodes for temperature sensing in an EPI layer immediately above
- Power transistors for heating and p/n junctions for temperature sensing

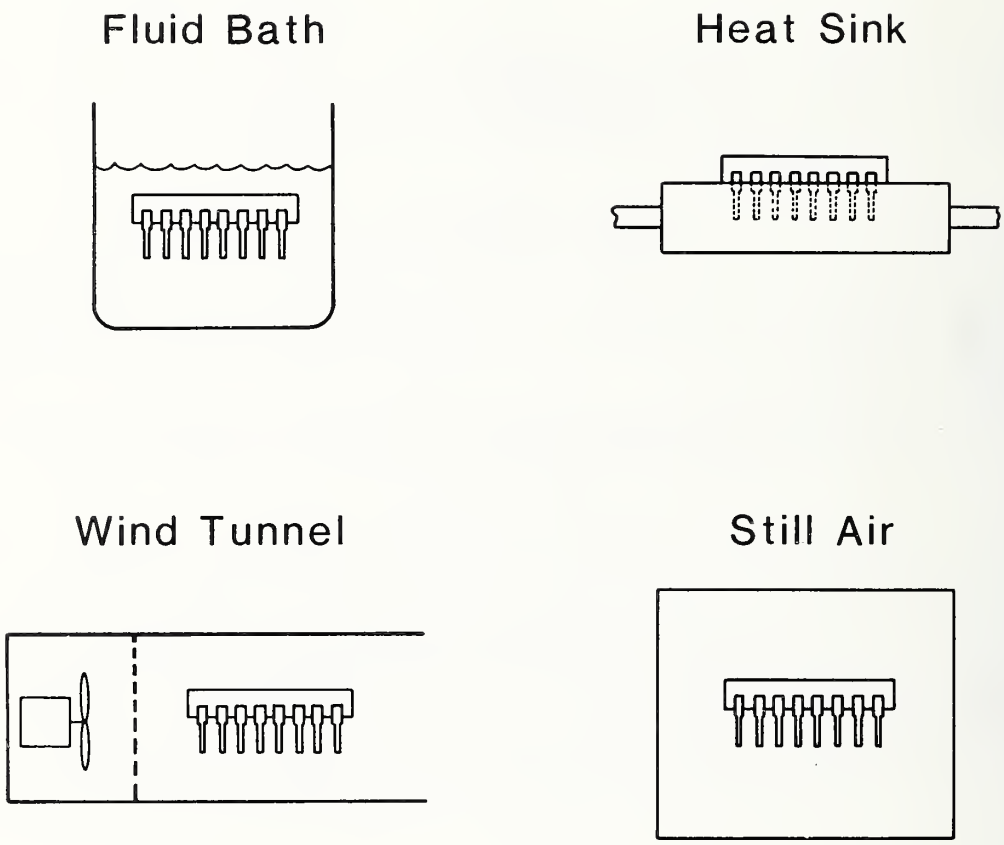
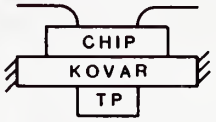


Figure 30. Package mounting arrangements.

TABLE 9

Computer Simulations of the Thermal Characteristics of Various Chip-Package Configurations

PICTORIAL DESCRIPTION	TEMPERATURE (°C)			THERMAL RESISTANCE (°C/W)			NOTES
	T_J	T_C	T_{TP}	$R_{\theta JC}$	$R_{\theta J-TP}$	$R_{\theta J-HS}$	
	121	77	-	10.8	-	13.9	Power dissipation at each of 4 junctions of thermal test chip
	117	75	-	10.4	-	12.8	40 Al bond wires heat sunk at substrate
	120	77	-	10.7	-	13.5	Substrate size increased Heat sink (HS) on bottom only
	152	110	-	10.6	-	21.7	Heat sink on sides only
	152	109	109	10.7	10.7	21.6	Thermal probe (TP) tip added with solder contact to substrate
	151	109	108	10.7	10.9	21.6	Thermal probe included with grease, probe-to-substrate
	123	82	81	10.4	10.5	14.5	Ceramic substrate with grease, probe-to-substrate

(after Baxter et al., Ref. [44])

for a variety of heat-sinking conditions. Support of this concept is also seen in figure 31 in which Brown [45] plots measured thermal impedance curves for a ceramic package with an integral aluminum heat sink under a variety of mounting and heat-sinking conditions. Note that for times less than approximately 10 s, the thermal impedance for all mounting conditions is the same. Although these results are encouraging, further studies are needed since agreement between mounting techniques such as the temperature-controlled heat sink and the fluid bath is generally poor.

The temperature-controlled heat-sink mounting method, which is usable for thermally characterizing packaged devices for both the direct and indirect measuring methods, is the most widely documented approach [12,46]. An example of a temperature-controlled heat sink for a dual-in-line package is shown in figure 32. In general, detailed documentation for the mounting methods depicted in figure 30 does not exist in the open literature.

Direct Measurement Procedures – Techniques for measuring the temperature of semiconductor chip surfaces have been utilized for many years. Approaches using liquid crystals, thermographic phosphors, laser scanners, liquid-gas (bubble) formation techniques, and infrared microradiometers have been quantified and used with varying degrees of success [7,9-11,47-51]. Each of these techniques presents a unique set of problems ranging from cost effectiveness and spatial and temperature resolution to ease of implementation and degree of contamination. The techniques are generally considered to be nondestructive, although this may be a matter of semantics since in all cases the chip surface is exposed and in most cases it is coated with a substance that is a potential contaminant. Since the infrared technique is the most widely used, it is the only one considered here, and the information presented has some relevance to the other techniques.

A pictorial representation of an infrared microradiometer is shown in figure 33. For semiconductor device studies, the temperature-sensing element used is generally a liquid-nitrogen-cooled indium antimonide detector. A good discussion on the use of infrared techniques for measuring the temperature of integrated circuits can be found in two papers published in the late sixties [50,51]. The information presented in table 10 summarizes some of the precision and accuracy considerations to be addressed [51], even today, if one is to utilize effectively the infrared technique.

Indirect Measurement Procedures – Temperature-sensitive electrical parameters of the particular packaged device being characterized are used as indirect indicators of chip surface/junction temperature in this measurement procedure. Generally, the forward voltage of a p-n junction is used as the temperature-sensitive electrical parameter. Resistors, diodes, or transistors are used to generate heat at or near the chip surface. The case temperature is measured on the outside of the package at a point in the main heat flow path between the chip and heat-dissipating medium. For discrete semiconductor devices, the temperature-sensing element is not separated from the heating element as is the case for most presently used integrated circuit thermal test chips. When the heating element also incorporates the temperature-sensing element, a switching method is used in implementing the indirect measurement procedure [46]. When the heating and sensing elements are separate, no switching is involved. Thermal test chips can be designed in which the

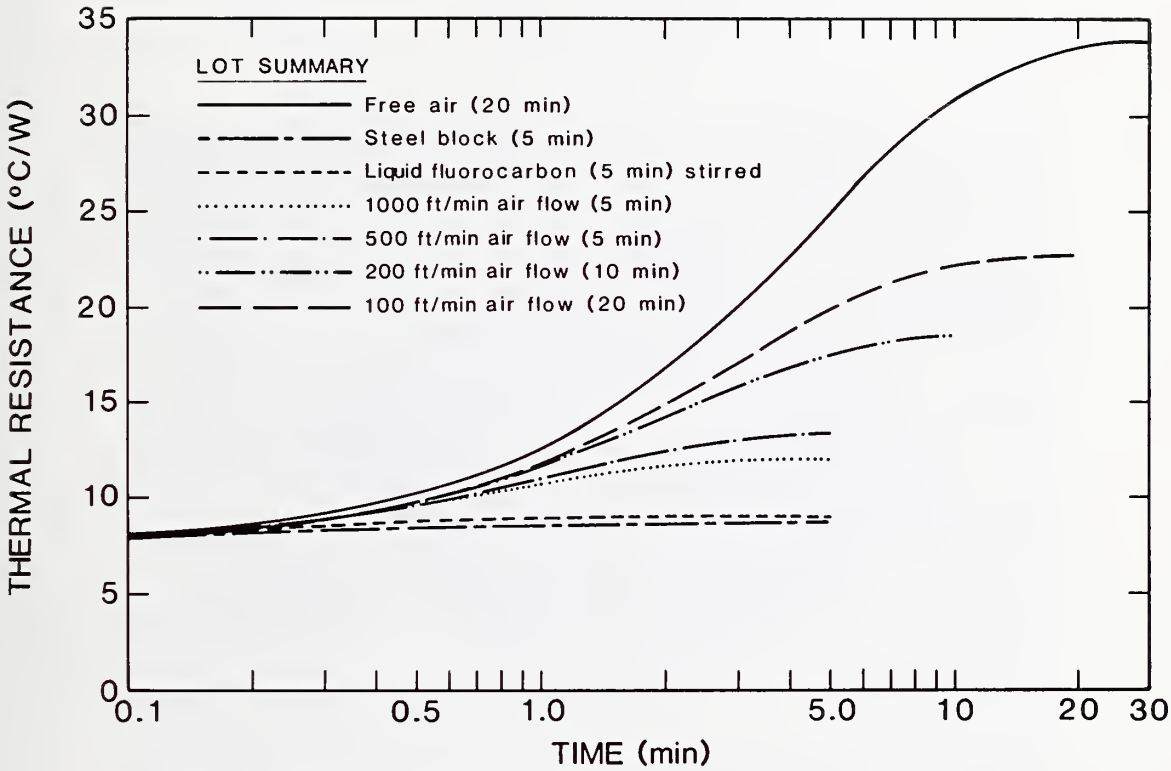


Figure 31. Thermal response measurements for an alumina chip carrier package with an integral aluminum heat sink for various mounting and cooling configurations.

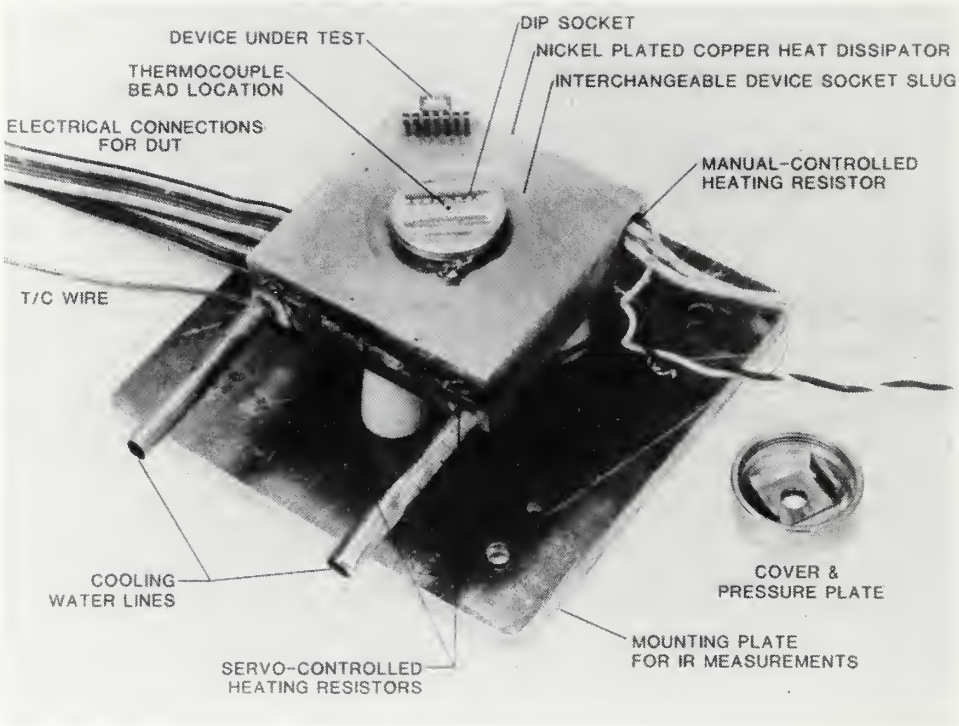


Figure 32. Example of a temperature-controlled heat sink.

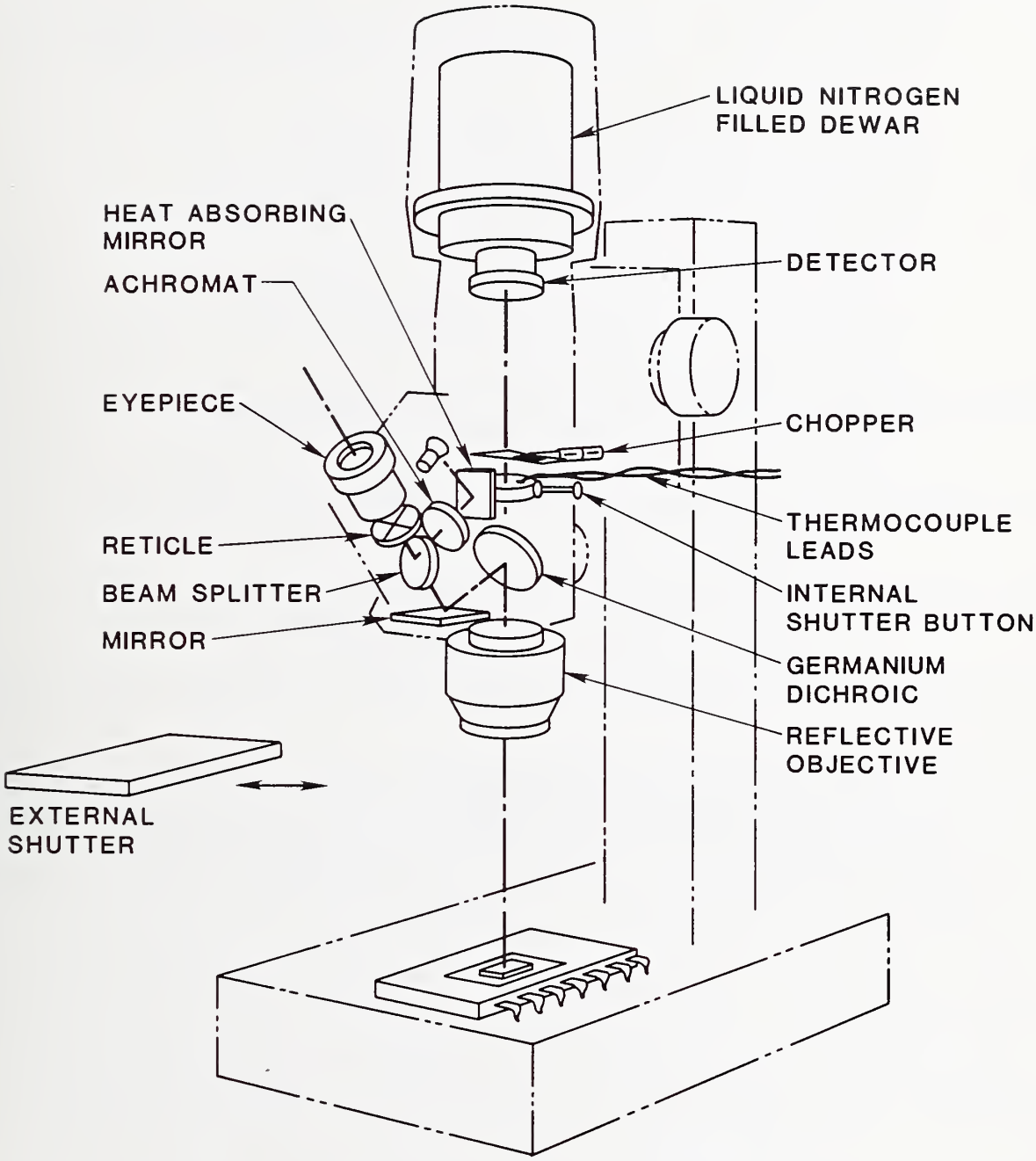


Figure 33. Example of an infrared microradiometer. (After Baxter et al., Ref. [44])

TABLE 10

Precision and Accuracy of Infrared Measurements

Hardware-Dependent Factors

- Mechanical instabilities
- Changes in chopper temperature
- Optical defocusing due to temperature changes
- Specimen ambient temperature fluctuations

Calibration Considerations

- Variations in specimen emissivity
- Variations in specimen transmission
- Poor constant emissive coatings
- Point-by-point calibrations for thermal mapping

sensing element is either separate from or incorporated in the heating element. Also, if the heating element is a transistor, care should be taken to avoid operating conditions where current crowding occurs [2,52]. To calculate the packaged device surface/junction-to-case thermal resistance, the following equation is used:

$$R_{\theta JC} = \frac{(T_J - T_C)}{P(Avg)} = \frac{(V_{MH} - V_{MC})}{P_H} \left(\left. \frac{\Delta V_{MC}}{\Delta T_{MC}} \right|_{I_M} \right)^{-1} \tag{10}$$

where

I_M = measuring/calibration current (mA);

V_{MH} = value of temperature-sensitive parameter (mV), measured at I_M and corresponding to the temperature of the chip surface/junction heated by P_H;

T_{MC} = calibration temperature (°C), measured at the reference point on the device case;

V_{MC} = value of the temperature-sensitive parameter (mV), measured at I_M and a specific value of T_{MC}; and

$\Delta V_{MC}/\Delta T_{MC}$ = temperature coefficient of the temperature-sensitive parameter (mV/°C), measured at I_M.

Equation (10) is used to calculate thermal resistance for both switched and nonswitched chip designs. The general procedure for implementing the measurement can be summarized as follows [46,53]. The temperature coefficient of the temperature-sensitive parameter is obtained by externally heating the device in an oven or on a temperature-controlled heat sink. The temperature-sensitive parameter is measured as a function of the reference point temperature at a specified constant measuring current. The reference point temperature range used during this calibration procedure should include the temperature range encountered when internal heating power is applied to the device. The measuring current is generally chosen such that the temperature-sensitive parameter decreases linearly with increasing temperature over the range of interest and that negligible internal heating occurs. The value of the temperature coefficient of the temperature-sensitive parameter is then calculated from the calibration curve, V_{MC} versus T_{MC}.

When internal heating power is applied to the device, the reference point temperature is held constant at a preset value. First, V_{MC} is measured with the same measuring current used during calibration. Then the device is operated with steady-state heating power applied. V_{MH} is then measured, with the same measuring current used during calibration. $R_{\theta JC}$ can then be calculated using eq (10).

Details for implementing the indirect techniques for measuring thermal resistance can be found in the literature [12,29,46,53] and are not discussed here. Some general comments

are in order, however. In implementing this type of measurement procedure, the following concerns should be addressed:

1. Long-term, single-operator, repeatability measurements of junction-to-case thermal resistance of power transistors, mounted on a temperature-controlled heat sink, had a standard deviation of the resulting junction-to-case temperature difference of approximately 0.5 °C [12]. It is for this reason that a chip surface/junction-to-reference-point temperature difference of at least 20 °C is desirable. However, a potential difficulty with producing a large temperature difference is that there is a tendency to exceed the power dissipation design rating of the integrated circuit or thermal test chip being measured. Although the device may not be destroyed or degraded, what sometimes occurs is that the IR drop in the leads and contacts becomes significant, which can lead to an overestimate of the power dissipation in the active area of the device.

2. The temperature at a specific location on the case of the device being thermally characterized is held constant at a preset value when internal heating power is applied. Because the temperature of the device package is not uniform, it is important to be able to measure at all times the temperature at the same location on the package. While the device is dissipating internal power, the temperature gradient along the package surface which is in contact with a temperature-controlled heat sink is a function of the package material thermal conductivity. For example, for a TO-3 encased power transistor at 60 W of power dissipation, a copper case can have a temperature difference from an extreme edge of the bottom to a point on the bottom directly beneath the chip (a distance of about 2 cm) of about 2 °C; an aluminum package, a difference of about 3 °C; and a kovar or steel package, a temperature difference of about 6 °C [22]. Because most integrated circuit packages are made with materials which have a thermal conductivity that is lower than kovar, it is very important to measure the temperature each time at the same location on the case.

IC Thermal Standardization Activities

Standardized measurement techniques to thermally characterize integrated circuits have been of interest to the semiconductor industry and its customers for many years [29]. However, these techniques come from the body of work that was specifically directed towards conduction-cooled power transistors. Little work had been focused specifically on still- and forced-air convective cooling of integrated circuits. Until recently, the impetus for standardized measurement techniques in this area came from the requirement for MIL-SPEC parts [28,46], and the focus has generally been on ceramic packages that were conduction-cooled. Recently, the computer industry has taken a more active role in efforts to provide standardized techniques for the thermal characterization of integrated circuits. The computer industry is generally concerned with plastic-encapsulated and ceramic-packaged devices that are, for the most part, convection cooled. Thus, the present concern in some quarters is for standardization of package-mounting arrangements and wind tunnels [43,54-56].

Presently active in the improvement and standardization of thermal characterization tech-

TABLE 11

IC Thermal Test Method and Specification Standardization

1. "Accepted Practices for Making Microelectronic Device Thermal Characteristics Test – A User's Guide," JEDEC Engrg. Bull. No. 20, Electronic Industries Assoc., Washington, DC.
2. "Thermal Characteristics," Method 1012.1, MIL-STD-883C Test Methods and Procedures for Microelectronics, Dept. of Defense, Washington, DC.
3. "Unencapsulated Thermal Test Chip," SEMI G32-86 Guideline, 1989 Book of SEMI Standards, Vol. 4, Packaging Div., SEMI, Inc., Mountain View, CA.
4. "Junction-to-Case Thermal Resistance Measurements of Molded-Plastic Packages," SEMI G43-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Div., SEMI, Inc., Mountain View, CA.
5. "Still- and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of IC Packages," SEMI G38-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Div., SEMI, Inc., Mountain View, CA.
6. "Junction-to-Case Thermal Resistance Measurements of Ceramic Packages," SEMI G30-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Div., SEMI, Inc., Mountain View, CA.
7. "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance Measurements of Semiconductor Packages," SEMI G42-88 Specification, 1989 Book of SEMI Standards, Vol. 4, Packaging Div., SEMI, Inc., Mountain View, CA.
8. "Thermal Transient Testing for Die Attachment Evaluation of Integrated Circuits," SEMI G46-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Div., SEMI, Inc., Mountain View, CA.

niques for integrated circuit chips and packages are the Electronic Industries Association's JEDEC JC-13.2 Committee on Government Liaison for Microelectronic Devices, the Department of Defense through the Defense Electronics Supply Center, and the Semiconductor Equipment and Materials International's (SEMI) Ceramic and Plastic Packages Standards Committees (see table 11 for details). Technical expertise and a willingness to actively participate in the development of standards are always welcomed by the various groups involved in these efforts.

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This Special Publication reviews the thermal properties of power transistors and integrated circuits and discusses methods for characterizing these properties. The discrete devices discussed include bipolar transistors and metal-oxide-semiconductor field-effect-transistors. Measurement problems common to these devices, such as deciding the reason for requiring a particular measurement, adequate reference temperature control, selection of a temperature-sensitive electrical parameter, and separation of electrical and thermal effects during measurement are addressed. Due to the inherent difficulties in measuring and analyzing the thermal properties of active integrated circuits, an approach using specifically designed thermal test chips for evaluation of new die-attachment and packaging schemes is finding wide acceptance in the industry. In this Special Publication, indirect (i.e., electrical) measurements, direct (e.g., infrared) measurements, and computer simulation techniques for thermally characterizing integrated circuits are discussed in terms of their usefulness in characterizing VLSI packages.

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