cannot guarantee that we will be able to do so.

Sheleen Dumas,

Department PRA Clearance Officer, Office of the Chief Information Officer, Commerce Department.

[FR Doc. 2022–22190 Filed 10–12–22; 8:45 am]

BILLING CODE 3510–07–P

DEPARTMENT OF COMMERCE

International Trade Administration

[A–570–954]

Certain Magnesia Carbon Bricks From the People's Republic of China: Final Results of Antidumping Duty Administrative Review; 2020–2021

AGENCY: Enforcement and Compliance, International Trade Administration, Department of Commerce.

SUMMARY: The U.S. Department of Commerce (Commerce) continues to determine that the 30 companies subject to this administrative review of the antidumping duty (AD) order on certain magnesia carbon bricks from the People's Republic of China (China) are part of the China-wide entity because they did not demonstrate eligibility for separate rates. The period of review (POR) is September 1, 2020, through August 31, 2021.

DATES: Applicable October 13, 2022.

FOR FURTHER INFORMATION CONTACT: Nathan James, AD/CVD Operations, Office V, Enforcement and Compliance, International Trade Administration, U.S. Department of Commerce, 1401 Constitution Avenue NW, Washington, DC 20230; telephone: (202) 482–5305.

SUPPLEMENTARY INFORMATION:

Background

On June 9, 2022, Commerce published the preliminary results of this administrative review.[1] We invited parties to comment on the *Preliminary Results.* No party submitted comments. Accordingly, the final results remain unchanged from the *Preliminary Results.*

Scope of the Order [2]

The scope of the *Order* covers magnesia carbon bricks from China. For a complete description of the scope of the *Order, see* the *Preliminary Results.*

Final Results of Administrative Review

We received no comments, and made no changes to the *Preliminary Results.* We continue to find that the 30 companies subject to this review did not file a no-shipment certification, a separate rate application, or a separate rate certificate. Thus, Commerce continues to determine that these companies have not demonstrated their eligibility for separate rate status. In this administrative review, no party requested a review of the China-wide entity, and Commerce did not self-initiate a review of the China-wide entity. Because no review of the China-wide entity is being conducted, the China-wide entity rate is not subject to change as a result of this review. The rate previously established for the China-wide entity is 236.00 percent.[3]

Assessment Rates

Commerce will determine, and U.S. Customs and Border Protection (CBP) shall assess, antidumping duties on all appropriate entries covered by this review in accordance with section 751(a)(2)(C) of the Tariff Act of 1930, as amended (the Act). For the 30 companies subject to this review, we will instruct CBP to apply the China-wide rate of 236.00 percent to all entries of subject merchandise during the POR. Commerce intends to issue assessment instructions to CBP no earlier than 35 days after the date of publication of the final results of this review in the **Federal Register**. If a timely summons is filed at the U.S. Court of International Trade, the assessment instructions will direct CBP not to liquidate relevant entries until the time for parties to file a request for a statutory injunction has expired (*i.e.,* within 90 days of publication).

Cash Deposit Requirements

The following cash deposit requirements will be effective upon publication of the final results of this administrative review for shipments of subject merchandise from China entered, or withdrawn from warehouse, for consumption on or after the publication date of this notice, as provided by section 751(a)(2)(C) of the Act: (1) for previously investigated or reviewed Chinese and non-Chinese exporters that received a separate rate in a prior segment of this proceeding, and which were not assigned the China-wide rate in this review, the cash deposit rate will continue to be the existing exporter-specific rate published for the most recently completed segment of this proceeding; (2) for all Chinese exporters of subject merchandise that have not been found to be entitled to a separate rate, the cash deposit rate will be the China-wide rate of 236.00 percent; and (3) for all non-Chinese exporters of subject merchandise which have not received their own rate, the cash deposit rate will be the rate applicable to the Chinese exporter that supplied that non-Chinese exporter. These deposit requirements, when imposed, shall remain in effect until further notice.

Notification to Importers

This notice also serves as a final reminder to importers of their responsibility under 19 CFR 351.402(f)(2) to file a certificate regarding the reimbursement of antidumping duties prior to liquidation of the relevant entries during this POR. Failure to comply with this requirement could result in Commerce's presumption that reimbursement of antidumping duties occurred and the subsequent assessment of double antidumping duties.

Administrative Protective Orders

This notice also serves as the only reminder to parties subject to administrative protective order (APO) of their responsibility concerning the return or destruction of proprietary information disclosed under APO in accordance with 19 CFR 351.305(a)(3). Timely written notification of the return or destruction of APO materials or conversion to judicial protective order is hereby requested. Failure to comply with the regulations and terms of an APO is a violation subject to sanction.

Notification to Interested Parties

We are issuing and publishing these final results in accordance with sections 751(a)(1) and 777(i) of the Act, and 19 CFR 351.213(h) and 351.221(b)(5).

Dated: October 5, 2022.

Lisa W. Wang,

Assistant Secretary for Enforcement and Compliance.

[FR Doc. 2022–22273 Filed 10–12–22; 8:45 am]

BILLING CODE 3510–DS–P

DEPARTMENT OF COMMERCE

National Institute of Standards and Technology

[Docket Number: 221004–0210]

Manufacturing USA Semiconductor Institutes

AGENCY: National Institute of Standards and Technology, Department of Commerce.

[1] *See Certain Magnesia Carbon Bricks from the People's Republic of China: Preliminary Results of Antidumping Duty Administrative Review; 2020–2021,* 87 FR 35161 (June 9, 2022) (*Preliminary Results*).

[2] *See Certain Magnesia Carbon Bricks from Mexico and the People's Republic of China: Antidumping Duty Orders,* 75 FR 57257 (September 20, 2010) (*Order*).

[3] *Id.*

ACTION: Notice; request for information.

SUMMARY: The National Institute of Standards and Technology (NIST) is seeking public input to inform the design of, and requirements for, potential Manufacturing USA institutes to strengthen the semiconductor and microelectronics innovation ecosystem, which could include design, fabrication, advanced test, assembly, and packaging capability. These Manufacturing USA institutes are envisioned in Title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America) to support efforts in research and development as well as education and workforce development, and that Act also provides for complementary initiatives including the National Semiconductor Technology Center, the National Advanced Packaging Manufacturing Program, and the NIST laboratories program supporting measurement science and standards. Responses to this Request for Information (RFI) will inform NIST's development of funding opportunities for federal assistance to establish Manufacturing USA semiconductor institutes.

DATES: Comments must be received by 11:59 p.m. Eastern time November 28, 2022. Written comments in response to the RFI should be submitted according to the instructions in the **ADDRESSES** and **SUPPLEMENTARY INFORMATION** sections below. Submissions received after that date may not be considered.

ADDRESSES:

For Comments

Comments may be submitted by either of the following methods:

- *Electronic submission:* Submit electronic public comments via the Federal eRulemaking Portal.

1. Go to *www.regulations.gov* and enter NIST–2022–0002 in the search field,
2. Click the ''Comment Now!'' icon, complete the required fields, and
3. Enter or attach your comments.

- *Email:* Comments in electronic form may also be sent to *MfgRFI@nist.gov* in any of the following formats: HTML; ASCII; Word; RTF; or PDF.

Please submit comments only and include your name, organization's name (if any), and cite ''Manufacturing USA semiconductor institutes'' in all correspondence. Comments containing references, studies, research, and other empirical data that are not widely published should include copies of the referenced materials.

All comments responding to this document will be a matter of public record. Relevant comments will generally be available on the Federal eRulemaking Portal at *http://www.Regulations.gov* and on NIST's website at *https://www.nist.gov/oam/manufacturing-usa-semiconductor-institute-request-information-rfi.* NIST will not accept comments accompanied by a request that part or all of the material be treated confidentially because of its business proprietary nature or for any other reason. Therefore, do not submit confidential business information or otherwise sensitive, protected, or personal information, such as account numbers, Social Security numbers, or names of other individuals.

For RFI Informational Webinars

NIST will hold informational webinars explaining how the public can submit comments. Details about these informational webinars, including dates and registration deadlines, will be announced at *https://www.nist.gov/oam/manufacturing-usa-semiconductor-institute-request-information-rfi.*

FOR FURTHER INFORMATION CONTACT: For questions about this RFI contact: Kelley Rogers in the Office of Advanced Manufacturing, National Institute of Standards and Technology, telephone number 301–219–8543 or email *MfgRFI@nist.gov.* Please direct media inquiries to NIST's Office of Public Affairs at (301) 975–2762.

SUPPLEMENTARY INFORMATION:

Background

Semiconductors are fundamental to nearly all modern industrial and national security activities, and they are essential building blocks of critical and emerging technologies, such as artificial intelligence, autonomous systems, next generation communications, and quantum computing.

The U.S. semiconductor industry has historically led in many parts of the semiconductor supply chain, such as research and development (R&D), chip design, and manufacturing. Over the past several years, the U.S. position in the global semiconductor industry has faced numerous challenges. In 2019, the United States accounted for 11 percent of global semiconductor fabrication capacity, down from 13 percent in 2015 and continuing a long-term decline from around 37 percent in 1990. Semiconductor packaging also presents a critical supply chain challenge since less than 3% of global packaging capacity is in North America.[1] Much of the overseas semiconductor manufacturing capacity is in Taiwan, South Korea, and, increasingly, China.[2]

The fragility of the current global semiconductor supply chain was put squarely on display in 2020. The industry faced significant disruptions as a result of the coronavirus pandemic, a fire affecting a major supplier in Japan, and a severe winter storm that disabled production in facilities in Texas for several days.[3] These events, together with other factors, such as pandemic-induced shifts in consumer demand, contributed to a global semiconductor shortage that affected multiple manufacturing sectors that rely on semiconductors as critical components for their finished products. Especially severely hit was the automotive industry, which saw plants idled for months.[4]

The Department of Commerce published a Request for Information (or ''RFI'') in September of 2021 on the semiconductor supply chain (86 FR 53031, September 24, 2021). More than 150 responses were received from commenters including nearly every major semiconductor producer and representative companies that consume these products across multiple industry sectors. These responses provided new insight into the complex and global semiconductor supply chain.[5] Respondents pointed out a major supply and demand gap that is increasing annually, with very limited inventory on hand for key industries.

To strengthen the U.S. position in semiconductor R&D and manufacturing, Congress authorized a set of programs in Title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021, Public Law 116–283, as amended by sections 103 and 105 of the CHIPS Act of 2022 (Pub. L. 117–167, Division A), codified at 15 U.S.C. 4651 *et seq.* (hereinafter, CHIPS for America Act). This comprehensive set of programs is intended to restore U.S. leadership in semiconductor manufacturing by providing incentives and encouraging investment to expand manufacturing capacity for the most advanced

[1] *https://semiengineering.com/expanding-advanced-packaging-production-in-the-u-s/.*

[2] *https://www.semiconductors.org/wp-content/uploads/2020/09/Government-Incentives-and-US-Competitiveness-in-Semiconductor-Manufacturing-Sep-2020.pdf.*

[3] *https://www.ept.ca/features/global-chip-shortage-a-timeline-of-unfortunate-events/.*

[4] *https://hbr.org/2021/02/why-were-in-the-midst-of-a-global-semiconductor-shortage.*

[5] *https://www.commerce.gov/news/blog/2022/01/results-semiconductor-supply-chain-request-information.*

semiconductor designs as well as those of more mature designs that are still in high demand, and would grow the research and innovation ecosystem for semiconductor and microelectronics R&D in the United States, including the investments in the infrastructure necessary to better integrate advances in research into semiconductor manufacturing.

President Biden's American Jobs Plan [6] calls for at least $50 billion to fund this set of programs. As funded by section 102 of the CHIPS Act of 2022:

- $39 billion is available for a program to incentivize investment in facilities and equipment in the United States for the fabrication, assembly, testing, advanced packaging, production, or research and development of semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment;
- $11 billion is available to support several R&D and infrastructure investments including the establishment of a National Semiconductor Technology Center, investments in advanced packaging, the creation of up to three Manufacturing USA institutes targeting semiconductors, and expansion of NIST's metrology R&D in support of semiconductor and microelectronics R&D.

Under Section 9906(f) of the CHIPS for America Act, the Director of NIST may establish up to three Manufacturing USA Institutes described in section 34(d) of the NIST Act (15 U.S.C. 278s(d)) that are focused on semiconductor manufacturing. In addition, the Secretary of Commerce may award financial assistance to any Manufacturing USA institute for work relating to semiconductor manufacturing. Such institutes may emphasize the following:

(1) Research to support the virtualization and automation of maintenance of semiconductor machinery.

(2) Development of new advanced test, assembly and packaging capabilities.

(3) Developing and deploying educational and skills training curricula needed to support the industry sector and ensure the United States can build and maintain a trusted and predictable talent pipeline.

Request for Information

This RFI outlines the information NIST is seeking from the public to inform the development of up to three Manufacturing USA semiconductor institutes that will strengthen leadership and national resilience of the U.S. semiconductor and microelectronics industry and other industries that rely on microelectronics, through research and development of manufacturing technology, and enhanced education and workforce development.

The following questions cover the major areas about which NIST seeks comment. They are not intended to limit the topics that may be addressed. Responses may include any topic believed to have implications for the development of Manufacturing USA semiconductor institutes, regardless of whether the topic is included in this document. Any one of the topics listed below, on its own, in combination with other topics listed, or in combination with other topics not contained in this notice, could be the basis of a Manufacturing USA semiconductor institute.

When addressing the topics below, commenters may address the practices of their organization or a group of organizations with which they are familiar. If desired, commenters may provide information about the type, size, and location of the organization(s). Provision of such information is optional and will not affect NIST's consideration.

NIST is seeking comments on the following questions, and encourages responses from the public, including key stakeholders in the semiconductor and microelectronics ecosystem, for the purpose of informing the design of a funding opportunity for Manufacturing USA semiconductor institutes:

Institute Scope

1. The Manufacturing USA semiconductor institute program is one component of an $11 billion R&D effort that includes the National Advanced Packaging Manufacturing Program, the National Semiconductor Technology Research Center and the NIST laboratories. The entire R&D program is intended to be interconnected and comprehensive, with no gaps and minimal redundancy, to position the United States for technology and workforce leadership in the semiconductor and microelectronics sector for the long-term prosperity of the nation. Additionally, the Manufacturing USA authorizing statute specifies that new institutes must not substantially duplicate the technology focus of any other Manufacturing USA institute. From your perspective, what role do you envision for new Manufacturing USA semiconductor institutes that will best complement the other R&D investments and remain consistent with the programmatic purposes of Manufacturing USA? Since the Secretary of Commerce may award financial assistance to any existing Manufacturing USA institutes for work relating to semiconductor manufacturing, what role do you envision for existing, federally-sponsored Manufacturing USA institutes with respect to semiconductor manufacturing?

2. The technological breadth of innovation in semiconductors and microelectronics is likely larger than can be served by any single Manufacturing USA institute. Therefore, each Manufacturing USA semiconductor institute should have an appropriate scope to ensure that each institute is impactful and does not duplicate efforts of other programs. Historically, institutes in the current network of existing Manufacturing USA institutes have generally been funded for an initial 5 years at $150 million to $600 million, including federal funding and cost-sharing (co-investment) from non-federal partners. What would be the ideal scope and corresponding financial investment from federal and non-federal partners, for a Manufacturing USA semiconductor institute to achieve the needed impact on competitiveness?

3. Potential technology areas of focus that could be addressed by the Manufacturing USA semiconductor institutes to complement the National Advanced Packaging Manufacturing Program and the National Semiconductor Technology Research Center in Question 1 are listed below. What are your thoughts on the appropriateness of each for the scope of work for a Manufacturing USA semiconductor institute? What other topics should be included in the scope of an institute?

- *Chip-package architectures and co-design* of integrated circuits and advanced packaging. May include artificial intelligence, security, test methodologies, etc.
- *Technologies to increase the microelectronics manufacturing productivity* of American workers, lower costs and offset the drastic shortfall of skilled workers.
- *Assembly and Test metrologies* to develop new analytical equipment and analysis capabilities based upon standards.
- *Coding and system software* with novel computing paradigms and architectures, including chiplet compatibility with earlier generations.

[6] *https://www.whitehouse.gov/briefing-room/statements-releases/2021/03/31/fact-sheet-the-american-jobs-plan/.*

• *Integration of security into packaging,* interposers and/or substrates.
• *High Density Interposers and substrates,* incorporating new materials and designs.
• *Chiplet-enabled trusted packaging* facilities that obviate the need for trusted foundries.
• *New materials,* such as glass for substrates, or compound semiconductors.
• *Environmental Sustainability* for semiconductor manufacturing.
• *Analog and Gigahertz Technology* materials and metrology, enabling beyond 5G, the Industrial Internet of Things and Industry 4.0.
• *Performance and Process Modeling and Metrology*

4. What criteria should be used to select technology focus areas in delineating the scope for a Manufacturing USA institute focused on semiconductor manufacturing?

5. What technology focus areas that meet the criteria suggested in Question 4 above would you be willing to co-invest in?

Institute Structure and Governance

6. Existing Manufacturing USA institutes were launched and operate in alignment with the design principles published in 2012 as the *National Network for Manufacturing Innovation: A Preliminary Design* (*https://www.manufacturingusa.com/reports/national-network-manufacturing-innovation-preliminary-design*). Are there any unique considerations for the semiconductor and microelectronics sector that may require modifications to the conventional design for any Manufacturing USA semiconductor institutes under consideration?

7. Semiconductor R&D and manufacturing cover substantial technical breadth. What business models or best practices should be employed by a Manufacturing USA semiconductor institute to support U.S. leadership and effectively manage emerging technologies to support commercialization? What advantages or disadvantages would there be to one ''super-sized'' Manufacturing USA semiconductor institute that would cover the technology sector broadly? Since Congress authorized the NIST Director to establish up to three institutes, what advantages or disadvantages would there be for multiple Manufacturing USA semiconductor institutes each with a smaller scope focused on a specific technology area? How would one Manufacturing USA semiconductor institute or multiple institutes structure relationships with other significant partners to spur collaborative work?

8. What membership and participation structure for a Manufacturing USA semiconductor institute would be most effective for ensuring participation by industry, academia, and other critical stakeholders, particularly with respect to financial and intellectual property obligations, access, and licensing? Based on your knowledge of current Manufacturing USA institute practices, are the needs of potential semiconductor institutes different than for other institutes?

Strategies for Driving Co-Investment and Engagement

9. The authorizing statute for Manufacturing USA requires at least an equal non-federal co-investment in Manufacturing USA institutes to match the federal investment. From your perspective, what are the most significant considerations to garner support for the required co-investment for a Manufacturing USA semiconductor institute? What is the anticipated impact of the new Investment Tax Credit (ITC) for industry established in the CHIPS Act on the level of investment in the new Manufacturing USA semiconductor institute(s), in facilities, including for manufacturing equipment and construction? How might a Manufacturing USA semiconductor institute be set up to best leverage the Investment Tax Credit?

10. For the required non-federal co-investment for a Manufacturing USA semiconductor institute, with respect to the different types of co-investment (*e.g.,* cash, equipment donations, facilities access, etc.), are there factors unique to the semiconductor industry that would impact how the co-investment could be structured to best support the institute?

11. What arrangements for co-investment proportions and types could help a Manufacturing USA semiconductor institute sustain operations in the absence of continued federal support?

12. A Manufacturing USA semiconductor institute should support domestic competitiveness. How should relationships with foreign entities be structured or constrained to support domestic manufacturing priorities while maximizing the opportunities to leverage international expertise and resources? In what circumstances should the Manufacturing USA Semiconductor institutes and NIST as the federal sponsor, consider membership requests from foreign-owned businesses?

13. How should a new Manufacturing USA semiconductor institute engage other existing Manufacturing USA institutes (*https://www.manufacturingusa.com/institutes*), including those awarded funds for work related to semiconductor manufacturing, and other manufacturing related programs and networks such as the Manufacturing Extension Partnership (*https://www.nist.gov/mep*) and the U.S. Department of Energy's Next Generation Power Electronics National Manufacturing Innovation Institute (''Power America'')?

14. How should a Manufacturing USA semiconductor institute interact with State and local economic development entities?

15. How should a Manufacturing USA semiconductor institute coordinate with and inform standards development bodies on the need to modify existing or develop new standards as a result of this initiative?

Education and Workforce Development

16. How could a Manufacturing USA semiconductor institute best support advanced manufacturing workforce development and/or awareness at all educational levels (*e.g.,* for K–12 through post-graduate students)?

17. How could a Manufacturing USA semiconductor institute best engage and leverage the diversity of educational and vocational training organizations (*e.g.,* universities, community colleges, trade schools, etc.)?

18. How could a Manufacturing USA semiconductor institute best ensure that advanced manufacturing workforce development activities address the industry's priorities?

19. How could a Manufacturing USA semiconductor institute best leverage and complement existing education and workforce development programs?

20. What measures could assess Manufacturing USA semiconductor institute performance and impact on education and workforce development?

21. How might a Manufacturing USA semiconductor institute integrate research and development activities and education to best prepare the current and future workforce?

22. How could a Manufacturing USA semiconductor institute help build a steady pipeline of skilled workers? What knowledge, skills and abilities will future workers need, and are there workers with those skills currently employed in other sectors?

23. How could a Manufacturing USA semiconductor institute broaden the talent base (*i.e.,* embrace diversity, equity, inclusion, and accessibility; reach women and minority

communities, engage non-traditional workers, engage separating service members, veterans, and families) to modernize the workforce?

24. What type of education and workforce development activities should a Manufacturing USA semiconductor institute support (*e.g.,* curricula, online education, hybrid, entrepreneurship opportunities, credentialing, regional development, train the trainers, internships/apprenticeship, learning labs, etc.) and why?

Metrics and Success

25. What metrics could be used to best evaluate the performance of a Manufacturing USA semiconductor institute in accelerating innovation, and any associated impacts on economic competitiveness and national security? Are there sector-specific metrics for an institute in the semiconductor technology space?

26. What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute on education and workforce development in support of U.S. competitiveness?

27. What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute in establishing and expanding the U.S. semiconductor manufacturing ecosystem?

28. What constitutes a successful first year for a Manufacturing USA semiconductor institute? What forms of support, and from which partners, are needed to ensure a successful first year?

Alicia Chambers,

NIST Executive Secretariat.

[FR Doc. 2022–22221 Filed 10–12–22; 8:45 am]

BILLING CODE 3510–13–P

DEPARTMENT OF DEFENSE

Office of the Secretary

Defense Business Board; Notice of Federal Advisory Committee Meeting

AGENCY: Office of the Deputy Secretary of Defense, Department of Defense (DoD).

ACTION: Notice of Federal Advisory Committee meeting.

SUMMARY: The DoD is publishing this notice to announce that the following Federal Advisory Committee meeting of the Defense Business Board (''the Board'') will take place.

DATES: Closed to the public Wednesday, November 9, 2022 from 9:00 a.m. to 11:00 a.m., 3:00 p.m. to 4:10 p.m., and from 6:00 p.m. to 7:30 p.m. Open to the public Thursday, November 10, 2022 from 8:30 a.m. to 12:35 p.m. All Eastern time.

ADDRESSES: The open and closed portions of the meeting will be in the Pentagon Library Conference Center Room M1 and 4D880 in the Pentagon, Washington DC. The open public portions of the meeting will be conducted by teleconference only. To participate in the open public portion of the meeting, see the Meeting Accessibility section for instructions.

FOR FURTHER INFORMATION CONTACT: Ms. Jennifer Hill, Designated Federal Officer (DFO) of the Board in writing at Defense Business Board, 1155 Defense Pentagon, Room 5B1088A, Washington, DC 20301–1155; or by email at *jennifer.s.hill4.civ@mail.mil;* or by phone at 571–342–0070.

SUPPLEMENTARY INFORMATION: This meeting is being held under the provisions of the Federal Advisory Committee Act (FACA) (5 U.S.C., app.), the Government in the Sunshine Act (5 U.S.C. 552b), and 41 CFR 102–3.140 and 102–3.150.

Purpose of the Meeting: The mission of the Board is to examine and advise the Secretary of Defense on overall DoD management and governance. The Board provides independent, strategic-level, private sector and academic advice and counsel on enterprise-wide business management approaches and best practices for business operations and achieving National Defense goals.

Agenda: The Board will begin in closed session on November 9, 2022 from 9:00 a.m. to 11:00 a.m. with opening remarks by Ms. Jennifer Hill, the DFO and the Board's Chair, Hon. Deborah James. The Board will receive a classified brief on the resiliency of the Defense Industrial Base from Hon. Kathleen Hicks, Deputy Secretary of Defense, followed by a classified update on DoD events by Secretary of Defense, Hon. Lloyd J. Austin III. The DFO will then adjourn the closed session. The Board will reconvene in closed session on November 9, 2022 at 3:00 p.m. Ms. Jennifer Hill, the DFO will open the closed session. Next, the Board will receive a classified briefing on streamlining DoD intelligence processes by Hon. Ronald S. Moultrie, Under Secretary of Defense for Intelligence & Security. Hon. Deborah James, the Board's Chair will provide remarks and the DFO will adjourn the closed session. The Board will also meet in closed session November 9, 2022 from 6:00 p.m. to 7:30 p.m. The DFO will open the closed session followed by the Chair's welcome. The Board will receive a classified brief by Hon. Heidi Shyu, Under Secretary of Defense for Research and Engineering on how the Department is preparing for future conflicts. The DFO will adjourn the closed session. The Board will begin in open session on November 10, 2022 at 8:30 a.m. with opening remarks by the DFO and Chair's welcome to members and guests by Hon. Deborah James. Next, will be a presentation, deliberation, and vote on the Defense Business Board ''Recommendations to Improve Department of Defense Business Health Metrics'' study led by Ms. Erin Hill, Chair, Business Transformation Advisory Subcommittee. The Board will then receive a follow up brief on the dissolution of the Office of the Chief Management Officer and current business improvement efforts by Hon. Michael B. Donley, Director, Administration and Management. Hon. Gilbert Cisneros, Under Secretary of Defense for Personnel and Readiness, will provide an update on DoD Civilian Training. Closing remarks by the Chair, Hon. Deborah James and the DFO will adjourn the open session. The latest version of the agenda will be available on the Board's website at: *https://dbb.defense.gov/Meetings/Meeting-November-2022/.*

Meeting Accessibility: In accordance with Section 10(d) of the FACA and 41 CFR 102–3.155, it is hereby determined that portions of the November 9–10, 2022 meeting of the Board will include classified information and other matters covered by 5 U.S.C. 552b(c)(1) and that, accordingly, the meeting will be closed to the public on November 9, 2022 from 9:00 a.m. to 11:00 a.m., from 3:00 p.m. to 4:10 p.m., and from 6:00 p.m. to 7:30 p.m. This determination is based on the consideration that it is expected that discussions throughout these periods will involve classified matters of national security. Such classified material is so intertwined with the unclassified material that it cannot reasonably be segregated into separate discussions without defeating the effectiveness and meaning of these portions of the meeting. To permit these portions of the meeting to be open to the public would preclude discussion of such matters and would greatly diminish the ultimate utility of the Board's findings and recommendations to the Secretary of Defense and to the Deputy Secretary of Defense. Pursuant to section 10(a)(1) of the FACA and 41 CFR 102–3.140, the portion of the meeting on November 10, 2022 from 8:30 a.m. to 12:35 p.m. is open to the public. Persons desiring to attend the