ENSURING AMERICAN LEADERSHIP IN MICROELECTRONICS

HEARING

BEFORE THE

COMMITTEE ON SCIENCE, SPACE, AND TECHNOLOGY

OF THE

HOUSE OF REPRESENTATIVES

ONE HUNDRED SEVENTEENTH CONGRESS

FIRST SESSION

DECEMBER 2, 2021

Serial No. 117–40

Printed for the use of the Committee on Science, Space, and Technology

Available via the World Wide Web: http://science.house.gov

U.S. GOVERNMENT PUBLISHING OFFICE
46–150PDF WASHINGTON : 2023

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C O N T E N T S

December 2, 2021

ENSURING AMERICAN LEADERSHIP IN MICROELECTRONICS

THURSDAY, DECEMBER 2, 2021

HOUSE OF REPRESENTATIVES,
COMMITTEE ON SCIENCE, SPACE, AND TECHNOLOGY,
Washington, D.C.

The Committee met, pursuant to notice, at 10:03 a.m., via Zoom, Hon. Eddie Bernice Johnson [Chairwoman of the Committee] presiding.

U.S. HOUSE OF REPRESENTATIVES
COMMITTEE ON SCIENCE, SPACE, AND TECHNOLOGY
HEARING CHARTER

Ensuring American Leadership in Microelectronics

Thursday, December 2, 2021
10:00 am – 12:00 pm
Zoom

PURPOSE

On Thursday, December 2, 2021, the Committee on Science, Space, and Technology will hold a hearing to examine the status of U.S. leadership in advanced semiconductor development and manufacturing; to discuss how new investments and partnership models can support continued U.S. leadership; and to explore the role of the federal government in supporting domestic semiconductor innovation and manufacturing throughout the supply chain.

WITNESSES

- **Dr. Ann Kelleher,** Executive Vice President and General Manager of Technology Development, Intel
- **Mr. Manish Bhatia**, Executive Vice President, Global Operations, Micron Technology, Inc.
- **Dr. Michael Witherell**, Director, Lawrence Berkeley National Laboratory
- **Dr. Mung Chiang**, Executive Vice President and John A. Edwardson Dean, College of Engineering, Purdue University

OVERARCHING QUESTIONS

- What is the state of U.S. leadership in advanced microelectronics R&D and manufacturing in the United States?
- Why is it important for the United States to maintain leading capabilities in both R&D and manufacturing of advanced microelectronics? What are the consequences of a loss of leadership?
- What is the appropriate role of the Federal government in supporting microelectronics research, innovation, and domestic manufacturing? How can the Federal government most effectively partner with the private sector and the research community?
- To what extent does the *CHIPS for America Act* address what is needed to maintain U.S. leadership in microelectronics innovation? Are any updates to CHIPS or additional legislation necessary to ensure a coordinated, transparent and effective Federal partnership with the private sector, universities, and National Labs to advance U.S. microelectronics innovation and manufacturing?

MICROELECTRONICS OVERVIEW

Advanced microelectronics are a primary driver of economic growth and scientific advancement. Microelectronics is a term describing all aspects of the miniaturization of electronic circuits and components, from fundamental research to design to manufacturing. Semiconductors are a subset of microelectronics. Most modern semiconductors are integrated circuits, also called "chips", which are sets of miniaturized electronic circuits composed of active discrete devices (e.g., transistors), passive devices (e.g., capacitors), and their interconnections, all of which are layered on a thin wafer of semiconductor material (e.g., silicon). These chips enable nearly everything in our modern lives —from smartphones and cars to nuclear weaponry.

Semiconductors can be classified into three major product groups based on function:[1]

- Microprocessors and Logic Devices are the integrated circuits functioning on binary codes (0 and 1) that are used for the interchange and manipulation of data in computing.
- Memory Devices are used to store information. This segment includes dynamic random-access memory (DRAM), a common type of memory used to store the data or program code needed by a computer processor to function.
- Discrete, Analog, and Other (DAO) semiconductors transmit, receive, and transform information dealing with continuous parameters, such as temperature. For example, analog devices are used to translate analog signals, such as light, touch, and voice, into digital signals. Discretes, such as transistors and diodes, perform a single electrical function on each chip.

MICROELECTRONICS INNOVATION IN THE UNITED STATES

The United States has a long history of innovation in microelectronics. U.S. government investments in research helped lead to the invention of early computers and transistors in the 1940s, as well as the first integrated circuit in the 1950s.[2] In the 1980s, the rapid rise of Japan's semiconductor industry led the federal government to establish a research consortium to support U.S. competitiveness in semiconductor technology, also known as SEMATECH. From 1988 through 1996, Congress provided approximately $870 million to SEMATECH through the Defense Advanced Research Projects Agency (DARPA), which was generally matched by industry contributions.[3] While the Government Accountability Office found that SEMATECH had a significant impact on U.S. semiconductor manufacturing and R&D performance,[4] the SEMATECH board of directors ultimately declined additional federal funding in 1996 and the consortium was later absorbed into the New York Polytechnic Institute in 2015.

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[1] Antonio Varas et al., "Strengthening the Global Semiconductor Supply Chain in an Uncertain Era," Semiconductor Industry Association, April 2021.
[2] Michaela Platzer et al., "Semiconductors: U.S. Industry, Global Competition, and Federal Policy," Congressional Research Service, October 26, 2020.
[3] Ibid.
[4] "Federal Research: Lessons Learned from SEMATECH," U.S. General Accounting Office, September 28, 1992.

The Federal Government continues to invest in semiconductor research across many different agencies and mission areas. The U.S. semiconductor industry has continued to lead the world in R&D spending, investing nearly one-fifth of its annual revenue in R&D each year.[5] In 2020, the U.S. semiconductor industry investment in R&D totaled $44.0 billion.[6]

"Moore's Law"

The semiconductor industry has a rapid internal product development cycle. This was first described by Gordon Moore, then R&D Manager for Fairchild Semiconductor, in 1965.[7] Moore's law, as his observation later became known, states that the number of transistors that can be cost-effectively included on an integrated circuit will double every 18 months to two years, making chips smaller, faster, and cheaper. This observation held for decades, in part because of the industry's high level of research and investment spending. However, this two-dimensional scaling of the chip is reaching its physical limits as chip complexity has increased due to new applications such as artificial intelligence, 5G, and the internet of things. The industry can no longer rely solely on this process to make the necessary generational improvements that will enable future chip iterations, including breakthroughs in energy efficiency, new materials, are more.[8] Long term grown will require fundamental breakthroughs in microelectronics technology.

THE GLOBAL SEMICONDUCTOR LANDSCAPE

Semiconductor production includes three segments: (1) design, (2) manufacturing/fabrication, and (3) assembly, testing, and packaging (ATP). In some cases, these steps are all performed by a single company, called an integrated device manufacturer (IDM). Major U.S. headquartered IDMs include Texas Instruments, Intel, and Micron. Other semiconductor companies, called fabless firms, only do design in-house. Fabless firms purchase fabrication services from a semiconductor factory and ATP services from an outsourced semiconductor assemble and test company. Semiconductor factories, also referred to as fabs or foundries, are often characterized by the size of the wafer that chips are printed on and the size of the transistor gate length printed on each chip.[9] Only a small number of fabs—none of which reside in the United States—produce the most state-of-the-art semiconductors. Additionally, the semiconductor production process requires several types of inputs, including materials, manufacturing equipment, software, and intellectual property, some of which is produced only outside of the United States.

While the Unites States is the current global leader is semiconductor sales and R&D, the competitive landscape for semiconductor development is shifting. In 2020, the U.S.

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[5] "2021 State of the U.S. Semiconductor Industry," Semiconductor Industry Association, June 2021.
[6] Ibid.
[7] Gordon E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics Magazine,* Vol. 28, No. 8, April 19, 1965, accessed through Georgia Tech.
[8] "The Decadal Plan for Semiconductors" Semiconductor Research Corporation, January 2021.
[9] Platzer et al., "Semiconductors: U.S. Industry, Global Competition, and Federal Policy."

semiconductor industry accounted for 47 percent of global semiconductor sales.[10] Furthermore, the United States leads in many parts of the semiconductor market, including manufacturing equipment and semiconductor design.[11] However, over the last few decades, much of the U.S. manufacturing capacity has been offshored. The U.S. share of global semiconductor manufacturing decreased from 37 percent in 1990 to just 12 percent today.[12] Much of this capacity has moved to Taiwan, South Korea, and Japan, and China.[13] For example, Taiwan accounts for 47 percent of the global capacity to manufacture advanced logic semiconductors, such as those used in smart phones or data centers.[14]

China, which accounts for roughly 25 percent of global consumption of semiconductors (roughly equal to that of the United States), is also heavily investing in domestic semiconductor capacity.[15] China is investing $150 billion with the stated goal of gaining 40 percent of the world's new manufacturing capacity by 2030.[16] While the country remains two to three generations behind in advanced semiconductor manufacturing capacity,[17] China has demonstrated the ability to rapidly close technology gaps.

Supply Chains, Disruptions, and Shortages

Demand for semiconductor output has grown consistently over the last two decades, with the Semiconductor Industry Association (SIA) predicting a 19.7 percent increase in global sales in 2021 and a subsequent 8.8 percent increase in 2022.[18]

From design to final sale, a single chip can progress through more than 1,000 production steps and cross 70 international borders.[19] When businesses started to close due to the COVID-19 pandemic in 2020, there was an abrupt and cascading global shortage of semiconductors. This shortage was primarily caused by significant swings in demand throughout the pandemic. Chip manufactures first slowed production due to lockdowns and a reduction in demand from their customers, who canceled their chip orders assuming a lengthy economic downturn. However,

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[10] "2021 State of the U.S. Semiconductor Industry."
[11] Antonio Varas et al., "Government Incentives and U.S. Competitiveness in Semiconductor Manufacturing," Semiconductor Industry Association, September 2020.
[12] Ibid.
[13] South Korea specializes in all production steps, while Taiwan is dominant in most advanced manufacturing and ATP. Japan specializes in manufacturing equipment. European nations, especially the Netherlands, the United Kingdom, and Germany, specialize in manufacturing equipment, materials, and core IP. Currently, China is the leader in ATP and raw materials.
[14] Varas et al., "Government Incentives and U.S. Competitiveness in Semiconductor Manufacturing."
[15] Varas et al., "Strengthening the Global Semiconductor Supply Chain in an Uncertain Era."
[16] Stephen Ezell, "Moore's Law Under Attack: The Impact of China's Policies on Global Semiconductor Innovation," the Information Technology and Innovation Foundation, February 18, 20201.
[17] Debbie Wu et al., "Why the World Is Short of Computer Chips, and Why It Matters," *Washington Post*, April 21, 2021.
[18] "Global Semiconductor Sales Increase 1.9% Month-to-Month in April; Annual Sales Projected to Increase 19.7% in 2021, 8.8% in 2022," *Semiconductor Industry Association*, press release, June 9, 2021.
[19] Saif Khan, "The Semiconductor Supply Chain Assessing National Competitiveness," the Georgetown Center for Security and Emerging Technologies, January 2021.

chipmakers soon saw surging demand in other sectors as new activities become more commonplace, such as remote healthcare, work-at-home, and virtual learning. When economic forecasts proved wrong, the original customers re-ordered chips, creating a significant backlog.

Several other events spurred the shortage. Stockpiling by certain companies and industries before the pandemic—especially Chinese companies seeking to weather U.S. trade restrictions—further tightened supply. Natural disasters also impacted chip manufacturing. For example, a Renesas plant in Japan, which primarily serves car manufacturers, had its production significantly delayed due to a fire.[20] Finally, truck shortages and global shipping backups have significantly stalled inputs that go into the manufacturing of semiconductors and their delivery to the customer.

The shortage affected many downstream sectors, such as car manufacturing and consumer electronics. For example, a General Motors plant in Kansas City was closed from February to September due to a lack of chips.[21] Notably, many semiconductor firms are no longer manufacturing the types of legacy chips that are used in vehicles and home appliances, instead focusing capacity on cutting-edge designs. This trend has further exacerbated shortages. Some analysts believe that the most problematic chip shortages will begin to ease in the third or fourth quarter of 2021, but it could take through 2022 for shortages to end.[22]

THE CHIPS FOR AMERICA ACT

To re-shore chip manufacturing and to advance U.S. competitiveness in microelectronics, in December 2020 Congress enacted the *Creating Helpful Incentives to Produce Semiconductors for America Act, or the CHIPS for America Act*.[23] The *CHIPS for America Act* establishes a grant program at the Department of Commerce that would incentivize new domestic semiconductor manufacturing facilities and workforce development. It also creates a multilateral semiconductors security fund to support development of measurably secure supply chains, as well as a Department of Commerce study to analyze the capabilities of the U.S. industrial base to support the national defense in the light of significant global supply chain interdependencies.

The law also supports several research and development related activities. First, it establishes an interagency working group, advised by an industrial advisory committee, to develop a national strategy for semiconductor research and development. The Act directs the Department of Commerce to support semiconductor R&D through multiple mechanisms, including a National Semiconductor Technology Center (NSTC) to conduct research and prototyping of advanced

[20] "Japanese carmakers assess impact of fire at Renesas chip plant," Reuters, March 21, 2021.
[21] Carlos Moreno, "Workers Return To GM's Fairfax Plant On Monday, Months After Mass Layoffs," *NPR*, September 20, 2021.
[22] Samuel Moore, "How and When the Chip Shortage Will End, in 4 Charts," IEEE, June 21, 2021.
[23] Creating Helpful Incentives to Produce Semiconductors for America Act (CHIPS for America Act), Title XCIV, The William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021, H.R. 6395, 116th Congress.

chips, a Manufacturing USA Institute for domestic semiconductor manufacturing, and a center on advanced semiconductor packaging. The Act directs the National Institute of Standards and Technology (NIST) specifically to conduct metrology research to accelerate the development of next generation semiconductors. Finally, the Act requires the Department of Defense to establish a national network for microelectronics research and development to support prototyping new semiconductor technologies for commercialization—commonly referred to as the "microelectronics commons."

Funding for the CHIPS Act, a total of $52 billion over five years, has been passed by the Senate as part of the *U.S. Innovation and Competition Act* (USICA). The House has passed several pieces of legislation within scope of USICA. House and Senate Leadership have called for a formal conference on the package of competitiveness bills.

The Department of Commerce has expressed its intent to delegate authority for the grant programs authorized in CHIPS to NIST. NIST has significant technical expertise to build on but will need additional expertise and administrative capabilities and staffing to implement the programs. The agency has actively engaged with the private sector and other stakeholders for months, in anticipation of the CHIPS funding being enacted.

CONTINUING CHALLENGES TO U.S. LEADERSHIP IN MICROELECTRONICS RESEARCH AND MANUFACTURING

Driving Transformational Advancements

The coming end of Moore's Law, as previously stated, presents major technological challenges and opportunities for progress in microelectronics. Future progress and innovation will require an approach that advances relevant materials science; device technologies; processing and packaging technologies; manufacturing technologies; circuit, chip, and system architecture; and software system and algorithm development in a co-design fashion.

The Department of Energy (DOE) has a decades-long history of working directly with industry and academia to drive scientific advancements in the areas mentioned above. DOE's microelectronics research is underpinned by its National Laboratory complex, as illustrated by the Department's recent decision to provide $54 million to support National Laboratory-based projects to advance research in microelectronics.[24] These activities are part of a longer term, crosscutting microelectronics initiative that, as articulated by a 2018 report from the DOE Office of Science, exemplifies a "fundamental rethinking" in what is needed to advance "the science behind the materials, synthesis and placement technologies, architectures, and algorithms."[25] Key to the Department's justification for its ambitions in microelectronics are its scientific user

[24] "DOE Announces $54 Million to Increase Energy Efficiency in Microelectronics Technologies," U.S. Department of Energy, August 25, 2021.
[25] "Basic Research Needs for Microelectronics: Report of the Office of Science Workshop on Basic Research Needs for Microelectronics, October 23-25, 2018," U.S. Department of Energy.

facilities, which both rely on and help drive advancements in microelectronics. These facilities, which are utilized annually by thousands of academic and industry researchers, include particle detectors, microscopes, X-ray and neutron sources, data centers, networks, and high-performance computers.

Bridging the "Lab-to-Fab" Gap

There is a general concern that the United States has underinvested in maturing breakthrough ideas for semiconductor technology to the point of manufacturing them domestically. This "lab to fab" innovation gap, known generally as the "valley of death" for technological innovation, is the phase between developing a concept or a product and scaling it into a profitable innovation that the market adopts. This phase often leads to early-stage technologies being shelved indefinitely or prematurely abandoned.[26] Importantly, funding is not the only challenge in bridging the valley of death. Companies need access to facilities, tools, and personnel suitable for demonstrating the ability to produce an innovation at commercial scale. Even well-funded startups struggle to secure time at fabs and foundries to test their products, as they compete with larger companies for access.[27]

There is an earlier valley of death from fundamental research to prototyping. Many different government agencies and other groups support early-stage semiconductor research, from the National Science Foundation to the Semiconductor Research Corporation. However, many of these funding sources stop short of supporting prototyping. Only a few U.S.-headquartered companies have the resources, infrastructure, and expertise to translate basic research into commercial production. Venture capital firms have also drastically reduced their funding to hardware companies in recent years in favor of software-driven companies with fast time-to-market and low capital expenditures.[28] The DOD led microelectronics commons was conceived to address this earlier gap.

Maintaining Competitiveness in Advanced Packaging

In addition to manufacturing, the United States has lost market share in advanced packaging. This process, called assembly, testing, and packaging (ATP), involves cutting a finished wafer into individual chips. Each chip is mounted on a frame with wires that connect the chip to external devices and enclosed in a protective casing. Traditionally, ATP was shipped overseas to countries with comparatively low wages because it is the most labor-intensive part of the manufacturing process. As a result, U.S. industry currently only has 2 percent of the global market share in ATP services.[29] R&D in advanced packaging in the United States has also lagged as relatively few research institutions focus on the topic as a priority.

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[26] "Nanomanufacturing--Emergence and Implications for U.S. Competitiveness, the Environment, and Human Health," U.S. Government Accountability Office, May 19, 2014.
[27] "American Innovation, American Growth: A Vision for the National Semiconductor Technology Center (NSTC)."
[28] Dr. Walden Rhines, "Predicting Semiconductor Business Trends After Moore's Law," SemiWiki.com, 2019.
[29] "2021 State of the U.S. Semiconductor Industry."

Many observers now believe breakthroughs in packaging will be key to improving chip efficiency beyond Moore's law because the packaging provides an alternative avenue for innovation in density and size of products. Other countries are heavily investing to get an advantage in next generation packaging. For example, the Taiwan Semiconductor Manufacturing Company (TSMC) announced in June 2021 that it would partner with 20 Japanese companies to establish an R&D center dedicated to advanced packaging design.[30]

Building a Workforce

While federal investments to grow domestic semiconductor manufacturing capacity will likely increase the number of semiconductor-related jobs in the United States,[31] concerns remain about the U.S. capacity to fill those jobs. As of 2018, there were over 4,000 open technical positions in the United States among prominent semiconductor firms.[32] The pandemic has only worsened the industry's supply of high skilled workers. In comments to NIST on strengthening the semiconductor workforce, the Semiconductor Industry Association (SIA) listed the following workforce-related challenges: a lack of supply of U.S. workers with advanced education, a lack of academic programs supporting emerging technologies, high competition among tech industries for high skilled workers, low awareness of the semiconductor industry among graduate students in STEM, a lack of hands-on training to prepare graduates for work on the manufacturing floor, a lack of diversity in STEM, and retention issues due to cultural differences between young workers and the older workforce.[33]

While the *CHIPS for America Act* addresses some of these issues through its incentive program for workforce training and through its newly established R&D programs, targeted workforce programs may be necessary to establish a lasting microelectronics workforce.

Accessing Material Inputs

Increased production of semiconductors in the United States would require increased domestic production of materials (including critical materials), chemicals, and gases. Regarding critical materials, it is often a difficult and lengthy process to establish domestic critical mineral production. A June 2021 report from the White House found that a reasonable estimate for this process is "not less than ten years."[34] Domestic production of other materials, chemicals, and gases used in semiconductor manufacturing is also somewhat limited. Both the U.S. Geological

[30] Scott Foster, "TSMC eyes 3D chip packaging edge in Japan," *Asia Times,* June 21, 2021.
[31] "The Positive Impact Of The Semiconductor Industry On The American Workforce And How Federal Industry Incentives Will Increase Domestic Jobs," Semiconductor Industry Association, webinar, May 2021.
[32] "Challenges and Opportunities Facing Semiconductor Workforce," Semiconductor Industry Association, May 30, 2018.
[33] "Current and Future Workforce Needs to Support a Strong Domestic Semiconductor Industry," Semiconductor Industry Association, comments to National Institute of Standards and Technology, August 15, 2018.
[34] "Building Resilient Supply Chains, Revitalizing American Manufacturing, And Fostering Broad-Based Growth," the White House, 100-Day Reviews under Executive Order 14017, June 2021.

Survey and NIST maintain lists of materials and gases used in semiconductor production.[35] With the exception of a few of these materials, such as Helium and Silicon, most of these materials are not produced or refined in the United States.[36] A lack of domestic access to these materials has further exacerbated supply chain delays.

Overcoming Environmental Challenges

The semiconductor industry faces significant environmental challenges. It both contributes to and is affected by climate change. It takes a significant amount of energy to produce semiconductors. Companies need to take raw silicon then melt and purify it—a process that produces a significant amount of carbon. For example, TSMC, the current largest chip producer in the world, was responsible for 15 million tons of carbon in 2020.[37] The Semiconductor Research Corporation, a nonprofit organization that funds semiconductor R&D, has committed to funding research to produce sustainable, energy efficient chip architectures.[38] In addition, Intel has said 82 percent of its energy in 2020 came from green sources such as solar and geothermal.[39]

Climate change has also harmed semiconductor production around the globe, adding to supply chain delays. For example, in February 2020, a cold snap in Texas created power outages that severely impacted semiconductor manufacturing in the state, leading to a months-long backup in production.[40] Producing chips also requires a lot of water, and severe drought in Taiwan has added to production delays.[41]

[35] "Mineral Commodity Summaries 2020," U.S. Geological Survey, January 2020; "Index of Semiconductor Process Gases," National Institute of Standards and Technology, accessed November 2021.
[36] John VerWey, "No Permits, No Fabs: The Importance of Regulatory Reform for Semiconductor Manufacturing," Georgetown Center for Security and Emerging Technologies, October 2021.
[37] Alex Crawford et al., "The Chip Industry Has a Problem With Its Giant Carbon Footprint," *Bloomberg*, April 2021.
[38] "Energy Efficient Computing: from Devices to Architecture," Semiconductor Research Corporation, 2021.
[39] Sam Shead, "The global chip industry has a colossal problem with carbon emissions," *CNBC*, November 3, 2021.
[40] Wu et al., "Why the World Is Short of Computer Chips, and Why It Matters."
[41] Emanuela Barbiroglio, "No Water No Microchips: What Is Happening In Taiwan?" *Forbes*, May 31, 2021.

Chairwoman JOHNSON. The hearing will come to order. Without objection, the Chair is authorized to declare recess at any time.

Before I deliver my opening remarks, I wanted to note today that the Committee is meeting virtually. I want to announce a couple of reminders to Members about the conduct of this hearing. First, Members should keep their video feed on as long as they are present in the meeting. Members are responsible for their own microphones. Please also keep your microphones muted until you are speaking. And finally, if Members have documents they wish to submit for the record, please email them to the Committee Clerk, whose email address was circulated prior to the hearing.

Welcome to today's hearing, and welcome to our distinguished panel of witnesses. I look forward to hearing your insights on how we can ensure the United States' leadership in microelectronics.

It wasn't news to the experts, but the last 2 years have brought into full public view the vulnerabilities in our microelectronics supply chains. Chips operate almost every piece of technology in our lives, from cell phones to cars. They are essential to our national security. Yet, the U.S. share of global semiconductor manufacturing decreased from 37 percent in 1990 to just 12 percent today. Hindsight allows us to see that our government and industry suffered a collective failure of imagination when we thought we could offshore our chips manufacturing capacity without consequences. Today, a single chip might go through 1,000 production steps in 70 countries before reaching its final product. It took a global pandemic to expose the weaknesses of that approach. But we should not be fooled that this is a once-in-a-100-year problem.

Fortunately, the semiconductor industry still leads the world in research and innovation. In 1954, the very first commercial silicon transistor was developed by Gordon Teal at Texas Instruments (TI) in Dallas, Texas. In 1958, Jack Kilby of TI invented the integrated circuit (IC). And ever since then, because of investments by both the U.S. Government and industry, we continue to lead in microelectronics innovation.

However, current technology is approaching certain physical limits. Long-term growth will require breakthroughs in everything from fundamental materials science to manufacturing processes. In the meantime, other countries are stepping up their investments. In particular, China is already outspending the United States to bolster its domestic semiconductor capacity. Moreover, they're investing in research and innovation like they never did before. They no longer want to just manufacture yesterday's chip. They want to lead in innovating tomorrow's chip. That poses both an economic and national security risk to us.

To help maintain U.S. competitiveness in microelectronics, Congress passed the *CHIPS for America Act.* The *CHIPS Act* would make substantial investments in the future of semiconductor R&D (research and development). The act also includes incentives to bring semiconductor manufacturing back to our shores.

I support full funding for the *CHIPS Act.* However, a one-time infusion of funding will not be enough to maintain U.S. leadership in microelectronics innovation. Advancing U.S. leadership in microelectronics will require a long-term, whole-of-government strategy. While incentives to re-shore capacity now are important, the future

will be shaped by how we invest in innovation and the technical work force. That is what we know and do best in this Committee. The Science, Space, and Technology Committee is ready to work with the Administration, industry, and the research community to oversee the implementation of the *CHIPS Act.*

In addition, we will continue to explore opportunities to strengthen and expand our investments in microelectronics research, including at the Department of Energy (DOE). This hearing is the beginning of a long-term effort by our Committee.

I thank you to the expert witnesses that are here today, and I look forward to the discussion.

[The prepared statement of Chairwoman Johnson follows:]

Good morning and welcome to today's hearing. And welcome to our distinguished panel of witnesses. I look forward to hearing your insights on how we can ensure United States leadership in microelectronics.

It wasn't news to the experts, but the last 2 years have brought into full public view the vulnerabilities in our microelectronics supply chains. Chips operate almost every piece of technology in our lives, from cell phones to cars. They are essential to our national security. Yet, the U.S. share of global semiconductor manufacturing decreased from 37 percent in 1990 to just 12 percent today. Hindsight allows us to see that our government and industry suffered a collective failure of imagination when we thought we could offshore our chips manufacturing capacity without consequence. Today, a single chip might go through 1,000 production steps in 70 countries before reaching its final product. It took a global pandemic to expose the weaknesses of that approach. But we should not be fooled that this is a once-in-a-hundred-year problem.

Fortunately, the U.S. semiconductor industry still leads the world in research and innovation. In 1954, the very first commercial silicon transistor was developed by Gordon Teal at Texas Instruments in Dallas TX. In 1958, Jack Kilby of TI invented the integrated circuit. And ever since then, because of investments by both the U.S. government and industry, we have continued to lead in microelectronics innovation. However, current technology is approaching certain physical limits. Long term growth will require breakthroughs in everything from fundamental materials science to manufacturing processes.

In the meantime, other countries are stepping up their investments. In particular, China is already outspending the United States to bolster its domestic semiconductor capacity. Moreover, they are investing in research and innovation like they never did before. They no longer want to just manufacture yesterday's chip. They want to lead in innovating tomorrow's chip. That poses both an economic and national security risk to us.

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Advancing U.S. leadership in microelectronics will require a long-term, whole of government strategy. While incentives to re-shore capacity now are important, the future will be shaped by how we invest in innovation and the technical workforce. That is what we know and do best in this Committee. The Science, Space, and Technology Committee is ready to work with the administration, industry, and the research community to oversee the implementation of the *CHIPs Act.* In addition, we will continue to explore opportunities to strengthen and expand our investments in microelectronics research, including at the Department of Energy. This hearing is the beginning of a long-term effort by our Committee.

Thank you again to the expert witnesses before us today. I look forward to the discussion.

With that, I now recognize Ranking Member Lucas for his opening statement.

Chairwoman JOHNSON. The Chair now recognizes Mr. Lucas for his opening statement.

Mr. LUCAS. Thank you, Chairwoman Johnson, for holding this morning's hearing.

Every American who has tried to buy a car, tractor, or even a refrigerator lately, knows that we're facing severe supply chain shortages. In many cases, these shortages are being driven by global disruption to the supply chain for semiconductors or chips, as many of us refer to them.

Microelectronics, the devices made from semiconductor materials, are critical to how we live and work. They power phones, make our cars safer, our homes smarter, and help us store and protect virtual information. It is also vital to us. They are not only essential to our economic security but our national security as well.

The Chinese Communist Party (CCP) has made it clear that it wants to dominate the globe in key technology areas, and part of their technology strategy is to increase China's share of the semiconductor market through both investment and acquisition. U.S. technology companies obtain as much as 90 percent of their semiconductor chips from Taiwan, a huge risk given the geopolitical situation in the region.

Microelectronics are necessary for the technologies of the future. Harnessing new applications such as artificial intelligence, 5G, and quantum sciences, will require fundamental breakthroughs in microelectronics technology. While the factors that led to today's chip shortage are worthy of their own examination, our focus today is forward-looking: How do we secure America's leadership in advanced chip design? How do we regain our leadership in semiconductor manufacturing? We must answer these questions to ensure we never face a chip shortage or disruption in the United States again.

Congress took the first steps to address this issue last year by passing the *CHIPS for America Act* as a part of the Fiscal Year 2021 *National Defense Authorization Act.* The *CHIPS Act,* which, when introduced, was referred solely to the Science Committee for jurisdiction, authorized programs to advance U.S. research and development, promote industry, government partnerships, and incentivize domestic fabrication of chips.

Today's hearing should provide critical guidance as Congress and the Administration consider how to implement and fund the *CHIPS Act.* I have no doubt this will be a major legislative and oversight priority for our Committee for years to come.

To lead in advanced microelectronics, the United States will need to make strategic investments along the entire innovation pipeline, from fundamental research and education, to design, to manufacturing. The Federal Government has a long tradition of investing in fundamental research for microelectronics, including through academic research institutions and Federal laboratories that are supported by the National Science Foundation (NSF), the Department of Energy, and the National Institute for Standards and Technology (NIST).

Dr. Witherell will help tell us how DOE and its laboratories have worked with industry and academia to drive scientific advancements in areas such as materials science, energy efficiency, and novel devices. Access to materials, including critical minerals, chemicals, and gases will be the key to increasing domestic technology production. Unfortunately, the United States has limited quantities of many of these critical materials, so research into al-

ternative and manufactured materials could be the answer to domestically producing advanced semiconductors.

Another challenge, which the *CHIPS Act* takes steps to address, is advanced packaging. Experts believe that breakthroughs in packaging will be key to improving chip efficiency beyond the regular doubling of computing capabilities predicted by Moore's Law. I look forward to hearing from our witnesses today about what will make a national advanced packaging manufacturing program successful.

Developing a strong work force in the United States to support the microelectronics industry is another challenge we need to solve. In the next 5 years, companies estimate that we'll need at least 42,000 semiconductor engineers nationwide. That demand is even higher for the full spectrum of workers needed, from skilled technicians and operators with associate degrees to those with advanced degrees. I hope our witnesses will provide some recommendations on how we can build this work force.

As Congress looks to strengthen U.S. chip manufacturing and advance our competitiveness in microelectronics, we must look to lessons from the past. We've been here before. In the 1980's, the Federal Government took strong actions to combat Japan's dominance in microelectronics. They included establishing a research consortium to support U.S. competitiveness in semiconductor technology, also known as SEMATECH. This government-industry partnership lasted until 1994. It helped the United States regain the lead for a time, but competing industry interests, waning government support, and other factors led to a decline that has put us where we are today.

During this time, IMEC was also established and is still in operation today. IMEC has created an international ecosystem for more than 600 world-leading industry partners and a global academic network focused on developing and testing cutting-edge semiconductor innovations. I know several of our witnesses have worked with both consortiums, and I look forward to hearing what lessons can be taken from each and used to inform the establishment of a National Semiconductor Technology Center (NSTC) and the Department of Defense's microelectronics commons.

In closing, I'd like to note that yesterday marked 2 weeks since the Democratic leaders of the House and Senate announced that there would be a conference on the Senate-passed *U.S. Innovation and Competition Act, (USICA)* and the innovation bills that our Committee carefully crafted and passed on a bipartisan basis. Unfortunately, we're still waiting on the details of that conference. Chairwoman Johnson and I are ready to go. We've been ready to go for months. It's time for leadership to move forward on a bipartisan conference of all of the Committees of jurisdiction.

The Senate bill will include significant funding for the *CHIPS Act.* And while I think there are still details to be worked out on exactly how that funding should look, time is in short supply to address our future domestic chip needs. We need to act now because I can tell you that our competitors aren't waiting.

No matter what the final vehicle is for funding the *CHIPS Act,* I look forward to working with my colleagues to get it done as soon as possible.

Thank you, Chairwoman Johnson, and I yield back the balance of my time.

[The prepared statement of Mr. Lucas follows:]

Thank you, Chairwoman Johnson, for holding this morning's hearing.

Every American who has tried to buy a car, tractor, or even a refrigerator lately, knows that we are facing severe supply chain shortages. In many cases, these shortages are being driven by global disruption to the supply chain for semiconductors or "chips".

Microelectronics, the devices made from semiconductor materials, are critical to how we live and work. They power our phones, make our cars safer, our homes smarter, and help us store and protect vital information. They are not only essential to our economic security but our national security as well.

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This government-industry partnership lasted until 1994. It helped the U.S. regain the lead for a time, but competing industry interests, waning government support, and other factors led to a decline that put us where we are today.

Chairwoman JOHNSON. Thank you very much.

If there are Members who wish to submit additional opening statements, your statements will be added to the record at this point.

At this time I'd like to introduce our witnesses. Our first witness will be introduced by Ms. Bonamici.

Ms. BONAMICI. Thank you so much, Chairwoman Johnson. It is my pleasure to introduce Dr. Ann Kelleher, Executive Vice President and General Manager of Technology Development at Intel Corporation, which has several hubs or campuses in the district I represent, and employs more than 20,000 Oregonians. Dr. Kelleher is responsible for the research, development, and deployment of next-generation silicon logic, packaging, and test technologies that power the future of Intel's innovation.

Previously, Dr. Kelleher was the General Manager of Manufacturing and Operations where she oversaw Intel's worldwide manufacturing operations, as well as corporate quality assurance and corporate services. Dr. Kelleher joined Intel in 1996 as a Process Engineer and has tremendous expertise to offer as a witness in this hearing. I want to thank her for being here with us this morning and look forward to her testimony.

Thank you, Madam Chair, and I yield back.

Chairwoman JOHNSON. Thank you very much. Our next witness is Mr. Manish Bhatia. He is the Executive Vice President of Global Operations at Micron Technology. In this role, he is responsible for driving the vision and direction for Micron's end-to-end operations. Prior to joining Micron in 2017, he served as Executive Vice President of Silicon Operations at Western Digital Corporation. He also served as Executive Vice President of Worldwide Operations at SanDisk Corporation when it was acquired by Western Digital.

Our third witness is Dr. Michael Witherell. He is the Director of Lawrence Berkeley National Laboratory (LBNL), a position he has held since January of 2016. Prior to his position at Berkeley, he served as the Vice Chancellor of Research at the University of California, Santa Barbara from 2005 to 2016 and was the Director of Fermi National Accelerator Laboratory from 1999 to 2005. He is a member of the National Academy of Sciences and a Fellow of the American Physical Society and American Association for the Advancement of Science.

Our final witness—somebody——

STAFF. Dr. Baird.

Chairwoman JOHNSON. Dr. Baird will introduce. Dr. Baird, you're recognized.

Mr. BAIRD. Thank you, Madam Chair. And it's indeed my pleasure to introduce to you an individual from Indiana's Fourth Congressional District and Purdue University. Dr. Mung Chiang currently serves as the Executive Vice President of Purdue University for Strategic Initiatives, the John A. Edwardson Dean College of Engineering, and the Roscoe H. George Distinguished Professor in the Elmore Family School of Electrical and Computer Engineering. Dr. Chiang's research on communication networks received a 2013

Alan T. Waterman Award, the highest honor to scientists and engineers under the age of 40 in the United States. And he has been the recipient of several other awards and distinctions.

Most recently, Dr. Chiang founded the Center for Tech Diplomacy at Purdue, which intends to bring engineering expertise to policymakers in a way that demonstrates the inextricable links between technology, technology advancements, and national interests.

So, Dr. Chiang, we are very happy to have you here with us today, and we really look forward to your testimony. Thank you. I yield back.

Chairwoman JOHNSON. Thank you very much.

As our witnesses should know, you will each have 5 minutes for your spoken testimony. Your written testimony will be included in the record for the hearing. When you have completed your spoken testimony, we will begin with questions. Each Member will have 5 minutes to question the panel.

We now will start with Dr. Kelleher.

TESTIMONY OF DR. ANN KELLEHER,
EXECUTIVE VICE PRESIDENT AND GENERAL MANAGER
OF TECHNOLOGY DEVELOPMENT, INTEL

Dr. KELLEHER. Chairwoman Johnson, Ranking Member Lucas, and Members of the Committee, thank you for inviting me to testify today. I lead Technology Development at Intel where we research and develop process and packaging technologies for Intel's products. We also ramp this technology into high-volume manufacturing.

Over the past 10 years, Intel has invested more than $75 billion in process and packaging R&D and U.S. manufacturing capital. Over the next 10 years, Intel anticipates spending approximately $150 billion. This will cover our recently announced expansions in Arizona, New Mexico, and a U.S. greenfield site, as well as our future technology R&D.

Intel's investments demonstrate our enduring commitment to the United States technology leadership where we conduct all of our process technology R&D and the majority of our manufacturing.

Semiconductors are fundamental to U.S. technology leadership, our economy, and our national security, and we're the fourth-largest U.S. export sector in 2020. Recent supply chain disruptions due to COVID–19 and widespread chip shortages illustrate the risk to our economy and the danger of losing our ability to make leading-edge chips in the United States.

America has lost significant share of semiconductor production to Asia over the last 30 years. For decades, countries in Asia have provided substantial incentives driving a 30 percent cost disadvantage for chipmaking in the United States and a corresponding decrease in the U.S. global share of manufacturing, and that dropped from 37 percent to 12 percent.

At the same time, designing and manufacturing leading-edge chips has also become increasingly more expensive. A recent paper from Boston Consulting Group highlighted the fact that investments required to develop the next advance in chipmaking has grown 40-fold over the last 20 years. Due to this dramatic increase, fewer manufacturers globally are able to make the investment re-

quired to develop leading-edge semiconductor technologies. In 2000, more than 25 companies built leading-edge chips, but today only three leading-edge manufacturers of logic technology remain, and Intel is the only one left in the United States.

Three essential ingredients are necessary for a strong U.S. semiconductor industry: manufacturing process technology, including IP (intellectual property) and know-how based in the United States; U.S. fab capacity to support the growing demand in the United States and worldwide; and advanced packaging capability and capacity. But these essential elements are being challenged by the 30 percent cost disadvantage and the lack of public funding for R&D.

Forty years ago, Federal investment in semiconductor R&D was more than double that of private investment, but today, U.S. private investment is nearly 20 times that of public funding. Federal investments is urgently needed to level the playing field and reverse the erosion of U.S. semiconductor industry.

Congress must enact funding of the new semiconductor manufacturing and R&D programs created in the *CHIPS for America Act* as soon as possible. The *CHIPS Act* has the right framework to create a strong U.S. semiconductor industry, and I'm confident that, if funded in a robust and sustained manner, these programs will significantly contribute to American technology leadership. Once funded, the Federal Government will need to effectively implement the *CHIPS Act* most significant new R&D program, the National Semiconductor Technology Center, or NSTC, and the National Advanced Packaging Manufacturing Program.

For the NSTC, Intel recommends priority R&D—prioritizing R&D on future breakthrough challenges that align with industry goals, leveraging existing industry infrastructure to save time and reduce cost. NSTC should be led by a neutral nonprofit that can reconcile conflicting needs in the industry.

For the packaging program, Intel recommends establishing a physical location for the participants to work together to develop leading-edge cost-effective packaging technologies in the United States. The program should encompass packaging integration efforts across the semiconductor ecosystem.

The Committee has an important oversight role regarding the *CHIPS Act* program, and Intel looks forward to working with you to provide our perspective on how to effectively implement these programs. Thank you for holding this stakeholder hearing, and I look forward to answering your questions.

[The prepared statement of Dr. Kelleher follows:]

House Committee on Science, Space, and Technology

"Ensuring American Leadership in Microelectronics"

Testimony of Dr. Ann Kelleher

Executive Vice President & General Manager, Technology Development, Intel Corporation

December 2, 2021

Chairwoman Johnson, Ranking Member Lucas, and members of the Committee, thank you for inviting me to testify about the status of advanced semiconductor development and manufacturing in the United States, and to share my perspective about new federal investment and public-partnerships to support U.S. leadership in semiconductor innovation and manufacturing throughout the supply chain.

I am the Executive Vice President and General Manager of Technology Development at Intel Corporation, which is the group at Intel dedicated to advancing Moore's Law by creating new transistor architectures, wafer, and packaging processes that we turn into products for the personal computers and cloud infrastructure we are using to safely conduct this hearing, as well as for emerging technologies like 5G networks, artificial intelligence (AI), Internet of Things (IoT), and quantum computing.

Semiconductors are fundamental to U.S. technology leadership, our economy, and national security. They represent the fourth largest U.S. export sector, and the pandemic has only accelerated the adoption of digital infrastructure powered by semiconductors. Recent supply chain disruptions due to COVID-19 and widespread chip shortages illustrate the risks to our economy and the danger of losing our ability to make advanced chips in the United States.

Yet America has lost significant share of semiconductor production to Asia over the last 30 years. For decades, countries in Asia have provided substantial incentives to build domestic semiconductor champions, driving a 30 percent cost disadvantage for chipmaking in the U.S. and a corresponding decrease in U.S. share of global chip manufacturing. Since 1990, that share has dropped from 37 percent to 12 percent, and it is projected to erode further to 9 percent by 2030.

Federal investment is urgently needed to reverse this erosion by leveling the playing field for America's semiconductor industry. Almost one year ago, Congress took a critical step by authorizing new semiconductor manufacturing and R&D programs through the CHIPS for America Act. In June, the Senate approved $52 billion in appropriations for the CHIPS Act through the bipartisan U.S. Innovation and Competition Act. Now, Congress must finish the job by enacting CHIPS funding as soon as possible. Intel is doing its part to invest in American leadership by conducting the majority of our R&D and manufacturing in the United States, and we look forward to partnering with the federal government through the CHIPS Act programs to enhance domestic semiconductor R&D and manufacturing.

As the only U.S. semiconductor company with the depth and breadth of intelligent silicon, platform, software, architecture, design, manufacturing, and scale, as well as innovation and leading-edge manufacturing capabilities here in the U.S., Intel is uniquely positioned to help the U.S. regain leadership.

Executive Summary

A November 2021 paper from the Boston Consulting Group (BCG) identified the three essential ingredients for a strong U.S. semiconductor industry: i) manufacturing process technology, including intellectual property (IP) and know-how based in the United States; (ii) U.S. fab capacity to support growing demand in the U.S. and worldwide, and (iii) advanced packaging capability and capacity. BCG also identified the two most significant gaps currently facing the United States in establishing those three ingredients: (i) a 30 percent or more cost disadvantage with East Asia that U.S. chipmakers face; and (ii) public funding for R&D, which lags both Taiwan and Korea where the most advanced semiconductors are currently manufactured. Forty years ago, federal investment in semiconductor R&D was more than double that of private investment, but today, U.S. private investment is nearly twenty times that of public funding.

The U.S. government will need to effectively leverage funding from the CHIPS Act that will be allocated to new and existing R&D programs to ensure we achieve and maintain American technology leadership. To do so, the government should take an inventory of existing federal R&D programs and partnerships with private industry to identify the critical technology gaps, and with the help of the Industrial Advisory Committee established pursuant to the CHIPS Act, determine how best to fill those gaps by using existing infrastructure in combination with new resources. These efforts should be part of developing a national semiconductor strategy and technology roadmap. The two most significant new R&D programs under the CHIPS Act are the National Semiconductor Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP).

- NSTC. Intel recommends the NSTC prioritize R&D on future breakthrough challenges that align with industry goals, and leverage existing industry infrastructure to save time and cost. NSTC should be led by a neutral non-profit that can reconcile conflicting views, such as around IP policy.

- NAPMP. High-performance chips rely heavily on advanced packaging technology, and that reliance coupled with the current worldwide capacity constraints, has highlighted the need for self-sufficient domestic packaging infrastructure. The NAPMP should establish a Package Research Center (or Centers) that allow for packaging integration – combining all the different parts together to develop and demonstrate a complete solution that improves chip performance and reduces its size.

The CHIPS Act has the right provisions to create a strong U.S. semiconductor industry, and we have confidence that if funded in a robust and sustained manner, these programs will significantly increase supply chain resiliency and contribute to American technology leadership.

Background

Intel Corporation is the world's largest semiconductor manufacturer,[1] employing over 110,000 people globally and approximately 53,000 in the United States. Intel is headquartered in Santa Clara, California and has innovation hubs in Oregon, Arizona, California, New Mexico, and Texas. Intel builds most of its product designs within its own leading-edge manufacturing and advanced packaging network, and offers foundry services for fabless chip design companies. Intel invested around $33 billion in capital expenditures and $27 billion in R&D from 2019-2021, the majority of which is conducted here in the United States.[2] Intel ranks sixth among publicly-traded U.S. companies in its individual R&D investment, and directly contributed almost $26 billion to U.S. Gross Domestic Product (GDP) in 2019, with a total GDP impact to the U.S. economy of $102 billion.[3]

Intel is making unprecedented new investments in U.S. semiconductor manufacturing capacity. Earlier this year, we announced plans to invest $20 billion in the construction of two new fabrication facilities in Arizona,[4] and to invest $3.5 billion in our New Mexico facility for the manufacturing of advanced semiconductor packaging technologies.[5] We also have announced our intention to select a new U.S. greenfield site worth up to $100 billion in investment over the next decade. These plans demonstrate Intel's ongoing commitment to leadership investments in R&D and capital expenditures in the United States, investments that enhance U.S. technological leadership and ultimately U.S. national and economic security.

Each job at Intel is estimated to support up to 13 other jobs elsewhere, meaning Intel directly or indirectly supports more than 700,000 full-time and part-time jobs in the United States.[6] Our workforce is highly educated with approximately 90 percent of people working in STEM related professions. We employ many disciplines of technical experts including engineers, chemists, physicists, and mathematicians. In the United States Intel regularly hires graduates with associate degrees, baccalaureate, master's and PhD's. In recent years on average Intel has hired over 150 students graduating from PhD programs, a significant proportion of the graduates in targeted fields across the country.

Intel is one of only three semiconductor manufacturers in the world making advanced semiconductors and the only one with its research and development anchored in the United States. The semiconductor products that Intel manufactures provide the foundations for technologies ranging from personal computing, cloud computing, artificial intelligence (AI), Internet of Things (IoT), 5G, autonomous vehicles, quantum computing, to high-performance-compute solutions, that advance humanity's understanding of, and response to, society's most pressing challenges.

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[1] See IBISWorld Industry Report 33441a, "Semiconductor and Circuit Manufacturing in the US," June 2020.
[2] See https://www.intel.com/content/www/us/en/newsroom/news/us-economic-impact-study.html#gs.0juavq.
[3] Id.
[4] See https://www.intel.com/content/www/us/en/newsroom/news/idm-manufacturing-innovation-product-leadership.html#gs.zog0za.
[5] See https://www.intel.com/content/www/us/en/newsroom/news/new-mexico-manufacturing.html#gs.0i5sdw.
[6] See https://www.intel.com/content/www/us/en/newsroom/news/us-economic-impact-study.html#gs.0juavq.

Technology Development at Intel

I lead Intel's Technology Development organization, which creates the baseline technology underpinning Intel's products and the manufacturing technology required to bring innovations into the physical world. This team's work resulted in an average of over 1,000 US patents filled per year over the last several years. I will provide a brief overview of the major teams and our process technology roadmap.

Components Research invents, develops, and demonstrates viable revolutionary and game-changing process and packaging technology options for enabling Moore's Law extension and Intel product differentiation. They then transfer those innovations and enabling technologies to other Technology Development organizations for their use in manufacturing development. This team also champions and directs over 200 university research projects annually.

Logic Technology Development is widely recognized as one of the preeminent silicon process engineering organizations in the world, consisting of approximately 8,000 employees based primarily in Hillsboro, Oregon. It produces the 'heart' of Intel products, the transistor, that is used to build a microprocessor. To maintain a predictable Moore's Law driven cadence of silicon products, at any given time, approximately four to five logic process technologies are in various stages of the development cycle, from Pathfinding to Deployment. In addition, based on strategic direction or specific product needs, two to three specialty process flows, such as advanced memory or analog/RF processes, are typically in one of the development stages.

Our **Design Enablement Group** enables both internal and external design teams to deliver winning products on Intel's cutting-edge technologies. They are responsible for delivering best-in-class Process Design Kits, which are Computer-Aided Design representations of the silicon technology to enable designs. This team also works closely with Logic Technology Development to optimize the transistor development, routing and tools, flow and methods to deliver best-in-class power, performance, and area for Intel's products. Lastly, they deliver foundational IP and test-chips and test vehicles which are a critical part of the technology development for yield and IP learning.

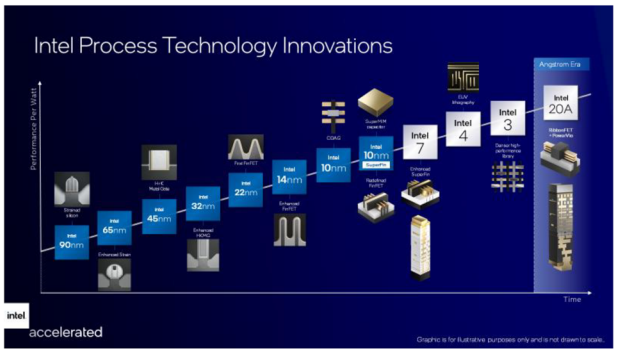
The **Assembly Test and Technology Development Group** is the world leader in advanced packaging technologies with a strong portfolio of 2.5D and 3D advanced packaging offerings. This team has substrate and assembly factories to develop leading edge packaging technologies. They create industry-leading known good die sort and test capability, and they offer package design services and silicon package co-design enablement and offer world-class board assembly.

Intel's Process Technology Roadmap

Earlier this year, I helped unveil one of the most detailed process technology roadmaps that Intel has ever provided, showcasing a new node naming system and breakthrough technologies that will power new products through 2025 and beyond, including:

- **RibbonFET**, our first new transistor architecture in more than a decade
- **PowerVia**, an industry-first new backside power delivery method

- **High NA EUV**, our plans to adapt next-generation High Numerical Aperture extreme ultraviolet lithography

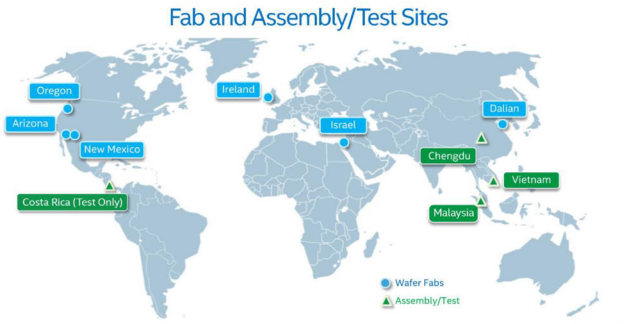


Intel's technology roadmap relies on new levels of innovation, including not only deep transistor-level enhancements, but also innovations all the way up the stack to the interconnect and standard cell level. The company has moved to an accelerated pace of innovation to enable an annual cadence of process improvements.

Manufacturing at Intel

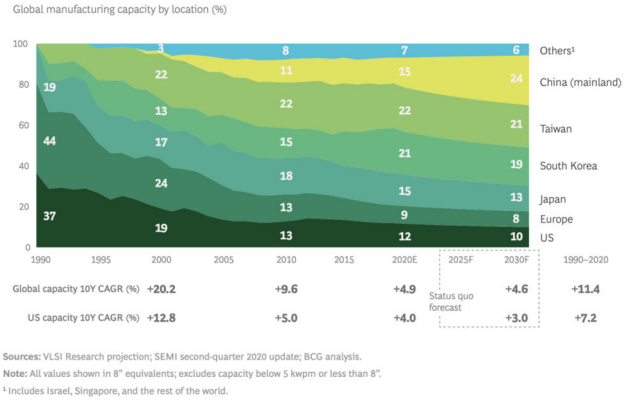
While Intel conducts the majority of manufacturing in the United States, our global manufacturing scope and scale enable us to provide our customers with a broad range of leading-edge products. Integrated manufacturing has been foundational to our success, enabling product optimization, improved economics, and supply resilience. As semiconductor manufacturing becomes more complex, Intel is one of the few remaining firms in the world, and the only one in the United States, that can do both leading-edge design and manufacturing in-house.

Intel has nine global manufacturing sites—five for silicon wafer fabrication and four for the assembly and testing of our products. We operate in a network of manufacturing facilities integrated as one factory to provide the most flexible supply capacity. Our new process technologies are transferred identically from our central development fab in Oregon to each manufacturing facility. After transfer, the network of factories and the development fab collaborate to continue driving operational improvements. This enables fast ramp of the operation, fast learning, and better quality control.



State of U.S. Semiconductor R&D and Manufacturing

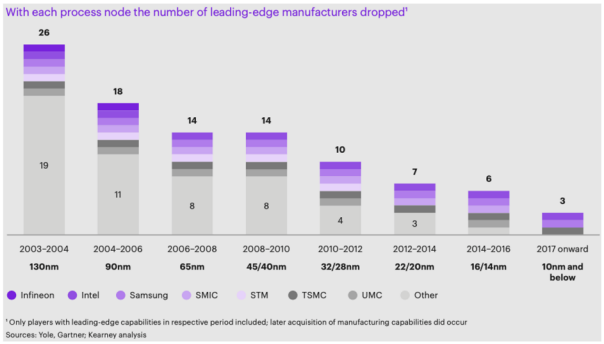
The U.S. share of semiconductor manufacturing capacity has experienced a precipitous decline over the last 30 years. In 1990, the United States represented 37 percent of the world's supply of semiconductors but today comprises only 12 percent, a share forecasted to decline even further without intervention.[7] In contrast, Asia is now home to about 75 percent of the world's total semiconductor manufacturing capacity. This imbalance exists mostly because foreign governments have invested heavily in chip manufacturing incentives while the U.S. government has not.



Designing and manufacturing leading-edge chips has become increasingly costly at each node size. The capital expenditures required to build and outfit a leading-edge fab have grown exponentially from around $3 billion just a decade ago to $20 billion today. Substantial investments into process

[7] See https://www.semiconductors.org/resources/sia-summary-of-bcg-sia-report-government-incentives-and-u-s-competitiveness-in-semiconductor-manufacturing/

technology development are also necessary to master the processes required to operate a leading-edge fab, but integrated circuit scaling is getting more difficult as traditional devices reach their scaling limits. As a result, lithography is now the most important step in fabricating integrated circuits and is also the most expensive in terms of total wafer processing cost. Due to these dramatic increases in manufacturing and technology development expenses, fewer and fewer manufacturers globally can absorb the investments required to develop the latest node sizes (see figure below).[8] Today, only three leading-edge logic manufacturers remain: Intel, Samsung, and TSMC.



Advanced packaging technologies are also undergoing a major transition from primarily connecting small geometry wiring on a die to the looser wiring density on system board to connecting small geometry wiring between many die inside one package. This 3D Heterogeneous Integration, using novel package technology as its core building block, is becoming vital to the semiconductor industry as traditional chip scaling slows down. Currently, less than two percent of the capacity for assembly, test and substrate manufacturing is in the United States. With the reported investments of Asian countries coupled with that of Asian private sector companies in 3D packaging, the United States and U.S. based companies are becoming further challenged to maintain their leadership.

[8] See https://www.kearney.com/communications-media-technology/article/?/a/europes-urgent-need-to-invest-in-a-leading-edge-semiconductor-ecosystem.

Intel's Ponte Vecchio, a product targeted for Argonne National Laboratory's exascale Aurora Supercomputer, represents the current state of the art in packaging.

A November 2021 paper from the Boston Consulting Group (BCG) identified the three essential ingredients for a strong U.S. semiconductor industry: 1) U.S. fab capacity to support growing demand in the U.S. and worldwide, 2) advanced packaging capability and capacity, and 3) manufacturing process technology including IP and know-how based in the United States.[9] BCG also identified the two most significant gaps currently facing the United States: the 30 percent cost disadvantage faced by chipmakers domestically and public funding for R&D which lags both Taiwan and Korea. Forty years ago, federal investment in semiconductor R&D was more than double that of private investment ($1 billion federal to $0.4 billion private). But today, private investment is nearly $40 billion, vastly exceeding the federal government investments of $1.7 billion in semiconductor-specific R&D and $4.3 billion in research in semiconductor-related fields."[10]

Federal government support for both R&D and manufacturing is needed to address these gaps and maintain a world-leading U.S.-based semiconductor industry. The CHIPS for America Act enacted in the National Defense Authorization Act for Fiscal Year 2021 established an effective framework of federal programs and public-private partnerships to address R&D and manufacturing challenges, including the following:

- **Financial Assistance Program** to incentivize investment in facilities and equipment for semiconductor fabrication, assembly, testing, advanced packaging, or R&D,
- **National Semiconductor Technology Center** (NSTC) public-private consortium to conduct research and prototyping of advanced semiconductor technology,
- **National Advanced Packaging Manufacturing Program** to strengthen domestic semiconductor advanced test, assembly, and packaging capability, and

[9] See https://www.bcg.com/publications/2021/establishing-leadership-in-advanced-logic-technology
[10] See https://www.semiconductors.org/sparking-innovation/

- **Industrial Advisory Committee** to advise the federal government on matters relating to microelectronics R&D, manufacturing, and policy.

These programs must be funded by Congress as soon as possible so that implementation can begin. Other countries in Asia and the EU are doubling down on their existing investments in semiconductor development and manufacturing, and the United States risks being left further behind.

National Semiconductor Technology Center (NSTC) Recommendations

Intel has been working with many groups including The Semiconductor Alliance to make recommendations for the NSTC. MITRE Engenuity, a non-profit arm of MITRE, and The Semiconductor Alliance recently developed and published a white paper to address the challenges of bridging the valley of death and driving innovation.[11] Intel supports the group's vision, which outlines how a carefully planned NSTC will address key challenges for the semiconductor industry:

- **A Marketplace of Competitive Ideas –** Launch Breakthrough Challenges that align industry around revolutionary goals that result in competitive products manufactured in the United States.
- **A Whole-of-Nation Effort –** Leverage and develop access to a nationwide network of existing facilities at U.S. companies to save cost and time.
- **High-Impact Investment and Incubation –** Establish an investment fund that fills emerging companies' need for capital and connects companies with resources and facility access to de-risk technology maturation.
- **A Workforce of the Future –** Invest in a robust domestic semiconductor workforce through curriculum development, internship and job opportunities, scholarships, vocational training programs, and K-12 educational resources.
- **Neutral, Balanced, and Resilient Governance –** Create an effective governance model that mitigates conflicts of interest and remains focused on the good of the nation and the U.S. semiconductor industry.
- **Accountability to U.S. Government Objectives –** Coordinate with existing and future U.S. government programs.

Intel also believes the following key guiding principles are critical to the NSTC's success:

- **Governance Framework** – 1) Should be led by a neutral non-profit, not a member of the industry, 2) should be focused on the needs of U.S. semiconductor manufacturers and their key suppliers, and 3) should not include foreign semiconductor manufacturers as a part of the governance.
- **Funding** – Should come from both the federal government and participating U.S. companies, prioritize U.S. companies' R&D leadership, focus on revolutionary research projects targeted for 6-12 years out, and must enable long-term sustainment of the NSTC.
- **Prototyping Projects** – Best done 1) by one leading U.S. company with invited participation from key suppliers or research groups, 2) in a U.S. company's facilities for cost and efficiency

[11] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, MITRE Engenuity November 2021, available at https://info.mitre-engenuity.org/semiconductor-alliance-vision-for-nstc

benefits, and 3) may include research partners from other companies or universities at the discretion of the lead company, but results are considered proprietary.

- **IP Policy** – Intellectual property (IP) should be owned by the companies doing the research, not by NSTC, and pre-competitive research can be collaborative multi-company projects.

In the semiconductor industry, breakthrough technologies can take over 10 years to become commercially marketable, manufacturing fabs cost tens of billions of dollars, and technical risk is high. Without investment, many ideas have no domestic path from "lab to fab." Funding, while critical, is not the only thing that companies need to shepherd new technologies across the valley of death. It is equally critical to have access to facilities, tools, and personnel suitable for demonstrating the ability to produce an innovation at commercial scale. While some prominent market leaders like Intel have their own corporate facilities for prototyping and scaling novel technologies, they tend to be the exception rather than the rule, and these facilities are typically not accessible to external teams.

National Advanced Packaging Manufacturing Program Recommendations

The rapid proliferation of high-performance products that rely on advanced packaging technology, coupled with the current worldwide capacity constraints, have highlighted the need for a robust, self-sufficient domestic infrastructure ranging from research through development to production. A critical imperative to meet these challenges and the requirements of the National Advanced Packaging Manufacturing Program is to establish a Package Research Center (or Centers) that allows for packaging integration – combining all the different parts together to develop and demonstrate a complete solution that improves performance and reduces size. This integration should span the complete ecosystem – from manufacturers to customers, from university researchers (faculty and students) to staff from the industrial sector, from material suppliers to equipment suppliers, from software providers to hardware providers.

With the establishment of a dedicated center for advanced assembly, test, and substrate development, basic integrated flows can be demonstrated, and prototypes built that meet key performance and quality and reliability metrics and enable rapid scaling in a domestic based manufacturing base. A center would provide a location for participants from academia, U.S. companies and the U.S. government to work together to develop leadership technologies and an educated and highly capable work force to support an innovative and robust domestic packaging industry. In Intel's discussions with many universities and with industrial partners, there is a strong consensus to establish this type of joint development center, which would build on the multi-tiered programs and projects where Intel collaborates across the ecosystem.

In addition, a Package Research Center should develop next generation substrate technologies that continue to support Moore's Law requirements and the development of heterogeneously integrated micro-systems. Package substrates are currently manufactured overseas, which puts our supply chain at risk. A Package Research Center could explore cost-effective manufacturing techniques to enable package substrates to be domestically manufactured and integrate advanced smaller geometry higher performances substrate technologies with assembly and test technologies.

Workforce Perspectives

Ensuring U.S. leadership in semiconductors also requires a reliable workforce, including workers with advanced degrees in STEM fields and other highly trained technical workers. Fewer U.S. students, however, are choosing the semiconductor industry as a career choice, which threatens to make workforce availability a limiting factor to a strong U.S.-based semiconductor industry. Approximately 90 percent of Intel's employees work in STEM-related technical roles—from engineering, physics, and chemistry to cooling, filtration, and technical maintenance. Filling new jobs in each of these fields, especially at a time when competition for technology workers is only intensifying, presents additional challenges that we cannot fully address on our own.

More government assistance—at the federal, state and local level—is needed to address shortfalls in the STEM talent pipeline, including the longstanding gaps in access to STEM education and training that have been magnified by the global pandemic. Government and industry must partner together to both expand educational/training opportunities and increase interest in STEM fields. Particular attention needs to be focused on females and students from low-income communities who continue to be underrepresented in the STEM pipeline.

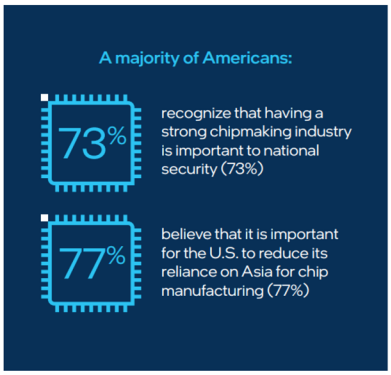
We must also work together to significantly increase access to, and participation in, STEM-related higher education—from technical training to post-doctoral research. Efforts must be made to increase and scale scholarships in engineering, computer science, and other critical STEM fields, as well as graduate research fellowships and post-doctoral programs. We must also provide additional support to community colleges, vocational institutions, and other entities that educate and train individuals in related technical disciplines. Such entities include the U.S. Armed Forces, where Intel has found success in recruiting experienced individuals for technical roles in our fabs.

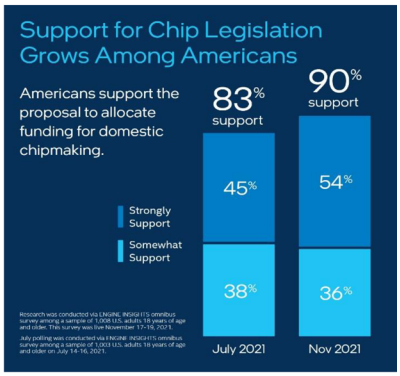
Relatedly, we know that we will never solve the shortage in STEM workers without a specific focus on underrepresented minority groups. One successful model is the **National GEM Consortium**, which is already supported by the NSF and has helped to increase diversity in the STEM workforce. Through the program, Intel supports minority students seeking graduate STEM degrees—including through financial assistance, internships, and mentorship—often leading to successful careers at Intel. NSF support can benefit similar collaborative programs, including partnerships with Historically Black Colleges and Universities (HBCUs) and other minority-serving institutions. In 2017, for example, Intel launched a $4.5 million program with six HBCUs to increase participation in electrical engineering, computer engineering, and computer science. These partnerships have yielded results – for example, at Howard University, enrollment in computer science and computer engineering has increased by 55 percent and 47 percent, respectively. With government support, potentially through the NSTC, these and similar programs could reach many more students to help bolster the domestic semiconductor industry workforce.

Call to Action on CHIPS for America Act Funding

The CHIPS for America Act offers a vital course correction for the United States which will provide essential domestic semiconductor capacity and act as a counterbalance to the policies of other countries designed to concentrate global chipmaking in East Asia. Intel supports robust funding from Congress as soon as possible to implement the CHIPS Act's semiconductor manufacturing and R&D programs. Time is of the essence: American businesses in every sector across the economy are facing a semiconductor shortage, and the only way to alleviate the current supply-demand imbalance long term is to increase manufacturing capacity by funding and implementing the CHIPS Act.

Recent nationwide polling of Americans indicates an understanding of the importance of the chipmaking industry to the U.S. economy and national security, and widespread support for Congressional action to allocate federal funding for the industry.





This Committee has an important oversight role regarding many of the CHIPS Act programs, and Intel looks forward to working with you to provide our perspective on implementation of these programs going forward. Thank you for holding this important stakeholder hearing, and I look forward to answering your questions today and working with you to advance U.S. semiconductor manufacturing and R&D.

Ann Kelleher Biography

Dr. Ann B. Kelleher is Executive Vice President and General Manager of Technology Development at Intel Corporation. She is responsible for the research, development and deployment of next-generation silicon logic, packaging and test technologies that power the future of Intel's innovation.

Previously, Dr. Kelleher was General Manager of Manufacturing and Operations, where she oversaw Intel's worldwide manufacturing operations including Fab Sort Manufacturing, Assembly Test Manufacturing and strategic planning, as well as corporate quality assurance and corporate services. Before that, she served as co-general manager of the Technology and Manufacturing Group.

Dr. Kelleher joined Intel in 1996 as a process engineer, going on to manage technology transfers and factory ramp-ups in a variety of positions spanning 200mm and 300mm technologies. She started her manufacturing leadership journey as the factory manager of Fab 24 in Leixlip, Ireland. She has also been the site manager of Intel's Fab 11X fabrication facility in Rio Rancho, New Mexico, and plant manager of Intel's Fab 12 facility in Chandler, Arizona. She then became General Manager of the Fab Sort Manufacturing organization where she was responsible for all aspects of Intel's high-volume silicon manufacturing.

Dr. Kelleher holds a bachelor's degree, a master's degree and a Ph.D. in electrical engineering, all from University College Cork in Ireland.

Chairwoman JOHNSON. Thank you very much.
Mr. BHATIA.

**TESTIMONY OF MR. MANISH BHATIA,
EXECUTIVE VICE PRESIDENT, GLOBAL OPERATIONS,
MICRON TECHNOLOGY, INC.**

Mr. BHATIA. Chairwoman Johnson, Ranking Member Lucas, and Members of the Committee, I am honored to appear before you today to discuss the status of U.S. leadership in advanced semiconductor development and manufacturing, particularly as it relates to memory and storage technology.

Chairwoman Johnson, please allow me to congratulate you on your upcoming retirement, and thank you for your decades of distinguished service. My thanks to you and to the Members of this Committee who are spearheading the bipartisan effort to ensure long-term U.S. leadership in critical semiconductor research development and manufacturing capability. With your permission, I will submit my full statement for the record.

I testify today as Executive Vice President of Global Operations at Micron, the world's memory and storage technology leader. Micron is the only company developing leading-edge memory and storage technology in the United States and the only firm manufacturing DRAM, dynamic random-access memory (RAM), or NAND flash memory in the United States.

Headquartered in Boise, Idaho, Micron is the world's fourth-largest semiconductor integrated device manufacturer and the second largest in the United States. We have 43,000 team members worldwide and nearly 10,000 of them located in facilities across the United States, including in our Manassas, Virginia, facility where we manufacture memory and storage solutions that are critical to driving growth in the expanding automotive, industrial, and networking markets.

Today, I hope to leave you with two key takeaways. First, memory and storage technologies are essential to a digital and data-intensive future for the United States. And second, long-term substantial investment in leading-edge semiconductor research and development and manufacturing is vital for the United States to maintain technology leadership across diverse end applications from the cloud to the edge and everywhere in between.

Memory and storage are foundational for every computing paradigm. Creating a meaningful domestic manufacturing base through funding of incentives program such as those included in the *CHIPS for America Act* and implementation of a refundable investment tax credit will enable a domestic supply of these essential devices.

Micron designs, develops, and manufactures industry-leading semiconductor memory and storage products, the most common of which are DRAM, which provides rapid access to data for processing, and NAND flash, which provides long-term data storage. These products are critical to all sectors of the U.S. economy and to national security.

By providing foundational capability for artificial intelligence and 5G across the data center, the intelligent edge, and consumer devices, Micron's products unlock innovation across industries, including healthcare, automotive, and communications. Computing

workloads of the future are increasingly data-intensive, requiring highly reliable, high-performing, and power-efficient advanced memory and storage solutions to optimize results.

Memory and storage have grown from 10 percent of the global semiconductor industry revenue in the year 2000 to about 30 percent of the semiconductor industry revenue today. We expect this trend to continue. For example, 5G phones have 50 percent more memory and twice the storage content as compared to 4G phones. Autonomous vehicles of the future will require as much DRAM and NAND storage as today's servers as cars become data centers on wheels.

Conversely, domestic semiconductor manufacturing has experienced a steady decline. For example, in 1990 the United States had 37 percent of global chip manufacturing capacity and now accounts for only 12 percent, and only 2 percent of global memory production. Micron has developed and is producing the world's most advanced DRAM technology 1-alpha nanometer, as well as the most advanced NAND technology, 176-Layer. Our technology leadership is based on an unwavering commitment to innovation in both research and development with our aggressive technology roadmap and manufacturing where we deliver these industry-leading technologies at scale.

We believe Congress should focus on three key areas when considering the conditions under which long-term U.S. leadership of this—of these critical semiconductor technologies can flourish: research and development, manufacturing, and work force development. We stand ready to work with this Committee and others in Congress and the executive branch to ensure the United States achieves and maintains the world's leading digital and data-intensive economy in the decades ahead.

Thank you again, Chairwoman and Members of the Committee, for the opportunity to participate today, and I look forward to your questions.

[The prepared statement of Mr. Bhatia follows:]

Testimony of Manish Bhatia, Executive Vice President, Global Operations, Micron Technology, Inc.

Before the Committee on Science, Space, and Technology

"Ensuring American Leadership in Microelectronics"

December 2, 2021

Chairwoman Johnson, Ranking Member Lucas, and members of the Committee, I am honored to appear before you to discuss the status of U.S. leadership in advanced semiconductor development and manufacturing, particularly as it relates to memory and storage technology. Chairwoman Johnson, please also allow me to congratulate you on your upcoming retirement and thank you for your decades of distinguished service. My thanks to you and to the members of this committee who are spearheading the bipartisan effort to ensure long-term U.S. leadership of critical semiconductor R&D and manufacturing capability. With your permission I will submit my full statement for the record.

I testify today as Executive Vice President of Global Operations at Micron – the world's memory and storage technology leader. Micron is the only company developing leading-edge memory and storage technology in the United States, and the only firm manufacturing DRAM or NAND in the United States. Headquartered in Boise, Idaho, Micron is the world's fourth largest semiconductor integrated device manufacturer and the second largest in the United States. We have 43,000 team members worldwide, with nearly 10,000 of them located in facilities across the United States, including in our Manassas, VA facility where we manufacture memory and storage solutions that are critical to driving growth in expanding automotive, industrial and networking markets.

I hope to leave you with two key takeaways:

- First: memory and storage technologies are essential to a digital and data-intensive future for the United States; and

- Second: long-term, substantial investment in leading-edge semiconductor R&D and manufacturing is vital for the United States to maintain technology leadership across diverse end applications from the cloud to the edge and everywhere in between. Memory and storage are foundational for every computing paradigm. Creating a meaningful domestic manufacturing base through funding of incentive programs such as those included in the CHIPS for America Act and implementation of a refundable investment tax credit will enable a domestic supply of these essential devices.

The Critical Role of Memory and Storage

Micron designs, develops and manufactures industry-leading semiconductor memory and storage products – the most common of which are DRAM and NAND. These products are critical to all sectors of the U.S. economy and national security. By providing foundational capability for AI and 5G across data center, the intelligent edge and consumer devices, Micron's products unlock innovation across industries including healthcare, automotive and communications. Computing workloads of the future are increasingly data intensive, requiring highly reliable, high performing and power efficient advanced memory and storage solutions to optimize results.

Memory and storage have grown from 10% of the global semiconductor industry revenue in the year 2000 to about 30% of the semiconductor industry today. We expect this trend to continue. For example, 5G phones have 50% more memory (DRAM) and double the storage (NAND) content as compared to 4G phones. Autonomous vehicles of the future will require as much DRAM and NAND storage as today's

servers, as cars become data centers on wheels. Conversely, domestic manufacturing has experienced a steady decline. For example, in 1990, the U.S. had 37% of global chip manufacturing capacity and now only accounts for 12% (and only 2% of global memory production).

We believe Congress should focus on three key areas when considering the conditions under which long-term U.S. leadership of these critical semiconductor technologies can flourish: research and development, manufacturing, and workforce development.

Investment in Research and Development

Micron has developed and is producing the world's most advanced DRAM technology – 1 alpha nanometer – as well as the most advanced NAND technology – 176 layer. Our technology leadership is based on an unwavering commitment to innovation in both R&D, with our aggressive technology roadmap, and manufacturing, where we deliver these industry-leading technologies at scale.

Micron invests substantially in research and development. In our fiscal year 2021, R&D spending was nearly $3 billion and we plan to increase that by about 15% in 2022. We have consistently expanded our Technology Innovation Center of Excellence in Boise, Idaho over the past decade. We're also proud to partner with the Departments of Energy and Defense, as well as the National Science Foundation, on leading-edge research initiatives that will further drive technology leadership and fuel technologies of the future.

The results of this commitment to innovation are clear; Micron is responsible for nearly 50,000 patents and counting, deploys new technology innovations and associated products at least every two years, and currently produces the world's most advanced memory and storage solutions.

The U.S. government maintains and Micron supports a range of successful R&D programs designed to advance U.S. technology leadership. As it considers new investments in R&D, as with the National Semiconductor Technology Center, the United States should complement these existing programs by focusing needed resources on bridging the gap between the lab and production for new technologies.

Several challenges prevent foundational research undertaken at universities, labs, and start-ups from transitioning to commercialization. This gap widens as semiconductor technologies advance. The U.S. Government can promote successful commercialization by facilitating prototyping capabilities for new and innovative technologies. Micron recommends that the U.S. government fund research focused on advanced memory and storage technology including:

- *To enable AI and next generation cloud and communication capabilities*, investment in near-memory and in-memory compute advancements to achieve an order-of-magnitude improvement in performance for future high-performance systems.

- *To provide 10-fold energy efficiency gains,* investment in heterogeneous integration of memory and storage with data generation (sensor) and data processing (compute) through establishment of advanced prototyping infrastructure.

- *To enable new storage technologies and emerging memory fabrics with 10 to 100-fold density, performance, and energy efficiency,* investment in materials, architecture, simulation and advanced design methodology.

New, focused investment in semiconductor-related research will accelerate industry's own efforts and play a key role in industry's ability to maintain U.S. technological leadership.

Investment in Domestic Manufacturing

To continue to lead the world in innovation, the United States must also strengthen its domestic manufacturing capacity. A stronger domestic industrial base will both ensure a secure supply chain and accelerate domestic R&D. In doing so, it will also create highly skilled jobs and stronger communities.

Micron is proud to operate the only memory and storage manufacturing facility in the United States at our Manassas, Virginia facility. We are committed to investing in the future of memory and storage manufacturing, having pledged to invest more than $150 billion globally over the next decade in leading-edge memory manufacturing and R&D, including potential U.S. fab expansion.

Congress can take two immediate steps to set the conditions for long-term U.S. leadership in semiconductor manufacturing: fully fund The CHIPS for America Act and provide a refundable investment tax credit to give companies the confidence to invest in the U.S. semiconductor ecosystem and technology leadership for the long-term.

The United States should focus support toward leading-edge manufacturing capabilities to maximize the commercial success of the investments which will in turn fund future R&D innovation.

Investments must also take into account that memory and storage manufacturing must be made on a massive scale to be competitive, that operating costs in the United States are higher than in Asia, and that many foreign governments provide incentives to attract and sustain advanced manufacturing.

To be commercially viable over the long term, memory and storage fabs must produce at very high volumes. Multiple clean room facilities are required to achieve this scale, each costing more than $15B fully equipped.

Further, it costs 35% to 45% more to build and operate a fab at scale in the United States than in lower-cost markets. Additionally, there is significant investment in leading edge R&D that must be amortized at scale to recover the investment. The technology developed in R&D requires continuous improvement after it is transferred to manufacturing to improve process margin for yield, cost, manufacturability, and quality. These are all critical factors to scalability. In order to overcome these scale and operating cost challenges, CHIPS funding and a refundable investment tax credit are imperative to enable domestic memory manufacturing to expand.

Finally, U.S. government investment is required to keep pace with other governments' investments in their own industries, which reduce our competitors' operating costs. For example, South Korea has said it will invest more than $450 billion in the semiconductor industry by 2030. Reports suggest China is on track to invest more than $150 billion from 2014 through 2030.

Investment in a Qualified Workforce

The United States must also invest now to ensure it has the workforce it needs for the future. From a workforce perspective, the industry is already in crisis. The technical positions required by our industry range from process engineers, product engineers, chemists, fabrication engineers, test engineers, quality engineers, technical marketing and field engineers to fab technicians and operators. The majority of these highly-skilled technical positions require an advanced degree or backgrounds in electrical engineering, chemical engineering, mechanical engineering, materials science, physics, electronics, data science, cloud computing, automation, digital security and artificial intelligence and machine learning. Candidates with these backgrounds are already highly employable and the shortage in these relevant skills has a tangible impact on our workforce.

Micron remains focused on developing our critical talent to focus on data analytics, smart manufacturing and emerging AI applications and related process improvements for the future. To build the workforce we need for our fab in Virginia and world-class research center in Boise, Micron partners closely with academic institutions at all levels—K-12, community colleges, and universities. We work with them to build curricula, provide internships and scholarships and the equipment and materials students need to prepare for work in today's industry, and help onboard them into long-term careers. We also partner with reskilling programs, including those focused on veterans, to transition high potential individuals into the industry.

We expect these shortages will continue — and these impacts will worsen — without a concerted, government-supported effort to improve STEM workforce availability and diversity at our U.S. universities and colleges. We will continue to strengthen these partnerships, but positioning the United States for continued expansion requires the focused attention of the federal government on strengthening the workforce. Congress should continue and expand funding to increase STEM education at all levels, enable the expansion of vocational programs at community colleges, promote re-skilling programs, and facilitate public-private partnerships to train and employ new entrants in the industry.

Conclusion

Memory and storage are essential elements of all technology solutions. With the recent unparalleled attention on the semiconductor industry and supply chain challenges, Congress is well-positioned to act. The United States must keep pace with the rate of technological change – and human innovation. I am proud that Micron is a pillar of the U.S. semiconductor industrial base, and we stand ready to work with this Committee and others in Congress and the Executive Branch to ensure the United States achieves and maintains the world's leading digital and data-intensive economy in the decades ahead.

Manish Bhatia

Executive Vice President, Global Operations
Micron Technology, Inc.

Manish Bhatia is the executive vice president of Global Operations at Micron Technology. He is responsible for driving the vision and direction for Micron's end-to-end operations. Mr. Bhatia joined Micron in 2017.

Mr. Bhatia most recently served as the executive vice president of Silicon Operations at Western Digital Corporation. Prior to that, Mr. Bhatia held several executive roles at SanDisk Corporation and was the company's executive vice president of Worldwide Operations when it was acquired by Western Digital. Prior to SanDisk, Mr. Bhatia's career included positions at Matrix Semiconductor, McKinsey & Company and Saint Gobain Corporation.

Mr. Bhatia earned bachelor's and master's degrees in mechanical engineering from the Massachusetts Institute of Technology and a master's degree in business administration from MIT's Sloan School of Management, which he attended as a Leaders for Manufacturing fellow.

Chairwoman JOHNSON. Thank you very much.
Dr. Michael Witherell.

TESTIMONY OF DR. MICHAEL WITHERELL,
DIRECTOR, LAWRENCE BERKELEY NATIONAL LABORATORY

Dr. WITHERELL. Hello. Chairwoman Johnson, Ranking Member Lucas, and distinguished Members of the Committee, thank you for holding this important hearing to focus light on this critical national challenge. I appreciate the opportunity to provide testimony.

I've been Berkeley Lab's Director since 2016, was previously Director of Fermilab. For over a decade I've become steadily more concerned about the increasing threat to the Nation's leadership in semiconductors. Strengthening the Nation's entire microelectronics ecosystem, breakthrough research, technology development, and domestic manufacturing at scale is imperative for the Nation. I do not need to convince people at this hearing how central the advanced semiconductor industry is to much of our economy.

Although industry has the central role, it is increasingly clear that our Nation's ability to lead the world in the development and deployment of advanced semiconductors will require a strong commitment across the entire Federal Government. It really is the time for an all-hands-on-deck approach that requires new investments across the innovation ecosystem, industry, academia, and the Department of Energy national laboratories.

Why should DOE have a major role in the national microelectronics initiative? First of all, as you are aware, the Department of Energy is the largest supporter in the United States of the physical sciences and is the national leader for research in the fields that underpin microelectronics: physics, chemistry, materials science, and computer science. This leadership has led to over 100 Nobel Prizes awarded to DOE-affiliated researchers, many for breakthroughs with profound impact on society.

Second, sustained Federal investment at the national labs has developed highly managed teams of the world's best scientists and built world-class large-scale research facilities. These represent a unique combination of assets that the labs can bring to the full R&D ecosystem that is needed to help meet the current challenge. These lab assets can be deployed immediately with appropriate support.

Third, the continuation of microelectronics evolution along the path of business-as-usual would require an unsustainable amount of the world's energy budget. We cannot meet the national energy goals without addressing the future of microelectronics. Conducting research to dramatically improve the energy efficiency of microelectronics is a science and technology challenge that falls squarely within the DOE's energy mission space.

I want to emphasize that the DOE national labs already have a long history of working together with the semiconductor industry on precompetitive research that has helped push the boundaries of what silicon chips can do. Several facilities have been developed at DOE labs to support the semiconductor industry's existing capability to fabricate devices with feature sizes of several nanometers.

Semiconductor companies working collaboratively here at Berkeley Lab have made over $160 million in investments at a special-

ized facility at our Advanced Light Source to support the industry's campaign to shrink the feature size on chips to widths and depths of a few dozen atoms using extreme ultraviolet UV lithography. This industry investment is even larger than stated in my written testimony since we just did a full search of the records over the history of that center.

The DOE Office of Science invests more than this for the underlying operation of the x-ray light source facility that hosts this center. The investment from industry has been for the specialized instrumentation, research, and components that enabled the center to leverage the Federal investment.

For another example, among many, the Center for Nanoscale Materials at Argonne National Laboratory offers extreme scale device processing, as do all five of the nanoscale research centers at DOE labs. And the MESAFab (Microsystems Engineering, Science and Applications Fabrications) complex at Sandia National Laboratories develops and maintains core semiconductor capabilities needed to support the DOE's nuclear security mission.

In addition, the world-leading advanced x-ray sources at DOE labs enable researchers to characterize with high-precision the new materials and novel devices needed for ultraefficient computing. Completing the cycle of technology development requires the computer modeling capabilities that the DOE's high-performance computing facilities provide with specialized software and applications developed for these platforms.

I would also like to emphasize the importance of developing a highly trained work force needed to keep us as the leader.

So, in conclusion, our Nation's global reputation for innovative technology is due in large part to the health of the entire ecosystem for research, development, and deployment with a focus on establishing a domestic manufacturing base. This will require a full science-to-systems approach that leverages the national labs to provide the fullest possible support to the industry.

Thank you for allowing me this opportunity to speak to you today.

[The prepared statement of Dr. Witherell follows:]

ENSURING AMERICAN LEADERSHIP IN MICROELECTRONICS

A Hearing of the Committee on Science, Space, and Technology
U.S. House of Representatives

Thursday, December, 2, 2021

Testimony of Dr. Mike Witherell
Director of Lawrence Berkeley National Laboratory

Introduction

Chairwoman Johnson, Ranking Member Lucas, and distinguished Members of the Committee, thank you for holding this important hearing and for inviting me to provide testimony. It is addressing one of the most important economic challenges the nation is facing, one that I have been speaking about for several years. I am heartened by the Committee's and Congress's focus on it - particularly on the important role that the Department of Energy can play in maintaining this critical capability for the economy and for national security.

I am Mike Witherell, Director of the Lawrence Berkeley National Laboratory. Founded in 1931 on the belief that the biggest scientific challenges are best addressed by scientists and engineers working together in teams, Berkeley Lab and its scientists have been recognized with 14 Nobel Prizes and 15 National Medals of Science. Today, Berkeley Lab researchers develop sustainable energy and environmental solutions, create novel materials, advance the frontiers of computing, and probe the mysteries of life, matter, and the universe. Scientists from across the United States and around the world rely on the Lab's facilities for their own discovery science. The Lab is a multiprogram national laboratory, managed by the University of California for the U.S. Department of Energy's Office of Science.

I've been Berkeley Lab's director since 2016, and was previously director of Fermilab from 1999-2005. I also served as Vice Chancellor of Research at the University of California Santa Barbara for ten years. Over the past two decades, I have become more and more concerned about the increasing threat to the nation's leadership in semiconductors. Strengthening the nation's entire microelectronics ecosystem - research, technology development and commercialization at scale - is imperative for the nation. And to address that threat adequately, as representatives of the semiconductor industry have repeatedly pointed out, requires a whole-of-government approach. Every national asset must be deployed and all resources and activities must be well

coordinated. It really is the time for an “all hands-on deck” approach that requires new investments across the innovation ecosystem – industry, academia, and the Department of Energy national laboratories.

Background

After over eight decades of federal investment in research and development at the national laboratories and universities, the Department is today the largest supporter in the U.S. of the physical sciences and is the national leader for research in the fields that underpin microelectronics: physics, chemistry, materials science, and computer science. As a measure of this impact, over one hundred Nobel prizes have been awarded to scientists affiliated with the Department of Energy and its laboratories. Because of this leadership in research and the unprecedented facilities and capabilities available for solving national problems, DOE and its national laboratories are well prepared and uniquely outfitted to continue to play a key role in the nation’s microelectronics ecosystem.

The DOE is a mission-focused agency, focusing on advancing the national interest in energy solutions, environmental sustainability, and national nuclear security. The fourth core mission of the Department is supporting the basic science that underpins and enables advances across the Department's other core mission areas. DOE and the national labs have it in their DNA to work in broad, multidisciplinary teams to meet objectives and address technology challenges that require a sustained R&D effort.

Because of DOE’s mission focus and extraordinary research capabilities, the Department and its national laboratories have successfully tackled several grand scientific national challenges, like the Human Genome Project and the development of innovative battery technologies. A unique signature of the DOE national labs is their ability to encourage, incentivize, and facilitate a tightly managed team science approach to address national challenges with the urgency they demand. They also have a proven ability to protect national security and economic interests.

Everyone arguing for a national campaign to recapture international leadership in microelectronics recognizes that the semiconductor industry has the central role. But, we also know that success requires an ecosystem of national assets supporting industry. The national laboratories bring to this ecosystem a unique capability to design, build, and steward world-leading, large-scale scientific user facilities. These facilities include the world’s most powerful supercomputers, tools that can image individual atoms in 3-D, and unique genomic and biomolecular research facilities. And they are available to support researchers from all components of the nation’s research

ecosystem -- academic, federal, and private industry. Over 36,000 researchers annually, many funded by agencies across the federal government, including NIH, NSF, NASA, and USDA, and by industry and foundations, use the national laboratories' facilities to conduct their research and technology development.

The DOE Role

Why should DOE have a major role in the national microelectronics initiative? I have just argued that the mandate to meet the DOE's mission objectives has led the national laboratories to develop highly managed teams of the world's best scientists and unique large-scale research facilities. The national laboratories contribute a unique array of assets to the science-to-systems ecosystem needed for this national campaign. And because of the federal investments made at the national laboratories over decades, these assets can be deployed immediately to help meet the current microelectronics challenge.

I have already discussed the leadership role that DOE holds in the fields of science and engineering that underlie microelectronics. In addition, the DOE national laboratories already have a long history of working together with the semiconductor industry on pre-competitive research that has helped push the boundaries of what chips can do and contributed to extending the life of Moore's law.[1] For example, the EUV lithography development facility at Berkeley Lab has been supported as a public-private partnership for more than two decades, with continuing investment from semiconductor industry partners. As a Lab Director, this investment sends me a clear confirmation that we are providing R&D services that are valuable to this industry.

In addition, the continuation of microelectronics' evolution along the path of business as usual would require an unsustainable amount of the world's energy budget. Although microelectronics make up around 5% of the world's energy consumption today, the current trajectory would put it at around 25% by 2030.[2] We cannot meet the national energy goals without addressing the future of microelectronics. Conducting research to dramatically improve the energy efficiency of microelectronics is a science and technology challenge that falls squarely within the DOE's energy mission space.

For those who understand the capabilities and history of the DOE, it is clear why and how the national laboratories can, and if given the opportunity, will make unique and profound contributions to addressing the microelectronics challenge. The Department

[1] Sparking Innovation: How Federal Investment is Semiconductor R&D Spurs U.S. Economic Growth and Job Creation. Report Supplemental: Appendice C., p. 13

[2] Decadal Plan for Semiconductors, Chapter 5, page 18, SRC 2020.

and its Laboratories have had a transformative impact on the global development of a wide range of strategic technologies, including energy storage, structural biology for medical research, genomics, and space propulsion.

The DOE strength in scientific research enables foundational discovery across a broad landscape that is focused on overcoming the barriers to technological advancement. Although we don't know the detailed designs for future generations of semiconductors, we do know that they will need new materials, novel devices, and even new algorithms. We also know from experience how we can help accelerate the design-build-test-learn cycle by which we translate new science-based technologies to commercialization.

The DOE labs contain the largest collection of nanoscale materials synthesis and characterization capabilities in the US at their user facilities. The Nanoscale Science Research Centers (NSRCs) offer extensive extreme scale nanofabrication tools and are DOE's premier user facilities for interdisciplinary research to understand and control matter at the nanoscale, serving as the basis for a national program that encompasses new science, new tools, and new computing capabilities. The DOE's x-ray light sources, neutron sources, and electron microscopes have unmatched capabilities to characterize materials and microelectronic devices. Taken together, these facilities would bring to the microelectronics initiative:

- the ability to rapidly develop novel materials with transformative electrical properties;
- a deeper understanding of quantum systems and their promise to transform computing; and
- imaging of atomic organization and chemical interactions at unprecedentedly small scales to advance more efficient devices for information processing and storage.

In addition to these remarkable facilities, the DOE laboratories have established R&D hubs and centers custom-designed to work with a specific industry sector to accelerate the cycle that translates innovations into mature technologies ready to be incorporated into products that can compete in the marketplace. The collaborative Team Science approach is successfully applied in multi-laboratory research institutions like the Joint Center for Energy Storage Research led by Argonne, the Liquid Sunlight Alliance led by Caltech, and the Critical Materials Hub led by Ames National Laboratory. The DOE Bioenergy Research Centers, including the Joint BioEnergy Institute (JBEI) at Berkeley Lab, have a remarkable record of moving biotechnologies to industry. To take just a single example, JBEI has generated intellectual property that has resulted in 99 issued patents, 150 licenses to industry, and 11 startups. Such R&D hubs do not replace

industrial laboratories, but rather they give a competitive advantage to those aligned with the national economic interest. This approach would add an extra boost to the national microelectronics campaign.

DOE also has recently developed new capabilities and resources that use data science and artificial intelligence to accelerate the materials discovery process. A trailblazing example of this is the Materials Project at Berkeley Lab. The Materials Project harnesses high performance computing for high-throughput searches for new materials - increasing throughput for discovering new electronic materials and devices by a factor of 1000x over current methods. With more than 220,000 users, over 10,000 daily unique visitors to the site and millions of data records demanded and delivered daily (average around 2M; peaks around 45M) the Materials Project is the world's most popular and utilized online materials research tool. Applied to the microelectronics challenge, researchers would more quickly and efficiently identify ideal candidate materials to help reduce the energy consumption and improve the efficiency of semiconductors.

The proposed National Semiconductor Technology Center (NSTC) is envisioned as a large, distributed center supported by several federal agencies to conduct research and prototyping of advanced semiconductor concepts in partnership with the private sector. The DOE laboratories have the capability to translate newly developed materials and process innovations into test devices and then scale them to the point that they can be fed into the chip-level processing at the NSTC. The national laboratories will be central players in setting up a pipeline that can accelerate the translation from science and engineering to technologies ready for demonstration at industrial scale.

Public-Private Partnerships

There is a long history of public-private partnerships at the national laboratories. Several technology industries understand the value proposition in taking advantage of the national laboratories for their research and technology development programs. As I have already shown, the steady investment by the federal government has produced national laboratories that have an unprecedented combination of broad scientific expertise, state-of-the-art facilities, and a highly managed approach to mission-critical R&D. Many industry sectors have formed sustained partnerships with the laboratories, using them as a force multiplier to become more competitive.

Industry also widely views the national laboratories as objective and neutral, since it is part of our mission to work in an even-handed way with all federally-approved private partners. Notable examples of successful public-private partnerships at the national

laboratories include the previously mentioned work with the semiconductor industry, as well as sustained partnerships in high performance supercomputing, advanced battery research, and pharmaceutical research and development.

Several facilities and key expertise have been developed at DOE laboratories to support the semiconductor industry's existing capability to fabricate devices with feature sizes of several nanometers. As referenced previously, semiconductor companies, working collaboratively at Berkeley Lab, have made over $90 million in investments at the Advanced Light Source to shrink the size of chips to widths and depths of a few dozen atoms by using extreme ultraviolet (EUV) lithography. Argonne National Laboratory offers extreme scale device processing at the Center for Nanoscale Materials, one of DOE's five Nanoscale Science Research Centers mentioned earlier. The MESA Fab complex at Sandia National Laboratories develops and maintains core semiconductor processing capabilities and capacity needed to support the DOE's nuclear security mission. Another example is how industry and academia are partnering with and leveraging Princeton Plasma Physics Laboratory and its expertise in plasma science to to meet the present and future challenges of semiconductor device fabrication. Low temperature plasmas are essential tools in semiconductor chip manufacturing.

In addition, the world-leading advanced x-ray light sources at DOE laboratories enable researchers to characterize with high precision the new materials and novel devices needed for ultra-efficient computing. Completing the cycle of technology development requires the computer modeling capability available at the DOE's High Performance Computing (HPC) facilities, in addition to specialized software and applications developed specifically to take advantage of these unique computing platforms. To keep the U.S. internationally competitive in high performance computing, the DOE and the national laboratories have successfully partnered with industry suppliers to co-design entirely new generations of supercomputing systems through projects such as the Exascale Computing Project. In these public-private partnerships, industry provided matching funding for DOE's investments and lab scientists and facilities have been tightly integrated into those efforts.

Finally, the pharmaceutical and biotech industry have a long and productive partnership with several national laboratories. Industry leverages the x-ray light sources at the labs for imaging proteins to advance drug discovery and speed the drug development pipeline. At Argonne and Berkeley Lab, the pharmaceutical industry has invested more than $130 million over the past 20 years in capital investments, including crystallography beamlines, and in direct research support.

STEM Workforce

I would also like to emphasize the importance of developing the highly trained workforce needed to keep the nation's standing as a global leader in microelectronics. The Departments of Materials Science and of Electrical and Computer Engineering at U.S. universities are the best in the world. But they will need to scale up their programs to train many more graduate students who have hands-on experience with the new technologies needed for the future of microelectronics. The DOE national laboratories employ over 5000 of the nation's best graduate students and postdoctoral researchers, enabling them to work on these strategic technologies and exposing them to the world-class instrumentation and facilities at the labs. To continue as the global leader in microelectronics, the nation will have to make an investment in developing the talented scientists and engineers who will forge this revolution.

Conclusion

In conclusion, a successful and efficient effort to harness the power of the U.S. federal research enterprise to drive dramatic gains for the microelectronics industry will fully leverage the existing tens of billions of dollars of investments at the national laboratories and will make strategic, new investments in their capabilities and facilities. Appended to this testimony is a joint national laboratory response to a 2018 DARPA Request for Information. This document provides more examples of capabilities at the national laboratories that may advance the nation's quest to regain international microelectronics leadership.

DOE Multi-Laboratory Response to DARPA RFI

"MICROELECTRONICS R&D FACILITY CAPABILITIES FOR PROTOTYPING"

Response to DARPA-SN-21-06

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The Department of Energy (DOE) National Laboratories offer a wide variety of powerful national user facilities and unique capabilities that can accelerate innovative R&D and prototyping for next generation microelectronic devices.

Additional Points of Contact

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Silicon Catalyst
Lawrence Berkeley National Laboratory
Pacific Northwest National Laboratory
Brookhaven National Laboratory
Battelle Memorial Institute
Argonne National Laboratory
Pacific Northwest National Laboratory
Lawrence Livermore National Laboratory
Argonne National Laboratory / U. Chicago
Sandia National Laboratories
Argonne National Laboratory
Brookhaven National Laboratory
Lawrence Berkeley National Laboratory
Los Alamos National Laboratory
Argonne National Laboratory
Pacific Northwest National Laboratory
Oak Ridge National Laboratory

A. Background

There is no existing coordination mechanism in industry, academia, or at a consortium for the introduction of disruptive technologies that require optimization across the computing technology stack. This is necessarily the proper role for government, namely establishing crosscutting scientific fundamentals and addressing first order computing stack (2nd column in Fig. 1) alignment and scale-up challenges. By attacking these elements simultaneously and with sufficient resources, a dramatic reduction can be achieved in the time it takes to move discoveries to the point where industry will make the investments to bring the new technologies to market. Historically, that time lag has ranged from 12 to 20 years even for "drop-in" technologies such as lithography transitions and transistor improvements in CMOS semiconductor manufacturing. Advances affecting several layers of the computing stack could very well take much longer unless a more coordinated and integrated approach is taken.

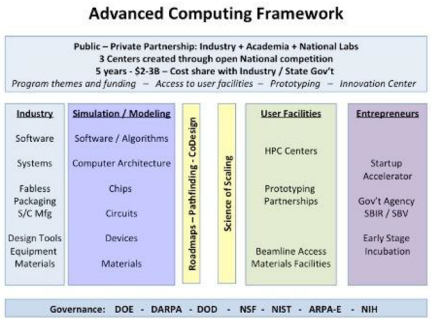

Figure 1

Combined with collective US experience in industry and academia, the DOE National Labs have the necessary scale, are fundamentally designed to address substantial interdisciplinary challenges, have the fundamental science and user facility infrastructure, and have capabilities across all hierarchical levels that need to be optimized. The National Labs are also widely viewed as objective and neutral in a way that individual competitors (or even academia) are not.

The challenges in successfully executing a collaborative program that includes such a diversity of participants are considerable. The purpose of this integrated DOE National Laboratory response is to propose solutions and facilitate a constructive dialogue, leading to a consensus on a path forward. The ultimate goal is to establish a neutral and execution-focused national initiative that can effectively down-select to the most promising emerging research innovations, attack the most critical gaps and unknowns with sufficient resources, and ultimately accelerate the technology development pipeline.

Since advances will necessarily be disruptive to current business models, there is a fundamental need for unbiased guidance and coordination. The involvement of the DOE National Labs, including their strategic assets in basic science, user facilities, and codesign capabilities can fulfill that objective. Their engagement will also assure that their unique concentration of scientists and application exploration at advanced user facilities are readily accessible, as these capabilities are not duplicated in the private sector.

Leveraging advances in electronics and computing are fundamental to the missions of several key government agencies. They share a common goal to continue US leadership and achieve asymmetric advantage by catalyzing innovations and incorporating them first. The capabilities that are described in this RFI response will be more effective in a single integrated *DOE Microelectronics Commons* than if pursued as loosely coupled Lab-centric agendas. Dispersing responsibility will not achieve the critical mass of resources necessary to invest at the scale required to tackle one of the greatest technology challenges of our generation. Moreover, the continuing advances in computing and its foundational technologies will be directly exploited by other grand challenges in science and technology where differentiation is increasingly found by applying artificial intelligence techniques (built upon advanced semiconductors, architectures and algorithms) to massive data streams to benefit our economy, defense and security.

Success Criteria: Implementing a private-public partnership is inherently complex, especially given the stakeholders' breadth: multiple government agencies, horizontally integrated industry participants within a vertical technology stack, academia from leading institutions, and the National Labs. This RFI response is intended to lead to follow up interactions for how DOE National Lab capabilities can be integrated into, and contribute to a multi-agency National Initiative in microelectronics prototyping, research and development.

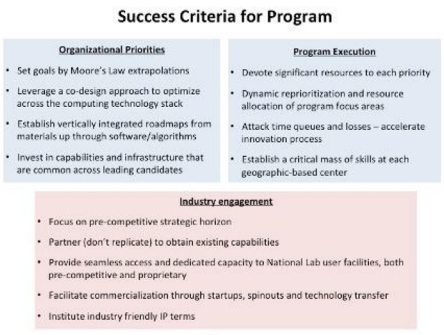

Figure 2

Hard won experiences from past collaborative efforts in basic science, technology development and manufacturing inform the proposed solutions. Of prime importance is governance, organization design, and advisory bodies' roles, and the ability to dynamically allocate resources to evolving program priorities.

The DOE National Labs have established guiding principles and success criteria (Fig. 2) for setting goals, establishing priorities, executing projects, and engaging industry. Initially, staffing private-public partnerships with the right leadership and technical skills will be the key hurdle. Attention then must shift to developing a repeatable process to evaluate candidate technologies against a clear set of goals and metrics that sustain historical scaling trends. There needs to be rapid feedback loops using models and simulations that connect and optimize across the technology hierarchy to provide guidance in technology selection and identification of key gaps to basic understanding and scaling. These in turn must be translated into projects that are prioritized with appropriate budgets and resources.

B. Facilities Overview

The DOE offers groundbreaking microelectronics capabilities and facilities in the following areas.

Fundamental Materials Science Discovery, Characterization and Synthesis: DOE basic materials science research, has a system of user facilities that accelerate our ability to discover, and design elemental excitations in condensed matter at the atomic scale. Those include systems where the principles of quantum mechanical and competing spin-orbital and lattice interactions will enable new states of correlated matter and ordered phases. This will allow an exquisitely fine energy scale control of the states, such as reducing the energy consumption in a nanoscale switch from 1pJoule to 1AttoJoule. The DOE Basic Energy Sciences "Grand Challenges" report as the guiding principle leading to the discovery of new materials, phenomena and processes that will ultimately lead us to a totally new paradigm of information processing, storage and communication.

Light Sources for Advanced Metrology and Imaging: the DOE's X-Ray light sources (synchrotrons such as the APS, NSLS-II, ALS, SSRL, X-ray Free Electron Lasers such as LCLS-II, and beam accelerators such as CEBAF) will enable researchers to identify, model, and demonstrate the new materials and devices for ultra-efficient computing. Examples include low voltage transistor concepts such as the TFET, photonic devices, spintronics, and novel memory devices. It requires advances in DOE's material modeling capability together with advances in algorithms from applied mathematics and data processing from DOE's CS and applied mathematics research programs.

Material/Device Scale Modeling and simulation DOE ASCR/ASC can apply its expertise in advanced computing and system performance modeling/simulation to exploit new device and materials systems and packaging technologies developed in the first two thrusts. Components include accelerators, on-chip wide-bandgap devices, photonic blocks, and emerging memory devices. Additionally, services such as DOE's *Materials Project enables HPC high-throughput search for new materials to increase throughput for discovering new electronic materials and devices by a factor of 1000x* over current methods.

***Architecture/Systems Modeling and Simulation*:** The value of more-than-Moore, and emerging post-CMOS materials or device technologies cannot be understood without projecting their impact on the performance and efficiency of the ultimate computer systems and architectures that they ultimately target. DOE's extensive portfolio of circuit, architecture, and system-level modeling tools enable better understanding of the performance impact of these emerging approaches on target applications and enable early exploration of new software systems that would make these new architectures useful and programmable. The goal of these architectures is to remove overheads in current designs, as well as offer hardware and thus more efficient support for important functionality for security and resiliency.

Advanced Manufacturing, Prototyping and Integration: This leverages DOE's expertise in EUV lithography e.g., the DOE led and industry supported EUREKA program. Other examples include the Sandia MESA fabrication center that can provide silicon photonics and compound semiconductor

research multi-project wafer (MPW) runs for collaborative R&D activities, as well as heterogeneous integration capabilities for making hybrid lasers and modulators on silicon photonics. Argonne offers extreme scale device processing at the Center for Nanoscale Materials cleanroom. Together, these facilities use advanced materials to develop novel nanomanufacturing methods, including EUV lithography, heterogeneous integration of advanced photonics and wide bandgap devices, and scalable engineered multi-layer thin films to fabricate photonics nanowire heterostructures. 3D stacking-is increasing density enabling photonic and memory layers on top of logic layers, and even multiple memory and logic layers interleaved. This radical change challenges assumptions embedded in current architectures, and would provide a new dimension to extend Moore's Law scaling.

B.1 Fundamental Materials Science Discovery, Characterization and Synthesis

The DOE labs contain the largest collection of nanoscale materials synthesis and characterization capabilities in the US at their user facilities. The Nanoscale Science Research Centers (NSRCs) offer extensive extreme scale nanofabrication tools and are DOE's premier user facilities for interdisciplinary research to understand and control matter at the nanoscale, serving as the basis for a national program that encompasses new science, new tools, and new computing capabilities.

The NSRCs are a set of DOE Office of Science sponsored research user facilities available for use by the international science community to advance scientific and technical knowledge in the areas of nanoscale science. The NSRC Program was established as a major component of the DOE contribution to the U.S. Government National Nanotechnology Initiative (NNI). NNI involves twenty departments and agencies that collaborate toward *"a future in which the ability to understand and control matter at the nanoscale leads to a revolution in technology and industry that benefits society."* The nanoscience centers are co-located with other major nanoscience-related user facilities such as neutron or synchrotron light sources.

The mission of the NSRCs is twofold: to enable the external scientific community to carry out high-impact nanoscience projects through an open, peer-reviewed user program, and to conduct in-house research to discover, understand, and exploit functional nanomaterials for society's benefit. To fulfill this mission, the NSRCs house the most advanced facilities for nanoscience research and employ world-class scientists who are experts in nanoscience and enjoy working with external users. The NSRCs complement each other with their instrumentation and capabilities, the different thrusts of their in-house research programs, and the technical expertise of their staff.

The NSRC Program

- Operates a national network of geographically distributed Facilities that leverage other facilities and expertise at DOE National Laboratories.
- Has world-leading capabilities and scientific expertise to create, characterize and understand novel nano-structured materials.
- Provides state-of-the-art nanoscience tools and expertise for research by non-profit or business organizations, whether small or large, for use-inspired research.

- Is available free-of-charge for non-proprietary work if the user intends to publish the research results in open literature.
- Proprietary work can also be supported on a full cost recovery basis.
- Serves users from all U.S. states and many countries around the world.
- Enables thousands of scientists to perform cutting edge nanoscience research each year.
- Contributes to the success of America's current and future research leaders.

The five NSRCs are:

- Center for Functional Nanomaterials (CFN) at Brookhaven National Laboratory
- Center for Integrated Nanotechnologies (CINT) at Los Alamos National Laboratory and Sandia National Laboratories
- Center for Nanophase Materials Sciences (CNMS) at Oak Ridge National Laboratory
- Center for Nanoscale Materials (CNM) at Argonne National Laboratory
- The Molecular Foundry (TMF) at Lawrence Berkeley National Laboratory

Across the National Laboratories there are a broad-array of microelectronics-relevant capabilities. For example, the CFN nanofabrication facility is focused on preparation of nanostructures and prototype devices made from a wide variety of materials. This research-focused cleanroom houses tools for the full fabrication workflow, including optical (2D and 3D) and electron-beam lithography, deposition of a wide variety of materials, and etching for pattern transfer. This facility is strongly focused on demonstration of novel nanomaterials, and not for fabrication of full CMOS microelectronics. The CFN nanofab thus provides crucial access to tools for the earliest phases of R&D into novel concepts that go beyond the current assumptions of commercial foundries.

Another example is the Molecular Foundry's nanofabrication facility, which focuses on understanding and applying advanced lithographies, thin film deposition, and characterization, with emphasis on the integration of inorganic, organic, and biological nanosystems that have the potential for nanoelectronic, nanophotonic, and energy applications. One of the Foundry's central research themes is on single-digit nanofabrication and assembly that aims to organize and structure material with critical features of dimensions at or below 10 nm, i.e., on the single-digit nanometer and atomic scales, to create nanoscale devices and architectures in inorganic, biological, or hybrid systems. Work in this theme is accomplished by developing protocols to visualize, understand, and implement methods of self-assembly and lithography in a variety of systems. Nanofabrication activities are facilitated in a roughly 4,850 square foot (450 m2) cleanroom, mainly Class 1000, which also includes Class 100 and Class 10 areas for nanofabrication/lithography, clean measurements and electron beam lithography.

B.2 Light Sources for Advanced Imaging and Metrology

The DOE operates world-class light sources that enable the scientific study of materials with nanoscale resolution and exquisite sensitivity. These facilities have cutting-edge capabilities for x-ray imaging and high-energy resolution analysis to capture atomic-level data on a wide variety of

materials, from biological molecules to semiconductor devices. X-ray characterization tools offered at synchrotron sources provide comprehensive quantitative capabilities for supporting microelectronics research and development. The tools range from matured techniques to novel methods taking advantage of the cutting-edge capabilities that are available at synchrotron X-ray light sources across the labs. Below are some examples of the capabilities of these facilities for microelectronic materials discovery and characterization.

Hard X-Ray Sources (APS and LCLS-II): The Advanced Photon Source (APS) offers a 100X-1000X increase in brightness and beam coherence expected by 2023. This will enable examination of 100 micron^3 sized material at 10s of nm resolution. Ultrafast electron microscopy for stroboscopic imaging and diffraction examination of materials at ps timescales, and dynamic imaging at sub-ns timescales. Extensive molecular beam epitaxy, atomic layer deposition and sputter capabilities. When it comes online, LCLS-II will be able to image complete chip designs in 3D at the nano-scale resolution.

X-Ray, Ultraviolet, and infrared Sources (NSLS-II): For example, the NSLS-II has a suite of x-ray characterization tools using soft and hard x-rays, revealing crystalline structure, atomic coordination, elemental composition, chemical states, electronic band structure, magnetic ordering, and three-dimensional imaging with nanoscale resolutions. These tools can be used under in-situ or operando conditions. Structural and spectroscopic tools can reveal the atomic-level heterogeneity and switching mechanisms in non-volatile memory (NVM) devices or material systems. X-ray scattering using coherent x-rays exhibit high sensitivity to electronic and magnetic ordering in a range of material systems that have potential application in microelectronics. NSLS-II has a unique strength in nanoscale x-ray imaging in two separate modalities: full-field imaging and scanning microscopy. Its full-field imaging capability has the world-leading measurement throughput with spatial resolutions at 30 nm, at least by a factor 10 faster than other synchrotron facilities. This method is highly effective in visualizing the 3D structure in integrated circuits (IC) for validating structural integrity. The scanning microscopy capability utilizes the world-leading x-ray beam size down to 10 nm, providing high sensitivity to crystalline strain, chemical heterogeneity, and morphology. This multimodal imaging capability finds effectiveness in quantifying strain-field in 3D gate interfaces such as nanosheets or providing chemical mapping for the buried nanoscale junctions that are inaccessible by electron-based imaging tools. NSLS-II has active collaborations with DMEA, academia, and industry, utilizing these novel capabilities for microelectronics investigations.

Soft-X-Ray Sources (ALS): For example, theThe ALS is a DOE-BES funded user facility and operates synchrotron radiation experiments for academic and industry users. The ALS together with its partners offers proprietary and nonproprietary access to its beamlines. A range of tools are available to investigate processes and materials relevant to the microelectronics community. Together with the Center for X-ray Optics (CXRO) the ALS offers capabilities to study and test EUV lithography technology and materials, e.g photoresists, photomasks and optical surfaces. The ALS also offers soft x-ray tools for the nanoscale chemical characterization of materials using x-ray scattering and imaging probes. Chemical processes, e.g. in resists or at interfaces, can be interrogated using operando characterization techniques such as ambient pressure photoemission and absorption spectroscopy. The ALS also offers a full suite of fundamental materials

characterization techniques, such as angle resolved photoemission for electronic structure studies, e.g. of quantum materials for next generation computing technologies, scattering and diffraction imaging techniques to interrogate electronic and magnetic phases, and basic structural and physical characterization tools, for example x-ray diffraction and microtomography to understand the fundamental operation of microelectronic devices at the nano-scale.

B.3 Material & Device Modeling and Simulation

Synthesizing a new material and implementing a new device heterostructure at atomic scale can be extremely time consuming and costly. To accelerate the discovery process, the DOE has created scalable computational models of materials and devices that make use of DOE's supercomputers to perform high-throughput simulation of materials and microelectronic devices *before* they are built. This greatly accelerates the evaluation of a wide-variety of options to focus efforts on the subset that offers the most promise.

The Materials Project for Automated Discovery of Microelectronic Materials: The Materials Project, is pushing the bounds of what is possible for microelectronic materials by design. MP can target data generation and uncovering design rules for novel materials relevant to domestic prototyping, including discovering and tuning multiferroics, wide bandgap semiconductors, and spin filters. This will significantly reduce the financial burden associated with failed integration of category materials because of theoretical limits on performance or synthesizability. The Materials Project is one the most visible databases of computed materials properties -- containing detailed properties of over 135,000 materials, including fundamental thermodynamics, electronic structure, elastic, piezoelectric, and dielectric tensors. All of this data can be accessed via easy-to-use interfaces through the web interface or the REST API. There is also the ability to contribute data back to the Materials Project via MPContribs, which provides the infrastructure for searchable data sets with full APIs and visibility on the Materials Details pages. This provides a rapid proliferation of data to the over 165,000 registered users for the Materials project.

As a core program of the LBL Materials Sciences Division, access to MP tools and data are free of charge. Access to staff time for customization, exploration of new scientific challenges, or generating new data sets require direct funding. For funded projects, MP has a sandbox model that enables controlled access to data available via the website. Select users have access to the core MP data and data produced for these sandboxes via the same familiar interfaces. MP currently remains a core program with a scientific focus rather than a user facility with the funding to support infrastructure upkeep and active user engagement at no or little cost. MP already serves a broad spectrum of the community from industrial to academics via community outreach: user forum, workshops, open-source codes, and significant email engagement. MP continues to grow, in-particular as MP expands to serve the large semiconductor community.

Materials Science and Electronic Structure Simulations – relevant to microelectronics, optics, quantum materials and device physics BNL lab leads a multi-lab team ExaLearn – which is a

codesign center for Exascale Machine Learning Technologies – we can leverage ExaLearn's "Design" pillar to integrate AI/ML methods into eCAD tools, and to support the National Labs investments in open source hardware design and simulation tools – although this is beyond the remit of the current project. ExaLearn coordination and integration could act as a model for future efforts in codesign for microelectronics hardware and architectural improvements.

Simulation and Modeling of Microelectronic Devices on Leadership Class Systems Applied mathematicians and computer scientists at LBNL, under funding from the DOE Exascale Computing Project, have created scalable modeling and simulation tools to analyze emerging post-CMOS microelectronic devices (electronic, spintronic, nanomagnetic and nanomechanical). AMReX (https://amrex-codes.github.io/) software framework to provide a tool for multiscale physical modeling of electromagnetic fields and related physics involved in microelectronic circuitry -- enabling device-scale simulations that are far beyond the reach of commercial tools. The resulting open-source code, ARTEMIS (Adaptive mesh Refinement Time-domain ElectrodynaMics Solver), contains support for dispersive material properties, user-defined excitation and boundary conditions, and heterogeneous physical coupling present in next-generation microelectronics. Future plans include the incorporation of multi-level adaptive mesh refinement, support for more complex geometries, additional physical modules such as superconducting and solid mechanics, and a design feedback workflow in collaboration with researchers performing atomistic-level simulations to design new materials for microelectronics applications. All of the code is open source and therefore universally available.

LAMMPS Molecular Dynamics Simulator: LAMMPS is a classical molecular dynamics code with a focus on materials modeling. The code has potentials for solid-state materials (metals, semiconductors) and soft matter (biomolecules, polymers) and coarse-grained or mesoscopic systems. It can be used to model atoms or, more generically, as a parallel particle simulator at the atomic, meso, or continuum scale. Source code is released for public use under the GNU General Public License. Information and source code releases are available at: https://lammps.sandia.gov

There are many more such open source materials and chemistry modeling codes available supported by the CMS initiative
https://science.osti.gov/bes/Research/Computational-Materials-and-Chemical-Sciences-CMS-CCS

B.4 Circuit, Architecture and System-level Modeling and Simulation

Next generation microelectronics will leverage extreme domain specialization at all scales, from high-performance computing devices, to autonomous systems, to distributed arrays of sensors, for a variety of applications. Areas such as machine learning and data analytics, which can greatly benefit from domain-specialized accelerators, are still quickly evolving the algorithmic methods, making it extremely difficult to design such accelerators by hand. Novel hardware design automation tools are required that can translate a high-level language formulation of an algorithm, to a variety of accelerator implementations ready to be fabricated and evaluated along different metrics and

constraints. Such design automation tools today are a critical part of the hardware prototyping and fabrication pipeline, providing a critical frontend element to microelectronics evaluation and fabrication activities. Tools to perform high-level and logic synthesis, technology mapping, and floorplanning, together logic cells represent critical elements of the design flow that so far have presented significant limits in availability and integration.

The DOE laboratories are developing a new generation of open source generators and synthesis tools to enable a quick design cycle from high-level specification to fabrication and rapid prototyping.

Circuit Simulation Capabilities: Xyce - is an open source, SPICE-compatible, high-performance analog circuit simulator, capable of solving extremely large circuit problems (10s to 100s of times larger and more complex than commercial SPICE-simulators can handle), using a differential-algebraic equation formulation for execution on large-scale parallel computing platforms. Xyce was developed internally at Sandia National Laboratories and funded by the National Nuclear Security Administration's Advanced Simulation and Computing (ASC) program. It also supports serial execution on all common desktop platforms, and small-scale parallel runs on Unix-like systems. The code is open source and released under the GNU General Public License. Information and source code is available at, https://xyce.sandia.gov

Computer Architecture Simulation: The Sandia Structural Simulation Toolkit (SST) was developed to explore innovations in highly concurrent systems where the ISA, microarchitecture, and memory interact with the programming model and communications system. The package provides two novel capabilities. The first is a fully modular design that enables extensive exploration of an individual system parameter without the need for intrusive changes to the simulator. The second is a parallel simulation environment based on MPI. This provides a high level of performance and the ability to look at large systems. The framework has been successfully used to model concepts ranging from processing in memory to conventional processors connected by conventional network interfaces and running MPI. Software repository: https://github.com/sstsimulator/sst-core

PARADISE++ is a post-Moore HPC (High-Performance Computing) system simulation framework to enable large scale simulations of post-Moore architectures built using emerging post-CMOS devices and technologies such as nanomagnetic, carbon nanotube, MESO, and is extensible to other emerging device technologies. Efficient simulation methods and algorithms are needed to successfully employ large scale parallel simulation of the future Beyond Moore HPC systems. PARADISE extends state of the art simulators like the SST simulator with a view of making post-CMOS system simulation flexible, scalable and extensible.

Logic in Memory Emulator (LiME) is an FPGA-based hardware memory subsystem emulator. The emulator can be configured to capture every memory access issued to the memory subsystem without perturbing the running software application. Memory traces for graph traversal (BFS) and DOE simulation benchmarks have been collected and made available to the DOE community. LiME can be configured to emulate a wide range of memory read and write latencies. The emulator is also

designed for easy insertion of custom logic to emulate near memory processing. Two accelerators, a programmable gather/scatter unit (Data Rearrangement Engine) and a key/value lookup engine have been evaluated through LiME and are available in GitHub. LiME is particularly valuable for codesign since a full software stack including application software components, OS, and drivers are emulated. Software repositories: https://github.com/LLNL/lime and https://github.com/LLNL/lime-apps

High Level Synthesis for Rapid Prototyping: PandA is an open source framework that includes methodologies supporting the research on high-level synthesis of hardware accelerators, on parallelism extraction for embedded systems, on hardware/software partitioning and mapping, on metrics for performance estimation of embedded software applications and on dynamic reconfigurable devices. The high-level synthesis tool, named Bambu, is able to generate custom hardware accelerators in hardware description languages (Verilog and VHDL), starting from high-level languages (such as C/C++ and others). Bambu interfaces with GCC and LLVM. Maintained at Politecnico di Milano, the toolchain includes significant contributions from PNNL, with several advanced synthesis methodologies that target parallel applications and irregular workloads (such as graph analytics). The tool can generate accelerators quickly instantiable on Field Programmable Gate Arrays (FPGAs), and is also able to interface to logic synthesis tools for Applications Specific Integrated Circuits (ASICs), including the opensource flows developed under the DARPA IDEA program (OpenRoad, and LS Oracle), PandA is available at: https://panda.dei.polimi.it

SystemC-clang is an open source SystemC to Hardware Description Language translator in active development through collaboration between LLNL and U of Waterloo. A floating point compression pipeline optimized to scientific data (1D, 2D, 3D arrays) has been implemented in SystemC and translated to FPGA. SystemC was particularly valuable for codesign since a scientific C++ application could drive the hardware accelerator, and iterative refinement from behavioral to cycle accurate descriptions could be evaluated in a single test environment. Software repository: https://github.com/anikau31/systemc-clang

OpenCGRA: OpenCGRA is a parameterizable and powerful open source CGRA (Coarse-Grained Reconfigurable Arrays) generator to generate synthesizable Verilog for different CGRAs based on user-specified configurations (e.g., CGRA size, type of the computing units in each tile, communication connection, etc.). OpenCGRA uses modular design and standardized interfaces between modules. The configurability and extensibility are maximized by its parametrization system to fit in various research and industrial needs. implemented leveraging PyMTL, OpenCGRA has been also exercised with heuristic design space algorithms. OpenCGRA is available at: https://github.com/pnnl/OpenCGRA

Minos Computing Library (MCL): MCL is a modern task-based, asynchronous programming model for extremely heterogeneous systems. MCL abstracts the low-level hardware details of a system, supporting the execution of complex workflows that consists of multiple, independent applications. This capability can also drive the execution of computational tasks on custom hardware designs implemented using hardware simulators or emulators, such as SST or FPGA accelerators. Importantly, MCL facilitates the execution of current applications on emerging data flow

accelerators (SambaNova, Cerebras, Xilinx Versal). MCL is available at:: https://minos-computing.github.io/

SODA Synthesizer: The Software Defined Architectures (SODA) Synthesizer is a new modular open source synthesis infrastructure. Leveraging several community efforts, the synthesizer is able to consider a variety of inputs that can interface with the Multi-Level Intermediate Representation (MLIR) compiler infrastructure, implements a synthesis backend fully integrated within the LLVM framework, and is able to generate a circuit representation in FIRRTL (the Flexible Intermediate Representation for RTL), a circuit-level IR that further simplifies the retargetability and integrability of the generated accelerators to different types of devices (FPGAs, ASICs, and more). Initially focused on Machine Learning frameworks in support of the DARPA Real Time Machine Learning Program (RTML), the retargetable frontend will be able to accept several general purpose and domain specific languages that can interface with MLIR. The backend will be able to interface with OpenCGRA, or generate RTL for FPGAs and ASICs, supporting both open source and commercial toolchains. The whole design flow will be able to perform optimization and design space exploration both at the front-end and middle-end level.

Microelectronic testing in harsh environments Brookhaven hosts the NASA Space radiation laboratory (NSRL) which provides users with beams of all ions from protons to thorium, ranging in energy from 50 MeV to 1500 MeV (ion species dependent), and extracted from the Booster accelerator with masses and energies similar to the cosmic rays encountered in space. A 100-meter transport tunnel and beam line then deliver these beams of simulated space radiation to a 400-square foot shielded target hall. NSRL's beams of ions impinge on user-provided targets and allow researchers to determine the effects of radiation on microelectronics.—As the total ionizing dose radiation tolerance of most processes increased in recent years the focus has shifted towards susceptibility for single event effects caused by radiation, specifically high energy protons and heavy ions. Irradiation studies at NSRL enable users to characterize failure modes in electronics and develop the corresponding mitigations.

B.5 Operating Model

B.5.a Is your facility available only to your organization and its collaborators?

The DOE operates national user facilities that can be used by any scientific organization on a no fee basis for open science research, or full cost recovery basis for proprietary research. One important reason for establishing America's National Laboratory system immediately after World War II was to provide a home for large-scale, costly scientific facilities that universities could not afford. Such facilities were believed to be essential to sustaining America's leadership in science. The construction and operation of large-scale scientific user facilities have been integral to the mission of the DOE Office of Science from the earliest days.

Today, the DOE Office of Science maintains and operates 28 user facilities at DOE National Laboratories across the country as shared resources for the scientific community, with no fee

access determined on a competitive basis using peer review. Tens of thousands of researchers make use of these facilities each year.

These facilities—including advanced supercomputers, particle accelerators, large x-ray light sources, neutron scattering sources, specialized facilities for nanoscience, and others—have become increasingly vital tools of scientific discovery. They have also become an important component of national economic competitiveness.

B.5.b Is your facility available to external groups from academia, the commercial sector, and the start-up community for prototyping?

DOE User Facilities are open to the global scientific community and generally follow a simple proposal based system. Proposals, if selected, enable use at no cost to the user - in return for publishing or sharing of scientific data using FAIR data principles. These facilities include the DOE BES Nanoscience Research Centers, the Advanced Computing Centers and the Synchrotron light and neutron source centers. The facilities noted above are available to external groups both from academia and the commercial sector.

Broadly Accessible Open Source Tools for Codesign: The DOE National Laboratories create open source hardware/software codesign tools to assist with architectural analysis and hardware/software codesign. For example, DOE advanced microelectronics simulation codes such as Xyce, AMReX, and PARADISE++ are all broadly available via open source licenses so that they can be used by scientists and engineers in industry or academia. DOE and DARPA applications and workflows are complex and heterogeneous. They execute multiple computationally different methods in parallel on highly-customized processors and require accuracy, response time, and low-power consumption that might not be necessary in other domains. The time-to-market for a new hardware design is also critical in many domains and could be as tight as 12-18 months. Evaluating new architectural designs in this context is challenging: Methodologies and tools to perform HW/SW codesign studies and evaluate novel technologies (especially if disruptive) need to be agile and flexible but, at the same time, accurate and reliable. These methodologies should enable researchers to 1) focus on the relevant part of the application that may benefit from the new design or technologies, 2) understand how the new hardware design relates to the rest of the application (performance and power improvements, data movement across devices), 3) provide quick turn-around information to discard architectural designs that will not be efficient, 4) easily combine the novel design with existing compilers, programming models, and workflow managers. In other terms, it is key to be able to take an existing application and replace computing devices with novel architectural designs (drop-in) without excessive disruptive modifications to the original code and while maintaining a realistic execution environment for all the other application components and methods.

Access to Leadership HPC Facilities: The DOE National Labs support high performance computing via the Leadership Computing Facilities at ANL and ORNL, and the National Energy Research Scientific Computing center at LBNL. The national impact of these computing facilities is realized via DOE's broad portfolio of scientific and engineering computational applications.

Many of these applications are open source and can be strategic elements of the infrastructure to support domestic microelectronics prototyping. Under the goals of the DOE Exascale Computing Initiative, a broad spectrum of these applications were developed to support codesign collaborations among National Lab computer and computational scientists and US computer industry counterparts that developed advanced architecture concepts for exascale computing systems. Both companies and academic researchers can apply for free access to the leadership-class supercomputing facilities (OLCF, ALCF, and NERSC) using the DOE INCITE program (https://www.doeleadershipcomputing.org/proposal/call-for-proposals/)

Additional Services for Business Development Support: All of the DOE National Labs have business development centers and business incubators with a successful track record. These include Argonne's Chain Reaction Innovations, LBNL's Cyclotron Road, SNL's MESA, SNL and LANL's CINT, LANL's National High Magnetic Field Laboratory, Laboratory for Ultrafast Materials and Optical Science, ORNL's Spallation Neutron Source.

C. Domestic Prototyping Infrastructure

C.1 Advanced Manufacturing and Prototyping

DOE's manufacturing and prototyping capabilities use advanced materials to develop novel nanomanufacturing methods, including EUV lithography, heterogeneous integration of advanced photonics and wide bandgap devices, and 3D stacking, are increasing density enabling memory layers on top of logic layers, and even multiple memory and logic layers interleaved. This leverages DOE's expertise in EUV lithography (the DOE led and industry supported EUREKA program). This radical change challenges assumptions embedded in current architectures, and would provide a new dimension to extend Moore's Law scaling.

EUREKA EUV Program: As an example of the high-impact microelectronics-relevant technology-translation enabled by DOE light-sources, the Center for X-Ray Optics (CXRO) at the ALS offers significant prototyping and design services for EUV for the microelectronics industry. The industry-funded EUREKA Program at Berkeley Lab is the current incarnation of the 25 year EUV lithography program at Berkeley Lab originally started in 1997 in partnership with the EUV LLC industry consortium and then taken over by the SEMATECH consortium in 2001 and finally transitioned to the EUREKA partnership in 2015. With the successful commercialization of EUV lithography, which the Berkeley Lab program played a key role in, EUREKA is now focused on the long-term extension of EUV lithography to sub-3-nm nodes. The EUREKA facilities at Berkeley Lab include several unique resources critical to developing the manufacturing materials of the future including both photoresists and masks. On the photoresist front, the facilities include the 0.5-NA EUV micro-exposure tool (MET5) which is the world's highest resolution projection lithography tool as well as a variety of radiation chemistry diagnostics tools enabling the detailed understanding of the interaction of EUV photons with patterning materials. On the EUV mask front, the facilities include the world's highest resolution EUV microscope for the study of EUV mask defects and next generation mask materials as well as an EUV scatterometry tool enabling the measurement of optical properties of materials in the EUV regime as well as characterizing EUV mask phase shift materials which is seen as a critical enabling technology for scaling EUV lithography to future technology nodes. This unique instrument also enables the characterization of EUV mask phase shift materials which are seen as a critical enabling technology for scaling EUV lithography to future technology nodes.

MESA MPW Fabrication Center: The Sandia MESA fabrication center that can provide silicon photonics and compound semiconductor research multi-project wafer (MPW) runs for collaborative R&D activities, as well as heterogeneous integration capabilities for making hybrid lasers and modulators on silicon photonics.

Materials Characterization and Synthesis for Microelectronics: The Brookhaven CFN nanofabrication facility is focused on preparation of nanostructures and prototype devices made from a wide variety of materials. This research-focused cleanroom houses tools for the full fabrication workflow, including optical (2D and 3D) and electron-beam lithography, deposition of a wide variety of materials, and etching for pattern transfer. This facility is strongly focused on

demonstration of novel nanomaterials, and not for fabrication of full CMOS microelectronics. The CFN nanofab thus provides crucial access to tools for the earliest phases of R&D into novel concepts that go beyond the current assumptions of commercial foundries.

Center for Nanoscale Sciences: Argonne offers extreme scale device processing at the Center for Nanoscale Materials cleanroom. The JEOL 8100 electron beam lithography with consistent, multilayer alignment at <10 nm. Ultrathin dielectrics including 2D ferroelectric doped oxides, conformal deposition tools.

Integration of synthesis, fabrication, characterization and modeling: All National Labs have the multi-disciplinary teams that are able to provide vertical integration of manufacturing capabilities with novel materials synthesis, characterization diagnostics, unique fabrication technologies, and associated modeling and simulation capabilities. For example, PNNL is pursuing research to understand new quantum phenomena with the integration of 2D magnetic or superconducting materials and highly doped oxides. The research team is using a unique pulsed laser deposition system to fabricate scalable engineered multi-layer chalcogenide thin films into quantum photonics nanowire heterostructures.

C.2 Gaps & Opportunities

Research into next-generation concepts for computing---including beyond-CMOS designs, co-located memory/computation, and neuromorphic circuits---critically requires testing novel materials and nano-devices in realistic contexts; that is, integrated into a semiconductor device. Currently there is a critical gap between the traditional foundries---which can produce full integrated circuits but are necessarily resistant to admitting novel materials that would contaminate their stringent workflow---and research nanofabs---which can produce novel structures but cannot typically produce full circuits. Resources are needed to bridge this gap, and to enable research and design workflows where novel materials and designs for circuit elements (transistors, memory cells, neuromorphic switches) and integration concepts (e.g. 3D and heterogeneous integration) can be tested in integrated circuits. Such a capability could be enabled by upgrading existing cleanrooms to provide the needed capability, or by streamlining passage of substrates between different nanofabrication facilities to enable coordination of their respective capabilities. If this critical gap is filled, progress in the design, testing, and validation of novel concepts for computing elements would dramatically accelerate. Understanding the physics of devices under extreme conditions (e.g. temperature or radiation) and developing models for dedicated design and processing is another gap that access to facilities which adequate characterization-modeling-implementation cycle flow would help to fill.

Director Mike Witherell
Lawrence Berkeley National Laboratory
Biography (2021)

In January of 2016, Michael Witherell was named the director of Berkeley Lab by the University of California's Board of Regents. A leading physicist with a highly distinguished career in teaching, research and managing complex organizations, Dr. Witherell has received numerous honors and recognitions for his scientific contributions and achievements. This is the second DOE national lab that he has led; he served as the director of Fermi National Accelerator Laboratory (Fermilab) in northern Illinois. He then went on to serve as Vice Chancellor for Research at UC Santa Barbara, where he also held the Presidential Chair in Physics. Throughout his tenure at Berkeley Lab, Director Witherell has championed a vision of stewardship of Lab's people, research, and resources that make LBNL's mission possible. An important part of this stewardship is the Lab's robust commitment to diversity and equity, as well as a culture of inclusion.

Director Witherell first arrived at UCSB in 1981 as an assistant professor of physics from Princeton University. Soon after joining UCSB, he led an experiment (at Fermilab) that collected and studied the first large sample of charmed particles observed with a silicon microstrip vertex detector. As a result of that experiment, he was awarded the W. K. H. Panofsky Prize in Experimental Particle Physics from the American Physical Society in 1990.

In 1999, Director Witherell was appointed director of Fermilab, the DOE laboratory dedicated to high-energy physics. During his six years as director, Fermilab upgraded the Tevatron accelerator complex, the highest-energy collider then in operation. The laboratory also completed a $150 million project to build a long-baseline neutrino facility, which sent a beam of neutrinos 450 miles underground to a detector built at the Soudan Underground Laboratory in northern Minnesota.

In 2005 he rejoined UCSB as vice chancellor for research (VCR), where he managed research administration and technology commercialization. He also supervised interdisciplinary research institutes in marine science, earth science, neuroscience, social sciences, and ethnic studies, in addition to the California Nanosystems Institute and six sites of the UC Natural Reserve System.

In 2010, while continuing in his role as VCR, Director Witherell returned to his research on the nature of dark matter. He joined the LUX collaboration, which completed the most sensitive search for interactions of dark matter particles with normal matter.

Director Witherell is also part of an international research team that designed the LUX-Zeplin (LZ) project, an experiment that will be three orders of magnitude more sensitive than LUX. In 2014, the LZ project was selected as the largest next-generation dark matter experiment in the DOE's High Energy Physics program.

Director Witherell is a member of the National Academy of Sciences and a fellow of the American Physical Society and the American Association for the Advancement of Science. He currently chairs the Board on Physics and Astronomy at the National Academies; sits on the Committee on Science, Engineering and Public Policy at the National Academies; is a member of the American Physical Society's Physics Policy Committee; and serves on the Board of Directors for Science for Nature and People. He is the 2004 recipient of the Energy Secretary's Gold Award.

He received his Ph.D. from the University of Wisconsin, Madison, in 1973 and his B.S. from the University of Michigan, Ann Arbor, in 1968.

Chairwoman JOHNSON. Thank you very much.
Our final witness is Dr. Mung Chiang.

TESTIMONY OF DR. MUNG CHIANG,
EXECUTIVE VICE PRESIDENT AND DEAN
OF ENGINEERING COLLEGE, PURDUE UNIVERSITY

Dr. CHIANG. Chairwoman Johnson, Ranking Member Lucas, and distinguished Members of the Committee, thank you for the opportunity to testify today. My name is Mung Chiang, the Executive Vice President for Strategic Initiatives at Purdue University and the John A. Edwardson Dean of College of Engineering. This year Purdue's College of Engineering became the largest engineering school to be ranked among top five in the United States with over 15,000 students enrolled. It also has over 100 faculty members working in microelectronics and related fields.

Our digital economy is built on silicon. It helps to visualize the supply chain in five steps. First, it's the raw materials and gases needed to make chips. Then there is hardware that goes into chip factories. Third is the design of chips and the software tools used in such design. And American companies continue to lead the world in chip design. Then there's manufacturing, taking all of the above into a factory. The physical making of a chip goes through many processes. Some factories focus on logic chips while others on memory and storage chips. And finally, assembly, test, and packaging. Once chips are made, they need to be packaged and integrated into the market electronic products and eventually find their way into phones, cars, fighter jets, and more.

Much of the discussion these days zooms in on the manufacturing step. There are two different types of business models. One is to make chips designed by the same company, and the other is to make chips designed by other companies, the foundry model. With increasing specialization in the semiconductors industry over the past 3 decades, many companies have chosen to become "fabless" and rely on the foundry. This in turn enhances the foundry's benefits of scale and sharpens its ability to deliver cutting-edge manufacturing under a service mindset and trust with the foundry customers.

For the semiconductor industry in the United States across the whole supply chain we are in the critical years now. Universities have three unique roles to play in this silicon moment. One is to help create synergy with companies large and small to bridge the fundamental research advances with commercially deployable technologies. The innovation ecosystem works best when we create synergy across major companies in manufacturing and in design, small to medium disruptors with their investors and researchers and teachers at universities.

Our second role is educating and retraining large numbers of engineers, technicians, and operators. Ideally, the university can create knowledge and jobs together, generating both new positions and the talent needed to fuel the positions.

And third, universities, especially land-grant institutions such as Purdue, have an obligation to serve as an economic driver for the State, and there's no greater opportunity today than in microelec-

tronics. And Purdue is proud to be a partner with the State of Indiana developing strategies and providing a talent pool.

And for the future of chips, the ultimate supply chain is that of human talent. In just the next 5 years at least 42,000 semiconductor engineers need to be trained and ready nationwide. The number will continue to climb well into the next decade.

There is a growing gap between the supply and demand for microelectronic and semiconductor engineers across the spectrum from associate and bachelor degrees to master's and Ph.D.'s. And some specific steps need to be made, including revising, invigorating, and expanding the microelectronics curricula with expanded use of hands-on training, online learning, partnership with community colleges and engagement with industry, and also to scale up such educational programs and substantially increase the number of scholarships for undergrads and fellowships for graduate students in the United States.

And third, to fund research development programs that push the boundaries of science and engineering and facilitate the translation of new discoveries into applications.

Action is indeed needed now. Passing the *USICA (United States Innovation and Competition Act of 2021)* and funding the *CHIPS Act* this month will be a crucial and timely win for the national security, economic security, and job security in our country. Thank you.

[The prepared statement of Dr. Chiang follows:]

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Written Testimony to the House Committee on Science, Space, and Technology

Ensuring American Leadership in Microelectronics

December 2, 2021

Mung Chiang
Executive Vice President, Purdue University
John A. Edwardson Dean, College of Engineering
Roscoe H. George Distinguished Professor of ECE

Introduction

Chairwoman Johnson, Ranking Member Lucas, and Members of the Committee, thank you for the opportunity to testify today. I am Mung Chiang, Executive Vice President for strategic initiatives at Purdue University, the John A. Edwardson Dean of the College of Engineering, and the Roscoe H. George Distinguished Professor of Electrical and Computer Engineering. Purdue University is world renowned for education, research, intellectual capital, facilities, and industrial collaborations. In 2021, Purdue's College of Engineering became the largest engineering school to be ranked among top five in the U.S., with over 15,000 students enrolled. Purdue has over 100 faculty members working in microelectronics and related fields who currently carry out research with over $110M in federal funds for research and development.

Here is a summary of the points I will make today: The U.S. must reclaim global leadership in tool development, material processing, manufacturing, and packaging of semiconductors. We need significant support from partnerships across academia, industry, national labs, and government to keep up with the pace of workforce demand for this critical industry. The ongoing discussion on legislation toward these goals has reached a critical point.

State of Semiconductors Industry in the U.S.

Our digital economy is built on silicon: microelectronic chips with up to tens of billions of transistors "printed" on feature sizes as small as one-ten-thousandth of a strand of hair. Innovative technologies, amazingly, continue to extend the life of Moore's Law: doubling the transistor density every two years, as we have seen throughout the past half-century.

For the American semiconductor industry, we are currently in the critical years. One constant reminder is the difficulty for all kinds of companies, such as the automakers, to access chip supply and continue their production. To fully understand the picture, it helps to visualize the supply chain in five steps:

- Raw materials and gases needed to make chips: some of these are rare and hard to come by.
- Hardware tools that go into the chip factories: some of these are very specialized and expensive, at over $100M per piece.

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- Design of chips, as well as the software tools used in such design: many semiconductor companies have become "fabless," as they do not fabricate, or manufacture, the chips they design.
- Manufacturing: taking all of the above into a factory, the physical making of chips goes through many processes. Some factories focus on logic chips while others on memory chips.
- Assembly, Test, and Packaging: Once chips are made, they need to be packaged and integrated into the microelectronic products and eventually find their way into phones, cars, fighter jets, and more.

There remains substantial American industry leadership in certain hardware and all software tools, and in many sectors of fabless chip design. However, there is significant dependence on foreign countries for raw materials and gases.

Much of the discussion these days zooms in on the manufacturing step, and to some degree, advanced packaging. There are two very different types of business models for manufacturing:

- Make the chips designed by the same company.
- Make chips designed by other companies: the "foundry" model.

With increasing specialization in the semiconductors industry over the past three decades, many companies have chosen to rely on a foundry model. This enhances the benefits of scale and sharpens the ability to deliver cutting edge technologies, developing the service mindset and trust with foundry customers.

Along the entire semiconductor supply chain, the U.S. is now facing a pivotal moment on 3 P's: protect, promote, and partner. Protect through export control, promote through investment, and partner through on-shoring like-minded nations' technologies to America. An impactful example is the investment by Taiwan Semiconductor Manufacturing Company (TSMC) in Arizona. Since TSMC's announcement in May 2020, it has snowballed in scale and triggered an avalanche of strategic moves across the industry and governments.

Demand for chips is exploding, and chip shortages are in the news and are pinching the supply chain of other sectors of the economy. Any nation that aims to control its destiny must lead in semiconductor manufacturing, but today, the U.S. share of global semiconductor fabrication is only 12%, down from 37% in 1990, according to the Semiconductor Industry Association, despite the fact that the U.S. is the largest end-user of semiconductors, accounting for 47% of the global market.

Today, leading edge chip fabs cost more than $10B each, and designing leading edge chips can cost $500M each and require design teams with hundreds of engineers. Leading edge chips make possible the cloud computing and increasingly powerful artificial intelligence (AI) that we access through edge devices such as our smartphones. Applications like these have voracious appetites for computing, data, and communications. To realize the promise of these technologies, the performance of electronic systems must continue to improve at the pace it has for the past 60 years, during which the performance of chips was increased by making transistors smaller and smaller and placing more and more of them on a chip. New ways to increase performance at the

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leading edge must be found because the limits of making transistors smaller have almost been reached.

The semiconductor industry faces another challenge – one that arises from its success. Chips are becoming the critical, differentiating factor in more and more products, which is creating an urgent need for affordable, custom, product-specific electronics. Electronics used in national defense is one critical example, but an increasing number of commercial companies are also seeing the need for custom electronics that differentiates them from their competitors.

The vast majority of applications do not require custom electronics. In fact, the chip shortages that we hear about today are not at the leading edge, but rather, at so-called, "legacy technology nodes." Chips are more and more pervasive and are in more and more products, but few companies have the expertise or the ability to afford the custom, product-specific designs that are needed. To fully realize the opportunities we have, new ways to advance performance at the leading edge must be found, but the times also call for the democratization and differentiation of electronics, which will require a fundamental rethinking how electronic systems are designed, packaged, and qualified. We need to unleash U.S. creativity and innovation to make the second half of the "silicon century" even more exciting and impactful than the first half.

Universities have three unique roles to play:

- One is to help create synergy with companies large and small to bridge fundamental research advances with commercially deployable technologies. Innovation ecosystem works best when we create synergy across major companies in manufacturing and in design, small to medium disrupters with their venture capital investors, and researchers and teachers at universities.
- A second role is educating and retraining larger numbers of engineers, technicians, and operators. Ideally, universities can create jobs and knowledge together, and generate both new positions and the talent needed to fill the positions.
- Universities, especially land grand institutions such as Purdue, have an obligation to serve as an economic driver for the state and there is no greater opportunity today than in microelectronics. Purdue is proud to be a partner with the State of Indiana developing strategies and providing a talent pool to fill the jobs of the future.

Workforce for Semiconductors Industry

For the future of chips, the ultimate supply chain is that of human talent.

In just the next five years, at least 42,000 semiconductor engineers need to be trained and ready nationwide. And the number will continue to climb well into the next decade. The first critical factor in re-shoring and re-energizing the U.S. microelectronics industry is to attract the most talented and energetic young people to careers in semiconductors. Today, there are not enough science, technology, engineering, and math (STEM) students in the U.S. The demand for engineers in fields such as artificial intelligence is exploding, and smaller numbers of students are choosing to pursue careers in microelectronics, further leading to a growing gap between the supply and demand for microelectronics engineers. This gap exists across the spectrum from skilled technicians and operators with associate and bachelor degrees to those with advanced

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degrees such as Master's and Ph.D.'s. This gap is especially acute in the defense sector where more U.S. citizens are needed.

Growing U.S. microelectronics manufacturing from its current level (12% of global revenue) and maintaining our strong position in design and software tools (80% of global revenue) will require a much larger workforce. This is a grand challenge that universities, companies, and government must address together in a coordinated way.

Students today are aware of the excitement and opportunities in fields such as machine learning, data science, autonomous systems (which are critically dependent on rapidly advancing electronics), but they tend to view microelectronics as an old, mature, and not very exciting field. We must find ways to make students aware of the opportunities for careers in microelectronics, the need for creative new solutions, and the impact they can have on society. They should understand that they are not entering the tail end of a maturing industry, but the beginning of a new era in electronics. Some specific steps that should be taken now are:

- Revise, re-invigorate, and expand microelectronics curricula for a new era by offering new certificates, minors, and degrees dedicated to semiconductors, both to students and to practicing engineers who need to be constantly upskilled.
- Expand partnerships with community colleges and universities to increase the supply of skilled technicians, augment internships with national labs, and increase funding for these programs from agencies such as NSF, DOD, DOE, and DOL.
- Universities should work with industry to define the types of hands-on training that is necessary for the different types of careers in microelectronics. A plan for online and "virtual hands-on" education should be developed so that students at any university or community college in the U.S. can prepare for careers in semiconductors.
- A strategy for stronger industry engagement in workforce development should be developed. For example, students studying microelectronics should be able to find internship opportunities as easily as students studying computer science. More courses should be taught with, or taught by practicing microelectronics engineers.

Purdue Is Leading the Way: New Degrees and Online Courses, Defense Workforce Preparation, Hands-on Training, and Nation-wide Partnerships

Aspiring to be the pinnacle of excellence at scale, Purdue confers over 3,000 BS, MS, and PhD engineering degrees every year, while the undergraduate program ranks among the top 10, the graduate program among the top 4, and the online graduate program top 3 in the U.S.

Purdue University's Elmore Family School of Electrical and Computer Engineering announced two months ago that it is introducing America's **first suite of degrees and credentials dedicated to semiconductors**. This includes a new Master's degree in semiconductors and microelectronics (to be offered both residential and online), an undergraduate minor degree, and several online certificates. Students will learn both the manufacturing and design of chips, as well as the entire supply chain: the chemical engineering of gas reaction, the mechanical engineering of tool development and packaging, the material engineering of new manufacturing materials, and the industrial engineering of supply chain and logistics optimization. Courses will

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be supplemented with hands-on learning in one of the largest clean rooms in academia, and virtual simulation projects. The first students will be able to enroll starting next spring semester in some of these offerings.

Purdue is also a leader in **online education**. An example is the nanoHUB, the premier open and free platform for computational research, education, and collaboration in nanotechnology and related fields. Through the nanoHUB site, Purdue offers a rapidly growing collection of courses and simulation tools that run in the cloud. This platform will be expanded to scale up relevant courses for microelectronics and make them available to academic and industrial partners.

Purdue leads **SCALE, a 12-university consortium** that received a five-year, competitive award from the Department of Defense through Indiana's NSWC Crane, to educate the next generation of BS, MS, and PhD graduates, especially for defense applications. This microelectronics workforce development initiative blends classroom instruction with hands-on training and introduces students to concepts of secure and trusted microelectronics. A significant research investment through SCALE will not only add to the knowledge base but provide enhanced training for the students and add value for their future employers.

Purdue is home to the **Birck Nanotechnology Center (BNC)**, an interdisciplinary research infrastructure for 160 affiliated faculty members and their research groups from 36 academic units at Purdue. The 187,000 sf facility includes a 25,000 sq. ft. ISO Class 3-4-5-6 (Class 1-10-100-1000) nanofabrication cleanroom - the Scifres Nanofabrication Laboratory. This is the largest clean room of this quality in a U.S. university. This is the place where quality hands-on training occurs for hundreds of students, a much-needed feature for microelectronics workers. Despite how critical this facility is for training, the upgrading and maintenance is a challenge, equipment is expensive and quickly becomes obsolete. It is imperative to receive more support to maintain competitivity and train the next generation workforce on current, relevant technologies, rather than equipment dated decades ago.

Purdue is also creating **workforce development programs with Ivy Tech**, a state-wide community college with over 70,000 students, to train technicians and production workers needed in semiconductor foundries, and to create a significant pipeline of students from community colleges to a university degree.

No single university can do everything in semiconductor workforce development. Purdue understands that solutions to workforce problems have to be developed in partnership across sectors to deliver excellence at scale. In a **workshop** organized by Purdue on November 12, 2021, representatives from industry were joined by representatives from the U.S. Departments of Commerce and Defense, the National Science Foundation, national labs, and academia, to discuss scaling-up educational programs; online and hands-on training; knowledge and skills for technicians, BS, MS, and PhD graduates; special programs for trusted and assured electronics; and funding opportunities for comprehensive workforce development programs. This is just the first event in a series that will bring together the right stakeholders to solve the semiconductors workforce development issues and ensure the U.S. is the rightful leader in the field.

Purdue is also part of the **American Semiconductor Academy (ASA),** a partnership of 50 American universities and community colleges. The ASA initiative aims to secure America's global leadership in semiconductor manufacturing by encouraging universities to collaborate with each other through a distributed network across the country with diverse sources of talent,

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partner with companies to attract and develop talent, and foster innovation to fuel the growth of semiconductor manufacturing in the U.S.

Semiconductor fabs are expensive to build and operate, but they are still fundamentally a manufacturing facility. Various states in the U.S. have maintained their manufacturing DNA in their workforce. The State of Indiana has targeted the semiconductor industry for continued growth and has scaled up their efforts led by Governor Holcomb and Commerce Secretary Chambers. I am honored to **serve as the technology advisor to the state**, and together we are working to on a strategy to recruit industry and build a workforce to meet their needs and the needs of our nation.

We also launched the **Center for Tech Diplomacy at Purdue (CTDP)**, an independent think tank at the intersection of technology and U.S. foreign policy. There is a gathering, bipartisan appreciation of the impact of technology on national security, human rights, economic growth, democracy, and liberty. CTDP brings deep engineering expertise and training to policymakers in an understandable and relevant way that demonstrates the inextricable links between technology and policy.

The Moment Is Now

Universities cannot solve alone the R&D and workforce problems that the microelectronics industry faces today. Significant investment from the government is needed on four fronts:

1) scale up the educational programs including hands on training and online learning,
2) substantially increase the number of scholarships for undergraduates and fellowships for graduate students in areas related to the semiconductors supply chain,
3) fund research and development programs that push the boundaries of science, and
4) facilitate translation of new discoveries into applications.

A highly skilled, creative, innovative, and substantially larger microelectronics workforce is a critical factor in the nation's strategy to re-shore and re-energize U.S. microelectronics. There is a serious gap today in the supply and demand for microelectronics technicians and engineers, and the shortage of talent will grow even larger as we build microelectronics facilities in the hundreds of billions in the U.S. this decade.

Action is needed now. Every day that passes makes the U.S. more vulnerable to risks in the supply chain, gaps in defense technologies, and a dire shortage of qualified workers. Passing the United States Competition and Innovation Act (USICA) this month will be a crucial and timely win for the national security, economic security, and job security in our country.

Dr. Mung Chiang

Dr. Mung Chiang is the Executive Vice President of Purdue University for strategic initiatives, the John A. Edwardson Dean of the College of Engineering, and the Roscoe H. George Distinguished Professor in the Elmore Family School of Electrical and Computer Engineering.

Dr. Chiang's research on communication networks received the 2013 Alan T. Waterman Award, the highest honor to scientists and engineers under the age of 40 in the U.S. He is a recipient of the Terman Education Award conferred by the American Society for Engineering Education, the Kiyo Tomiyasu Technical Achievement Award conferred by the Institute of Electrical and Electronics Engineers, and a Guggenheim Fellowship. He is a fellow of the National Academy of Inventors and a foreign member of the Royal Swedish Academy of Engineering Science.

Dr. Chiang founded the Princeton EDGE Lab in 2009, which bridges the theory-practice gap in edge computing and co-founded a few startup companies with products used by tens of millions of people worldwide. His textbook "Networked Life," popular science book "The Power of Networks," and online courses have reached hundreds of thousands of students.

Most recently Dr. Chiang founded the Center for Tech Diplomacy at Purdue, which intends to bring engineering expertise to policymakers in a way that demonstrates the inextricable links between technology advances and national interests.

Chairwoman JOHNSON. Thank you very much. At this point we will begin our first round of questions. And the Chair recognizes herself for 5 minutes. I'd like each witness to comment. As you all have testified, the United States faces several challenges to maintaining U.S. leadership in microelectronics. They include a lack of domestic manufacturing and packaging capacity, a limited technical work force, technology transfer challenges, and multiple scientific challenges.

Given that the availability of resources may never be enough to fully address all of the many challenges, how should the Federal Government set funding and policy priorities, in particular since this is the Science Committee, how should we prioritize policies and funding to maintain leadership in semiconductor innovation?

Dr. KELLEHER. I will start. So my recommendation is that this Committee needs to look at some of the key breakthroughs that are needed for the long haul to maintain the overall research and development and the future of the industry. The funding which comes with the *CHIPS Act,* once the funding is received and arrives, it doesn't have an immediate impact as far as the longer haul, so I believe that we as a semiconductor industry need to identify the top key areas in terms of that we need to continue to develop the—from materials science, from lithography, from all the aspects that continues to keep moving our research in the 5 to 10—in the 10 to 15 years out so that we can set ourselves up for technology leadership for the long haul.

Mr. BHATIA. Chairwoman Johnson, I'll—I can go next. I believe that the prioritization should be toward leading-edge technologies, whether in research and development or in manufacturing. Chairwoman Johnson, as you noted in your introductory remarks and as Ranking Member Lucas noted in his, from the dawn of the semiconductor era with the mention of the integrated chip to—you know, to today, the thing that makes the semiconductor industry unique is the rate of change of technology and that cadence that continues to move every 18 to 24 months. New technologies are introduced that are higher performance, higher density, and lower power.

And so the biggest challenge that we face as an industry is continuing to maintain that—the leadership in advanced leading-edge capability for process technology, for device capability, and in manufacturing. So, you know, our recommendation is that the funding both for research and development, as well as for manufacturing, focus on leading-edge technologies because these are the areas that are going to ensure American leadership in microelectronics far into the future. And both the *CHIPS Act* and as well as the refundable tax incentives that are being proposed are both necessary measures to be able to ensure that this can happen.

Dr. WITHERELL. So I can go next. And I would say for the Federal investment in R&D, I think keeping that focused on the laboratories that are best connected with the industry, this has to be laser focused on working through the problems that industry is facing on developing the new technologies. And so there are longstanding partnerships, public-private partnerships on working through this, as we have at several of the laboratories and at some

academic laboratories as well to make sure that we're solving the problems that industry needs to work our way through this.

The other thing I would say is that we need a bigger work force, a more capable work force working in these hardware technologies than we have today. You heard about it from our Dean. Supporting the academic environment so we can grow this work force is essential, too.

Dr. CHIANG. Of course a mic check to see if you can hear me. Great, thank you. I was worried that, you know, I've lost my engineer's ability to adjust the volume on my computer, so great to know that you can hear me now.

Well, I want to just echo what my fellow panelists have already mentioned. There is the need to fund and prioritize ideas for the future, and then there is the need to fund the people that are needed today. The ideas for the future, as we mentioned, activities in R&D in areas such as advanced packaging, heterogenous integration, new material and going from two dimensions to three dimensions, are all essential to the continued R&D vibrancy of semiconductors industry in the United States.

As to the people that we need today, it will take a grand strategy across government, industry, educational institutions, K–12, and government national labs to work together, in particular, to deploy more online learning for upscaling and retraining of existing work force, to substantially increase the number of K–12 student pipeline into engineering programs in the country, and to increase the use of hands-on learning, industry internship opportunities to make sure that they are ready for the market. And all of these can be further supplemented by increasing the number of scholarships for undergraduates and fellowships for Ph.D. students in the country.

And finally, we do need indeed a diversity in the range of talents, including those who are in community colleges and also inclusivity in the geographic balance. There are many talents throughout the country, and they can all be part of the solution to the work force shortage problem.

Chairwoman JOHNSON. Thank you very much. The Chair now recognizes Mr. Lucas for 5 minutes.

Mr. LUCAS. Thank you, Madam Chair. And before I begin my questions, can I take a moment to introduce the newest Member of the Science Committee?

Chairwoman JOHNSON. Yes, you may.

Mr. LUCAS. Thank you, Chairwoman Johnson. And I'd like to welcome Mike Carey as the newest Member of our Committee. He joins us from Ohio's 15th District. He brings decades of experience in the energy industry. And I know he's eager to get to work helping us strengthen and modernize the American energy production with an all-above approach to new energy technologies. I know he'll be a valuable Member of the Committee. And he's learning the joys of our Wi-Fi and logging in on a web meeting right now, so it's a character-building experience. Thank you for joining us, Mike, and thank you, Madam Chair, for that.

Chairwoman JOHNSON. Well, thank you. Let me just welcome you say that you're joining the greatest Committee on the Hill. Thank you.

Mr. CAREY. That's what I've heard.

Mr. LUCAS. And the Chairwoman——

Chairwoman JOHNSON. Mr.——

Mr. LUCAS [continuing]. Is absolutely correct.

That said, in the remaining year of the Chair's time, we're going to work her really hard as we accomplish great things on this Committee.

Now, that said, Dr. Kelleher and Mr. Bhatia, as I mentioned in my opening statement, I'm interested in hearing from both of you about the lessons learned, good and bad, from the Federal Government's previous efforts to bolster U.S. competitiveness in microelectronics and its support of SEMATECH. I would also be interested in your insights on how IMEC is successful and where it may fall short. In other words, what characteristics of these programs should we consider adopting for the NSTC and other chips programs? And what should we avoid? Let's talk about the lessons we've learned.

Dr. KELLEHER. And maybe I will start with—I'll start with IMEC because I myself worked at IMEC earlier in my career, so I have firsthand knowledge. I have a lot of respect for IMEC and the work that it has done and its ability to make itself self-sustaining over the years and the work that it has done enabling for the basically research not just for Europe for worldwide.

I think one of the key learnings from IMEC is IMEC works in the research in its precompetitive space, and that precompetitive space enables it to do the early research that feeds into the overall industry as a whole. It feeds—it's in parallel to some of the universities, but it also feeds into the overall—basically the ecosystem as a whole. It—that precompetitive research goes to semiconductor fabs, and it goes to work with the equipment vendors and the material vendors, so basically it's quite strong.

I think one of the key things is we have a lot of basically discussion on how does one get access to prototyping, et cetera. IMEC is not a model that's set up for prototyping. IMEC is very much on the precompetitive space. So I think as we go forward at least one of the lessons learned is how do we take the equivalent of working with the research institutes and working with—for precompetitive space and funding that, as well as taking it further down the supply chain in terms of how we set up so that we enable prototyping and eventually enable turning that product into basically leading-edge products here within the United States.

I think I will let—given I'm consuming time, I will let Manish take SEMATECH.

Mr. LUCAS. Please.

Mr. BHATIA. Sure. Thank you, Dr. Kelleher and Ranking Member Lucas.

As you mentioned, when SEMATECH was founded almost 40 years ago, there were more than 20 American companies who were doing leading-edge process technology development, as well as manufacturing. And today, you know, really the two companies on the panel are the ones who are doing that left in the United States.

So the SEMATECH model, while it's served its purpose for a prior era, you know, a replication of that would not necessarily provide the same benefit that it did now because really Intel and Mi-

cron are the two companies that are doing leading-edge process development research and leading-edge manufacturing among the U.S. companies.

With regard to the—you know, what the focus for this Committee can be to help fill a gap that exists, we agree with Dr. Kelleher's comment that while focus on university research, as well as the national laboratory network has been—have been excellent programs and continue to be vital areas for long-term foundational research and those, you know, do need to have funding increased to be able to maintain our status as the leading—as leadership around the world, this transition from the labs of those national labs or of those universities to the fabs that we operate is the area that we can help to bridge with the National Semiconductor Technology Center's approach.

And rapid prototyping of new technologies to accelerate the time from their demonstrated feasibility in laboratories, in university or national lab environments until they can be commercialized and ramped at scale in high-volume manufacturing, this is the area that we should—we see as a primary focus for the funding for the NSTC.

Mr. LUCAS. Dr. Chiang, I want to thank you for your comments on the need to build a work force to meet the demands that will come from a growing domestic semiconductor industry. And I'm—especially appreciated your comments on the need to train technicians and production workers. Like Indiana, which has Ivy Tech, Oklahoma has a remarkable program with CareerTech. Tech schools and training offer a tremendous opportunity to train, reskill, upskill America's work force. Can you please elaborate on how Purdue is working with Ivy Tech to develop work force programs focused on skills needed by the semiconductor industry and how that potentially could serve as a model?

Dr. CHIANG. Thank you, Ranking Member Lucas. I would be—first of all, again, mic check if I'm still all right with the volume. All right, fantastic.

Mr. LUCAS. I can hear you.

Dr. CHIANG. All right. Thank you. Indeed, it takes a whole partnership. No university by itself can fulfill the whole spectrum of needs. It takes partnership. And I highlight three partnerships. One is, as you mentioned, Purdue University has been partnering with Ivy Tech, which is our statewide community college system with over 70,000 community college students. And we also have started deploying a new set of degrees and credentials, including a dedicated degree at the master level for semiconductor supply chain, from the material and the gases needed, to the hardware tools needed to the manufacturing and the design and eventually to test, assembly, packaging. And third is the use of online learning to share these new spectra of curricula with other learning institutions.

And under President Mitch Daniels, Purdue University's leadership, Purdue Global, and Purdue Online for the West Lafayette main campus have rolled out a wide variety of online learning certificate opportunities so that even those who are in the work force today wanting to upskill or those who are remote learning and not

able to attend the university within Indiana will be able to benefit from these results.

Finally, I will just comment also how the industry and academia can work together even in the education space. It takes more than just recruiting but also actively participating in the design of these curricula and providing hands-on learning internship opportunities and providing work force training for their own employees through our online degrees. And these cut across the bachelor degree and associate degrees, as well as more advanced degrees, so that it's not just universities generating the supply of talent but truly industry and universities working together to design the curricula and to educate the work force together.

Mr. LUCAS. Thank you, Doctor. And thank you, Chair, for indulging me on the time. I yield back.

STAFF. Ms. Bonamici is recognized.

Ms. BONAMICI. Thank you so much, and thanks to the Chair and Ranking Member and our witnesses. And before I turn to my questions, I just want to acknowledge the Chairwoman and her recent announcement. Chairwoman Johnson, it has been and continues to be an honor serving with you and your leadership, and I'm looking forward to a very productive upcoming year before a more formal farewell.

It's clear that we have a lot of work to do to expand and preserve the role of the United States as a global leader in semiconductors. It is also clear that we need to swiftly provide funding through the *CHIPS Act,* as both the Chair and the Ranking Member have mentioned, to help reinvigorate our Nation's semiconductor industry.

And we've all heard about the semiconductor shortages, primarily pandemic-induced, disrupting countless sectors across the global economy. In the district I represent, which is often referred to as the Silicon Forest, is particularly vulnerable to these supply challenges. Thousands of my constituents, more than 40,000 Oregonians, currently work in the semiconductor industry, so there's tremendous potential for that number to grow.

And I want to note that every witness here today raised work force issues. Workforce readiness is a major limitation to expanding U.S. semiconductor leadership. And as a Member of the Education and Labor Committee, this is something that I care about deeply.

So, Dr. Kelleher, nice to see you again. Thank you for joining us. What on-the-job training program does Intel offer to prepare its own work force? And, as an industry leader in semiconductor employment, we're really interested in your opinion about what steps Congress could take to boost the industry's work force pipeline.

Dr. KELLEHER. Thank you very much for the question, and it's absolutely my honor to talk about work force development because it's very near and dear to my heart. When I was leading the manufacturing organization, it was also very important to me.

I was—the span of work force development covers—it covers an entire span within our factories. It covers the span from skilled technicians to operators right up to the most advanced researchers we can hire. Equally well we're building factories, and the entire trade availability and the entire trade skill is basically—is a declining skill and there's a shortage within the trade community. So I would say this entire semiconductor industry, the skills that needs

to be grown goes anywhere from in the construction industry to support the building of our factories right up to the most advanced researcher.

Within Intel ourselves we have quite a lot of training programs. We have in-house training programs where we—as we hire our technicians, there are in-house training on the equipment and a whole—and associated training to get them up to a certified level. We hire quite a lot from the military, and employees we hire from the military come to us with a really good standard, and that makes that training basically easier.

And we also work with the universities and the colleges, and over the years we have done many programs with the colleges that actually get the programs and the specifics that we need in—and is—some to train for folks we've already hired, to set up classes and to set up training programs so that we can hire from those.

So across the board I believe there needs to be a generic, I would say, focus and look to go anywhere from our supply into construction to enable us as an overall industry to build our factories.

And also with the universities and with the—I would say the less skilled aspect of it, but there is no low-paying job within the semiconductor industry. They're all skilled jobs. So——

Ms. BONAMICI. Thank you. And I'm sorry, I don't mean to cut you off. I just want to squeeze in a question real quickly for Dr. Witherell. Thank you for that comprehensive answer, which was really helpful.

Dr. Witherell, according to your testimony, the microelectronics energy consumption is projected to increase from 5 percent of the world's energy used today to 25 percent by 2030, which, of course, is a significant increase. And you recognize that research addresses challenges falls squarely within the DOE's mission. So what efforts are underway to research how to reduce energy intensity across the semiconductor supply chain? And do you have any examples? Thank you.

Dr. WITHERELL. Well, we are working on new materials and new devices to break through that energy barrier in semiconductors, and that's something that's actually squarely in the energy space of the DOE laboratories but also it's in the science and technology space, and so that's why we're putting that in the lead.

And the important thing is actually having—for this proprietary research to be doing in the labs but closely tied to what the industry is ready to do. And that's why these continuing public-private partnerships are important.

I also want to—as another example of that, Princeton Plasma Physics Lab is working on plasma processing with industry and academia for processing, which is another important thing I didn't have the time to mention in my testimony. So taking advantage of these existing partnerships is the way to get faster movement from the DOE laboratory into industry, which is what I think we're hearing about.

Ms. BONAMICI. Terrific, thank you so much. I'm out of time and yield back. Thank you, Madam Chair.

STAFF. Mr. Babin is recognized.

Mr. BABIN. Thank you, Madam Chairwoman Johnson and Ranking Member Lucas, and thank you to the witnesses as well for being here with us today.

Demand for semiconductors is at an all-time high, which is a trend unlikely to ease off for the foreseeable future in our country's evolving reliance on digital infrastructure. From smartphones to our defense technologies, semiconductors continue to play a critical role in our country, and investing in this industry should be a high priority for us.

Texas alone has seen several investments made in the semiconductor industry this year with Samsung announcing just last month a $17 billion investment for a new facility in Taylor, Texas, not in my district but I'm proud to have them in Texas, one of the biggest investments we've seen in many long years, maybe the largest.

It's important that we pursue American competitiveness in this industry. We recognize the role of partnering with companies abroad which are important players in our supply chain. So, Dr. Chiang, in your written testimony, when evaluating the semiconductor supply chain, you mentioned the three P's: protect, promote, and partner. Recognizing the importance of focusing on these key aspects of the supply chain, would you please elaborate on how the United States can best leverage our valuable taxpayer dollars with our allies to ensure the United States remains a leader in the global market? And how do we continue to encourage investments in the future in domestic growth and in American jobs?

Dr. CHIANG. Thank you very much——

Mr. BABIN. Yes, sir.

Dr. CHIANG [continuing]. Congressman, for the three P's, usually people are referring to public-private partnership, which is certainly important. Now, I was referring to the three dimensions of protect, promote, and partnership. And on the partnership front, we have to recognize that it helps for the United States to onshore like-minded nations' private-sector success. For example, Congressman, you just highlighted Samsung for careers investment——

Mr. BABIN. Right.

Dr. CHIANG [continuing]. Into Austin in Texas. Congratulations. And of course we——

Mr. BABIN. Thank you.

Dr. CHIANG [continuing]. Saw in May 2020 TSMC, Taiwan Semiconductor Manufacturing Company, one of the largest, the leading-edge manufacturer of semiconductor chips coming to the United States to Arizona. And we have other like-minded nation partners in the design space such as MediaTek, also from Taiwan, and we just mentioned some of the partnership with European countries as well. I think it is of utmost importance to encourage these partners to come to the U.S. shore, to create jobs in America, to produce results and intellectual property in the United States, and also to work with American companies both to create jobs for our students and to help us to train such students. And here at Purdue we're proud to work both with companies such as Intel and SkyWater and other American-headquartered companies, but also with companies such as TSMC and MediaTek.

Mr. BABIN. Right, thank you so very much.

Dr. Chiang, you also mentioned that the United States is the largest end-user of semiconductors in the global market but yet the U.S. share of semiconductor global fabrication is only 12 percent, a very low number. And, Dr. Kelleher, you highlight the same shocking percentages in your written testimony and going on to highlight the danger of losing our ability to make advanced chips in the United States. So, both of you, if you please would elaborate on what you see as the biggest threat to our semiconductor supply chains.

Dr. KELLEHER. Our biggest threat in terms of our semiconductor supply chain is our ability to continue to, I would say, invest and grow and keep that advanced leading-edge R&D and IP growing within the United States. We are at a fundamental disadvantage compared to some of the Asian countries when it comes to basically developing and manufacturing our chips, so if we lose our ability to actually continue to maintain that leading-edge manufacturing, it means that, as a supply chain, we're completely reliant on the rest of the world. And I don't believe that's a good place for the United States to be.

Mr. BABIN. No, ma'am. And, Dr. Chiang?

Dr. CHIANG. Thank you, Congressman. I agree with Dr. Kelleher's assessment that indeed we need to make sure that the entire supply chain is secure. That includes gas and materials needed, including rare-earth minerals. That includes the tooling companies. We have companies such as Applied Materials here in the United States, and Tokyo Electron, both work with Purdue and the State of Indiana. And that includes the manufacturing companies, as well as the chip design companies. And even more depressing numbers can be found when it comes to the final step, advanced packaging. We need to onshore or re-shore a lot more on the packaging front as well.

Here in the State of Indiana, Governor Eric Holcomb, and the whole team here have been trying to increase the presence of packaging, as well as manufacturing facilities. Some of that is upgrading existing ones in universities such as Purdue's Birck Nanotechnology Center and the nanoHUB virtual learning platform, and new ones.

And I would wrap up this brief comment and answer by highlighting the optimism that I have that, as somebody once said, never short on America and the Americans. The ingenuity and the creativity of our universities and companies and government labs is truly second to none. And as long as we continue to look forward to the most innovative R&D ideas and run faster than we have ever run before, then there is no limit as to what American ingenuity can do.

Mr. BABIN. Great. Thank you both so very much. And I yield back, Madam Chair.

STAFF. Ms. Stevens is recognized.

Ms. STEVENS. Dr. Kelleher, what can you tell me about the origin of semiconductors, given the company you work for and who your founder was, Dr. Gordon Moore?

Dr. KELLEHER. Well, let me start with just Gordon Moore, Robert Noyce, and Andy Grove are the three founders of Intel. Intel was

basically incorporated in 1967, 1968, so we're well over 50 years old as a company.

So semiconductors basically are the essence—and I speak very much for transistors right now and not memory—the essence of semiconductors is basically a switch. The essence of this switch is you can switch it on or off from a silicon perspective. And the combination of all of these transistors put together enable circuits to get designed, which ultimately are able to do computation analysis and very complex analysis. And as we progress over time, we're moving into the artificial intelligence space where there's overall trading in workload.

So over the years with the industry when it started, it was—basically we were working with very large dimensions. And not today when we look back we're not complex transistors, nor were they really large or complex designs, probably were viewed like that at the time but today when we look back, as we progressed over time, the nature of the semiconductor to make as we continue to advance on the Moore's Law scaling so that approximately every 2 years we're doubling the amount of transistors so that you can fit in a chip.

Ms. STEVENS. Right. And Dr. Witherell would know that—just pardon me on this front—because he would know that—Dr. Moore—and I know he wasn't the exclusive founder of Intel—was at the university level and then broke off, wasn't—was working for a semiconductor company and then joined to—you know, with his colleagues to form Intel. And it's quite inspiring, Intel and Micron. Mr. Bhatia—you also represent a very large employer, and we're very inspired by your companies, and we're inspired by the employability, the R&D.

The question is—and Mr. Bhatia touches on this in his testimony—is that at one point, right, we were innovating, we were inventing, we were creating these incredible enterprises of scale, producing in this country 40 percent of chips. And I come from Michigan and we've got an auto sector that relies on this, and we're at 12 percent today. And Mr. Bhatia talks about this, that, you know, it costs 35 to 45 percent more to have chip manufacturing in the United States. Why? Why? Why—can you—how do we make this more competitive for you? How do we compel you—because it's not just a feel good, right? It's not a cute thing to say, oh, we like manufacturing in this country. This is our bottom line. This is our economic competitiveness.

We have an EXIM (Export-Import) Bank in this country that gives us a platform to trade globally, to export. Many years ago—some of my colleagues might remember this who were here. This is on the other side of the aisle. They were going to get rid of the EXIM Bank. They were going to get rid of the EXIM Bank. And industry said, well, gosh, we won't be able to compete. Now here we are, the tide has rolled out billions and billions of loss of profit, losses of jobs. How do we bring it back? What do we need to do to bring it back here, get people back to work, and increase our production capabilities in the United States for semiconductors?

Mr. BHATIA. Well, Representative——

Ms. STEVENS. Go ahead.

Mr. BHATIA. I'm sorry, was that for—was that question for me?

Ms. STEVENS. It can be for you.

Mr. BHATIA. Sure. Sure.

Ms. STEVENS. I mean, everyone had a brilliant testimony.

Mr. BHATIA. Sure.

Ms. STEVENS. I mean, really, these testimonies were incredible.

Mr. BHATIA. So, Representative Stevens, thank you for that. I'll touch on that, and then I'll let—you know, let other panelists.

You know, to answer your question, the 35 to 45 percent cost gap to build and operate large-scale semiconductor manufacturing facilities between lower-cost regions in Asia and the United States is really comprised of three elements. The first is labor costs both for operating the fabs but also for construction of these fabs. These fabrication facilities, each one will cost multiple billions of dollars just build the clean room facilities before we even start to equip it. And then with equipment they become above—more than $15 billion for each individual site. So the labor costs for both the construction and the operation is the first element.

The second element is really the scale of the facilities. Over the last 20 years, Asian countries have had focused policies to be able to grow the ecosystem, to grow semiconductor manufacturing, particularly from memory into larger and larger scale. So when we're starting from small-scale or in some cases no scale, the economies of scale that are enjoyed in Asian countries because of the investment over the last 20 years drive a substantial cost gap as well.

And then the third piece is the government incentives that are there. And we believe that the *CHIPS Act* and a refundable investment tax credit that has been introduced and proposed, these are the right first steps to be able to try to reverse this trend and make it more cost-competitive for U.S. integrated device manufacturers to build large-scale semiconductor manufacturing facilities.

And the other point that you mentioned about jobs is very important. Each of these facilities require—create thousands of high-paying, high-value jobs whether you're talking about scientists in the labs or engineers operating the fabs or skilled trades operating this high-precision equipment and these very, very exacting and demanding clean room environments at facilities, these are high-paying jobs that are—that create long careers and improve the quality of lives for every one of the communities where we operate. So investing in the future in semiconducting manufacturing has benefits both economically, as well as in the local communities and their quality of life.

Ms. STEVENS. Well, I'm egregiously over time, but, Dr. Witherell, we're going to do—and, Dr. Chiang, we'll do QFR (questions for the record), you know, we'll do a question for the record because the public-private partnership component here is also incredibly imperative.

Thank you. I yield back.

STAFF. Mr. Gonzalez is recognized.

Mr. GONZALEZ. Thank you, Mr. Chair and Ranking Member Lucas, for holding this hearing and to our witnesses for joining us this morning.

I want to take a brief moment to thank Chairwoman Johnson for her leadership and commitment to our Committee over these many years. I've been a Member for 3 years now. I've announced my re-

tirement for a lot of reasons, one of which is this place just operates like a—I don't know, junior high is probably generous in many respects—with the exception of this Committee. And this Committee operates, and this place operates in large measure on the cadence of the leadership. As leadership goes, so does Congress.

And my belief is that this Committee is so effective because we have such effective leadership. And that starts with Chairwoman Johnson and Ranking Member Lucas. And so I am enormously grateful for her service. And I'm sad to see her go, but it's much earned, and she has certainly served our country and her district incredibly well. We will miss her.

But I'm cautiously optimistic—I'm very optimistic that whoever takes over in the coming years will carry on the tradition because we've been effective and we need to be effective as nothing more important from an economic development standpoint in my opinion than reshoring our semiconducting manufacturing.

I'll start with Mr. Manish Bhatia. You were just talking about these facilities, and I want you to kind of go a little bit deeper and give us a sense of the scale. When a new fab is produced, when we come and say, OK, we're going to make major investments in a community and increase our manufacturing, what does that look like from an economic development standpoint? Think of a—and I'm from Ohio. Think of a town in Ohio and what that—those sorts of things can mean, what those sorts of investments can mean for individual communities.

Mr. BHATIA. Sure. Thank you, Representative Gonzalez, and thank you also for your service.

The—you know, as I was starting to stay before, you know, to operate a large-scale semiconductor manufacturing facility requires thousands of employees of the manufacturer, whether they're engineers who are developing process or maintaining the process, managing the yields and the quality levels and the productivity through the fab who will also have almost an equal number if thousands of jobs of indirect employees who are on the site every day, whether it's to continue with construction or installation of this high-precision equipment, maintenance of this high-precision equipment, installation and maintenance of the specialized chemicals and gases that we need to operate the clean room or to manage the processes on the floor or to just operate the overall facility. So we're really talking about thousands of direct jobs that are employees of the manufacturer and then thousands of employees who are onsite that are from the contractors or the equipment companies or the chemical and materials companies.

And then you have the support in the community for those large-scale manufacturing operations. We believe that this—that, you know, that those thousands of jobs have a 3X multiplier in the community to be able to support these large-scale investments. As I mentioned, a single fab will cost more than—a modern fab today will cost more than $15 billion in capital investment. And when we talk about memory fabs and minimum-efficient scale, single-site facilities are not minimum-efficient scale today. We need multiple fab clusters similar to those that have grown up in Asia to be able to be cost-competitive. And so you're really talking about massive, long-term, decades-long investments that can prop up entire com-

munities and can improve the quality of life whether we're talking about high-paying jobs but you're also talking about the infrastructure in the community, healthcare——

Mr. GONZALEZ. Reclaiming my time just for a second because I only have a minute, but I appreciate the enthusiasm. And I would commit to everyone on—all of our panelists, Ohio is ready. Ohio is ready, willing, and able to support semiconductor manufacturing right now. So we are open for business. Please come. We will provide the incentives. We will do all that we can, I can assure you.

With my final point, you mentioned government incentives and refundable investment. We have to make it more cost-competitive. At the end of the day, the companies answer to shareholders and have to be more cost-competitive.

I'm just going to make a brief comment and then yield back. My Democratic colleagues are considering massive spending in various forms of tax increase through *Build Back Better.* Whatever you do, please, please, please be very cognizant of the fact that if you raise corporate taxes or if you do something to make us less competitive economically, that's going to reverse many of the benefits from the *CHIPS Act.* So buyer beware on that stuff.

With that, I yield back.

STAFF. Mr. Bowman is recognized.

Mr. BOWMAN. Thank you so much. And, Madam Chairwoman, I want to echo the sentiments. Congratulations on your retirement. Thank you so much for showing us the way—or showing me the way as a freshman in terms of how Congress is supposed to work. Thank you for your leadership on this Committee.

My question is for Dr. Kelleher. Thank you for your testimony. Intel is a large, very successful company that made $21 billion in profits last year and spent over $14 billion on stock buybacks. Intel's CEO (Chief Executive Officer) recently acknowledged that stock buybacks have undermined the firm's competitiveness. I believe Intel has been talking about expanding domestic manufacturing capacity for some time now, and it strikes me that you already have the ability to do so. What material impact would Intel's portion of *CHIPS Act* incentives really have? You touched on this earlier, but I wanted to come back to it. Why is a subsidy like this going to make the difference in terms of delivering new, leading-edge capacity in the United States?

Dr. KELLEHER. Well, first of all, I obviously very clearly said we have a lot of commitment to the United States and in terms of our investment in R&D and manufacturing over our 50-year history. This fundamentally, in terms of the *CHIPS Act,* is about enabling us to maintain competitiveness here within the United States.

We are continuing to invest in leading-edge technology development and manufacturing for us to continue to compete effectively and with competition worldwide. The *CHIPS Act* is absolutely essential for us to be able to do that. So I think that is my simple answer to you, Representative Bowman.

Mr. BOWMAN. OK, thank you. I may come back to you if time allows.

I had a question about creating pipelines for young people who want to go into careers in this sector. It was mentioned by a few of the witnesses. I want to focus on—someone mentioned K–12. I

want to focus on the high school setting. What should high school science and technology curriculum look like in order to prepare our students for postsecondary opportunities in these spaces? And I'll start with Mr. Bhatia if that's OK.

Mr. BHATIA. Thank you, Representative Bowman. And it's a personal passion of mine as well. You know, K through 12 is an area that Micron has focused considerably on in the communities where we operate, including Boise, Idaho, where we have our Research and Development Center of Excellence, and in Manassas, Virginia, where we also have tremendous manufacturing capability.

And in terms of K through 12 specifically, we have been working to develop STEM (science, technology, engineering, and mathematics) curriculum starting at a very early age and including being very inclusive to underrepresented groups who normally wouldn't have the opportunity or in the past haven't been able to have the opportunity to pursue a path in engineering or into semiconductor.

So the types of curricula that we encourage are of course around science and math but specifically around data science because the world of semiconductor manufacturing is getting more and more complex, really unlike any other manufacturing process on the planet. And so you really have to have both strong technical knowledge in science and technology but also understanding and appreciation of data and data science so that we can operate these highly complex manufacturing facilities very productively and with high quality and very, very low defectivity.

Mr. BOWMAN. Thank you so much for that concise answer.

Dr. Chiang, can you also jump in and just comment on that, please?

Dr. CHIANG. Thank you, Congressman Bowman. And I would just supplement Mr. Bhatia's answer with two more points. One is that universities also have a responsibility to work with K–12. For example, Purdue President Mitch Daniels started three Purdue polytechnic high schools throughout the State of Indiana, and we just graduated the first class of senior students. These are minority-serving high schools focusing a lot on STEM capabilities.

And second is that there is a mindset of problem-solving at this early age of education. It's not just about how much we cover in the material for high school students, but how much we allow them to uncover for themselves, more about their curiosity and their ability to learn. And that is fundamentally the point of education, especially for engineers. It's ultimately a problem-solving mindset that we can start instilling in their minds at high school age.

Mr. BOWMAN. Thank you so much. Dr. Chiang and Mr. Bhatia, I would like to followup with my office to continue this conversation. This is an issue that's near and dear to my heart. And for me it's a priority for us to create pipelines, K to 12 pipelines in historically underserved spaces. I believe it will take our economy to the next level and ensure that no other country can compete with us because we will finally invest in equitable ways across our country.

Thank you, Madam Chairwoman. I yield back.

STAFF. Mr. Baird is recognized.

Mr. BAIRD. Thank you, and thank Chairwoman Johnson. I want also express my appreciation for your leadership on this Committee. And, you know, I really appreciate you working with Rank-

ing Member Lucas and you stayed focused on the issues that I think are relevant to our Science Committee.

And then I always appreciate the witnesses being here. I am always intrigued by what I learn, and so I am sure that other people feel the same way.

But, you know, earlier this year I offered an amendment that would've allocated about $600 million to the National Science Foundation to support the R&D funding for basic research. Unfortunately, that didn't pass. But I really have a strong affinity for basic research, and I recognize how difficult it is to determine what basic research is important today that down the road becomes increasingly important or provides information essential to our society.

So, Dr. Chiang, I'm going to start with you. And would you mind speaking to the role that basic research and funding for the NSF plays in supporting the development of semiconductors that will be needed for cutting-edge technologies like artificial intelligence, quantum computing, and 5G? So if you would care to address that, I would appreciate it.

Dr. CHIANG. Thank you, Congressman. And thank you very much for your service and leadership in representing our district in Indiana.

Mr. BAIRD. Thank you.

Dr. CHIANG. I would like to echo what you just said, that the National Science Foundation, just like the Department of Defense, Department of Energy, and many other agencies of the U.S. Government, plays a unique and important role in continuing the long tradition of American creativity.

Now, in particular we need a collection of fundamental research often funded through the National Science Foundation, along with translational research sometimes funded through other agencies who work hand-in-hand together. NSF also funds quite a number of scholarships and fellowships, and we need more American students to be interested in pursuing STEM degrees at undergrad levels. And those with undergrad degrees, say, in engineering, would choose to continue to study for a master or Ph.D. degree. I know that they often are tempted by outstanding offers from the industry, such as leaders like Intel and Micron, but also we do want to incentivize and encourage a much larger number of them to stay on and pursue a graduate degree. And the National Science Foundation plays a critical role. And I hope that there will be many more graduate fellowships to a diverse population in this country in areas related to semiconductors.

Mr. BAIRD. Thank you. So, would it be fair to say that one of the things I see from this Committee standpoint and from the Federal investment or taxpayer dollars invested that some of the basic research that's conducting private industry cannot really justify so we could start the needle moving early on and then industry picks that up? We talk about the public-private partnership. Is that—would you say that's a correct analysis of this situation or——

Dr. CHIANG. Yes, sir. And I'll give one concrete example. There is this so-called valley of death coming from fundamental advances into commercially impactful deployable solutions. And one way to bridge this so-called valley of death is to create and upgrade exist-

ing facilities, for example, in semiconductors. We talked about two dimensions. One is the dimension of the feature size, and it's getting smaller and smaller down to 3 nanometers these days. And the other is the size of the wafer. And we are looking at 8 inch or 12 inch. And we have a substantial lack of 200 millimeter or 8 inch wafer production facilities in American universities. By upgrading some of those, including possibly here in the Midwest but in several regional nodes, that will open up a pathway of translation from fundamental research to industry-relevant solutions.

Dr. WITHERELL. And I'd like to add one thing if I could. That's one of the things that the national laboratory centers do is work on these concepts that are still not ready for commercial production because they're too risky. And by—as long as we're working closely with industry and what they want to do, we can develop in these centers things to take the risk out, and then it's ready to actually move to a profit-making organization.

Dr. KELLEHER. I would like to echo support in that, that the role in precompetitive research is absolutely critical and can feed into industry.

Mr. BAIRD. So, Madam Chair, I see that I'm out of time, but I could go on for another hour here. And I'm sure you don't want that, so thank you. I yield back.

STAFF. Mr. McNerney is recognized.

Mr. MCNERNEY. Well, I thank the Chair. Really, Ms. Johnson, Eddie Bernice Johnson, you've shown tremendous leadership over the years since I've been here. We're going to have a hard time finding a successor to fill your shoes.

But I also thank the witnesses. This is an important issue for the future of our country. And I'm going to take this in a slightly different direction. Semiconductor manufacturing does use massive amounts of both energy and fresh water. We need to increase domestic manufacturing without being susceptible to supply chain disruptions, but at the same time, we have to balance the resources needed by local communities. And this has a bearing on the reliability of the supply chain.

Dr. Kelleher, Intel has a presence in semiarid Western States and broke ground on two new semiconductor fabrication facilities in Chandler, Arizona, this year. Meanwhile, a multiyear megadrought has caused water shortages across the West, a trend that is expected to worsen in the coming decades. What steps has Intel taken to improve water efficiency of the semiconductor manufacturing process and to reduce the impact of the facility on local water systems?

Dr. KELLEHER. So the overall water conservation and reuse of water is a key aspect of all our technology development and within our manufacturing, our overall manufacturing sites. To date we have 90 percent of the water use restored to the environment, and we are heading for a path and we've given ourselves a very clear goal, which we're working toward to be—by 2025 100 percent restoration to the environment. By 2030 we're aiming to be a net positive. We do—not only do we do a significant amount of work in our facilities in terms of water reuse, we also work with the communities in terms of water restoration. And we've had—we have sev-

eral projects in the Arizona region where we've been working with—overall with the communities in terms of water restoration.

We spend a significant amount of money in our facilities to actually help and drive and enable this, so it's a key aspect of our overall development and manufacturing, our footprint—our water footprint, our climate footprint, our use of electricity, and our use of green power. So this is a very important aspect to us.

Mr. MCNERNEY. Well, thank you. And I'd like to see the information that supports that.

Dr. KELLEHER. Absolutely. I will provide it.

Mr. MCNERNEY. Very good. Mr. Bhatia, Micron has the same issues. Would you respond to the same question?

Mr. BHATIA. Sure. So thank you, Congressman McNerney, and agree this is an incredibly important issue for all of us everywhere around the world. And Micron has made a strong commitment, including a commitment to spend $1 billion over the next several years in capital investments to be able to reduce our carbon footprint through emissions program reductions to be able to increase the utilization of renewable energy. In fact, we set a goal to be 100 percent utilization of renewable energy in the United States by 2025. We are working to be able to reach 100 percent water reuse by 2030 on a global basis, and we're also working to reduce waste to landfill in all of our locations around the world as well. So we have a—are very focused in all of these areas.

Mr. MCNERNEY. OK. Well, we need to get to sustainability.

Dr. Witherell, you know, I certainly appreciate the national laboratories. I've been to LBNL and Lawrence Livermore and Lawrence Berkeley labs several times. But I know you are conducting crosscutting research on the causes and impacts of the drought. Have the labs devoted any resources to improving the water efficiency of semiconductor manufacturing?

Dr. WITHERELL. Well, we—first of all, we have the National Alliance for Water Innovation here I should say that's actually working on the reuse of water and how to reuse it for purposes. But in general where we actually are putting most of our priorities is how to develop semiconductors that are more energy-efficient, which is actually the—as the biggest leverage on the environment. And that's something that much of our research is doing at the moment.

Mr. MCNERNEY. OK, thank you. I'm concerned about what happened in Taiwan this last summer when a manufacturing was forced to shut down and tank in water, and that put the whole system at risk. Is Intel taking steps in the U.S. plants to increase resilience against water shortages?

Dr. KELLEHER. Absolutely. We are constantly looking at our water use and working to reduce our water use and overall reuse of the water that we use. So yes.

Mr. MCNERNEY. OK, thank you. And I'll yield back.

STAFF. Mr. Webster is next. You're muted, Mr. Webster.

Mr. WEBSTER. Thank you, Chairman and Ranking Member, for putting together this forum. This is really an excellent dialog and also just in the review we're doing some of the things that have already passed. I know the—understand to build a foundry is about $10 billion. Then I heard later here on this panel that it's maybe $15 billion more, and that's getting into real money. And so I would

ask you, Dr. Kelleher, if you could kind of elaborate on what you think is the maximum amount we could do with the money we've given to this program that we could do as far as foundries? And are you also in agreement with what was said before, that the sub foundries are scattered around would be an even better way to do it? Is that true?

Dr. KELLEHER. Well, first of all, I agree with the numbers, and I know my—speaking about the numbers was building the facilities, it's anywhere $15-$20 billion, and the amount that's spent on a given facility obviously is very much dependent on the size of the facility.

Overall, Intel is—we've been very clear we're opening our fabs up for foundry here within the United States, and we're opening up for overall from our foundry so that we can open up the use of our fabs to basically the fabless designer—the fabless companies so that we can make foundry available here within the United States.

I think overall I would go—take us back into the two pieces of where we spend our money within—from the *CHIPS Act.* I think we have to focus on R&D in terms of enabling our future because that is the long haul, and that's the long building of our future. And then there is the building of our overall U.S. manufacturing capability. And that I believe we need to continue to do. If you diverse—if you spread the money too much, then you actually won't end up getting, I would say, an overall effective bang for the dollar. But it becomes the appropriate and spreading of that money so that we can overall grow our foundry industry here within the United States and keep moving our leading-edge R&D.

Mr. WEBSTER. Yes, well, would that—would these foundries be focused on advanced semiconductors?

Dr. KELLEHER. Intel is focused on advanced semiconductors. Back in July I released our overall roadmap for the—for our—the next 4 to 5 years, and these technologies within Intel are available for—as foundry technologies. And yes is the answer.

Mr. WEBSTER. Yes. I've always been an admirer of Intel, and I thought it was interesting—how do you know which direction to head? I mean, there's a lot of directions that can happen. How do you focus in on just the amount you would play in or the amount—the few amount that you—the ones you would have?

Dr. KELLEHER. May I clarify the question? When you say how do we focus in, how do we focus in from a technology development or is it a broader question?

Mr. WEBSTER. No, it would just be the technology component.

Dr. KELLEHER. So there is—well, there are many aspects in terms of feeding the overall pipeline from the technology. There is the long-term 5 to 10 years out. There's a lot of items which are in the pipeline. We do research internally with Intel, but there's also research done in the universities. Slowly, as you progress over time, there's a filtering out in terms of which are the more likely candidates that would be successful for the future. And out of that filtering then there is—it's proven at the first level of concepts. Then we take it into development. And in that development we actually prove out that we can take it from the lab to fab concept, and that would be enabled for high-volume manufacturing. So it's a 5- to 6-year process in terms of going from the concept of an idea

to actually showing up in terms of a volume manufacturing. And sometimes it can be much longer than that depending on the aspect of the technology that is being developed.

Mr. WEBSTER. OK. So the—so you would be developing a component of a machine of some sort, i.e., a minicomputer or something like that. You would not be developing something for someone else who's building it. You would be developing something and someone else would use it. Is that——

Dr. KELLEHER. Correct. Correct. We develop chips, and we sell packaged chips, packaged designed to other customers, who then use those packaged chips, basically microprocessors, to build other products. Similarly, memory goes into those packages as well and goes into those products. So we're providing either wafers to our customers to the foundry or packaged products—packaged microprocessors to our other customers.

Mr. WEBSTER. OK. It just sounds like it's billions of dollars to build, so there's this cost for building these foundries, but also I assume it takes time to do that, and we may not have that time. Is there ways to take existing infrastructure and sort of meld them into this process so that we use the facilities we have but also are building new foundries at the same time?

Dr. KELLEHER. I think time is of the essence, but one of the key things that I said in my testimony is that I believe we should use existing infrastructure within Intel, Micron, within the other U.S. semiconductor companies so that we can shorten the time to get—and basically reduce the cost. And thereby, then, if we do big challenges across, as a number—as—across the industry here in the United States, using as much as possible of our existing infrastructure, that will allow us to get to results faster.

Mr. WEBSTER. Thank you very much. I yield back.

STAFF. Mr. Tonko is recognized.

Mr. TONKO. Thank you so much. Chairwoman Eddie Bernice Johnson, thank you for the strength that you've brought this Committee. I for one appreciate your leadership style and your accessibility to myself and our colleagues. It's just a good strength and a very important Committee, and you've led it masterfully, so thank you. And I look forward to the next year where we can continue to get good things done.

So I thank you and Ranking Member Lucas and our witnesses for joining us today for this very important hearing. The United States has long been a global leader in the research and development of semiconductor technology. In fact, New York's capital region that I represent has been home to trailblazers in this industry for now over 2 decades. So partnerships amongst our academic institutions, our regional industry, and government have enabled major breakthroughs in innovation in microchip technology. As our reliance on microelectronics in everyday life grows, it is critical for us to leverage strategic investments across government and industry to sustain our Nation's long-term economic and manufacturing competitiveness.

You may be aware that this Committee is currently examining ways to elevate DOE's role in the national microelectronics R&D effort. I'm working on legislation that would leverage DOE's capabilities, including the national labs and their partners in industry and

academia, to tackle foundational challenges in the scientific areas relevant to microelectronics. Such an effort would be separate from but complementary to National Semiconductor Technology Centers and would involve a broad-based research program, as well as a more focused center-based effort akin to the National Quantum Centers.

With that being said, Dr. Witherell, would you support such an approach?

Dr. WITHERELL. Yes, Congressman, thank you very much for your question. And say that if you look in my testimony, it makes many of the points that you bring up in the *MICRO Act* and so—which has—so I very strongly support that, especially the foundational role that DOE and the laboratories have in developing these underlying sciences and engineering that underpin our development.

And Dr. Kelleher said the right thing before. The advantage to the United States is to move faster than the other countries. That's the only way we're going to win this. We're not going to win it by beating them at bulk manufacturing. It's to be faster. And part of that faster is getting back to where the investment on the Federal side was more in keeping with the large investment on the private side so that we could engage this in the right way and do the precompetitive things that are best done in national laboratories and for the industry.

Mr. TONKO. Well, thank you. And the expertise that's housed at the national labs, if we could focus on that, what can that expertise contribute to our national effort to leading in microelectronics development and production?

Dr. WITHERELL. Well, let me take a—one example. We've been bringing artificial intelligence to use for advancing science faster, how you accelerate the cycle of trying new materials, see what works, and do it. You can do that faster in artificial intelligence than you can do it in the laboratory at times. So we have a materials project, which is designed around actually sorting through materials and seeing which are the ones that have the right properties faster than we've been able to do it in the laboratory. We have many examples like that.

Mr. TONKO. And how would you see this feeding into an effort like the NSTC, which would presumably be more focused on later-stage technology development?

Dr. WITHERELL. And I think the role, for example, DOE centers in this is getting through concepts faster to take the risk out and see which are the ones more promising for developing to the scale that you would have at an NSTC facility. You have more ideas feeding into that central facility.

Mr. TONKO. Thank you. And can the Department of Energy play a complementary role to advancing microelectronics R&D?

Dr. WITHERELL. Well——

Mr. TONKO. And——

Dr. WITHERELL. Yes, go ahead.

Mr. TONKO. I was going to encourage anyone else to offer comments, too, but let's hear from you.

Dr. WITHERELL. Well, I do say we have this longstanding connection with the industry and how does—how to best serve their pur-

poses, and I think it's just finding out how to continue that into the new technologies they're developing for the future.

Mr. TONKO. Any other comments from our other panelists?

Mr. BHATIA. I think I'll just echo the comments that Dr. Witherell made that, you know, continuing to have, you know, funding into advanced foundational research through the existing programs with the universities and the national labs, you know, is—you know, is paramount and that we do believe this network of decentralized technology centers can help with bridging the gap from those university and national laboratory environments to mass production by allowing industry consortia to leverage existing resources in the ecosystem to accelerate that time to market.

Mr. TONKO. Thank you very much. Well, I see my time has been used. I don't know if anyone else had a comment. Perhaps you can send it in written format to the Committee.

But with that, Madam Chair, I yield back.

STAFF. Mr. Garcia is recognized.

Mr. GARCIA. Yes, thank you very much. And to our witnesses, thanks for taking the time, very educational and enlightening. Obviously, we have a challenge on our hands.

My first question is geared toward Dr. Kelleher and Mr. Bhatia. For your respective companies' chip sector or chip divisions, what percentage of the bill of material for your products is coming from China? Dr. Kelleher, you can go ahead and——

Dr. KELLEHER. I will start with the majority of our manufacturing is in the United States.

Mr. GARCIA. Yes, the manufacturing I understand. What about the bill of materials? Where are we sourcing products whether it's rare-earth material or any sort of elements that buildup to your larger assemblies?

Dr. KELLEHER. We source our rare-earth materials and our resources worldwide. The precise percentage I would need to followup with you on.

Mr. GARCIA. I would appreciate that. I think that's important for us as a nation to understand what level of dependency we have in this very critical—what's effectively an Achilles tendon right now in terms of technology and capability. We have to characterize what percentage of the bill of materials is actually also coming from China.

Mr. Bhatia, do you have any idea from a Micron perspective?

Mr. BHATIA. Sure. Sure, so I'll echo that, you know, rare-earth materials, as you point out, are an area of weakness in the global semiconductor supply chain. We do also, as Intel does, source those globally. However, there is, as an industry, a strong reliance on China for those rare earths. So it's not so much the percentage of the bill of materials, but they are essential elements for many of the semiconductor processes. And so we have been actually working with members of the U.S. Government to encourage programs that would allow for exploration and mining and economic incentives to encourage production of rare-earth materials to be done in other areas around the world to increase the supply chain resiliency of those.

With regard to your other question in terms of the total bill of materials in China, I will have to get back to you. I would just say

that the semiconductor manufacturing bill of materials is largely driven by the equipment and the precision and the specialty chemicals and gases, so that's not so reliant on China other than these rare-earth materials. However, assembly and packaging, those other lower-value-added portions of the manufacturing process, those are areas where China has a large role. But there are multiple other areas where we source those packaging materials from across Asia.

Mr. GARCIA. OK. Thank you. And let me just clear, I'm not asking this, you know, to point fingers or to attribute fault, but I do think that with—just like any other major problem we have, the first critical step is self-awareness and characterizing where our weaknesses are. So I would appreciate if you guys could followup with a sort of bill-of-material breakout by whatever metric, whether it's cost, just part, assembly, percentage or, you know, weighted dependencies by country, though, if we can, just to get a sense of where we are dependent, especially with regards to China.

My other question for the two companies as well is what percentage of your revenue in this sector is coming from military applications versus just commercial applications?

Dr. KELLEHER. Well, I will need to followup with a precise number in that. We do support the U.S. Government in certain projects, and I will need to followup on that but over——

Mr. GARCIA. OK. Thank you, Doctor.

And, Mr. Bhatia, any idea on yours?

Mr. BHATIA. I'll have to followup as well. We certainly——

Mr. GARCIA. OK.

Mr. BHATIA [continuing]. Do support the U.S. Government. And we do see that memory, both the DRAM and NAND, are increasing portions of military applications, as they are with multiple other industrial and automotive applications. As well the bill of materials portion of those systems, advanced systems or advanced products continues to grow with regard to DRAM and NAND flash technology.

Mr. GARCIA. OK. Yes, because I think it's very—it's critically important that while the big companies and the big folks in the room are going down range with this overarching chip challenge, we can't forget that there is also a military application to a lot of these things that have different requirements. And while you're receiving government funding for things like the foundries and the R&D that goes into it, you need to have still connective tissue to other government agencies like DARPA (Defense Advanced Research Projects Agency), IARPA (Intelligence Advanced Research Projects Activity), you know, ARL (Army Research Laboratory), NRL (Naval Research Laboratory), to make sure you're baking in those requirements into your early design and then also partnering with small companies that are specializing in these applications. And there are several out there, happy to get you a list of those if you don't already have them. But we can't do these massive investments only to solve the commercial problems and then realize that we are still extremely vulnerable on the chip applications on the military side. And I think you guys will all agree with that. I think we've just got to synergize across multiple agencies and the small companies as well.

With that, I'm out of time. I yield back. Thank you.

STAFF. Ms. Wild is recognized.

Ms. WILD. Thank you so much. I appreciate this hearing and the opportunity to elevate an issue that affects workers and businesses in my district, which is Pennsylvania 7th, the Lehigh Valley of Pennsylvania. My community is home to many, many manufacturers, and I hear regularly from companies in a range of sectors about how the shortage of chips such as has been discussed today is affecting their production and their ability to regularly schedule workers.

One auto manufacturer, Mack Trucks, has faced production interruptions this year and unneeded complication. And, by the way, they have plenty of demand. It's not for lack of demand. But it's been a threat to some of their innovative work in spaces like zero-emission heavy-duty trucks, exactly the type of advances we want America to lead in.

We know the drivers behind this supply chain crunch are varied and largely connected to the pandemic, and I was proud to support the *CHIPS Act* last December. But a year later here we are. We need again to take bipartisan action on this urgent need and provide the appropriations for this law that the Senate has moved, as well as address some specific needs like automotive-grade chips. It's about the American economy, it's about good-paying jobs across industries, and is about our national competitiveness and security.

So with that said, my first question is for Dr. Chiang. In your testimony you discuss some specific partnerships on microelectronics in Indiana. We have spent some time in this Committee discussing geographic diversity of innovation. In July the Committee reported out my bipartisan *Regional Innovation Act,* and we are working to get that enacted as part of a larger competitiveness package. But that bill was technology-neutral. What do you see as the role of the microelectronics in the geographic diversity of innovation?

Dr. CHIANG. Thank you, Congresswoman. Indeed, the time to act is now. There is a sense of urgency, and this is key to our national security, economic security, and job security because many other industries in the digital economy depends on the access to chips. Otherwise, they will be furloughing employees whom they would happily be otherwise paying overtime.

And I also highly appreciate, Congresswoman, your highlighting the importance of being inclusive across different communities and diverse in the geographic locations. What we need in education and in R&D is a distributed network of many different parties. Here in the Midwest, for example, in my home State of Indiana, we have an abundance of customers, including automotive and medical, electronics industry.

We also have an abundance of a work force that still retains the manufacturing DNA. These semiconductor fabs, they are fancy, expensive, important factories. They are the factories of the future, and we have the manufacturing DNA in spades in Indiana.

And thirdly, if you look around, the drivable 5-hour distance from where I am right now in West Lafayette, Indiana, you will see an extremely high concentration of high-caliber universities, as well as community colleges, serving an incredible number of Amer-

ican students. So, I believe that, yes, we should emphasize on the inclusivity and the diversity of geographic locations to make sure that all parts of America get to benefit from and contribute to the resurgence of semiconductors.

Ms. WILD. Well, you must've read my mind. My district is one that is rich in higher education. We have six 4-year colleges with graduate programs. We have two unbelievable community colleges. And one of the things I'm particularly interested in is knowing how universities and community colleges can partner with States and local industries to capitalize on regional strengths so that we can contribute to the domestic microelectronic supply chain. I'd like to know whether you or anybody else on the panel would like to comment on how universities might go about doing that.

Dr. WITHERELL. Let me say one thing, that the user facilities at the national labs—I'll take Brookhaven National Lab as an example in New York where you have these nanoscale centers, they are user facilities that work with every university in the country in those providing—in some cases providing facilities that those universities can't themselves afford and make that available so these university researchers can develop their skills.

Dr. CHIANG. I concur with Dr. Witherell, that there are facilities such as the Birck Nanotechnology Center, which has the largest and cleanest clean room among all American universities here at Purdue. If we could upgrade it to be producing at the 200 millimeter scale of the wafer and open that up as a hub, a regional hub for other universities, for community colleges, and for industry partners to come together, that would become a very effective bridge for the country and for the region between the work force I mentioned and the R&D translation dimension of the problem.

Ms. WILD. Well, thank you for that. I'm out of time, but I'm going to ask my team to followup on that with you because it's an area that I think my district is in many ways uniquely situated to address this issue head-on with this merger or this alliance of higher ed and industry. Thank you so much, excellent hearing.

Dr. CHIANG. Yes, ma'am.

STAFF. Ms. Kim is recognized.

Ms. KIM. Well, thank you very much, Chair and Ranking Member, for hosting this hearing, and thank you to our witnesses.

I know the Senate and the House is now trying to work on, you know, proceeding with the conference process to, you know, hash out some of the differences between our two chambers. And as we do, I wanted to ask to any panelist what in your opinion are the top two or three areas of focus where the U.S. Government should invest $52 billion that was included in the Senate-passed *U.S. Innovation and Competition Act* in order to have the greatest sustaining impact to achieve our goal of American innovation and competitiveness in the industry?

Mr. BHATIA. I can start. I can just reiterate——

Ms. KIM. Mr. Bhatia.

Mr. BHATIA [continuing]. Representative Kim, that, you know, the—you know, as was mentioned, the cost of semiconductor research and development and the cost of building large-scale semiconductor fabrication facilities continues to go up and is very, very large. And so I definitely feel that the prioritization should go to-

ward leading-edge research and development on technologies that will be able to be in production for many, many years into the future, as well as leading-edge manufacturing fabrication facilities and definitely believe that we should be focusing on the technologies that will ensure American leadership in microelectronics well into the future.

And with the rate of change of technology being the defining characteristic of our industry, every 18 to 24 months we introduce new technologies, we need to make sure that we're future—that these investments are made with an eye toward the future, and also that, as we think about these investments, we understand that there will need to be even extended future investments to maintain—to keep ourselves on the leading edge.

Ms. KIM. Thank you.

Dr. KELLEHER. I concur with that as well in terms of first focusing on R&D and including—and ensuring that we—our IP is developed and maintained in the United States and from a leading-edge perspective and then expanding the fab capacity to support the growing demand. And also from—we cannot forget getting advanced packaging capability and capacity back here very clearly in the United States.

Ms. KIM. Thank you.

Dr. CHIANG. And I will echo that.

Ms. KIM. Yes——

Dr. CHIANG. Sorry, I——

Ms. KIM. Dr. Chiang, go ahead. Dr. Chiang, go ahead.

Dr. CHIANG. Yes. Thank you, Representative Kim. I will echo that by also highlighting that the ultimate supply chain in semiconductors is the supply chain of human talent. And we need to substantially invest in the human talent pipeline. Otherwise, we'll have hundreds of billions of dollars' worth of public-private partnership and the best facilities throughout the country and yet not adequate number of engineers to staff and operate it.

And there is also the need to ensure the connection between policymaking, and the policy implications to domestic and foreign policy is tremendous, and that's why at Purdue we launched this year the Center for Tech Diplomacy at Purdue as a think tank specialized at the intersection between technology and foreign policy. And I believe that the *USICA* bill and the *CHIPS for America Act* portion of it will be critical if we could indeed fund and appropriate that as soon as possible.

Dr. WITHERELL. Yes, and I think it's really supporting the whole ecosystem and it really is—all the Federal science agencies have to be engaged in this for this to work. It's that big a problem.

Ms. KIM. Thank you. Thanks for mentioning that, Dr. Chiang, because I was—during the markup, I was successfully able to put an amendment in the *NSF for the Future Act* and NISP (National Industrial Security Program) reauthorization related to STEM education.

That leads me to the next question of, you know, if any of you can touch on how much the decline in the supply chain or anything can be attributed to the work force development issues you had mentioned, and what is the role of STEM, high-skilled and tech-

nical education in the semiconducting industry's work force recovery?

Dr. KELLEHER. Well, I'll start, Representative Kim. I believe maintaining basically an educated work force and the supply of the work force so that we can continue to grow our industry here in the United States is absolutely critical. To this point, we have been with universities and with the various colleges have been able to source—with a lot of work, have been able to support adequate talent and resources, but it is becoming increasingly challenging. So that is absolutely going to be critical going forward to maintain the supply so that we can continue to resource the work going forward, particularly as we want to grow and expand.

Mr. BHATIA. Yes, and I'll just add—thank you for asking that, Representative Kim. You know, in addition to the—you know, the focus on university talent and graduate school talent for our leading-edge scientists for R&D and innovation, there's also—you know, the factories of the future are not like the factories of the past. Factories are becoming far more automated, far more complex manufacturing processes. We're utilizing artificial intelligence, machine learning, and big data to operate all of these leading-edge facilities to make them productive, to maximize the quality levels and the output that we're able to get from these facilities. And so the training really needs to be also for the skilled trades who are working in these factories. We need to be looking at—in addition to STEM education, reskilling of those from other industries. We need to be looking at reskilling of those with military background toward the technologies and the capabilities required to operate and maintain these mega-fab clusters for semiconductor manufacturing.

Ms. KIM. Thank you, all of the witnesses, for your responses. I know my time has gone significantly above, but thank you. I yield back.

STAFF. Mr. Casten is recognized.

Mr. CASTEN. Thank you. Thanks so much to all our witnesses.

You know, it strikes me that like so much of what our economy is seeing right now and all these constraints are—we just have these huge supply driven constraints. You know, we saw the Texas freeze shut down a bunch of refineries and the tightening gas markets. We saw a huge collapse in new rig production that's tightening up our natural gas markets. And of course a big part of the reason we're here today is because we had, you know, a drought in Taiwan that slowed up some production capacity there and of course that same Texas freeze slowing up capacity. Mr. Bhatia, I see you're nodding your head.

I am delighted we're having this and I'm delighted for all the thought you've put into trying to think about how we address those supply constraints in the system, but I have this nagging concern about the demand side. If I understand it right, an electric vehicle (EV) needs about 2,000 semiconductors, which is roughly twice the number of the non-EV, and EVs, which is great from a climate perspective, as an EV owner, it's great from a fun-to-drive perspective. There were, what, 10 percent of new vehicle sales last quarter, so they're surging.

And I guess I'll start with you, Mr. Bhatia, because I see you nodding your head. As we continue that modernization of our vehicle fleet and all the good things, we don't want to slow that down, what is that going to do to the demand for semiconductors? And even if we got rid of the current bottlenecks in the system, how big a deal is that in terms of the total demand balances?

Mr. BHATIA. So I think automotive—well, thank you, Representative Casten, for asking this question. And, you know, for today the automotive sector is not a huge consumer of memory or storage. However, it is for Micron the fastest-growing market for us as we look forward into the next decade. As I mentioned in my prepared comments, the autonomous vehicles of the future are really going to be—are going to have as much content as a data center does today. Even semiautonomous vehicles will have as much—in the next few years will have as much content as full-blown servers do today.

And so what this means, in order to ensure that we're able to keep up with this strong demand surge takes careful, long-term planning. And as you were describing the supply shortages that are plaguing multiple end markets today, you know, with automotive being one of the primary ones, I think it's worth noting that the memory industry and Micron in particular has not really been the primary bottleneck for the industry, and that's because the memory industry and we as a primary player in that industry plan over a long period of time how much capacity we think we need in line with the long-term demand trends that we see.

And that's why it's so important that the *CHIPS Act* and the refundable investment tax credit gets implemented with urgency because it's going to allow us to make sure that whether it's for logic or whether it's for memory, we're going to be able to have long-term investments that can be made to prevent these kind of shortages from happening in the future.

Mr. CASTEN. Well, thanks. I'd love to hear from others if you have thoughts that are contrary otherwise to that, but I know that I'm a little bit tight on time here and I want to move to Dr. Kelleher quickly.

We've had these—as I mentioned at the start, we've got these two—this plant in Taiwan that, you know, we had a drought and a water issue if I understand right. We had these plants in Texas that had the Texas freeze that slowed them up. The—to what degree—have you been thinking at Intel—should we be thinking about how to weatherize the supply chain of our chip industry in response to an increasingly volatile weather system? Because climate change ain't going away and it ain't slowing down. I wish that wasn't true. But to what degree is the supply chain is weatherized as it could be, and what could we do to improve that?

Dr. KELLEHER. Well, I'll start very—for—speaking about our—Intel's factories, which is basically from the start of the manufacturing of the silicon. We have very active—when we're selecting our sites—and this has been true over the last 30 years—we have a very strict criteria in terms of—on the environment or what could actually impact our factories to continue to keep running on an ongoing basis.

We also spend quite a lot of time evaluating our facilities' infrastructures themselves, and we invest quite a lot of money into the facilities themselves so we can robust ourselves against snowstorms, we can robust ourselves against all the various aspects that—in terms of—from an environment that can go wrong.

I think across the supply chain overall—one of the key things across the supply chain is I truly believe we should have no single point of success. I call them single points of success rather than single points of failure. But I think we truly need to look as an industry and continue to keep working that so that we continue to have not single points of success, that we can robust ourselves against unique—our environmental impacts that—our ecosystem impacts that causes, I would say, a continuity risk of keeping the supply chain running.

Mr. CASTEN. I see I'm out of time, but thank you so much, and I yield back.

STAFF. Mr. Feenstra is recognized.

Mr. FEENSTRA. Thank you, Chairwoman Johnson and Ranking Member Lucas. Chairwoman Johnson, I just wanted to say, congratulations on your upcoming retirement, and after a long and admirable career in public service. I truly admire all the work that you've done, working on a bipartisan basis. I also want to thank each of the witnesses for their testimony, and sharing their extensive research and experience with us.

This question is for Dr. Kelleher. I understand that most advanced semiconductors are currently being manufactured in Taiwan. As you know, there is concern that China may eventually attempt to invade Taiwan, and take ownership of its semiconductor expertise. We've already seen examples of the CCP poaching Taiwan's talent and intellectual property. Can you please speak to the importance of security IP and semiconductor expertise from this uncertainty? How would the Programs and *CHIPS Act* support this endeavor?

Dr. KELLEHER. I'll start with—first of all, I'll start with saying that back in July I outlined from Intel our—where we get back to overall leadership from a process perspective, and we're aiming to get there in 2025, and we're spending—pretty significant investment in that happening. One of the key things that I think we need to be—and I have said this in my testimony on multiple times, as I've been talking about this, is maintaining the IP within the United States. I think it's absolutely critical for United States leadership in semiconductor, our leading edge, that we maintain critical IP for that within the United States.

Then we—all of us have the appropriate policies, in terms of protecting that, and how we ensure that that IP maintains within the United States. But I think within this work, within this overall *CHIPS Act,* and within this overall—going—funding going forward, we need to enable that.

Mr. FEENSTRA. Thank you so much for those comments. I greatly appreciate it. Dr. Chiang, in my district, we're home to Iowa State University, which houses a microelectronics research center, which is doing fantastic work in developing new materials that could transform the speed and efficiency of computing, and increase the production of sustainable agriculture. Universities will be crucial to

increasing domestic microelectronics manufacturing to ensure that we have adequate jobs and a skilled work force that can fill these jobs. How can industry and universities work together to provide support in developing a stronger practice-orientated program, and provide necessary research and education laboratories for these essential infrastructures, and for training that could be appropriately made?

Dr. CHIANG. Thank you, Congressman, for the question, and indeed it is essential for universities of this country, and the private sector, to work very closely together, but there are three broad lanes. One is R&D collaboration, one is work force—not only recruiting, but development together, through internship, through upgrade to facilities, and through online learning. And the third is co-location, economic development that creates knowledge and jobs together, that creates the position to be filled, and the talent that can fill them.

And in this regard, here in my home State of Indiana, Governor Holcomb and his team, and Secretary of Commerce in our State, Brad Chambers, have been working very closely with universities such as Purdue to create that economic development engine. And I think that, well, in addition to R&D and work force, by co-locating physically, factories of the future, along with the work force of the future, that is the best way to both develop talent and to develop the manufacturing capacity.

Dr. WITHERELL. So, Congressman, I'd just like to add to the fact, of course, that Ames National Lab at Iowa State is also a very important contributor in this, and their Center for Critical materials, so let me call out a close partner of ours.

Mr. FEENSTRA. Yes. Well, I just wanted to comment on that, Dr. Witherell, that, you know, they lead the efforts in graphing research, quantum material discovery, and critical materials, and quantum materials holds promise for quantum computing, which I'm very passionate about, but also next generation information storage. How do you see graphing and quantum materials enabling the next generation of microelectronics?

Dr. WITHERELL. Well, I think this is part of the role of the National Laboratories, because we don't know which of these materials will end up winning the game a few years from now. This is a very fast moving thing, and so we need to have these laboratories that have the scale and R&D capacity to try these things, and find out which of the ones are low risk enough to be translated over into industry. That's what our job is.

Mr. FEENSTRA. Well, thank you so much for your comments, everyone. I—really excited about this hearing, and I yield back.

STAFF. Mr. Foster is recognized.

Mr. FOSTER. Thank you. Am I audible and visible here?

STAFF. Yes, you are, sir.

Mr. FOSTER. Great. Well, first I just want to also echo my congratulations to our Chairwoman on her pending retirement. She has a lot to be proud of in her service to the Science Committee, and to our country. And although I am probably best known as being Congress's strategic reserve of physicists, I've actually had a parallel existence in my career with integrated circuits. And when I worked for one of our witnesses today, Mike Witherell, when he

was Director at Fermi National Accelerator Lab, I was still very involved in custom integrated circuit design at Fermi Lab, where back in 1989 I had invented a type of specialized integrated circuit called the QIE, a charge integrator and floating point digitizer that's still being developed and used in high energy physics experiments. And it's probably been implemented in 10 increasingly advanced mixed analogue digital IC processes, so I've stayed a little bit current on the incredible advances there.

But, you know, before that, actually, when my little brother and I started our company back when I was 19, our very first prototypes were hand-wired using the Intel 8080 microprocessors, and the Intel 2002 static RAM. And when we needed an order of magnitude increase in computing power, we chose the Intel Digital Signal processor chip. And when we finally got our first production order, and needed an office, and an actual factory, we chose as our telephone number one ending in 4116, named for the Moss Tech MK–4116 16 kilobit dynamic RAM capacity, which seemed infinite at the time. So—our company's now been successful, has over 1,300 employees, manufactures about 70 percent of the electronic theatre lighting equipment in the U.S., and we've kept all those manufacturing jobs in the Heartland, which is something I'm very proud of.

But, because of the current chip shortage, at this moment, most of our engineering staff is busy not designing new products, but on redesigning existing products around chips that can actually be purchased on the open or gray markets, and trying to understand the massive misallocation of capital, where somehow, whoever it was that was running the financial operations of our economy generally, and specifically the big manufacturers saw, you know, somehow our financial system is more interested in speculating in bitcoin than building IC bands, and trying to understand how do we deal with that—the incentives that led to that misallocation of capital.

And so my question is—first, for Mr. Bhatia, did you really say that there were 176 mask layers in an advanced flash product? Is that—did I hear that correctly?

Mr. BHATIA. Not mask layers. First of all, Representative Foster, I congratulate you, and if you want a job, I think, you know, we definitely have a few open positions, and that would be terrific if you want to come back to our industry.

Mr. FOSTER. You need someone with less gray hair——

Mr. BHATIA. I—it sounds like you're plenty experienced. 3D—NAND flash technology, several years ago, stopped scaling in two—in the X and Y dimensions, and began scaling vertically. So we actually have—we stack 106—176 layers of NAND flash devices, active NAND flash devices on top of——

Mr. FOSTER. Got it.

Mr. BHATIA [continuing]. Each other.

Mr. FOSTER. OK—so these——

Mr. BHATIA. And that's the——

Mr. FOSTER [continuing]. Are physical stacking? That's the 176——

Mr. BHATIA. Yes, sir.

Mr. FOSTER. OK.

Mr. BHATIA. Yes.

Mr. FOSTER. Because that was——

Mr. BHATIA. All monolithic stacking that happens in fab, but this is how——

Mr. FOSTER. OK.

Mr. BHATIA [continuing]. The——

Mr. FOSTER. So—but a smaller number of mask steps? OK.

Mr. BHATIA. Yes.

Mr. FOSTER. That's less frightening. Now, you know, there's a narrative about commodity products, such as DRAM, and there was something that the U.S. somehow cannot, and should not, compete in. And I want to congratulate Micron for not buying into that narrative, but, obviously, it's been a struggle. And I think we have to appreciate that in the unregulated and unsubsidized free markets, this subjects commodity manufacturers to a huge boom and bust cycle. And so either we have to just grit our teeth and say we are going to occasionally interfere in the free market, and, you know, effectively develop one or two national champions in this technology, or we have to just say that's the free market, you know, only the fittest survive, only the paranoid survive. What's your best thoughts on that? Yes, you had mentioned, actually, that you don't think some iteration of the technology consortium would work these days just because that really—realistically only two U.S. champions of IC process development.

Mr. BHATIA. Yes.

Mr. FOSTER. How do we make that decision?

Mr. BHATIA. Yes. So, you know, I think the first thing to recognize about memory—by the way, I appreciate your recognition on the 4K Moss Tech device. That was many of our first DRAM devices. Memory is essential to all computing environments, and it really is going to continue to grow in content, whether you're talking about artificial intelligence in a data center, 5G in phones, or autonomous vehicles in the future, continue to be central. And, actually, memory technology accelerates at the fastest rate in the industry, and we're challenging the laws of physics on every single generation of DRAM or NAND flat.

And so, you know, we do believe it's an essential component of the semiconductor strategy for the United States, and investments do need to be made there, and really technology, and leadership in technology, like Micron has achieved, as well as high volume manufacturing, and excellence in productive smart manufacturing environments, these are the two core areas that we need to be investing in as a country, and, of course, Micron very focused on, because these are the core elements of competitive advantage in the memory industry. So I actually encourage that memory is considered to be very strategic as part of the *CHIPS Act,* and the investment tax credits that are being considered, unfold.

Mr. FOSTER. Yes. And, let's see, am I out of time here? The—can someone give me a quick estimate on the time? Because it's reading zero.

STAFF. Yes, you're out of time——

Mr. FOSTER. OK.

STAFF [continuing]. Mr. Foster.

Mr. FOSTER. All right. Well, I yield back, and if there's a possibility of a second round of questions, I'd be very interested.

STAFF. Mr. LaTurner is recognized.

Mr. LATURNER. Thank you, Madam Chairwoman. First and foremost, I just want to say, no matter how long the good people of the Second District in Kansas send me to—back to Washington, D.C., I will forever be grateful for being a part of this Committee. Not just because of—the subject matter has been so fascinating, and been so meaningful to be involved with, but because of the incredible example, Chairwoman Johnson, you have set, along with Ranking Member Lucas. It's a real example of how Washington could, and should, function. And so I just want to say that, and congratulate you on your retirement, a well-deserved retirement.

First to Dr. Kelleher, and then to Mr. Bhatia, while the purpose of U.S. Government investment in semiconductors is American competitiveness and innovation, working with non-U.S. companies that play a vital role in the supply chain, such as ASML, TSMC, and Samsung will be important. What do you think is the role of the National Semiconductor Technology Center, if any, in managing the relationships with non-U.S. companies and the U.S. government?

Dr. KELLEHER. Maybe I'll kick off with saying within the National Semiconductor, in terms of its funding and how it allocates, I think, first of all, I believe its governance needs to be led by U.S. semiconductors, and ensuring that the decisions in terms of priorities which are made within the NSTC are truly moving ahead the United States agenda. Within—and also that there is a prioritization given to the funding that ensures the breakthroughs that moves the research forward within the—that enables the United States.

I—other companies, such as ASML, TSMC, IMEC, all of those other companies, they have their potential roles to play. I'm not saying they're part of the governance, but they—depending on what are the unique challenges and breakthrough if I pick ASML? ASML is the unique company that has—providing UV lithography, which is absolutely critical for the world—semiconductors. So I think that IMEC also has one of the world's preeminent research centers, so I think there's an opportunity for us to work to enable that, because the supply chain is quite complex. But I think it needs to be situational, in terms of the challenge that's being worked on, rather than an absolute same answer for every project.

Mr. LATURNER. Thank you. Mr. Bhatia?

Mr. BHATIA. Yes, I'll agree. I mean, the U.S. doesn't have leadership in all areas of the semiconductor ecosystem, and there's some we don't even have U.S. companies that participate in. And so certainly there will, you know, need to be foreign company participation in certain areas. However, there is some—there are some elements where foreign participation could create competitive challenges for U.S. companies, and so I agree with Dr. Kelleher that, you know, those situations do need to be managed on a—you know, carefully, and on a case by case basis in certain areas.

Mr. LATURNER. Thank you both. This is for everyone, so feel free to—we can start with Dr. Kelleher again. In the past year alone we've seen how environmental disasters can disrupt the supply of semiconductors. In Taiwan, severe drought has limited water availability, leading to production delays. Domestically, Winter Storm

Yuri created power outages, resulting in a months-long backup in production. How can we create a domestic semiconductor industry that is more resilient to extreme weather, and how can we encourage the same on the international stage?

Dr. KELLEHER. I'd start with saying—and I'd go back to a point I made earlier. One of the first things that you need to do with your facilities is to robust your facilities so that your facilities and your supply chain are basically—that you have a Plan B when Plan A doesn't work. You need to robust the facilities so that they're actually robust against power interrupts, robust against environmental, like weather, snow, storms—doesn't matter. I—when I was running the factories, I've had my pick of environmental, and I also—when I ran a factory in Ireland, I knew every storm that was taking place in the Atlantic, because our slurries and polish, some of our materials, were on ships in the mid-Atlantic.

So I—one of the things is—it can never be ignored, in terms of—I—we call it our business continuity, or our supply chain continuity. That has to be built in, and you have to have a robustness, and not single points of success or single points of where you fail. So there's the facilities being built to robust against—I—not—weather and others, but there's also, for each of the unique, either equipment, materials, et cetera, how do we have alternative sources? Where are those sources based? Is there enough of us—of a distribution of where they're based so if something happens in one place, that should have the supply coming from the rest.

So it's not a one answer for all, it's quite a complicated piece of work. It takes dedicated focus on it to ensure that your factories can run seven by 24 for 30, 40, 50 years without impact.

Mr. LATURNER. Thank you, Dr. Kelleher. Unfortunately, I've run out of time, but I look forward to continuing this conversation. I yield back, Madam Chairwoman.

STAFF. Ms. Stansbury is recognized.

Ms. STANSBURY. Thank you so much. And, Madam Chair, like many this morning, I want to add my voice to the chorus of grateful Members who are so grateful for your many, many years of service, and your advocacy, and your work on behalf of our science and technology enterprise. You will be so missed, and we wish you all the best in your retirement, so thank you so much for your service.

And I'm excited to be here today to talk about an issue that is so important to my home State of New Mexico. You know, we're here to talk about semiconductors because they're essential to every aspect of our lives, to the functioning of our modern world, from powering our phones and our electric devices, to powering our grid, and the technologies that will help us fight climate change, and help to build the new world that we're all working so hard to build. And New Mexico is particularly well poised to help lead the charge here, and help to ensure American leadership in microelectronics thanks to our National Laboratories, and our commercial scientific industry, and our private industry, so we are proud to be leaders in this field that will determine the direction of technologies for years to come.

At Sandia National Labs, which is in my district, the labs have made groundbreaking discoveries for decades, changing technology

as we know it. Last year Sandia partnered with IBM (International Business Machines) to lead the field in research and development of next generation transistors, called Gate All-Around Nanosheet Field Effective Transistors. They use less power, and allow for faster computations. These transistors can help us continue Moore's Law long beyond what we had previously thought. And Sandia is also working with the private sector to develop memory devices that have nearly unlimited endurance, and withstand harsh environmental conditions that outperform current commercially based memory devices on the market.

While Sandia has already developed partnerships with commercial partners for these projects, a lot of the work that happens at our National Labs, as many of you know, actually never makes it to market, and so one of the things that we've been working on in this Committee, and I've been working with my colleague Senator Senator Luján, and others who sign on to our bill, which is the *Partnerships for Energy Security and Innovation Act,* is to create a nonprofit foundation that will help to align the R&D that happens at our National Labs with the private sector so that we can bring these technologies to market, and really bridge the lab to fab gap that we see in our science and technology enterprise.

And once we get those technologies to market, and out of the development stage, New Mexico stands ready to manufacture, to assemble, and to test those semiconductors, because we are proud to host an Intel campus, one of the Nation's leading integrated device manufacturers, in Rio Rancho, with is in the greater Albuquerque area, which announced earlier this year that it is investing $3.5 billion for the manufacturing of advanced semiconductor packaging technologies, which is expected to create thousands of jobs—so, as we've seen during the pandemic, semiconductors impact every aspect of our lives, and I look forward to working with the Committee to bring manufacturing jobs back to our country, and make sure we are leading the way in research and development in these critical areas.

But I think that one of the biggest obstacles that we face is the development of our STEM work force, and we see this in New Mexico every day, where we have thousands of vacant positions in our National Labs, in our engineering firms, in our research entities, and so I think one of the things that's really important, and I'd like to ask Dr. Witherell about this, in your testimony you note the importance of work force development to the future of domestic microelectronics, and you point out that this is especially relevant for our National Labs, who, of course, rely not only on thousands of scientists, but also on skilled technicians. And so I wanted to ask you, Doctor, if you could talk a little bit about what you think Congress can do to help foster that STEM work force so that we are prepared for the future?

Dr. WITHERELL. Thank you very much, and I will say that we at Berkeley also partner with Sandia on our Quantum Systems Accelerator Center, where we are pleased to work with them. But we—all of the laboratories are working very hard on developing the STEM pipeline at every stage. Of course, the obvious thing is we have a large faction of the postdocs working in these disciplines in the whole country—or at the labs that's producing, but we're also

trying to help with undergraduate education and K to 12. And the fact—New Mexico's a good example of this, where the laboratories there can have a very large impact on that institutional—but it's also true that, for the security laboratories, work force is the lab director's biggest problem, actually, just to have the work force to fill the pipeline at Sandia, Los Alamos, Livermore, so all of us are working on how to develop a large and diverse work force that can feed these things because, in the end, the Nation has to go faster than other nations.

Ms. STANSBURY. Yes. Thank you so much, Doctor, and I think you really put your finger on it, which is that we have to be building that pipeline from early childhood education, even, through our K through 12 system, but we do have an immediate challenge of how do we get more STEM professionals into the work force, and working in our labs and our public institutions, to ensure that we're at the forefront of this work. So I really appreciate your words, and your good work, and with that, Madam Chairwoman, I yield back.

STAFF. Mr. Lamb is recognized.

Mr. LAMB. Thank you, and I want to join everybody in congratulating Madam Chairwoman on her retirement, and thank her for the years of service that we have shared together, and all that I've learned. I want to start with Dr. Kelleher, to talk a little bit about the decisions that go into where to locate the manufacturing sites, the factories. I think you mentioned in your early testimony your presence throughout Arizona, and New Mexico, and your company, and others, I know, have talked about Texas. I represent the areas outside of Pittsburgh, Pennsylvania that were long the manufacturing hub for steel and other specialty metals, and kind of related industries, and we're doing everything we can to try to bring some of our manufacturing know-how, and particularly our land, which is still very well suited for manufacturing, the old—have not all been turned—and they're still sort of sitting there, waiting to be taken advantage of. And I just wonder if you had any insights for regions of the country like mine, to talk about what competitive advantage did you see in the Southwest, and how could we maybe, you know, look to match that or exceed it in a part of the country like Southwestern Pennsylvania?

Dr. KELLEHER. Well, if I speak, first of all, to part of the Southwest, our investments began in the Southwest 30, 40 years ago, so I was—and once you started an investment in a given site, you tend to continue to grow that investment within the site, given the level of infrastructure that you have made. One of the—so I speak more generically, in terms of our overall site selection process.

What we look for when we're doing—we have a very stringent criteria from—looking—from our site selection. We look at the—basically the—for the given sites that become available in any given State, we look at the—basically the land itself, right, and there are many factors you need to take into account when you're building a factory, in terms of the site readiness. It's its infrastructure, it's the—basically the availabilities of utilities in the infrastructure. It's also the—what does the supply chain support in a given area, and are you starting the supply chain support from scratch? It's also what is the—basically what is the work force available in a

given area, and what is the availability from—anywhere from unskilled work force to the skilled work force? And also there's a look at—in terms of the overall—I would say the given States in terms of their—how much they work with business, so that it becomes easy to do business in a given State. So there's an entire set of criteria by which we work through as we make our selections.

Mr. LAMB. I really appreciate that, and I see us having a fair amount of advantage on many of those metrics. Supply chain, I don't quite know. That might be one we have to work on. Any other witnesses want to address that? You know, obviously our connection to Carnegie Mellon really helps with the talent pipeline, but anyone else have anything else to offer for Southwestern Pennsylvania, and kind of the Rust Belt overall, as we look to make——

Mr. BHATIA. Well, I think I'll just amplify Dr. Kelleher's comments regarding, you know, infrastructure and work force. Those are two key elements. You know, the semiconductor manufacturing operation's complexity is, you know, is incredible, and it's continuing to get more and more complex. Fractions of a second of power loss can create significant disruption, and so the utility infrastructure, including electricity, availability of water, water treatment, all of those are key factors.

And then, as she mentioned, and as you're noting, the availability of, you know, skilled work force. Whether that's the proximity to top universities, or vocational schools and community colleges that can help us with the training and re-skilling of technicians to work on this highly precise equipment. These are all of the areas that we think about. And then just overall, an industrial backdrop, and an ability to have delivered industrial success stories over time, and, you know, the know how to be able to do it. Because when we make these decisions, they're not 5-year decisions or 10-year decisions. They're 30- or 40-year decisions, as Dr. Kelleher also noted.

Mr. LAMB. Right. Well, thank you very much. I think I'm out of time, but we have all of that in Southwestern Pennsylvania, so all of you listening right now, please keep us in mind in the future, and I very much appreciate your joining us for today's hearing. Thank you. I yield back.

STAFF. Mr. Kildee is recognized.

Mr. KILDEE. Thank you very much. And, at the risk of being repetitive, I just want to say what a great opportunity it's been for me to serve, and continue to serve for the next year or so, with Chairwoman Johnson. She's been an incredible leader, and the—as has been said, the example that both the Chairwoman and Ranking Member Lucas have set is an important example I think that the rest of Congress would do well to heed. We do have our differences, but we work them out in, I think, a mostly civil manner, and that's really important, so thank you. And thanks for holding this hearing.

I recently welcomed Secretary—Commerce Secretary Gina Raimondo to Michigan for a discussion on the global semiconductor shortage with auto workers, with business leaders, with other elected officials. And as we know, while the semiconductor shortage is affecting a lot of industries, it is disproportionately affecting the automotive sector, impacting thousands of workers that I represent

in my home district. We've seen layoffs at General Motors' Flint assembly plant over the summer, and some of our factories in Flint have been idle—in Michigan, I should say, have been idle since the spring. And that's why I've been working with others in the House to invest in legacy chips that are commonly used in automobiles.

And I know this has been the focus of this hearing, and it might be somewhat repetitive, but I want to make sure we get as much information on this as we can. We obviously have to get serious about strengthening our domestic semiconductor supply chain, and we have to act now to save American jobs, to ensure a robust domestic automotive manufacturing industry here in the U.S., not in other places.

So if I could start, Mr. Bhatia, in your testimony you advocate for the U.S. to focus on leading edge manufacturing capabilities, which makes sense, to maximize the commercial success of our investments, but as we know, these cutting edge fabs and foundries will take quite some time to build, as you've mentioned, even if we immediately fully fund the *CHIPS Act.* So here's the question, how can we leverage the existing infrastructure today, across industry, to kickstart manufacturing advances while we wait for these fabs to be built? What can we do in Congress, specifically, to address that issue?

Mr. BHATIA. Sounds—thank you, Representative Kildee. And, you know, first let me just echo your comment that, you know, we need to move with urgency now to meet—even though it will take years for the *CHIPS Act*'s funding and investment tax credits to improve the domestic supply chain for semiconductor manufacturing, we do need to move urgently. We need to get started now, because other countries around the world are not standing still either. So whatever, you know, gap exists today, the gap is only growing until we actually are able to start reversing that trend. And let me also agree that automotive is an incredibly important market for all semiconductor manufacturers, but for Micron as well, we're the No. 1 provider of memory solutions to the automotive industry globally.

What we have tried to do with this, and one of the things that we've been successful—and to ensure that we are not—memory has not been one of the primary bottlenecks for the automotive industry is working with our customers to move them toward newer technologies. And this is an area where closer collaboration between the semiconductor manufacturer, the system design houses, and third parties, as well as the Tier One OEMs (original equipment manufacturers) together to be able to make a concerted effort to qualify newer technologies, because investments, whether they come—spurred by the government or from industry, they will always lean toward the future and toward leading edge.

And so, in order to really future-proof what we've been working with our automotive customers to do is to get their engineering resources dedicated toward newer technologies. Because if there are requirements they need, we can focus on those more, you know, earlier in the process, and be able to get them to technology—newer technology sooner.

Mr. KILDEE. Thank you very much. And just in the last few minutes—or minute or so, Dr. Kelleher, of course, Intel produces per-

sonal electronics computers, but it's also involved in auto—the auto sector. How do we balance the need for—the needs of these different industries, of both leading edge chips and these legacy chips? What's the approach you take, or you think we should take, in terms of trying to find that right balance?

Dr. KELLEHER. I concur with Dr. Bhatia said, in terms of—at this point, I think working with the auto industry to move them to more leading edge nodes, so that, as we invest in the infrastructure, that the infrastructure reinvested, and she can help enable that industry for many years to come. Right, so I think the key part of it—and yes, Intel, we're involved working with the auto industry, but the key is to help start moving the auto industry from being in the very much older nodes, where many of the equipment doesn't exist anymore to even manufacturers to—onto the newer nodes so that we can continue to keep the auto industry in progression with the rest of the semiconductor industry, so then that—and we never then get to the point of where we have this level of disparity between the support of the auto industry and the rest of the industry.

Mr. KILDEE. Thank you very, very much. I see my time has expired. I thank all the witnesses for your excellent testimony, and Madam Chair, thank you for this hearing. I yield back.

STAFF. Ms. Ross is recognized.

Ms. ROSS. Thank you, and thank you, Madam Chair, for holding this hearing. And I just want to say, as a freshman, thank you for setting an example of being an outstanding Committee Chair, and showing civility, working across the aisle, and mentoring the next wave of legislators. So I really appreciate all that you've done, and I look forward to working with you the next year, as we do even more

I also want to thank the panelists for joining us today. As we've been hearing, these pandemic-driven shortages of semiconductors have revealed how dependent the U.S. economy is on foreign suppliers. And it's not just in semiconductors, it's in so many other things in our supply chain, but we've seen how essential semiconductors are to so much of what we do.

I represent the Research Triangle area of North Carolina, and I've seen in my area how these shortages have hurt our economy and our innovation ecosystem. And right now I've just—I'd like to let you know, if you don't know, in my district, it's the home of North Carolina State University, and we're—it's a leader in Power America, a public/private partnership between industry—or among industry, government, National Labs, and academia that's accelerating the commercialization of wide-band semiconductor technology. And after 5 years of Department of Energy funding, Power America now has 60 members, and is completely self-sufficient.

It's also spawning people to leave and go into startups, and so the startup economy is very big in the Research Triangle area. But microelectronic startups often find it difficult to commercialize their products. Even well-funded startups struggle to secure time at fabs and foundries to test their products as they compete with larger companies for access, and right now we need as many people working on this as possible.

So, Dr. Chiang and Dr. Witherell, how can we grow a semiconductor startup ecosystem here in the United States, and do we have the time for it?

Dr. CHIANG. Well, Congresswoman, thank you for the questions.

Dr. WITHERELL. Go ahead.

Dr. CHIANG. Please go ahead, Dr. Witherell.

Dr. WITHERELL. Well, I can say one thing—we have—in the laboratories, we have systems for doing startups from the laboratories, we—at Cyclotron Road here, and included we have startups coming out in semiconductor industry that are fellowships that are supported by DARPA now. So there is—but I will say, to lead to the Dean, the university is a much wider space for this, and so we should hear from him.

Ms. ROSS. Please.

Dr. CHIANG. Thank you, Dr. Witherell, and thank you, Congresswoman. Indeed, I am confident that Congress and the Cabinet, including Secretary Raimondo, will be very comprehensive in the strategies. And we just talked about, let's not forget, the legacy nodes that produce a lot of the chips needed, for example, for the automotive industry. We should also not forget the military needs, including work force. For example, Purdue, leads 12 universities working with the DOD in the SCALE (Scalable Asymmetric Lifecycle Engagement) Program for DOD semiconductor work force development. Let's not forget that we also have small enterprises, including startup companies.

But I think there's a reason why there is a lack of interest compared to other fields, because the time to generate return to the investors tends to be longer for semiconductor companies. Unlike fields such as artificial intelligence or mobile applications, semiconductor chips, especially at the leading nodes, takes hundreds, if not thousands of engineers, and hundreds of millions of dollars to go to a mature stage. And most of the investors are not patient enough when there are competing opportunities for their cash resources.

So, I think part of the solution could be to encourage more of the university/industry collaboration to encourage faculty and students to work with industry leaders, and take their passions, and take their research articles, into the potential translational path so that there's a larger volume of choices for the investors. And part of that is indeed, back to the *CHIPS Act,* to restore a free market balance. Not to tip it, but to restore it, so that investors will be more confident that there is a vibrant future for their investment in the semiconductors industry in the U.S. And that's yet another reason why the *CHIPS Act* funding will be so important not only to the major players, but also the upcoming small companies.

Ms. ROSS. Well, thank you very much. And I see my time has expired, so I yield back.

STAFF. Ms. Moore is recognized.

Ms. MOORE. Well, thank you so much, and, of course, I am so pleased with myself that I decided to be on the Committee with the Honorable Representative Eddie Bernice Johnson. I would've just killed myself if I didn't have the opportunity to see her in action, as she has been such an inspiration.

You know, I am going to sound repetitive, I'm sure, because I want to sort of relate to some of the things that I have heard before. Question really for Dr. Kelleher, and maybe—Dr. Chiang. You know, I am from Milwaukee, Wisconsin, and, of course, this is a place that we were known at one time to be the machine makers of the world. So I'm wondering, Dr. Chiang, when you talked about work force development and all that, we start talking about play space strategies to do things, will this funding enable a place like Milwaukee to have a level playing field by providing funding for training and upgrading—because we have a fantastic work force for generations that were accustomed to manufacturing? Or are we going to just be flyover country, and they're going to run off to California, or some of these other places?

And so I am very, very—you know, I talked to Deputy Director of Commerce Don Graves. He indicated he thought that the Midwest would be a great place to do this kind of work, and I am—I'm wondering, you know, if—you know, because Milwaukee's a great place. We've got a port, we've got water, there are deals that could be made with local governments regarding utilities and so on. Is it foolish to even hope that a place like Milwaukee could be a site?

Dr. CHIANG. Congresswoman—well, let me share the Midwest enthusiasm that you just expressed so well. And indeed, here in the Midwest, whether it's in Indiana, or Wisconsin, or any other States here in the middle of the country, we have a lot of customers, and I hope companies would want to be closer to their customers. We have a lot of talent, and I'm hoping that the work force development portion of the NSTC in the *CHIPS Act* will support a nationwide network that access diverse talents, and is geographically inclusive.

Ms. MOORE. Well, I appreciate that. Listen, I want to yield the rest of my time to Dr. Foster. I can't see my clock, but I would like to yield to Dr. Foster.

STAFF. Dr. Foster's not present right now.

Ms. MOORE. OK. Well, I know he was very eager to finish his questioning, and so I wanted to accommodate him, so I will yield back my time.

STAFF. Thank you. Mr. Pete Meijer is next.

Mr. MEIJER. Thank you, and thank you, Madam Chairwoman, for the hearing today, and for all of our panelists who are here. I want to second Ms. Moore's comment, and just note that—I think I haven't been in a private meeting among Members, or in a Committee hearing that has all touched on microelectronics without all of us making the respective cases for our districts on why they are best positioned, so there is strong support in, I think, not only recognition in the—how critical this issue is, but also on the opportunities that it presents.

And I guess specifically, you know, in Michigan, the semiconductor shortages that we've seen domestically have been dramatically impactful on our automotive industry, and not just on, you know, the big three, and the largest producers, but also in all of the constituent industries and manufacturers that are serving in there. As a Member of this Committee, I've been particularly engaged and interested in this issue of domestic manufacturing, and

specifically on semiconductor chips, and how we can support new programs within existing agencies like NIST to advance additional domestic production.

I was proud that earlier this year we were able to secure additional funding for the Manufacturing U.S.A. Institute, which passed unanimously in Committee, but unfortunately was not included in the final package passed by the House. These dollars would've gone toward research, development, education, training for our domestic semiconductor manufacturing pipeline, and I'm—retain some optimism that we'll be able to still complete that, given the number of tasks ahead of us on the Committee.

I guess my first question would be to Mr. Bhatia. It's my understanding that many experts believe, you know, breakthroughs in packaging will really be key to improving chip efficiency beyond the gains already achieved through Moore's Law. Can you share what the role of a Federal supported research and development center that's focused on—specifically on advanced packaging? You know, what could this bring, in terms of uniting stakeholders together to tackle this challenge?

Mr. BHATIA. Thank you for the question, Representative Meijer. And, you know, advanced—first of all, I'd like to say that, you know, we support the idea that there should be national—that the NSTC Center should be focused on specific areas and verticals, rather than one monolithic center. So a center focused on packaging makes a lot of sense, and where we really see the benefit is, as advanced—as the scaling of primary logic chips becomes more and more challenging, there is—and as memory becomes a larger portion of the semiconductor ecosystem, the ability to put heterogeneous packages together that combine logic chips from one company, and memory chips from another company, and possibly packaging technology from a third company together, these are the kinds of breakthroughs that are going to be needed to address both the performance requirements of computing paradigms of the future, as well as power requirements of the computing paradigms of the future. And so, you know, there really can be an important role played for packaging, where the number of companies coming together are from different parts of the industry.

Mr. MEIJER. And then I think that that packaging component, you know, with the exception of—I believe it was Dr. Foster, who—you know, a lot of us do not have personal experience within this industry, and it's obviously a highly complex, highly developed one, but I think the role of packaging within microelectronics is, you know, again, one of those limiting coefficients that is vital to the broader semiconductor industry, but sometimes it's a little bit missed when we're talking about a congressional—and next, Dr. Kelleher, in your written testimony you had described the advances that international rivals are making in the global semiconductor technology industry. Can you briefly share, you know, what are the consequences of having to import such advanced semiconductors, and what should that ultimate balance look like between, you know, domestic production, but still having potentially some international supply?

Dr. KELLEHER. Well, if I look at it over the last 50 years, we have done the majority of our manufacturing within the United States.

I believe for the—or basically going forward, our aim is to continue to do that, and I believe that—going back to—we were talking about supply robustness, et cetera, for the United States we should have a majority of manufacturing, or basically a significant increase of where we are from today, in terms of having our own independence.

I'll also loop back to the—your last question, if that's OK, around packaging? Intel has leadership in packaging, and all our IP and development on packaging is done here in the United States. A lot of the packaging right now, all their R&D and development work is done in Asia We truly believe that establishing a center around advanced package not—will continue to help us, continue to push the edge on leading—on overall packaging and maintaining that leadership, but we're also bringing the rest of the United States so that we'll be in ability not just to have the capability of it in the United States, but also the ability to manufacture it in the United States.

Mr. MEIJER. Thank you, Doctor, and my time is expiring, but I just want to thank again the Chairwoman for holding this, and our Ranking Member as well, and thank you to our witnesses being here today. I think this is a vital topic, and I hope that we see legislative progress on this in the short term. Thank you so much. I yield back.

STAFF. Mr. Beyer is recognized.

Mr. BEYER. Thank you very much. And I don't want to say goodbye to Chairwoman Johnson, because I'm looking forward to 13 more months of serving with her wonderful leadership, and maybe she'll change her mind. But I do want to wish you a very happy birthday tomorrow, Eddie Bernice, so congratulations. It's wonderful to—I'm glad you were born.

And to move on, Mr. Bhatia, a long time ago I was Lieutenant Governor of Virginia, and, with Governor George Allen, we cut the ribbon on the big silicon plant out in Manassas, Virginia, and Governor Allen said, we're moving on from the Old Dominion to the Silicon Dominion. What happened? How did everything end up in Taiwan, rather than in Virginia, or in the United States?

Mr. BHATIA. Representative Beyer, thank you, and thank you for participating in that ribbon cutting ceremony. And our Manassas, Virginia facility continues to operate, and provide, you know, important supply for the automotive industry, and networking industry, and other industrial industries. It's actually one of the key parts of our global supply chain network.

But what really happened was—I think that event that you were referring to was probably in 1998 or so, is that about right, roughly? And Micron acquired that site shortly thereafter, but in the middle of that, there was 20—it began 20 years of concerted policy by Asian countries to buildup ecosystems and scale to create favorable environments for semiconductor manufacturing.

There also happened to be the transition from the 200 millimeter technologies that have been talked about on this panel to 300 millimeter technology, and that's where Asian countries really focused on making sure they were building up their ecosystems as the industry transitioned in the early 2000's from 200 millimeter to 300 millimeter.

And particularly, in semiconductor memory, the scaling up of those facilities just provided tremendous economic advantages that, you know, the smaller sites in the United States, without the government support, without ecosystem development, just couldn't compete. And so the Asian countries, particularly around memory, did end up having much larger scale, manufacturing in much more cost-effective environments.

And this trend over the last 20 years, you know, won't be reversed overnight. It—you know, and *CHIPS,* and the investment tax credits that are proposed are a good start, and they are—you know, they—we need to act with urgency, because, as I mentioned before, the gap is only widening because Asian countries, many of them, are already outlining policies for long term decades of investment with tens or even hundreds of billions of investment. So we really do need to move quickly.

Over time we can see that this gap closes, whether that gap is in the production output, or in cost structure, as the scale factors start to come together, but we need to act now, and we need to get about reversing this trend if we want to have leadership in long——

Mr. BEYER. Thank you. Going to try to get one more question in for Dr. Chiang. You know, when I talk to my friends at Micron and Intel, they talk about, you know, billions of dollars to get the new plant up. How do we grow the semiconductor startup ecosystem? How do we help the little guys who are developing all the cool chemistry? I'm sure that when Bill Foster was winning his awards 30 years ago, he was probably doing it in a small lab.

Dr. CHIANG. Thank you, Congressman, for the question. And as we have already observed throughout this hearing, that the semiconductors industry is a large and diverse one, as is our country, the United States, and there are many different components and opportunities. For example, a startup company in the design of chips today will face a different kind of challenge than those focusing on packaging. And there are States whereby the largest factories will be located, and there are many other States where smaller fabs, legacy node fabs, or packaging centers might be created.

But, in general, I would say that as SIA (Semiconductor Industry Association) or SRC (Semiconductor Research Corporation), these industry consortia, have indicated, that we need to aid restore a free market balance, and *CHIPS Act* will help to accomplish a big portion of that goal. And second is that we need to encourage more students and faculty to work with industry in order to be the cofounders, or the first set of employees, of these startups. The fundamental root cause, I think, is that most of the investors view the investment into semiconductor startups not as potentially high return as some of the other startup investment opportunities. So, restoring market balance, and increasing the volume of the deal flow would help to tackle those challenges for the startups.

Mr. BEYER. Thank you very much, and, Madam Chair, I yield back.

STAFF. Mr. Obernolte is next.

Mr. OBERNOLTE. Thank you very much, and thank you to our witnesses for what's been a very fascinating and impactful hearing.

My first question is for Dr. Kelleher. In your testimony you discuss the fact that we have a 30 percent cost disadvantage in attempting to do semiconductor manufacturing here in the United States versus overseas. I wonder if you could just spend a minute and tunnel down on the cost drivers for that 30 percent difference, and what can be done to restore U.S. competitiveness in that area?

Dr. KELLEHER. I'll break it into probably three portions, right? First of all, labor. There's a labor cost difference between Asia and the United States. Second of all, the cost of building, and the cost of building the fabs in Asia, is less expensive than in the United States. And third, there is the incentives which are available within Asia from many of the countries are also—make it so that the combined of those three together is what gives the 30 percent cost disadvantage.

So I—the work that's going on here through the *CHIPS Act,* in terms of how it will potentially help us as we go—in our industry, not just from—and for R&D development, because that has also the same cost disadvantage, because it's done on the fabs by researchers, they—it will help to address the cost disadvantage against those with an—the—which is made within Asia, and actually gets us to be in a place to be more competitive.

Mr. OBERNOLTE. OK. I'm sorry, you—the last thing that you said, could you say that again? Because——

Dr. KELLEHER. I said——

Mr. OBERNOLTE [continuing]. That was going to be my next question, is what do we do—what can government do to help bridge that gap?

Dr. KELLEHER. I think there's two pieces. I'll break it down into—first of all, there is, within the *CHIPS Act*—moving forward with the *CHIPS Act,* and support—and particularly in the NSTC, and—basically consistently—and having a structured framework to fund into the R&D within the United States. And then the greater *CHIPS Act,* in terms of enabling leading edge, to be able to build out, it's basically the manufacturing of the leading edge technologies. So this—the *CHIPS Act* is absolutely key, in terms of working, and basically enabling that to come into play, so that it enables the industry to be able to start eating into that cost disadvantage.

Mr. OBERNOLTE. OK. So maybe you can tunnel down on this a little bit further, because I see this as two different problems, right? There's the problem that we are in danger of losing our position as the world leaders in the technology, and that's certainly something that we can catalyze a solution for, but then there's a separate problem that most of the manufacturing is not done here in the United States anymore, which has national security implications for us, so we want to see more of those fabs here, and not just the fabs for the last generation of technology, but the fabs for cutting edge technology be here.

So I see the *CHIPS Act*—I see how what you're saying is true for solving the first problem, but I don't see how that reduces that 30 percent cost disadvantage that's preventing those fabs from being here in the United States.

Dr. KELLEHER. I think through the *CHIPS Act,* in terms of the incentives from the U.S. Government, that will start eating into

that differential. And, ultimately, the choices where companies go to make their—to choose where their—build their fabs has—it goes back to what are the incentives available for a given country, as well as what is the supply chain, and the people, and the skills, and all of that. But the funding coming through in the *CHIPS Act* will start helping to turn the tide, and start eliminating the erosion of the manufacturing going offsite, and start bringing it back onsite to the U.S.

Mr. OBERNOLTE. OK.

Mr. BHATIA. Representative Obernolte, can I add a comment?

Mr. OBERNOLTE. Sure, go ahead.

Mr. BHATIA. Sure. I just want to—just had one data point, just so that—it's a Micron specific data point, but it's very common across the industry. The capital intensity of our industry, particularly memory, is tremendous. Micron will spend more than 30 percent of its revenue back in capital again every year, and so the—in addition to the *CHIPS Act,* an investment tax credit that refunds capital investment is a really key element to make sure that we can start to close this—Micron sees 35 to 45 percent cost gap, with much larger scale operations that are already in place in Asia for our competitors.

Mr. OBERNOLTE. Right. I think we are in complete agreement on that, but it would have to be very targeted, and I'm not sure what you have just described is sufficiently targeted, because, you know, the—we're kind of at cross purposes, where industry is pursuing, you know, the commercial incentives, where we in government have a national security justification for wanting those fabs to be here. So it does us no good if, you know, we catalyze further development in cutting edge technology if that technology is still manufactured and deployed in other countries. We need to solve both problems. But it's a fascinating discussion. I think that what you're hearing on the Committee is a willingness to work with industry in trying to solve both of those. So I want to thank our witnesses, and I'll yield back.

STAFF. Mr. Gimenez is recognized.

Mr. GIMENEZ. Thank you, thank you, and happy early birthday to the Chairwoman. I want to thank you for this hearing, and also to our Ranking Member. Thank you. I've got two or three questions that—for Ms. Kelleher. Is it true that Intel is planning to build new facilities, new manufacturing plants, in China?

Dr. KELLEHER. So Intel and the U.S. Government, we share a goal of addressing, basically, the ongoing industry-wide shortage of microchips, and we have explored a number of approaches with the U.S. Government. However, our key focus is on the significant ongoing expansion of our existing semiconductor manufacturing operations, as we have already announced, which work is ongoing in Arizona and New Mexico, and we're working on selecting a green-fueled site here in the U.S. and in Europe. This will take time, and, again, I urge Congress to fund the *CHIPS Act* so we can accelerate the progress here in the U.S.

Given the urgency of the shortage, we remain open to other solutions that would help meet high demand for semiconductors essential to innovation and economy, but, basically, we——

Mr. GIMENEZ. Ma'am, you're—I've only got a certain amount, is it a yes or no?

Dr. KELLEHER. So I'm not going to discuss specific—discussions with the U.S. Government here.

Mr. GIMENEZ. OK. So do you view China as a competitor, or do you use it—do you view it as a place of—it's an opportunity or a competitor? What do you view China as?

Dr. KELLEHER. China is part of our world market, but I also—I'm very clear on protecting my IP, from a technologies perspective, here in the United States.

Mr. GIMENEZ. OK. So I'll take that—the answer is you view it as an opportunity, it's part of the world market. Do you intend to seek grants from *CHIPS* if it is passed?

Dr. KELLEHER. Given Intel is the leading manufacturing and leading edge technology here within the United States, and we have had long investment history here in the United States——

Mr. GIMENEZ. I'll take that—I'm sorry, I'll take it as a yes. Again, I've got some questions, and I really need to go, so I'll take that as a yes. OK, you're going to seek funding from *CHIPS*. All right. We talk about—when you talk about supply chain, you have the chips themselves, but then what—the stuff that makes the chips, all right? And so, you know, the testimony is that the rare earth metals, all these metals that go into making the chips, they're actually—a lot of them come from China. Does the United States have the capacity, does it have the resources, the natural resources, to produce this in the United States?

Dr. KELLEHER. I think all of it—I don't believe yes, that there is, but this is an ongoing work that different parts—I know Dr. Bhatia said Micron is working with the United States, and Intel is also working with the U.S. Government, because this is a piece of work that—supply chain that we have quite a bit of work to do.

Mr. GIMENEZ. And is it because of regulations, et cetera, that we're not producing this stuff here in the United States? Is it because of us, we're doing something wrong here, Congress, the executive branch is doing something wrong so that we don't incentivize that production here in the United States? Because, actually, we bring all this manufacturing back, and we still don't have the supply chain for the chips themselves, we're not going to be anywhere, right? We need to have it all basically here. Would you agree with that?

Dr. KELLEHER. Having—basically a significant portion of the supply here in the U.S. absolutely will help, right. Your question, in terms of is it something legislation is doing, I would put it more that I think it needs to be raised in the importance in terms of within the supply chain. And I think once it raises within the importance of the supply chain, then the might of the entire industry works on it to get a better answer.

Mr. GIMENEZ. Is there any research going on into creating chips that don't need these materials, and need something which is abundant, or not quite as expensive, maybe not quite as exotic? Is there research to creating a chip—a cheaper chip that's just as good or better than what we've got right now?

Dr. KELLEHER. If you go back to, say, some of the core ingredients of the advanced materials that we use today, I think one of

the key aspects of—within NSTC and research of the future is how do we replace those with alternative materials? I mean, the periodic table is actively being used, in terms—and as we advance the technology, we typically end up using new—basically more elements of the periodic table. So I think one of the things I would like to see out of NSTC is an ongoing activity in terms of how we actually—and move ourselves to be from less dependent on some of those materials. And then——

Mr. GIMENEZ. All right. And so—and I know that my time is up, but my final comment would be that we would—hopefully the United States would be helping you develop those materials that would make us less reliant on outside sources to create these chips. And thank you so much, and again I yield back. Thank you.

STAFF. Mr. Waltz is recognized.

Mr. WALTZ. OK. Thank you, Mr. Chairman. And just to build on my colleague from Florida, Mr. Gimenez's, I thought very thoughtful and timely questions on the supply chain and on critical minerals, I've often spoken about, and worked on legislation in the Defense Department—on the Armed Services Committee for the Defense Department, trying to address the United States' heavy reliance on China for access to critical minerals. The Chinese Communist Party has openly threatened Japan, Australia, and others with withholding these critical minerals as part of—you know, and it's been in line with their geopolitical interests, and, frankly, in line with the dictatorship that the CCP is.

So I've introduced H.R. 2637, the *American Critical Mineral Independence Act.* It has a number of provisions to support research and development. Dr. Witherell, can you speak to what it would mean for the semiconductor industry to be able to understand and control minerals and to manufacture them, and to be able to process them, the role DOE labs, like Berkeley National Laboratory, and others play in making this the reality?

And, just to directly address Representative Gimenez's questions, I think we need to have an honest conversation about our own rules, in terms of mining on Federal lands, in terms of *NEPA (National Environmental Policy Act)* and our environmental restrictions, the fact that it takes on average a mining company in the United States 7 to 10 years to get an appropriate license, in Australia it's 2 to 4 years. So I think this is an interesting kind of academic conversation here, but we're not being honest with ourselves about the own—our own restrictions that we put on being able to control our own supply chain.

And I can tell you, sitting on the Armed Services Committee, we are losing badly, if you look at the trend lines of what the Chinese will be able to control, and what we're giving up. In fact, *Build Back Better,* that the House just passed, will close down America's largest copper mine, because it's on Federal lands. So, Dr. Witherell, can you speak to how critical this will be to be able to control the critical mineral supply chain?

Dr. WITHERELL. Well, there's enormous effort in—across the Dewey Laboratories on critical minerals and materials, and on developing—and it's everything from—and, of course, it's broader than semiconductors, batteries too, cobalt for batteries and other things. And we're working on developing—No. 1, thinking about

the new technologies, being able to use certain minerals that are not as rare so that we can actually build it. At the same time, there are efforts on how to get lithium in this country, how to get other minerals in this country, and that's going to be, I think, an increasing emphasis among the DOE laboratories in the future.

Mr. WALTZ. Well—no, thank you, I appreciate that. And, you know, I mean, it's interesting you mention lithium, which is obviously critical for battery manufacturing, which is critical for a green economy, which many of us support. However, I don't want to increase our dependency on our greatest adversary as the cost of having a green economy. And it's also worth noting that, in Afghanistan, we had the world's second largest known lithium reserve, third largest copper, fifth largest cobalt, and we just handed that over to the Taliban, who are now actively flirting with Chinese mining companies to exploit those resources.

Dr. Kelleher—so, I mean, the mistakes that we inflict on ourselves, and that, frankly, this administration's policies are inflicting on this entire effort, again, is something I think we need to have an honest conversation about. But, Dr. Kelleher, I wanted to—you know, again, I know you've been asked, and I apologize if I'm repeating here. You know, I applaud the investments made, and that you're looking to make in the United States, and I am concerned about Intel's plans to expand manufacturing in China.

Can you—and I know you talked about the cost differential. We know much of that is subsidized by the CCP, in terms of creating that differential. But, again, sitting on Armed Services, we are pulling our hair out trying to keep up militarily with Chinese investments, and then to watch American companies continue to invest there. I understand the cost differential of the United States, but we also have—you know, we can make investments into India, happy to help you with that. We can make investments into Vietnam, and there's kind of allied shoring, in addition to onshoring. So can you talk to those efforts?

Dr. KELLEHER. So some of our—we have manufacturing facilities within Vietnam. We have also manufacturing facilities within Malaysia, and we have—also have manufacturing facilities within Costa Rica.

Mr. WALTZ. Just in the interest of time, ma'am—I don't mean to cut you off, I'm just out of time. Can—why are we—why are you expanding in China, then, rather than those other facilities?

Dr. KELLEHER. I didn't say we were expanding in China. I——

Mr. WALTZ. OK.

Dr. KELLEHER [continuing]. Was very clear what we have announced is expansions here in the United States. And what we have formally announced is expansions here in the United States and in Europe. What I did say is I wasn't—directly to the question that the—that I got asked earlier is—discussions with the U.S. with respect to China, and I said, bottom line is, I'm not discussing that.

Mr. WALTZ. OK. Well, there's just been reporting of your expansion in Chengdu factory there that the Biden Administration has expressed serious concern about. I think that's what I was getting at. If you could send an answer for the record, I'd appreciate it.

Dr. KELLEHER. Sure.

Mr. WALTZ. Thank you, Chairman, for your indulgence.

Chairwoman JOHNSON. Thank you very much. I think that is the end of our witnesses. But before we bring this hearing to a close, I want to thank our witnesses for testifying before the Committee today. The record will remain open for 2 weeks for additional statements from the Members, and for any additional questions the Committee may ask of the witnesses. The witnesses now are excused, and the hearing is adjourned.

[Whereupon, at 1:28 p.m., the Committee was adjourned.]

Appendix I

Answers to Post-Hearing Questions

ANSWERS TO POST-HEARING QUESTIONS

Responses by Dr. Ann Kelleher

U.S. HOUSE OF REPRESENTATIVES
COMMITTEE ON SCIENCE, SPACE AND TECHOLOGY

Questions for the Record to:
Dr. Ann Kelleher
Executive Vice President and General Manager, Technology Development
Intel Corporation
Submitted by Representative Jamaal Bowman

1. If the government is going to play a more active role in supporting domestic chip production, and if one of our goals is to prevent future shortages and bottlenecks, it strikes me that we should be doing comprehensive monitoring of semiconductor supply chains. That way, when we're talking about giving public subsidies to very profitable corporations, we can make more informed decisions about what kind of interventions are necessary and helpful, and we can also try to anticipate problems. As far as I'm aware, there is very limited public data on semiconductor supply chains available at present. What kind of data does your company use when determining investment plans or supplier relationships? And what data could your company provide that would help the government do better strategic planning?

Answer:

As we have seen in the current chip shortage, there are few options to remediate shortages in the short term, but it is urgent and essential to collaborate on public-private sector solutions to prevent shortages from occurring again in the future.

While multiple private and subscription data sources cover semiconductor trends (e.g., WSTS, Gartner, and IC Insights),[1] one of the most important public indicators for government strategic planning is the global distribution of semiconductor manufacturing information, published by the Semiconductor Industry Association (SIA) in its public reports. For example, a report published by SIA and the Boston Consulting Group (BCG) clearly demonstrates the significant loss of market share for U.S. chipmaking since 1990.[2]

Intel believes it is essential to increase capacity for fabricating advanced semiconductors inside the United States. Intel is so committed to this goal that over the past twelve months, we have announced new investments including $20 billion for expanding capacity in Arizona, $3.5 billion for advanced packaging in New Mexico, the completion of a multi-billion-dollar expansion in Oregon, and most recently, at least $20 billion of investment to construct two new fabrication facilities in Ohio.

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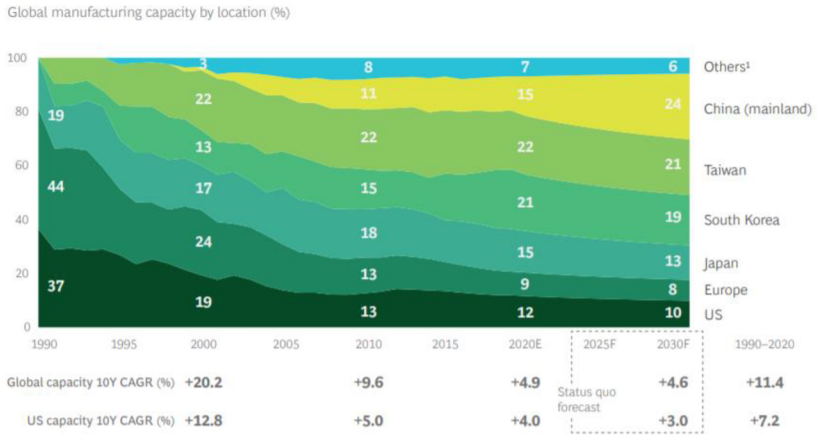
[1] See https://www.wsts.org/; https://www.gartner.com/en/industries/high-tech; https://www.icinsights.com/.
[2] See https://www.semiconductors.org/resources/sia-summary-of-bcg-sia-report-government-incentives-and-u-s-competitiveness-in-semiconductor-manufacturing/

A semiconductor fabrication facility (commonly known as a "fab") can take up to a decade to plan, including two to four years from site selection to production. In shaping its investment plans, Intel uses a combination of public data sources (including public and government economic forecasts and analyst projections) and proprietary data sources to build demand forecasts and competitive analysis that determine investment strategies. For example, see the data by analysts depicted in the chart below.



Sources: VLSI Research projection; SEMI second-quarter 2020 update; BCG analysis.
Note: All values shown in 8" equivalents; excludes capacity below 5 kwpm or less than 8".
¹ Includes Israel, Singapore, and the rest of the world.

Recently the U.S. Department of Commerce released findings from a voluntary September 2021 industry survey of semiconductor manufacturers and customers. The findings provide strong support for urgent action on measures to strengthen U.S. based chipmaking capacity and capability. To quote from the findings:[3]

But the semiconductor supply chain remains fragile, as demand continues to far outstrip supply.

In September 2021, the Department of Commerce launched a Request for Information (RFI) on the semiconductor supply chain that gave new insight into the complex and global semiconductor supply chain. The Department received more than 150 responses, including from nearly every major semiconductor producer and from companies in multiple consuming industries.

[3] See "Results from Semiconductor Supply Chain Request for Information," available at https://www.commerce.gov/news/blog/2022/01/results-semiconductor-supply-chain-request-information.

Some key findings release last month include:

- Median demand for chips highlighted by buyers was as much as 17% higher in 2021 than 2019, and buyers aren't seeing commensurate increases in the supply they receive. This is a major supply and demand mismatch.
- The median inventory of semiconductor products highlighted by buyers has fallen from 40 days in 2019 to less than 5 days in 2021 (see Figure 2). These inventories are even smaller in key industries.
- The RFI allowed us to pinpoint specific nodes where the supply and demand mismatch is most acute, and we will target our efforts moving forward on collaborating with industry to resolve bottlenecks in these nodes.
- The primary bottleneck across the board appears to be wafer production capacity, which requires a longer-term solution.

U.S. HOUSE OF REPRESENTATIVES
COMMITTEE ON SCIENCE, SPACE AND TECHOLOGY

Questions for the Record to:
Dr. Ann Kelleher
Executive Vice President and General Manager, Technology Development
Intel Corporation
Submitted by Representative Donald Norcross

1. Dr. Kelleher, in your testimony you noted that the United States is at a 30 percent cost disadvantage with East Asia for chipmaking, which corresponds with a decrease in the U.S. share of global chip manufacturing. You further state that federal investment is needed to level the playing field for America's semiconductor industry. Market reporting shows that Intel brought in over $70 billion in revenue and over $40 billion in gross profits in each of the last three years. Why are taxpayer funds needed to advance semiconductor manufacturing at a time when current and future demand is projected to be high and what specific factors lead to the 30% cost disadvantage with East Asia?

Answer:

The scale and the scope of the investment required to compete with other countries is enormous. Foreign competitors in Asia and their governments recognize the strategic value of semiconductor capabilities, and they have been investing heavily in their industries for decades. The Semiconductor Industry Association (SIA) recently reported that as much as 40 percent to 70 percent of the cost differential is directly attributable to government incentives.[4] As a result, the cost for Intel to open and operate a fab in the United States is 30 percent higher than the cost to foreign competitors of doing so in East Asia, and most of that difference is attributable to foreign government incentives.

SIA has estimated that, without government support, the U.S. share of semiconductor production will dip below 10 percent of the world total in this decade. Efforts to support the semiconductor industry are about leveling the playing field and shoring up the domestic semiconductor ecosystem, in which Intel is the only American company with the ability to design and manufacture advanced logic chips. Intel also is the only company that has invested in both advanced chip manufacturing and supporting R&D in the United States.

We applaud bipartisan efforts in Congress and the Administration to support the U.S. semiconductor ecosystem. Federal funding for the CHIPS for America Act programs and the enactment of a semiconductor investment tax credit will help ensure supply chain security and U.S. leadership in this semiconductor manufacturing does not further erode.

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[4] Antonio Varas, Raj Varadarajan, Jimmy Goodrich, and Falun Yinug, "Government Incentives and U.S. Competitiveness in Semiconductor Manufacturing," BCG and SIA, (Sept. 2020) at 4; available at https://www.semiconductors.org/wp-content/uploads/2020/09/Government-Incentives-and-US-Competitiveness-in-Semiconductor-Manufacturing-Sep-2020.pdf.

In summary, significant investments in capital expenditures and research and development are required for semiconductors manufacturers to stay competitive and keep pace with the advancements promised by Moore's Law. The ten-year cost of a state-of-the-art fabrication facility, including initial investment, periodic retooling to maintain competitiveness, and operating costs, ranges between $10 billion and as much as $40 billion, depending on the type of technology used and product manufactured.[5] In 2021, Intel invested $18.7 billion in capital expenditures and invested $15.2 billion in R&D during that period. Intel's R&D investments represent, on average, 20 percent of our total annual revenue--one of the highest among U.S. industries. As a result, Intel ranks sixth among publicly-traded U.S. companies in its individual R&D investment.

Intel has also committed to continuing our investments in the United States going forward. We announced more than $43 billion in planned investments over the last year to expand existing fabrication facilities in Arizona and New Mexico, to build two fabs on a brand-new site in Ohio.

[5] Antonio Varas, Raj Varadarajan, Jimmy Goodrich, and Falun Yinug, "Government Incentives and U.S. Competitiveness in Semiconductor Manufacturing," BCG and SIA, (Sept. 2020); available at https://www.semiconductors.org/wp-content/uploads/2020/09/Government-Incentives-and-US-Competitiveness-in-Semiconductor-Manufacturing-Sep-2020.pdf.

U.S. HOUSE OF REPRESENTATIVES
COMMITTEE ON SCIENCE, SPACE AND TECHOLOGY

Questions for the Record to:
Dr. Ann Kelleher
Executive Vice President and General Manager, Technology Development
Intel Corporation
Submitted by Representative Gwen Moore

1. To help increase the number of semiconductor manufacturing facilities in our country, a highly educated workforce is a key requirement. But that could also limit the places where these facilities could be located meaning vast parts of our country may not benefit from the robust investments in the CHIPS for America Act – even places that have a strong history of manufacturing and high numbers of available workers. When Intel is considering where in the U.S. to place any new facilities, what are the factors it is taking into account, including when it comes to workforce availability and training?

Answer:

Intel takes a comprehensive approach and considers numerous factors when it selects a new site to build a semiconductor fabrication facility. These factors include permitting business processes and investment pro-business conditions, physical characteristics of the land or constructability, utility infrastructure and transportation capability, construction and supplier capability, technical workforce availability and total cost of operating at the site.

It costs Intel between $10-$20 billion to construct and equip a semiconductor fabrication facility Manufacturing semiconductors also requires extreme precision, so susceptibility to weather events like hurricanes, tornados, and snowstorms, as well as ground conditions like the quality of the soil and likelihood of earthquakes are also key factors. In addition, reliable utilities like power and water, and transportation infrastructure, ensure that the fab can run continuously. Finally, the regional talent pipeline is another important consideration given the thousands of technical and skilled workers required to staff a fab. Therefore, proximity of both community colleges and universities that graduate and train students with relevant backgrounds are one of the key features Intel looks for when selecting a new site or expanding an existing facility.

2. How can we ensure that a new federal grant program to incentivize new domestic semiconductor manufacturing facilities and workforce development is allocated in manner that does not favor some jurisdictions over others? What role do you think the Department of Commerce should play in overseeing the distribution of the funds to ensure that all interested jurisdictions and entities can participate or be able to compete in an unbiased competition?

Answer:

The CHIPS for America Act includes specific criteria to determine eligibility for funding under the financial assistance program established in Section 9902 of that Act. Specifically, a company must have been offered a government incentive at the state level, made commitments to worker and community investment, and secured commitments from regional educational and training entities and institutions of higher education to provide workforce training. These unbiased criteria (i) incentivize the participation of state and local jurisdictions to offer government incentives and help train their workforce on semiconductor technology; and (ii) provide the Department of Commerce with an objective means to evaluate where to invest U.S. taxpayer money.

A number of states in the Southwestern, Western, and Eastern United States have historically offered favorable financial and other conditions to incentivize semiconductor manufacturing, and we are encouraged those new states and jurisdictions in the Midwest have started to show a strong interest. For example, Ohio recently announced commitments to bring semiconductor fabrication to the state, and Intel is planning to invest at least $20 billion in New Albany, OH to construct two new leading-edge fabs even though the state has no significant semiconductor presence today.

Intel suggests that the Department of Commerce also consider the following factors when selecting grant recipients for a proposed project to ensure the funds accomplish the purposes of the CHIPS Act:

- The project's contribution to American technology leadership and U.S. supply chain security
- Size, broader economic impact, and the number of American jobs it creates
- Ability of the recipient to leverage the federal contribution
- National security implications from the project and technology used
- The recipient's intellectual property protections, and
- The project's self-sustainment after federal investment is used

3. Workforce-related challenges including insufficient numbers of U.S. workers with the skills and training can be addressed by developing new programs, in conjunction with academic facilities, but training people takes time. How might such workforce challenges or any workforce gaps be addressed in the short term?

Answer:

Over the last 10 months, Intel has announced approximately $43.5 billion in new capital expenditures in the United States, including the construction of two additional semiconductor fabrication factories in Arizona and two new fabrication facilities in Ohio. Combined with the planned construction projects of other semiconductor companies, the additional workforce capacity needed will significantly strain the talent pipelines that feed into the semiconductor industry. These pipelines include the construction and trade workers needed to build and outfit the manufacturing facilities, the technicians needed to operate and maintain the facilities, and the advanced degree STEM professionals needed for the research and development that feed such facilities.

Meeting these workforce needs will require strong collaboration among industry partners, educational and vocational institutions, and officials at all levels of government. Intel and other industry leaders stand ready to do our part to address these challenges, and we are already working with educational institutions to establish and scale initiatives to fill tomorrow's workforce needs. But we cannot do this alone. Additional government funding is needed to fully scale these initiatives to meet industry needs. Intel, for example, is already collaborating with government partners and educational institutions to develop curricula focused on training and developing technicians and other STEM professionals to support semiconductor factories and packaging facilities. Intel is also working with non-profit organizations to pilot new workforce development initiatives, including a registered apprenticeship program for technicians. But without further government support, implementing these and similar programs at the necessary scale to meet industry-wide demand will be cost prohibitive.

As these programs are developed, Intel is implementing interim measures to address workforce challenges in the short term. For example, Intel is preparing to pilot two-week semiconductor "boot camps" for high school students in Arizona. Intel anticipates these boot camps will successfully prepare certain high school students for entry-level roles in our manufacturing facilities, where they can further train and develop their careers. Intel also operates facilities used to train trades workers on the critical skills needed to maintain and improve semiconductor factories and manufacturing tools. These and similar initiatives are implemented in collaboration with state and local partners, and they can also benefit from increased federal funding.

4. In your testimony, you mentioned that each job at Intel is estimated to support 13 other jobs elsewhere. Please elaborate on the indirect job opportunities – what are they, what kinds of skills might they entail, what kind of workforce training might be needed to prepare individuals for those positions?

Answer:

In 2020, Intel released a report based on federal data and economic modelling to describe Intel's impact on the U.S. economy and its labor force.[6] As described in that report, Intel's operations provide a significant impact to the U.S. economy through its operational spending, capital investments, and distribution channels. The overall impact includes both upstream and downstream impacts on the economy. Upstream impacts flow from Intel's operational spending and capital investment. For example, Intel purchases intermediate inputs and capital goods from a variety of other U.S. industries, supporting jobs in and spurring additional rounds of input purchases by these industries. Each business in Intel's upstream supply chain provides jobs and labor income and generates Gross Domestic Product (GDP). Other economic impacts are generated by the personal spending of Intel employees and the additional income earned by employees in the supply chain to Intel.

[6] *See* Intel, Intel's Impacts on the US Economy, https://download.intel.com/newsroom/2021/corporate/intel-impact-us-economy.pdf.

Downstream impacts flow from the distribution channels for Intel products and other products incorporating Intel components. These distribution channels include wholesalers, distributers, and retailers. Each business in the distribution channel also provides jobs and labor income and generates GDP.

In 2019, for example, Intel directly employed an average of 51,900 U.S. workers throughout the year. In addition, Intel indirectly supported 669,400 full-time and part-time jobs elsewhere in the U.S. economy. The largest component of Intel's total employment impact is attributable to its operational supply chain. Intel's purchases of services and goods from U.S. suppliers supported an estimated 376,600 jobs in other industries across the country. Additionally, Intel's capital investment supported 146,100 additional jobs, and Intel's distribution channel supported another 146,700 jobs. Combining these impacts, Intel's total employment impact on the U.S. economy was estimated to be 721,300 full-time and part-time jobs in 2019.[7]

As noted above, Intel's largest impact on employment relates to its operational supply chain. Intel's manufacturing and packaging operations, for example, support large supply chain ecosystems, including the creation of supply-chain clusters in each of our manufacturing locations. These suppliers choose to strategically locate nearby to reduce logistics-related expenses and take part in the cluster's exchange of capital, workforce, and innovation. By responding to Intel's supply requirements, local vendors grow their capabilities and create further self-sustaining opportunities for growth.

Intel works with more than 9,000 tier 1 suppliers in 89 countries. Our supply chain is incredibly diverse and includes:

- **Equipment for factory operations**, including tools and parts that support manufacturing and product development.
- **Manufacturing process inputs**, including silicon and chemicals.
- **Electronic design automation software** for designing electronic systems such as integrated circuits and printed circuit boards.
- **Construction services**, including labor, materials, supplies and services.
- **Professional Services**, including accounting, financial and legal services.

The jobs created by these supply chain partners cover a wide range of skills, including professional skills, advanced STEM skills, advanced manufacturing skills, and construction and trade skills. Intel and its supply chain partners are eager to partner with federal, state, and local government partners on initiatives to improve education and workforce development opportunities in each of these areas.

5. Dr. Kelleher, you stressed the importance of federal support for the development of prototypes. What more could the federal government do to support truly innovative

[7] *See* Intel, Intel's Impacts on the US Economy, https://download.intel.com/newsroom/2021/corporate/intel-impact-us-economy.pdf.

developments at the earliest stages of conception, particularly as it concerns microelectronics? Also, do you think that the current research and experimentation tax incentives adequately drive such innovation?

Answer:

The federal government can partner with private industry to make sure the U.S. has a strong technology and product pipeline that links precompetitive research to prototypes to high volume manufacturing. Specifically, the federal government should take immediate steps to fund needed semiconductor research and development efforts in a coordinated manner by establishing the National Semiconductor Technology Center Research (NSTC) and National Advanced Packaging Manufacturing Program (NAPMP) that are authorized under the CHIPS for America Act. These initiatives should leverage U.S. semiconductor company participation and existing infrastructure because industry is best positioned to drive early-stage innovations that can be commercialized and have a meaningful impact long term.

Intel has fueled job growth and the development of new technologies that have had significant economic benefits, from 5G to artificial intelligence. Intel invests $13 billion dollars annually into R&D on average, which is about 20 percent of our revenue. Intel's commitment to innovation is constant, particularly as we advance our manufacturing process. In 2021, Intel increased our historical investment in R&D even further to $15.2 billion. Additionally, we are committed to on-going investments in domestic semiconductor manufacturing capabilities as evidenced by our announced investments of over $43 billion in manufacturing operations in Ohio, Arizona, Oregon and New Mexico.

To enable and enhance investments into R&D, which is connected to the technology development intrinsic to our manufacturing, the U.S. must also create a supportive business environment for R&D. While the federal R&D tax credit is important, innovation is harmed under the current tax law. As of 2021, businesses must forgo the immediate deduction of their current year R&D investments and amortize those investments over several years. This tax change makes the U.S. one of two countries with this negative policy. Congress must act quickly to restore the immediate ability to deduct R&D expenses which had been in the law since 1954.

Amortizing R&D expenses discourages on-going investment in innovation. In fact, according to a 2019 EY report,[8] amortizing R&D spending would lead to the loss of over 20,000 U.S. R&D jobs in the first five years, with that number increasing to nearly 60,000 in the following five years. The ability to deduct R&D expenses is directly tied to investments and jobs. We applaud the bipartisan efforts of Congress to correct this policy and urge Congress to pass H.R. 1304 as soon as possible.

[8] EY "Impact of the amortization of certain R&D expenditures on R&D spending in the United States" (Oct. 2019), available at https://investinamericasfuture.org/wp-content/uploads/2019/10/EY-RD-Coalition-TCJA-R-and-D-amortization-report-Oct-2019-1.pdf.

For Intel, which maintains most of its R&D in the United States, the ability to innovate is directly tied to improving and enhancing our manufacturing process and advanced packaging technologies, as we move to smaller and smaller chip nodes. The immediate deduction of R&D expenses is critical to that endeavor. Semiconductors are a critical component in fueling innovation and enabling technology from medical equipment to smart phones to clean energy.

6. In your testimony, all of you have in one way or another talked about workforce challenges. These factories required highly skilled workers that can't just be plucked off the streets. But we also know that the STEM workforce already has a diversity issue and that challenge only worsens when you look at those with the master's and Ph.D. level degrees. This committee has spent a lot of time talking about the diversity issue in the STEM workforce under the leadership of our chairwoman. Some of you noted examples of efforts to diversify the STEM field, including working with HBCU's and MSI's but do you agree we would need to significantly scale up those investments to generate the types of workforce that you all need? And even without the federal government scaling up its efforts, are your companies/universities/organizations planning to scale up efforts to get a more diverse STEM workforce?

Answer:

Intel is deeply committed to expanding diversity and inclusion within its own workforce, as well as the semiconductor industry more generally. As noted in my written testimony, Intel has engaged in various collaborations with Historically Black Colleges and Universities (HBCUs) and other Minority-Serving Institutions (MSIs) to expand STEM education opportunities for underrepresented groups and further diversify the talent pipeline for Intel and the industry. Intel is also collaborating with community colleges across the country to expand and diversify the pipeline of technicians and other highly trained workers needed to maintain and operate semiconductor factories and packaging facilities.

These initiatives are already paying dividends, but they need to be scaled significantly to meet the industry's quickly escalating workforce needs. Educational institutions and other industry partners are now leveraging Federal, state, and local incentives where available to create new programs and scale existing ones. For its part, Intel recently announced an investment of $100 million in various federal and regional initiatives to expand and accelerate workforce development efforts, in conjunction with our decision to invest at least $20 billion to build new fabrication facilities in Ohio. Among other things, Intel is working to further develop educational and training curricula to meet the industry's needs and to partner with community colleges, research institutions, HBCUs, other MSIs, and other education stakeholders to scale these programs. Intel is also collaborating with industry stakeholders to develop a registered apprenticeship pilot program that can be scaled if successful. Additional federal, state, and local funding, however, will be critical to match the accelerating pace of workforce demands.

U.S. HOUSE OF REPRESENTATIVES
COMMITTEE ON SCIENCE, SPACE AND TECHOLOGY

Questions for the Record to:
Dr. Ann Kelleher
Executive Vice President and General Manager, Technology Development
Intel Corporation
Submitted by Representative Susan Wild

1. For the record, I would like to follow up on my question from the hearing regarding how higher education institutions can partner with states and local industries to capitalize on regional strengths and contribute to our domestic microelectronic supply chain.

   Dr. Kelleher, from your perspective as a leader at Intel, what are some ways your company has found success in workforce development through partnerships with community colleges, specifically, or other academic institutions, generally? Could you speak to any new or innovative workforce development strategies you would like to see industry pursue with higher education institutions?

Answer:

Intel has found great success by partnering with educational institutions, including community colleges, around the country. For example, Intel has helped the Portland Community College (PCC) in Oregon establish an extremely successful Microelectronics Technology program.[9] Intel regularly hires individuals graduating from this program and often hires most of its graduates each year. The PCC program is frequently used as a model for other educational institutions seeking to create similar offerings.

Along with Dell Technologies, Intel has also successfully partnered with community colleges to create and expand artificial intelligence (AI) education programs around the country. The AI for Workforce program launched in the fall of 2020 at Maricopa Community College (MCC) in Arizona and has since expanded to 31 schools across 18 states. In December, the American Association of Community Colleges announced a new partnership with Intel and Dell to further expand the program to all 50 states by 2023.[10] And as detailed in my written testimony, Intel has also successfully partnered with HBCUs and other MSIs to expand STEM education opportunities for traditionally underrepresented groups in the industry.

Intel is currently working to scale the above initiatives, including by expanding the number of community colleges offering instruction in microelectronics and related fields. Intel is also collaborating with a range of industry stakeholders to pilot a registered

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[9] *See* Portland Community College, *Microelectronics Technology*, https://www.pcc.edu/programs/microelectronics/.
[10] *See* American Association of Community Colleges, *American Association of Community Colleges Joins Hands with Intel and Dell Technologies to Advance Education in Artificial Intelligence*, https://www.aacc.nche.edu/2021/12/16/american-association-of-community-colleges-joins-hands-with-intel-and-dell-technologies-to-advance-education-in-artificial-intelligence/.

apprenticeship program for the industry in select locations, with the hope that such a program could be scaled in the future if successful.

Responses by Mr. Manish Bhatia

U.S. HOUSE OF REPRESENTATIVES
COMMITTEE ON SCIENCE, SPACE AND TECHOLOGY
Questions for the Record to:
Mr. Manish Bhatia
Executive Vice President, Global Operations
Micron Technology, Inc.
Submitted January 27, 2022

Submitted by Chairwoman Eddie Bernice Johnson

1. **The semiconductor industry faces significant environmental challenges. It both contributes to and is affected by climate change. Climate change has harmed semiconductor production around the globe, adding to supply chain delays. For example, in February 2020, a cold snap in Texas created power outages that severely impacted semiconductor manufacturing in the state, leading to a months-long backup in production. In the context of increasing concerns regarding resiliency, sustainability, and climate impact, how have climate-related events impacted Micron, and how is Micron addressing the impact its business has on the climate?**

   Micron proactively mitigates climate-related and other supply chain risk through thoughtful contingency planning and diversification of its supply chain. However, climate-related events have impacted Micron in recent years. For example, in the early months of 2021, we faced a drought in central Taiwan, which resulted in a reduction in the water supply for one of our DRAM fab sites. To mitigate the water shortage, we accelerated our water conservation efforts and secured alternative sources of water and did not see an impact to DRAM production output. As part of our broader sustainability goals, we are aggressively working to improve efficiency and resiliency across all of our operations.

   Micron is determined to achieve net zero impact on our planet. Being a technology leader, we develop products that use ever increasing process complexity at the leading edge, with thousands of steps, so we are continuously striving to find more efficient ways to operate our facilities and build our products. We are committed to ensuring that all our facilities meet our rigorous sustainability standards for energy, water, waste, and emissions throughout their operation cycle. By 2030, we expect to achieve a 75% reduction in emissions intensity, with the ultimate goal of achieving full carbon neutrality. This effort will be driven by our goal to achieve full reliance on renewable energy, beginning with our commitment to reach 100% renewable energy for our U.S. operations by 2025. We are also diligently working to ensure the full reuse and recycling of water and waste in all our sites. In our state-of-the-art research and development facility in Boise, Idaho, we are able to reclaim 75% of all process water thanks to innovative solutions.

   We believe that our ambitions are realistic and can be attained by partnering with our materials and equipment suppliers to develop new technologies which require fewer resources and consume less energy and produce fewer emissions and waste. In addition, as in other areas, Micron also recognizes the potential for collaboration with the communities that host our sites. We partner with these communities to encourage investment into environmental sustainability. We recently partnered with Prince William County in Virginia to install a Bandalong Litter Trap, a floating trash collector to keep trash out of county waterways.

   Finally, we are grateful that our sustainability efforts have been consistently recognized, including through the Dow Jones Sustainability Index, Newsweek's list of America's Most Responsible Companies, the Carbon Clean 200, and with the Responsible Business Alliance Platinum award.

Submitted by Representative Jamaal Bowman

1. **If the government is going to play a more active role in supporting domestic chip production, and if one of our goals is to prevent future shortages and bottlenecks, it strikes me that we should be doing comprehensive monitoring of semiconductor supply chains. That way, when we're talking about giving public subsidies to very profitable corporations, we can make more informed decisions about what kind of interventions are necessary and helpful, and we can also try to anticipate problems. As far as I'm aware, there is very limited *public* data on semiconductor supply chains available at present. What kind of data does your company use when determining investment plans or supplier relationships? And what data could your company provide that would help the government do better strategic planning?**

   Micron relies on a variety of factors to develop our investment plans and supply chain partnerships, including customer demand forecasts, evaluation of secular market trends, memory technology roadmaps, and clean room capacity requirements. Because of the long lead times involved in building, equipping and ramping production in new clean rooms, Micron takes a long-term view that goes out 5 to 10 years as we plan our manufacturing footprint. Through successful long-term planning for manufacturing capacity, Micron has been able to continuously implement our leadership technology roadmap throughout the last 24 months and ensure supply continuity for our customers. As a result, the primary bottlenecks in the semiconductor supply chain have not been from Micron. We would like to use our experience and expertise to bring the memory supply chain to the United States.

   The large scale of manufacturing required for memory, coupled with long lead times to build and equip a factory and higher costs in the United States are why it is so important for Congress to fund the CHIPS Act and pass an Investment Tax Credit for semiconductors. This will help ensure that large semiconductor producers invest with confidence in the long-term requirements for manufacturing such that the U.S. economy is not impacted severely by a chip shortage in the future. Additionally, global competition for domestic manufacturing capacity is strong, as support mechanisms, subsidies and incentives have been in place for the past two decades in all countries where we operate. A sustained and scalable incentive such as the Investment Tax Credit would help ensure the United States is competitive.

   In establishing supplier relationships, we are also proud to have established a supplier diversity program in 2019 with the aim of building mutually beneficial partnerships with diverse suppliers, referring to businesses that are majority owned by women, underrepresented communities, people with disabilities, members of the LGBTQ+ community, and veterans. As part of our goal, Micron has joined the National Minority Supplier Development Council, which aims to advance business opportunities for certified minority owned businesses, as well as the National Gay and Lesbian Chamber of Commerce (NGLCC).

Recognizing our impact as a large-scale global business, we also ask our partners to implement their own supplier diversity programs and make efforts to engage diverse businesses in support of Micron contracts. These expectations are embedded in Micron's Supplier Responsibility Expectations and Supplier Performance Management processes. In addition, as a corporate member of SEMI's Manufacturing Ownership Diversity working group, we are actively working with our peers in the industry to develop best practice standards in supplier diversity and drive adoption across our industry

The supplier diversity program has so far been a remarkable success. By the end of 2021, Micron has already tripled annual spending with diverse suppliers compared to our baseline of $104 million in FY2020.

We were pleased to provide a detailed report on our supply chain considerations in response to the Secretary of Commerce's "Request for Public Comments on Risks in the Semiconductor Supply Chain" published in September 2021, and would welcome the opportunity to discuss these issues further.

Submitted by Representative Gwen Moore

To help increase the number of semiconductor manufacturing facilities in our country, a highly educated workforce is a key requirement. But that could also limit the places where these facilities could be located meaning vast parts of our country may not benefit from the robust investments in the CHIPS for America Act – even places that have a strong history of manufacturing and high numbers of available workers. When Micron is considering where in the U.S. to place any new facilities, what are the factors it is taking into account, including when it comes to workforce availability and training?

When considering investments in new facilities, Micron takes into account a wide range of factors, including site suitability, labor availability, operational costs, and other community considerations.

As I discussed in my testimony, there is a shortage of both advanced science and engineering talent as well as skilled labor in the United States. Because of this, Micron invests heavily in the communities where we operate to help build the workforce that is required to support the advanced R&D and manufacturing requirements of our leading edge facilities. For example, to build the workforce we need for our fab in Virginia and world-class research center in Boise, Micron partners closely with academic institutions at all levels—K-12, community colleges, and universities. We work with them to build curricula, provide internships and scholarships and the equipment and materials students need to prepare for work in today's industry, and help onboard them into long-term careers. We also partner with various organizations on reskilling programs, including those focused on veterans, underrepresented groups, unemployed and underemployed adults, to transition high potential individuals into the industry.

The workforce challenge requires a national response. I urge Congress to continue to expand funding to increase STEM education at all levels, enable the expansion of vocational programs at community colleges, promote re-skilling programs, and facilitate public-private partnerships to train and employ new entrants in the industry. For example, Micron partnered with Year Up and Northern Virginia Community College (NOVA) to create a Fab Lab and a Mechatronics A.A.S. and Certification, which is promoted for underrepresented and unemployed/underemployed young adults.

A new semiconductor cluster for memory in the United States would create tens of thousands of highly skilled, high paying jobs and Micron stands ready to work with the region where this potential site could be located to ensure workforce development is prioritized.

1. **How can we ensure that a new federal grant program to incentivize new domestic semiconductor manufacturing facilities and workforce development is allocated in manner that does not favor some jurisdictions over others? What role do you think the Department of Commerce should play in overseeing the distribution of the funds to ensure that all interested jurisdictions and entities can participate or be able to compete in an unbiased competition?**

Growing the U.S. semiconductor workforce is a national challenge requiring a nationwide response. Micron encourages the Department of Commerce to expand access to training, education, and re-skilling programs across the country.

Investments in manufacturing facilities, however, must be directed to locations that provide the conditions for long-term economic success. For example, in assessing site suitability for manufacturing facilities, Micron takes into account a wide range of factors, including site suitability, labor availability, operational costs, and other community considerations. For a fab operation to be feasible and successful, a location must undergo rigorous evaluation in all of these areas.

Further, in considering investments, we should consider the laws of comparative advantage, focusing on areas where the United States can lead in a commercially viable manner in the long-term, while allowing allies to take the lead in areas where they are better suited. To that end, the United States should invest in leading edge process technologies and manufacturing—areas with the highest rate of change and highest level of complexity (capital intensity). Investments should be on leading edge technologies, given the longer lifecycle, lower risk of obsolescence and longer time to secure a return on investment.

At the same time, the U.S. Government should ensure that its investments in a given project are sufficient to ensure long-term viability and competitiveness in the global marketplace. U.S. Government investments in domestic industry must take into consideration the longstanding, substantial investments by Asian governments in their own countries' manufacturing capacity, as well as the 35-45 percent differential in operating costs between the United States in Asia.

The Department of Commerce should work closely with U.S. industry to determine which investments will yield the greatest advances for U.S. leadership in the semiconductor industry and which provide the greatest likelihood of long-term economic success. Successful and sustainable investments in new manufacturing facilities will benefit the national security and prosperity of the United States as a whole over the long term.

2. **Workforce-related challenges including insufficient numbers of U.S. workers with the skills and training can be addressed by developing new programs, in conjunction with academic facilities, but training people takes time. How might such workforce challenges or any workforce gaps be addressed in the short term?**

   While building a skilled domestic semiconductor workforce requires generational investments starting with early STEM education, Micron has also seen success in leveraging re-skilling programs on shorter timelines. Over the years, these programs have helped us transition high potential individuals into the semiconductor industry and set up local pipelines capable of working in manufacturing. We have promoted these programs across underrepresented and unemployed/underemployed groups as well as veterans, retraining them with relevant in-demand industry skillsets. Micron urges Congress to expand funding for such reskilling programs at the same time as it invests in the long-term growth of the U.S. engineering workforce.

3. **In your testimony, you discussed Micron's partnerships with academic intuitions of all levels, —K-12, community colleges, and universities – to prepare students for jobs in the semiconductor industry and reskilling programs. How successful have your reskilling efforts been, what is the target population for those efforts, and do you think those efforts can be scaled up at the levels that many communities will need to help generate your workforce?**

   A primary focus of our reskilling efforts has been on underrepresented and unemployed/underemployed groups as well as veterans. In the case of veterans, Micron has found that many of the technical skills that servicemembers in certain specialties develop are also strong foundations for success at Micron. Over the years, we have recruited significant numbers of former servicemembers. Once part of Micron, they are able to rely on our Veteran Employee Resource Group to receive critical professional support as they transition from active duty to a career at Micron.

   In addition, in conjunction with the Department of Defense's SkillBridge program for exiting military personnel, Micron strives to ensure that servicemembers transitioning to civilian life can also benefit from our broader academic partnerships, as illustrated by our work with Norfolk State University (NSU), a historically black university. Micron has installed a Nanofabrication Cleanroom at NSU, making it one of the few dozen academic institutions in the world with a cleanroom. The cleanroom has been made available for the use of not only NSU students, but also by participants in the SkillBridge program. With strong support from the federal government, efforts to serve exiting and former servicemembers can be scaled up across the industry. Reskilling programs are a critical element of a comprehensive workforce investment program, but will not alone be sufficient; the United States should couple them with investments in K-12, community colleges, and universities across the country.

4. **Mr. Bhatia, in your testimony, you recommended that Congress provide a refundable investment tax credit to support semiconductor manufacturing. Please explain why you think such a tax credit in addition to grants is an important tool. Also, do you think that the current research and experimentation tax incentives adequately drive microelectronic innovation? Can or should existing tax incentives also be improved to better support truly innovative developments at the earliest stages of conception?**

Current cost to build and operate a fab at scale in the United States is 35-45% higher than at our existing sites in Asia. Costs are lower in Asia in part because of lower native costs such as labor but also because there is a large semiconductor ecosystem in Asia where significant semiconductor manufacturing capacity exists today. Asian governments have pursued semiconductor investments for years with aggressive financial incentives in the form of grants and other subsidies that reduce costs for a company to both build and to operate in that respective country. To compete, the United States must offer comparable incentives in the form of grants, refundable investment tax credits or some combination of both in order to bridge both the construction and operating cost differences. The CHIPS grant program as envisioned currently will help to bridge the cost differential between the United States and Asia in upfront start-up costs, but the refundable investment tax credit is needed to bridge the differential in ongoing costs to operate a fab in the US as compared to Asia.

A refundable investment tax credit will also provide an equitable and efficient means to allocate government funds toward strategic projects with the greatest potential to have long term, sustained, high value impact on domestic semiconductor self-sufficiency. The Investment Tax Credit is a tool for the government to provide a certain and scalable form of support for semiconductor producers to invest in the long term requirements for semiconductor manufacturing to ensure reliable supply. Additionally, global competition for domestic manufacturing capacity is strong, as support mechanisms, subsidies and incentives have been in place for the past two decades in all countries where we operate. A sustained and scalable incentive such as the Investment Tax Credit would help ensure the United States is competitive.

As I discussed in my testimony, Micron invests substantially in R&D. In our fiscal year 2021, R&D spending was nearly $3 billion and we plan to increase that by about 15% in 2022. We have consistently expanded our Technology Innovation Center of Excellence in Boise, Idaho over the past decade. We're also proud to partner with the Departments of Energy and Defense, as well as the National Science Foundation, on leading-edge research initiatives that will further drive technology leadership and fuel technologies of the future. The results of this commitment to innovation are clear; Micron is responsible for nearly 50,000 patents and counting, deploys new technology innovations and associated products at least every two years, and currently produces the world's most advanced memory and storage solutions. Existing research and experimentation tax incentives have been critical to our success.

Innovation in microelectronics requires commitment to both foundational research itself and the process of transition the foundational research ideas to manufacturing and commercialization—i.e., crossing the "valley of death." Current U.S. research and

experimentation tax laws requiring companies to capitalize, and therefore delay deducting. Such expenditures disincentivize companies from making the investments necessary for the US to continue leading in microelectronic innovation. The U.S. Government can help by enacting legislation to replace the existing rules requiring capitalization with rules that allow for immediate expensing.

To drive truly innovative developments in microelectronics, the United States should increase the R&D credit percentage for expenditures incurred for microelectronics research. Alternatively, the United States could include R&D expenditures as a qualifying investment for the refundable investment tax credit.

5. **In your testimony, all of you have in one way or another talked about workforce challenges. These factories required highly skilled workers that can't just be plucked off the streets. But we also know that the STEM workforce already has a diversity issue and that challenge only worsens when you look at those with the master's and Ph.D. level degrees. This committee has spent a lot of time talking about the diversity issue in the STEM workforce under the leadership of our chairwoman. Some of you noted examples of efforts to diversify the STEM field, including working with HBCU's and MSI's but do you agree we would need to significantly scale up those investments to generate the types of workforce that you all need? And even without the federal government scaling up its efforts, are your companies/universities/organizations planning to scale up efforts to get a more diverse STEM workforce?**

Yes, we believe that the federal government has an irreplaceable role to play in investing in and nurturing the development of an expanded STEM workforce that genuinely reflects America's diversity. Significantly scaling up these investments would ensure that our industry has domestic access to the human capital that we need to remain internationally competitive against our rivals. Without a concerted, government-supported effort to improve STEM workforce availability and diversity at our U.S. universities and colleges, we expect that workforce shortages will continue — and these impacts will worsen. We therefore call upon Congress to increase funding to enhance STEM education at all levels and for diverse elements of the population, enable the expansion of vocational programs at community colleges, promote re-skilling programs, and facilitate public-private partnerships to train and employ new entrants in the industry.

Micron intends to strengthen our efforts to support groups that are underrepresented in the STEM workforce by providing them with the opportunity to develop the technical skills and expertise that they need in order to successfully join the workforce. Currently, through the Micron Gives STEM Education program, Micron works to foster a passion for STEM fields among underrepresented students each year. The program includes several initiatives specifically targeting women, including the "Girls Going Tech" initiative focusing on younger students and the "Women in Technical Career Events" initiative tailored to students Grades 9-12. Micron also runs a "Rural STEM" initiative aimed at helping students in rural communities gain a deeper understanding of STEM disciplines.

We are deliberate and proactive in our efforts to foster a diverse and supportive environment for employees of all backgrounds, genders, and sexual orientations. In fact, we were proud to have recently been named on the list of the Forbes magazine's Best Employers for Diversity. Additionally, many Micron employees serve on several K-12 education foundation boards and higher education Career & Technical Education (CTE) advisory boards.

Submitted by Representative Susan Wild

1. **For the record, I would like to follow up on my question from the hearing regarding how higher education institutions can partner with states and local industries to capitalize on regional strengths and contribute to our domestic microelectronic supply chain. Mr. Bhatia – from your perspective as a leader at Micron, what are some ways your company has found success in workforce development through partnerships with community colleges, specifically, or other academic institutions, generally? Could you speak to any new or innovative workforce development strategies you would like to see industry pursue with higher education institutions?**

Recognizing the critical importance of a highly-skilled workforce for the successful operation of our fab facilities across the United States, Micron has partnered closely with academic institutions at all levels—K-12, community colleges, and universities. Micron employees work with these institutions to strengthen curricula and provide the internships, scholarships, and equipment and materials that students need in order to prepare themselves to join our industry. We also help provide students with the onboarding support they need to begin long-term careers, as well as partner with reskilling programs to identify high-potential candidates and transition them into the industry. Micron's partnership with the Northern Virginia Community College (NOVA) provides an illustrative example of how tech firms can successfully partner with community colleges. Micron representatives serve on NOVA's board, and over the years we have provided financial and technical support to a series of initiatives at the college, including the creation of a Fab Lab and the development of a new Mechatronics Associate of Applied Science Degree and Certification program. Micron has also helped promote these opportunities to underrepresented groups as well as unemployed or underemployed young adults.

Micron also takes pride in collaborating with associations and institutions representing underserved groups such as the Society of Women Engineers, the Society of Hispanic Professional Engineers, and the National Society of Black Engineers, as well as Historically Black Colleges and Universities, to determine how Micron can best contribute to these groups' leadership in cultivating a STEM workforce that truly represents our country. We have also found that highlighting the potential for STEM skills to contribute to social good has been an effective avenue to spur interest in the field. Since 2015, we have partnered with the University of Washington to administer a program where students and researchers can work together to apply data science toward social causes of their own choosing. Micron has also set up a $1 million grant program to support students that are using AI in research projects that are aimed at benefiting society.

Based on the success of our initiatives, I believe that greater federal funding to support STEM education could make a tremendous impact on building a workforce that our country needs to grow and remain competitive in the future. I urge Congress to continue and expand funding to increase STEM education at all levels, enable the expansion of vocational programs at community colleges, promote re-skilling programs, and facilitate public-private partnerships to train and employ new entrants in the industry.

Responses by Dr. Michael Witherell

Lawrence Berkeley National Laboratory
One Cyclotron Road
Berkeley, CA 94720

Responses to Questions for the Record from the December 2, 2021, hearing "*Ensuring American Leadership in Microelectronics*"

Submitted by Representative Gwen Moore (D-WI)

1. In your testimony, all of you have in one way or another talked about workforce challenges. These factories required highly skilled workers that can't just be plucked off the streets. But we also know that the STEM workforce already has a diversity issue and that challenge only worsens when you look at those with the master's and Ph.D. level degrees. This committee has spent a lot of time talking about the diversity issue in the STEM workforce under the leadership of our chairwoman. Some of you noted examples of efforts to diversify the STEM field, including working with HBCU's and MSI's but do you agree we would need to significantly scale up those investments to generate the types of workforce that you all need? And even without the federal government scaling up its efforts, are your companies/universities/organizations planning to scale up efforts to get a more diverse STEM workforce?

LBNL Response:

Diversity in all forms, across educational and professional levels, is urgently needed to support future U.S. leadership in the field of microelectronics and more broadly across STEM disciplines. The nation will not be able to address the national challenges in health, energy, the environment, or economic competitiveness unless we all do a better job of preparing our young people for the critical jobs, and then recruiting them. The Berkeley Lab actively promotes diversity in its STEM education and workforce development activities at all levels. Further, we are examining new approaches to grow the diverse workforce necessary to effectively carry our mission into the future.

At the K-12 level, we have been expanding our efforts to develop and implement programs to connect our researchers to Bay Area students with the goal of generating excitement about STEM relevant to the Lab's mission. We concur that scaling-up such opportunities is necessary to yield a sufficient microelectronics workforce, as well as to advance the wide range of scientific fields that are important to the Lab. SEMI is an industry association representing more than 400 U.S.-based companies across the microelectronics design and manufacturing supply chain. At their December 2021 NIST/OSTP Microelectronics Roundtable it was pointed out that the diversity of our STEM students narrows dramatically in the transition from K-12 to college. More must be done to engage at the K-12 level so that diverse students are willing to enroll in STEM programs in college. New resources must support vocational education to create a diverse manufacturing workforce as well as exposure to research opportunities to develop our scientific and engineering workforce.

The recently established National Lab Education Council brings together education staff from across the complex and provides an opportunity to expand efforts and address barriers to STEM participation from an urban, rural and suburban perspective. This group recently developed a Pre-College Research Internship and Mentoring Experiences (PRIME) proposal, which if supported by Congress and DOE, would address technical gaps in skills and experiences between the high school and postsecondary levels.

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Responses to Questions for the Record from the December 2, 2021, hearing "*Ensuring American Leadership in Microelectronics*"

Berkeley Lab also has a set of programs offered at the pre-college, undergraduate, post-baccalaureate, and graduate levels that promote equal access to scientific and technical education in relevant fields. We support efforts to provide new resources to cross-cutting DOE workforce initiatives as a means of strengthening the pathways leading to careers in microelectronics and other STEM fields.

One of the most effective ways of increasing the diversity of the scientific workforce is to do a better job of recruiting and supporting Ph.D. scientists and engineers at the start of their careers. We have developed new programs in the last few years to support and mentor our postdoctoral researchers, keeping in mind the additional challenges that face those researchers who come from underrepresented and economically disadvantaged backgrounds.

The Berkeley Lab has an active Inclusion, Diversity, Equity, and Accountability (IDEA) program designed to support and enhance efforts across the organization to attract, develop, and retain diverse talent. The IDEA approach includes partnering with existing STEM pipeline-building programs targeting all educational and career stages as well as refining and amplifying outreach efforts.

While the Lab has active diversity and STEM education programs at all levels and is actively looking to build upon those efforts, we and the country have a long way to go to meet the national challenge. Historically, the DOE Labs were only supported for modest STEM education and workforce programs compared to other large federal science agencies. Additional investments would enable us to take those activities to a scale that meets our research needs, and we have the capabilities to obtain a good impact from such investments.

Submitted by Representative Susan Wild (D-PA)

1. For the record, I would like to follow up on my question from the hearing regarding how higher education institutions can partner with states and local industries to capitalize on regional strengths and contribute to our domestic microelectronic supply chain.

   Dr. Witherell, I appreciate your responses regarding how user facilities can partner with universities to help researchers develop their skills or to develop breakthroughs in microelectronics. I would like to ask if you have any other ways or strategies in which four year universities or community colleges could partner with federal, state, or private institutions to utilize or build upon regional capacities regarding the microelectronics supply chain?

LBNL Response:

Collaborative new approaches are needed to attract and train a much larger and more diverse workforce that is needed for the U.S. semiconductor industry to grow, leveraging community and

technical colleges, four-year universities, national laboratories, and companies across the microelectronics supply chain.

Universities and community colleges offer degree-oriented educational programs, while the national labs and companies offer complementary experiential learning opportunities and practical hands-on skills training. The American Semiconductor Academy (ASA) Initiative brings together four-year universities and community colleges to collaborate with each other and to collectively partner with industry to revitalize the semiconductor microelectronics curriculum and to coordinate hands-on training experiences for students at a local university, national lab or company R&D facility. This Initiative is driven by faculty across the nation who are engaged in semiconductor research and education at more than 50 universities, plus their community college partners. SEMI, an industry association representing more than 400 U.S.-based companies across the microelectronics design and manufacturing supply chain, is partnering with the ASA Initiative to bolster workforce education and training programs to grow and diversify the talent pool for the U.S. semiconductor industry. This partnership will build upon federally funded programs such as the Department of Energy's Minority-Serving Institution Partnership Program (MSIPP), the National Science Foundation's Advanced Technological Education (ATE) program, and the Department of Defense's Scalable Asymmetric Lifecycle Engagement (SCALE) program. It should be noted that the ASA is planned to be an independent and inclusive national semiconductor education and training network, open to all U.S. universities and colleges to participate, and to industry and government stakeholders to partner with. This initiative has been endorsed by over 30 companies, including the leading U.S. semiconductor manufacturing companies. **Congressional appropriation of workforce development funding to establish the ASA would grow the pool of talent for the U.S. semiconductor industry with the greatest speed, scale, and impact.**

Funding of the Micro Act, as part of the effort to provide emergency appropriations for implementation of the CHIPS Act, would also further education and outreach activities to boost the microelectronics workforce.

The Department of Energy Office of Science is also carrying out internal workforce development activities that could be amplified with new resources.

It would indeed be valuable to the nation to further these efforts as part of a comprehensive approach to boost the U.S. semiconductor industry.

Responses by Dr. Mung Chiang

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The Honorable Eddie Bernice Johnson
Chairwoman
Committee on Science, Space, & Technology
United States House of Representatives

The Honorable Frank Lucas
Ranking Member
Committee on Science, Space, & Technology
United States House of Representatives

Dear Chairwoman Johnson and Ranking Member Lucas,

I am writing in response to your letter of January 13, 2022 to provide responses to the questions posed by Representatives Gwen Moore and Susan Wild, and also to provide supplemental information regarding the semiconductor workforce initiatives that are addressing challenges identified by both government and industry, which are related to my testimony during the House Science Committee hearing on December 2, 2021 on *Ensuring American Leadership in Microelectronics*. I would like to highlight two relevant programs: The Scalable Asymmetric Life Cycle Engagement (SCALE) and the American Semiconductor Academy (ASA) initiative. Attached for reference are overviews of ASA and SCALE.

SCALE is a preeminent public-private-academic partnership coordinated by Purdue University on behalf of the Department of Defense. Together with over a dozen university partners across the country, SCALE aims to develop a highly skilled domestic microelectronics workforce, and to motivate talented STEM undergraduate and graduate students to embrace a career pathway in the Federal Government that will involve advancing critical semiconductor technology.

The SCALE model was developed to be an immersive educational program that combines government/defense industrial base internships with aligned research and mentoring. A consortium-based approach was used to achieve national reach to universities in targeted technical areas for scaling and replication of the program, while allowing a regional focus. The program was designed to be: scalable to multiple universities, replicable to additional microelectronics topics important to the federal government and industry, and asymmetric in its effect in training US students in areas of high need.

To address the critical need for workforce to support an expanded U.S. microelectronics industry, it is imperative that we further expand participation in the SCALE network, fund the initiative at a minimum of $600 million over a five-year period while expanding its scope, and ensure other current or future complimentary semiconductor workforce efforts supported by the federal government are aligned to ensure maximum success.

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In addition to successfully executing the mission of the SCALE program, Purdue University is pleased to collaborate with other existing and proposed public-private partnerships focused on supporting not only semiconductor workforce development, but also advancing semiconductor technology.

Purdue is co-leading the planning for **ASA**, which represents faculty from universities across the U.S. who encourage Congress to fund the U.S. Competitiveness and Innovation Act (USICA), especially the legislative provisions related to Creating Helpful Incentives for the Production of Semiconductors (CHIPS) for America Act, to appropriate funding to support a nationwide network of universities and colleges, such as an American Semiconductor Academy, to collaborate in addressing the urgent and growing workforce development needs of the U.S. semiconductor industry.

The ASA is a nationwide education and workforce development program implemented by a network of universities and colleges – including community colleges – geographically distributed across the U.S., organized into Western, Central, and Eastern Regions. ASA will increase and broaden access to education and technical training for careers in semiconductor manufacturing, to fill the pipeline of talent for chip manufacturers in the U.S.

ASA will increase and broaden access to education and technical training for careers in semiconductor manufacturing, to fill the pipeline of talent for chip manufacturers in the U.S. A revitalized curriculum in integrated circuit and systems design, semiconductor materials, devices and microfabrication technology will be developed jointly with the semiconductor industry and shared across the ASA network, to facilitate education of a broad diversity of undergraduate and graduate students, to prepare them to enter the U.S. semiconductor manufacturing workforce.

Purdue University is also a long-time partner of the **Semiconductor Research Corporation** (SRC), leading a number of its flagship centers in partnership with DARPA, NIST, and NSF, spanning the last four decades. SRC is a world-renowned, high technology-based consortium that serves as a crossroads of collaboration between technology companies, academia, government agencies, and SRC's highly regarded engineers and scientists. Through its interdisciplinary research programs, SRC plays an indispensable role in addressing global challenges, using research and development strategies, and advanced tools and technologies. Members of SRC work synergistically together to gain access to research results, fundamental IP, and highly experienced students to compete in the global marketplace and build the workforce of tomorrow. More than 20 premier semiconductor companies are members of SRC, partnering with more than 100 universities and multiple government agencies to advance semiconductor technology while supporting the semiconductor workforce.

Rebuilding the semiconductor production capacity will require a skilled workforce of all levels, ranging from technicians through engineers and scientists, and a similarly diverse network of universities/colleges and curricula to provide these talents. To address the critical need for workforce to support an expanded U.S. microelectronics industry, it is imperative that we engage universities and colleges across the nation in a network as modeled by ASA and SCALE.

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Such an educational network should:

- be an independent, neutral, not-for-profit platform that is broad, inclusive, and geographically diverse,
- be advised by companies across the semiconductor ecosystem to modernize the microelectronics curriculum,
- have the appropriate infrastructure and online platforms to provide meaningful laboratory experiences as part of the curriculum,
- make curricular materials, training facilities and industry-standard tools accessible to all participating schools, and
- coordinate practical, uniquely critical to the semiconductor industry, hands-on training ("tech apprenticeships"), for students who have successfully completed the prerequisite courses.

There should be an open and competitive process to participate in this education and training network. Participating schools should be held accountable to increase the number of graduates who enter the U.S. semiconductor manufacturing workforce, in proportion to the level of funding they receive. SCALE participants intend to coordinate closely with the proposed ASA network to avoid duplication of efforts, while fully supporting industry's workforce needs, alongside those of the federal government.

Following are the answers for the record to the three questions submitted.

Questions Submitted by Representative Gwen Moore

1. Workforce-related challenges including insufficient numbers of U.S. workers with the skills and training can be addressed by developing new programs, in conjunction with academic facilities, but training people takes time. How might such workforce challenges or any workforce gaps be addressed in the short term?

Indeed, there is a critical shortage of microelectronics talent now, and it will only get worse as we expand semiconductor manufacturing. Workforce development strategies must address both short and long-term challenges.

Four strategies can be successful in the short term:
1) leverage the rapidly growing STEM enrollments at public universities;
2) scale-up online training programs;
3) quickly engage community colleges and high schools; and
4) take advantage of the skilled workforce that our nation already has (e.g. in the armed services).

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With regard to strategy 1), most engineering colleges are currently experiencing rapidly growing enrollments, but as microelectronics manufacturing has been out-sourced over the past three decades, student awareness of the possibilities for exciting, impactful careers in microelectronics has declined. Students hear about artificial intelligence, data science, self-driving automobiles, precision agriculture, industry 4.0, etc., but most don't realize how critically dependent they are on semiconductors. Today's students generally see "semiconductors" as an old and mature field and don't realize the fast pace of innovation as a new era of microelectronics begins. Simply making the growing number of STEM students aware of the career opportunities in semiconductors can have short term impact. At Purdue, we are introducing minors and concentrations in semiconductors for undergraduate students. When coupled with internships provided by industry partners, we can make many more students aware of what a career in microelectronics can offer. These programs can include financial incentives such as scholarships, fellowships and access to free training programs for students who enroll or complete semiconductors courses. We believe that this approach will produce results quickly.

With regard to strategy 2), there is much that can be done to provide training through online programs and virtual tools. Purdue is home to the NSF-funded nanoHUB, an online resource for simulation, education, and collaboration created more than 25 years ago with a mission to lower the barrier to accessing and using sophisticated computer-aided-design (CAD) tools. Users can log in and run industry-strength CAD tools without the need to download, install, license, support, or maintain the software. The educational resources that support these tools have proven to be popular. Today, nanoHUB has more than 2 million annual visitors, of which 20,000 run nanoHUB-hosted numerical simulations. The nanoHUB has great promise to support a nation-wide workforce development program by giving colleges across the nation, regardless of their size, the ability to provide their students with access to industry-standard CAD tools, virtual "hands-on" experiences, and cutting-edge educational resources. (https://nanohub.org)

Concerning Strategy 3), the need for skilled technicians is perhaps the largest need for the semiconductor workforce. The two-year educational cycle for training technicians is much shorter than for BS, MS, and PhD engineers, so results can be achieved more quickly. Again, an issue here is awareness. Young people simply aren't aware of the opportunities in microelectronics or of the fact that these are high-paying jobs. A second issue is that community college students often prefer to stay in the region where they study. Broadening the manufacturing base geographically would greatly increase the student interest in these careers.

Finally, in regard to strategy 4), we should take advantage of the skilled workforce that we have and prepare them for new careers in semiconductors. For example, the armed services continually recruit and train a workforce to maintain its sophisticated equipment. Semiconductor manufacturers find that technicians with military experience are well-suited for semiconductor manufacturing. Building on programs like SEMI's VetWorks to transition military personnel to careers in semiconductors can have immediate impact. Another relevant workforce is mid-career engineers not currently working in microelectronics. Working with companies to define certificate programs that allow these engineers to bring their skills and experience to new careers in microelectronics can also have immediate impact. A significant part of the population chooses

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not to join the workforce now; the United States Labor Force Participation Rate was lower by 1.5% in December 2021 compared to February 2020, before the pandemic. Programs should be implemented to make it easier for these people to join the workforce, such as guaranteed employment upon completion of a training program.

Programs that address the four strategies mentioned above exist in various stages across the country, but funding and coordination are imminently needed to scale them up quickly and efficiently.

2. In your testimony, all of you have in one way or another talked about workforce challenges. These factories required highly skilled workers that can't just be plucked off the streets. But we also know that the STEM workforce already has a diversity issue and that challenge only worsens when you look at those with the master's and Ph.D. level degrees. This committee has spent a lot of time talking about the diversity issue in the STEM workforce under the leadership of our chairwoman. Some of you noted examples of efforts to diversify the STEM field, including working with HBCU's and MSI's but do you agree we would need to significantly scale up those investments to generate the types of workforce that you all need? And even without the federal government scaling up its efforts, are your companies/universities/organizations planning to scale up efforts to get a more diverse STEM workforce?

Absolutely, to address the critical talent shortage in microelectronics, we must engage all of the nation. We need creativity, passion, problem solving abilities, and diverse perspectives. All the universities with STEM programs agree that it is necessary not only to scale up the net number of students trained, but to also increase the diversity of students being trained. The universities are working hard to find solutions to the lack of diversity.

Purdue was the first University to offer a Women in Engineering Program, to launch a School of Engineering Education, and was the birth place of the Society of Black Engineers. These programs are now found in myriad universities across the U.S., each local chapter bringing value to their home organization and the region they serve. These programs have a significant contribution in attracting more diverse students and supporting them through graduation, but their funding is always a challenge. Universities are working to scale up training and diversity programs by partnering with community colleges, researching best methods to recruiting and supporting diverse students. However, these efforts are costly because investments are needed up front and there is pressure to not increase tuition. While universities will continue to support these programs, sustained and sizeable governmental funding will improve their ability to attract and serve more diverse students. Besides funding for programs, we also need more scholarships for underrepresented students and increase their awareness of career opportunities in microelectronics, just as we need to do for the overall student population.

Semiconductor education is significantly more expensive than STEM education in general because of the need for expensive laboratory facilities. Large universities with suitable laboratories and significant numbers of semiconductor faculty should partner with minority

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serving institutions (MSI) to make these facilities available and to bolster the semiconductor curriculum with courses that MSI's may not have the capacity to develop. Companies also face an urgent need for a more diverse workforce. SEMI, the industry association which represents more than 400 U.S. companies, has a number of initiatives underway directed at this objective; most major companies have similar programs. The diversity challenge must be addressed by engaging a coalition of universities and companies across the nation.

Question Submitted by Representative Susan Wild

1. For the record, I would like to follow up on my question from the hearing regarding how higher education institutions can partner with states and local industries to capitalize on regional strengths and contribute to our domestic microelectronic supply chain.

Dr. Chiang, I appreciate your responses regarding how user facilities can partner with universities to help researchers develop their skills or to develop breakthroughs in microelectronics. I would like to ask if you have any other ways or strategies in which four-year universities or community colleges could partner with federal, state, or private institutions to utilize or build upon regional capacities regarding the microelectronics supply chain?

Currently, the majority of the microelectronics manufacturing in the US is concentrated in a few states. An obvious step to access a broadly dispersed workforce is to build a more distributed manufacturing capacity. This involves a collaboration across all sectors – distribution of federal incentives to support regional manufacturing, engagement of state and local governments to provide infrastructure and business support, and partnerships with regional educational institutions to offer the desired training for the local workforce.

Purdue University announced in fall 2021 America's first suite of degrees and credentials dedicated to semiconductors. This includes a new Master's degree in semiconductors and microelectronics (to be offered both on-campus and online), an undergraduate minor degree, and several online certificates. Besides the inaugural semiconductor suite of degrees announced as a response to industry demand, Purdue has already created a Work While Learning program, enabling students to work towards their degrees while working full time. A good number of companies are subscribing to this model. This is in addition to the Co-Op program (one semester working, one semester taking classes) in which companies employ the same student for 3-5 rotations. Purdue is also creating a program with Ivy Tech, one of the largest community colleges in the US, where students who successfully complete the first two years at the community college local campus benefit from guaranteed admission to Purdue to complete the remaining requirements of a four-year degree. These programs reflect a tight industry – academia collaboration and can be replicated anywhere else in the U.S.

The government, primarily through the National Science Foundation but also through other organizations, is a good source of fellowships to train graduate students. Industry also contributes a number of scholarships towards educating undergraduate students. However, we

still need significant funding to enable every deserving student to complete an education without a financial burden. Scholarships and fellowships that enable students to stay closer to home to complete their education are a very good way to revitalize regional education and train the needed workforce. The government could also give more access to graduate and undergraduate students for hands-on training at national labs, which are regionally distributed.

Thank you for giving us the opportunity to provide this additional information for the congressional record.

Sincerely,

Mung Chiang

Mung Chiang
Executive Vice President, Purdue University
John A. Edwardson Dean, College of Engineering
Roscoe H. George Distinguished Professor of Electrical and Computer Engineering

Attachments:

Overview of American Semiconductor Academy initiative

Overview of the Scalable Asymmetric Life Cycle Engagement (SCALE) program

SCALE: A Workforce Development Model for Defense Microelectronics

Numerous national studies have identified the declining numbers of U.S. students pursuing education and, hence, careers in STEM fields.[1] This decline has had a particular negative impact on the U.S. Microelectronics Industry both in terms of US graduate and undergraduate degrees. This also negatively impacts the defense sector in terms of secure and trusted microelectronics. Competition for these limited graduates has further stressed U.S. government and defense industrial base (DIB) recruiting.

To address this challenge, the **Department of Defense Trusted and Assured Microelectronics program funded a pilot program ($22.7M) to attract, obtain, and retain a future workforce.** The objectives were to:

1) increase probability for successful recruitment to government/DIB,
2) produce a readier workforce,
3) advance knowledge share,
4) scale nationally
5) expand/replicate across additional DIB microelectronics technology areas.

The pilot program, **Scalable Asymmetric Life Cycle Engagement (SCALE),** has been designed and implemented to follow evidence-based principles, including undergraduate research experience programs that analyze relations between program components and participant outcomes using quantifiable metrics. The SCALE model was developed to be an **immersive educational program that combines government/DIB internships with aligned research and mentoring** to deepen understanding and relationship building.

A consortium-based approach was used to achieve national reach to the top universities in targeted technical areas for scaling and replication of the program, while allowing a regional focus. The program was designed to be: **scalable** to multiple universities, **replicable** to additional microelectronics topics important to the federal government, and **asymmetric** in its effect in training U.S. students in areas of high need.

The DoD identified five technical areas of greatest national need and provided seed funding in each area:

1) **radiation-hardening**
2) **heterogeneous integration and advanced packing**
3) **systems-on-a-chip**
4) **secure supply chains**
5) **embedded system security**

Government partners from DoD and NASA worked with the team to identify the knowledge, skills, and abilities (KSAs) that their employees will need in these specific areas as undergraduate and graduate students in the first year of each topic area, followed by at least four years of execution providing the unique curriculum for students accepted into the program.

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[1] See, for example, the *Industrial Capabilities Report to Congress 2020*, United States Department of Defense, *National Defense Strategy, 2018*; and National Research Council 2012 Report *Assuring the U.S. Department of Defense a Strong Science, Technology, Engineering, and Mathematics (STEM) Workforce.* https://doi.org/10.17226/13467.

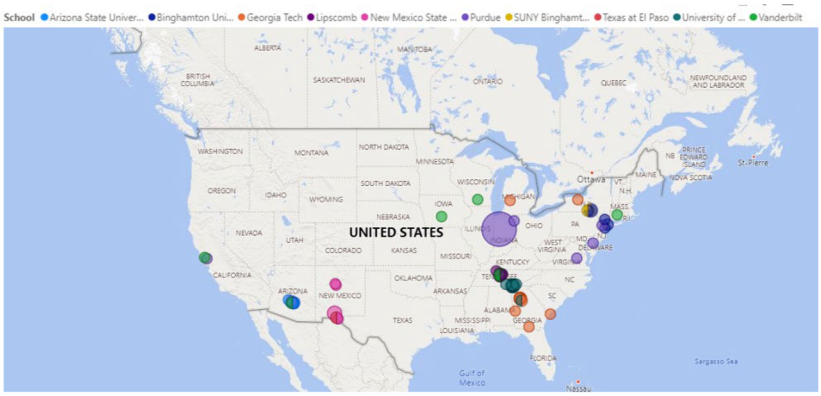
Purdue University leads the 16-university consortium across all five technical areas.

University Partners:
- Air Force Institute of Technology
- Arizona State University
- Brigham Young University
- Colorado-Boulder
- Georgia Institute of Technology
- Indiana University
- New Mexico State University
- Notre Dame University
- Ohio State University
- Purdue University (lead)
- St. Louis University
- SUNY-Binghamton
- University of California-Berkeley
- University of Florida
- University of Tennessee-Chattanooga
- Vanderbilt University

Government Partners:
- Missile Defense Agency (MDA)
- NSWC-Crane
- National Aeronautics and Space Administration (NASA)
- Office of the Secretary of Defense (OSD)
- Trusted & Assured Microelectronics
- Sandia National Laboratory
- US Navy Strategic Systems Program
- US Air Force & Air Force Materiel Command
- US Army Combat Capabilities Development Command

Industry Partners:
- Aerospace Corporation
- Boeing Corporation
- KBR
- Draper Labs
- General Dynamics
- L3 Harris
- Mercury Systems
- Northrop Grumman
- Reliable Microsystems
- Science Systems and Applications Incorporated (SSAI)
- Trusted Semiconductor Solutions

SCALE Network Map



Additional information available at https://www.purdue.edu/discoverypark/scale/

American Semiconductor Academy

Supplying talent and innovation for U.S. semiconductor manufacturing

Ensuring U.S. economic competitiveness and national security in the Digital Age

Leadership in semiconductor "chip" manufacturing requires a well-trained workforce and continuous innovation. The U.S. must invest in both **soft** infrastructure and **hard** infrastructure for a resilient domestic semiconductor ecosystem.

Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing.

The American Semiconductor Academy (ASA) will increase and broaden access to education and technical training for careers in semiconductor manufacturing, to fill the pipeline of talent for chip manufacturers in the U.S.

It also will facilitate the commercialization of innovations that originate in university research labs, through talent and technology transfer and startups, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Nationwide education & training NETWORK for the U.S. semiconductor manufacturing workforce

The ASA is a nationwide education and workforce development program implemented by a network of universities and colleges – including community colleges – geographically distributed across the U.S., organized into Western, Central, and Eastern Regions.

A revitalized curriculum in integrated circuit and systems design, semiconductor materials, devices and microfabrication technology will be developed jointly with the semiconductor industry and shared across the ASA network, to facilitate **education of a broad diversity of undergraduate and graduate students, to prepare them to enter the U.S. semiconductor manufacturing workforce**.

Hands-on experience with design of semiconductor devices and integrated circuits, microfabrication, and wafer processing tools will occur at topical hub universities in each of the Regions that are equipped and staffed to support this training. These facilities will be accessible to all students who have completed prerequisite ASA courses.

ASA funding would support curriculum development and dissemination, new faculty hiring, student scholarships and fellowships, industry internship, as well as equipment and facilities upgrades and all operational costs of hands-on workforce training at ASA universities and colleges.

Accelerated commercialization of innovation

The ASA will partner with the National Semiconductor Technology Center (NTSC) and U.S. semiconductor companies to **transfer talent and innovations from universities & colleges to the industry**.

Students who have completed the necessary ASA courses and training would qualify for "tech apprenticeships" at NTSC sites and also be well prepared for industrial internship opportunities.

University researchers who have demonstrated proof-of-concept of their innovations in an ASA lab would have facilitated access to NTSC resources to demonstrate the system-level benefits and scalability of their innovations, helping to bridge the gap from lab and fab.

Universities will continue to receive research funding directly from various sources to innovate new materials, processes, and devices that can dramatically improve chip performance, efficiency and/or cost.

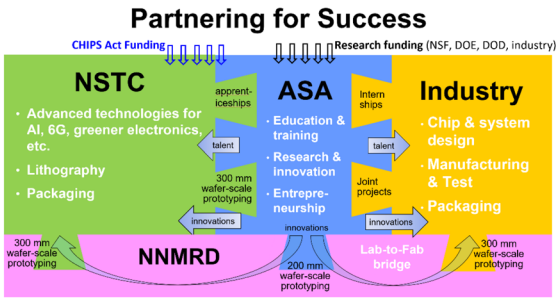
ASA funding would support tech apprenticeships and proof-of-concept prototyping on 300 mm wafers at NTSC sites designed to be flexible to incorporate new materials, processes, and devices into demonstration circuits and systems. It would also provide funding for startups to prototype their innovations at networked universities.

Economic Impact

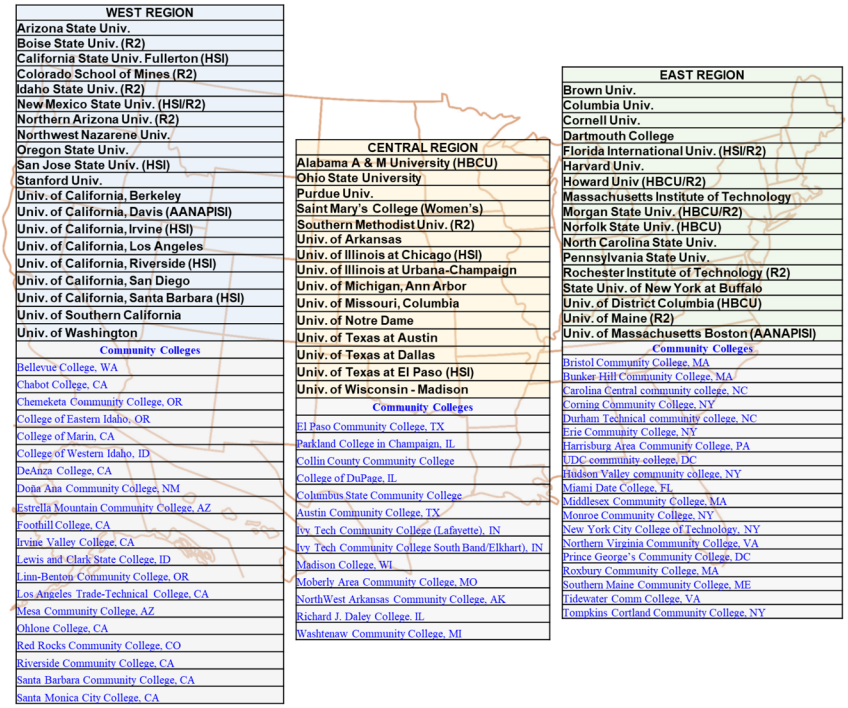
The **ASA will establish the soft infrastructure** (human and digital resources) **and hard infrastructure** (equipment and facilities) **needed to supply the technical workforce necessary for the U.S. to become a dominant producer of semiconductor chips.**

$50B invested by the federal government will result in 42,000 new jobs in semiconductor manufacturing over 5 years, leading to a total of 280,000 new jobs in the U.S. economy.

Only a broad and inclusive network of universities and colleges – the ASA – can meet this workforce development need.



Universities/Colleges Confirmed to be Interested to Participate in the ASA
(as of January 2022)



WEST REGION
Arizona State Univ.
Boise State Univ. (R2)
California State Univ. Fullerton (HSI)
Colorado School of Mines (R2)
Idaho State Univ. (R2)
New Mexico State Univ. (HSI/R2)
Northern Arizona Univ. (R2)
Northwest Nazarene Univ.
Oregon State Univ.
San Jose State Univ. (HSI)
Stanford Univ.
Univ. of California, Berkeley
Univ. of California, Davis (AANAPISI)
Univ. of California, Irvine (HSI)
Univ. of California, Los Angeles
Univ. of California, Riverside (HSI)
Univ. of California, San Diego
Univ. of California, Santa Barbara (HSI)
Univ. of Southern California
Univ. of Washington
Community Colleges
Bellevue College, WA
Chabot College, CA
Chemeketa Community College, OR
College of Eastern Idaho, OR
College of Marin, CA
College of Western Idaho, ID
DeAnza College, CA
Dona Ana Community College, NM
Estrella Mountain Community College, AZ
Foothill College, CA
Irvine Valley College, CA
Lewis and Clark State College, ID
Linn-Benton Community College, OR
Los Angeles Trade-Technical College, CA
Mesa Community College, AZ
Ohlone College, CA
Red Rocks Community College, CO
Riverside Community College, CA
Santa Barbara Community College, CA
Santa Monica City College, CA

CENTRAL REGION
Alabama A & M University (HBCU)
Ohio State University
Purdue Univ.
Saint Mary's College (Women's)
Southern Methodist Univ. (R2)
Univ. of Arkansas
Univ. of Illinois at Chicago (HSI)
Univ. of Illinois at Urbana-Champaign
Univ. of Michigan, Ann Arbor
Univ. of Missouri, Columbia
Univ. of Notre Dame
Univ. of Texas at Austin
Univ. of Texas at Dallas
Univ. of Texas at El Paso (HSI)
Univ. of Wisconsin - Madison
Community Colleges
El Paso Community College, TX
Parkland College in Champaign, IL
Collin County Community College
College of DuPage, IL
Columbus State Community College
Austin Community College, TX
Ivy Tech Community College (Lafayette), IN
Ivy Tech Community College South Band/Elkhart), IN
Madison College, WI
Moberly Area Community College, MO
NorthWest Arkansas Community College, AK
Richard J. Daley College, IL
Washtenaw Community College, MI

EAST REGION
Brown Univ.
Columbia Univ.
Cornell Univ.
Dartmouth College
Florida International Univ. (HSI/R2)
Harvard Univ.
Howard Univ (HBCU/R2)
Massachusetts Institute of Technology
Morgan State Univ. (HBCU/R2)
Norfolk State Univ. (HBCU)
North Carolina State Univ.
Pennsylvania State Univ.
Rochester Institute of Technology (R2)
State Univ. of New York at Buffalo
Univ. of District Columbia (HBCU)
Univ. of Maine (R2)
Univ. of Massachusetts Boston (AANAPISI)
Community Colleges
Bristol Community College, MA
Bunker Hill Community College, MA
Carolina Central community college, NC
Corning Community College, NY
Durham Technical community college, NC
Erie Community College, NY
Harrisburg Area Community College, PA
UDC community college, DC
Hudson Valley community college, NY
Miami Date College, FL
Middlesex Community College, MA
Monroe Community College, NY
New York City College of Technology, NY
Northern Virginia Community College, VA
Prince George's Community College, DC
Roxbury Community College, MA
Southern Maine Community College, ME
Tidewater Comm College, VA
Tompkins Cortland Community College, NY

ASA should be open to all U.S. universities and colleges

including R2/MSI, each paired with a community/technical college

Appendix II

Additional Material for the Record

LETTERS SUBMITTED BY REPRESENTATIVE EDDIE BERNICE JOHNSON

December 16, 2021

The Honorable Eddie Bernice Johnson
Chairman
Committee on Science, Space, & Technology
United States House of Representatives
2321 Rayburn HOB
Washington, DC 20515

The Honorable Frank Lucas
Ranking Member
Committee on Science, Space, & Technology
United States House of Representatives
2321 Rayburn HOB
Washington, DC 20515

Re: Ensuring American Leadership in Microelectronics

Dear Chairman Johnson and Ranking Member Lucas:

Thank you for holding your December 2, 2021, hearing on "Ensuring American Leadership in Microelectronics." This is a critically important topic and we appreciate the committee's focus on this multi-faceted issue. Apple believes that education and new or enhanced partnerships between education institutions and the private sector are key components to maintaining American leadership in microelectronics.

Education has always been a core value to Apple, and we have had a deep and longstanding connection to higher education. Over the past decade, however, we have seen a concerning shortage of students graduating from U.S. institutions with degrees in engineering, in particular in electrical engineering, silicon design and computer architecture. To help reverse this trend Apple has partnered with multiple engineering schools with initiatives to rejuvenate their programs. This past year we have also added four HBCU partner schools as part of our Racial Equity and Justice Initiative, with innovation grants to expand their coursework, scholarships, and internship opportunities in hardware engineering and silicon chip design. We see education as a great equalizing force and we're more dedicated than ever to supporting the educators, advocates and students leading the way.

Apple
One Apple Park Way
Cupertino, CA 95014
T 408 996-1010
F 408 996-0275
www.apple.com

At your hearing, you heard testimony about ambitious new approaches to ensuring American leadership in this arena, including the creation of a multi-institution partnership known as the American Semiconductor Academy (ASA). Apple applauds the goals of the ASA and initiatives like it that aim to increase access to education and technical careers in computer architecture, all aspects of silicon

engineering, microelectronic circuit and chip design, and facilitate the commercialization of innovations that originate in university research labs. Apple designs the key semiconductor integrated circuits required to deliver virtually all of its innovative products and sees the ongoing development of engineering talent at universities across the country as essential to future growth and innovation. If the ASA or similar initiatives are established, Apple expects to collaborate with them to help ensure their success.

Again, we appreciate the committee's attention to this important challenge and we look forward to the robust public-private partnership that will be vital to ensuring America's continued leadership in microelectronics.

Sincerely,

Tim Powderly
Senior Director, Government Affairs
Apple

December 16, 2021

The Honorable Eddie Bernice Johnson
Chairman
Committee on Science, Space, & Technology
United States House of Representatives
2321 Rayburn HOB
Washington, DC 20515

The Honorable Frank Lucas
Ranking Member
Committee on Science, Space, & Technology
United States House of Representatives
2321 Rayburn HOB
Washington, DC 20515

Dear Congresswoman Johnson and Congressman Lucas,

Subject: Workforce development infrastructure for the U.S. microelectronics industry

We are writing to provide supplemental information regarding the American Semiconductor Academy (ASA) initiative mentioned in Dr. Mung Chiang's testimony during the House Science Committee hearing on December 2, 2021 on *Ensuring American Leadership in Microelectronics*. Attached for reference is a one-page overview of the ASA initiative, along with 30 corporate letters of endorsement from across the U.S. semiconductor industry. (An additional letter from Apple Inc. will be submitted under separate cover.)

We represent faculty from universities across the U.S. in expressing to you a hope that Congress will include language in the bill that will fund the Creating Helpful Incentives for the Production of Semiconductors (CHIPS) for America Act, or similar legislation, to appropriate funding to support a nationwide network of universities and colleges to collaborate in addressing the urgent and growing workforce development needs of the U.S. semiconductor industry. Rebuilding the semiconductor production capacity will require a skilled workforce of all levels, ranging from technicians through engineers and scientists, and a similarly broad educational network and multidisciplinary curricula to provide these talents.

Such an educational network should be geographically diverse and inclusive, and

- be advised by companies across the semiconductor ecosystem to modernize the microelectronics curriculum,
- have the appropriate physical and digital infrastructure to provide meaningful experiential learning experiences as part of the curriculum,
- make curricular materials, training facilities and industry-standard tools accessible to all participating schools, and
- coordinate practical hands-on training ("tech apprenticeships") - uniquely critical for the semiconductor industry - for students who have successfully completed the prerequisite courses.

There should be an open and competitive process to participate in this education and training network. Participating schools should be held accountable to increase the number of graduates who enter the U.S. semiconductor manufacturing workforce, in appropriate proportion to the level of funding they receive.

Thank you for giving us the opportunity to provide this additional information for the congressional record. If the committee would like additional information, please contact Tsu-Jae King Liu at tking@eecs.berkeley.edu.

Sincerely,

John Dallesasse, *Interim Associate Dean for Facilities & Capital Planning*
Grainger College of Engineering, University of Illinois at Urbana-Champaign

Stephen Goodnick, *Deputy Director*, LightWorks®, *David and Darleen Ferry Professor of Electrical Engineering*
Arizona State University

Quanxi Jia, *SUNY Distinguished Professor, Empire Innovation Professor,* and *National Grid Professor of Materials Research*
State University of New York at Buffalo

Tsu-Jae King Liu, *Dean* and *Roy W. Carlson Professor of Engineering*
University of California, Berkeley

Mark Lundstrom, *Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering*
Purdue University

Kang Wang, *Distinguished Professor and Raytheon Chair in Electrical Engineering*
University of California, Los Angeles

Attachments:

Overview of American Semiconductor Academy (ASA) initiative + list of ASA planning universities
Letters of endorsement for the ASA initiative

American Semiconductor Academy

Supplying talent and innovation for U.S. semiconductor manufacturing

Ensuring U.S. economic competitiveness and national security in the Digital Age

Leadership in semiconductor "chip" manufacturing requires a well-trained workforce and continuous innovation. The U.S. must invest in both **soft** infrastructure and **hard** infrastructure for a resilient domestic semiconductor ecosystem.

Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing.

The American Semiconductor Academy (ASA) will increase and broaden access to education and technical training for careers in semiconductor manufacturing, to fill the pipeline of talent for chip manufacturers in the U.S.

It also will facilitate the commercialization of innovations that originate in university research labs, through talent and technology transfer and startups, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Nationwide education & training NETWORK for the U.S. semiconductor manufacturing workforce

The ASA is a nationwide education and workforce development program implemented by a network of universities and colleges – including community colleges – geographically distributed across the U.S., organized into Western, Central, and Eastern Regions.

A revitalized curriculum in integrated circuit and systems design, semiconductor materials, devices and microfabrication technology will be developed jointly with the semiconductor industry and shared across the ASA network, to facilitate **education of a broad diversity of undergraduate and graduate students, to prepare them to enter the U.S. semiconductor manufacturing workforce**.

Hands-on experience with design of semiconductor devices and integrated circuits, microfabrication, and wafer processing tools will occur at topical hub universities in each of the Regions that are equipped and staffed to support this training. These facilities will be accessible to all students who have completed prerequisite ASA courses.

ASA funding would support curriculum development and dissemination, new faculty hiring, student scholarships and fellowships, industry internship, as well as equipment and facilities upgrades and all operational costs of hands-on workforce training at ASA universities and colleges.

Accelerated commercialization of innovation

The ASA will partner with the National Semiconductor Technology Center (NTSC) and U.S. semiconductor companies to **transfer talent and innovations from universities & colleges to the industry**.

Students who have completed the necessary ASA courses and training would qualify for "tech apprenticeships" at NTSC sites and also be well prepared for industrial internship opportunities.

University researchers who have demonstrated proof-of-concept of their innovations in an ASA lab would have facilitated access to NTSC resources to demonstrate the system-level benefits and scalability of their innovations, helping to bridge the gap from lab and fab.

Universities will continue to receive research funding directly from various sources to innovate new materials, processes, and devices that can dramatically improve chip performance, efficiency and/or cost.

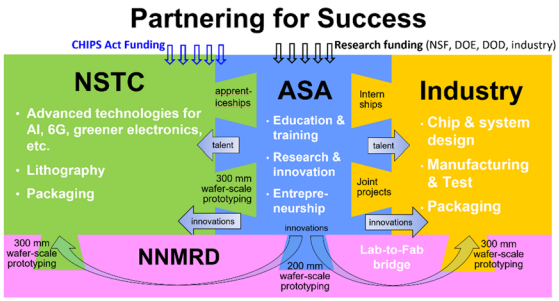
ASA funding would support tech apprenticeships and proof-of-concept prototyping on 300 mm wafers at NTSC sites designed to be flexible to incorporate new materials, processes, and devices into demonstration circuits and systems. It would also provide funding for startups to prototype their innovations at networked universities.

Economic Impact

The **ASA will establish the soft infrastructure** (human and digital resources) **and hard infrastructure** (equipment and facilities) **needed to supply the technical workforce necessary for the U.S. to become a dominant producer of semiconductor chips.**

$50B invested by the federal government will result in 42,000 new jobs in semiconductor manufacturing over 5 years, leading to a total of 280,000 new jobs in the U.S. economy.

Only a broad and inclusive network of universities and colleges – the ASA – can meet this workforce development need.



Universities/Colleges Confirmed to be Interested to Participate in the ASA
(as of December 2021)

WEST REGION
Arizona State Univ.
Boise State Univ. (R2)
California State Univ. Fullerton (HSI)
Colorado School of Mines (R2)
Idaho State Univ. (R2)
New Mexico State Univ. (HSI/R2)
Northern Arizona Univ. (R2)
Northwest Nazarene Univ.
Oregon State Univ.
San Jose State Univ. (HSI)
Stanford Univ.
Univ. of California, Berkeley
Univ. of California, Davis (AANAPISI)
Univ. of California, Irvine (HSI)
Univ. of California, Los Angeles
Univ. of California, Riverside (HSI)
Univ. of California, San Diego
Univ. of California, Santa Barbara (HSI)
Univ. of Southern California
Univ. of Washington
Community Colleges
Bellevue College, WA
Chabot College, CA
Chemeketa Community College, OR
College of Eastern Idaho, OR
College of Marin, CA
College of Western Idaho, ID
DeAnza College, CA
Dona Ana Community College, NM
Estrella Mountain Community College, AZ
Foothill College, CA
Irvine Valley College, CA
Lewis and Clark State College, ID
Linn-Benton Community College, OR
Los Angeles Trade-Technical College, CA
Mesa Community College, AZ
Ohlone College, CA
Red Rocks Community College, CO
Riverside Community College, CA
Santa Barbara Community College, CA
Santa Monica City College, CA

CENTRAL REGION
Alabama A & M University (HBCU)
Purdue Univ.
Saint Mary's College (Women's)
Southern Methodist Univ. (R2)
Univ. of Arkansas
Univ. of Illinois at Chicago (HSI)
Univ. of Illinois at Urbana-Champaign
Univ. of Michigan, Ann Arbor
Univ. of Missouri, Columbia
Univ. of Notre Dame
Univ. of Texas at Austin
Univ. of Texas at Dallas
Univ. of Texas at El Paso (HSI)
Univ. of Wisconsin - Madison
Community Colleges
El Paso Community College, TX
Parkland College in Champaign, IL
Collin County Community College
College of DuPage, IL
Austin Community College, TX
Ivy Tech Community College (Lafayette), IN
Ivy Tech Community College South Band/Elkhart), IN
Madison College, WI
Moberly Area Community College, MO
NorthWest Arkansas Community College, AK
Richard J. Daley College, IL
Washtenaw Community College, MI

EAST REGION
Brown Univ.
Columbia Univ.
Cornell Univ.
Dartmouth College
Florida International Univ. (HSI/R2)
Harvard Univ.
Howard Univ (HBCU/R2)
Massachusetts Institute of Technology
Morgan State Univ. (HBCU/R2)
Norfolk State Univ. (HBCU)
North Carolina State Univ.
Pennsylvania State Univ.
Rochester Institute of Technology (R2)
State Univ. of New York at Buffalo
Univ. of District Columbia (HBCU)
Univ. of Maine (R2)
Univ. of Massachusetts Boston (AANAPISI)
Community Colleges
Bristol Community College, MA
Bunker Hill Community College, MA
Carolina Central community college, NC
Corning Community College, NY
Durham Technical community college, NC
Erie Community College, NY
Harrisburg Area Community College, PA
UDC community college, DC
Hudson Valley community college, NY
Miami Date College, FL
Middlesex Community College, MA
Monroe Community College, NY
New York City College of Technology, NY
Northern Virginia Community College, VA
Prince George's Community College, DC
Roxbury Community College, MA
Southern Maine Community College, ME
Tidewater Comm College, VA
Tompkins Cortland Community College, NY

ASA should be open to all U.S. universities and colleges

including R2/MSI, each paired with a community/technical college

[Public]

Advanced Micro Devices
7171 Southwest Pkwy Austin, TX 78735
USA

Date: November 23, 2021

Re: American Semiconductor Academy Initiative

AMD is proud to endorse the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy.

As a leading provider of high-performance-compute solutions that are critical to our national economy, security, and infrastructure, AMD strongly supports thoughtful steps designed to strengthen the United States based semiconductor design and manufacturing ecosystem -- and we believe the establishment of the ASA is crucial to achieving that goal.

As the 2020–21 global chip shortage has made clear, leadership in semiconductor design and manufacturing is critical for both economic competitiveness and matters of national security. However, achieving such leadership requires a commitment to investing in both human capital and physical infrastructure that, together, will ensure we have a resilient domestic semiconductor ecosystem. Additionally, such investments must include the modernization of educational curricula and research & training facilities to complement industry investments in advanced design and manufacturing. If the ASA is established, AMD intends to collaborate with the ASA on critical research projects and curricula that serve to advance industry capability and train the workforce of the future of semiconductor manufacturing.

Worldwide, governments are investing heavily in university programs that underpin their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor ecosystem. AMD looks forward to working with the newly established ASA and doing our part to ensure the United States is ready for the next iteration of semiconductor design, production, and innovation.

Sincerely,

Mark Fuselier
SVP AMD Technology & Product Engineering

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

December 1, 2021

Whom It May Concern:

The 2020–2021 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness, but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research and training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Analog Devices, Inc. ("ADI") endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy ("ASA"), to:

1. increase access to education and technical careers in semiconductor manufacturing; and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments have recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The ASA could leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for the United States to, once again become a dominant producer of semiconductor chips.

ADI operates at the center of the modern digital economy, converting real-world phenomena into actionable insight with its comprehensive suite of analog and mixed signal, power management, radio frequency, and digital and sensor technologies. If the ASA is established, ADI intends to collaborate with the ASA in developing relevant experimental curriculum to help ensure its success.

Sincerely,

Daniel Leibholz
SVP and Chief Technology Officer
Daniel.Leibholz@analog.com

APPLIED MATERIALS®

3050 Bowers Avenue I P.O. Box 58039
Santa Clara, California 95054, U.S.A.
Telephone: 408 727 5555
www.appliedmaterials.com

December 15, 2021

Re : American Semiconductor Academy Initiative

To Whom It May Concern :

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore Applied Materials endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to:

- increase access to education and technical careers in semiconductor manufacturing, and
- accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Founded over 50 years ago in Silicon Valley, Applied Materials is the world's largest provider of semiconductor manufacturing equipment. The company's tools are used to produce virtually every semiconductor in the world - from the most advanced nodes to legacy chips. The company is headquartered in Silicon Valley with global manufacturing based in Austin, TX and additional key sites in Arizona, Massachusetts, Montana and New York.

If the ASA is established, Applied Materials intends to collaborate with ASA to help ensure its success.

Sincerely,

John D. Kania
Managing Director and Head of Government Affairs
Applied Materials, Inc.

axcelis

December 15, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical not only for economic competitiveness, but also for national security. The U.S. must invest in both soft and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Axcelis Technologies, Inc. endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to:

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Axcelis (Nasdaq: ACLS), headquartered in Beverly, Mass., has been providing innovative, high-productivity solutions for the semiconductor industry for over 40 years. Axcelis is dedicated to developing enabling process applications through the design, manufacture and complete life cycle support of ion implantation systems, one of the most critical and enabling steps in the IC manufacturing process.

If the ASA is established, Axcelis intends to collaborate with ASA to determine how Axcelis can best support ASA's mission to modernize educational curricula and establish research and training facilities to complement industry investments in advanced development and manufacturing.

Sincerely,

Mary G. Puma
President and Chief Executive Officer

Axcelis Technologies, Inc. · 108 Cherry Hill Drive, Beverly, MA 01915-1053 · 978.787.4000 phone

Broadcom
15101 Alton Parkway
Irvine CA 92618
broadcom.com

October 21, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

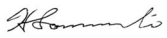
The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore Broadcom endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Broadcom is one of the largest semiconductor companies in the world. We are headquartered in California. We source the majority of our chips from Asia. We need access to the most advanced technologies to keep our chips at the leading edge of the market. We incorporate very advanced analog and mixed-signal designs into our products and require a constant supply of the best and brightest chip design talent in the world. We very much support the ASA initiative. It is imperative that we continue to invest in design and manufacturing capabilities in the U.S. If the ASA is established, Broadcom is happy to be a resource and partner with local universities to advance the ASA goals and help ensure its success.

Sincerely,



Henry Samueli, Ph.D.
Chairman, Broadcom Inc.
samueli@broadcom.com

cadence

Cadence Design Systems, Inc.
2655 Seely Avenue
San Jose, CA 95134

October 11, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Cadence Design Systems, Inc. endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Cadence Design Systems is a pivotal leader in electronic design, building upon more than 30 years of computational software expertise. The company applies its underlying Intelligent System Design strategy to deliver software, hardware and IP that turn design concepts into reality. The world's most innovative companies rely on Cadence solutions to deliver extraordinary electronic products from chips to boards to systems for the most dynamic market applications including consumer, hyperscale computing, 5G communications, automotive, aerospace, industrial and health. If the ASA is established, Cadence intends to collaborate with ASA by providing members access to our consumer grade software, training, solutions, development kits, and development of educational resources that enable a seamless transition of all students and faculty into the workforce to help ensure its success.

Sincerely,

Anirudh Devgan

Anirudh Devgan
President
T: 408.428.5002

December 15, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. In addition to incentivizing domestic commercial manufacturing for the near term, the U.S. should invest for the long-term re-invigoration of the domestic semiconductor technology pipeline. This should include the modernization of educational curricula and research & training facilities. Therefore, Cerfe Labs endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

As a semiconductor startup attempting to mature a new microelectronics technology, we have observed the uneven playing field in semiconductor technology commercialization, with governments from Europe to Asia placing more focused incentives on the translational research to commercialization readiness, as well as on expanded university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Currently, Cerfe Labs runs our R&D program in Belgium, where there has been a long history of focused investment leading to the Imec ecosystem. If the ASA is established, Cerfe Labs would intend to repatriate our R&D activity, engaging with ASA talent and facilities. We have in fact taken a small first step with an Air Force SBIR collaboration with one of the participating university institutions, but the global competitiveness challenge requires a focused ASA-type program rather than a collection of SBIR grants.

Sincerely,

Greg Yeric

CTO
Cerfe Labs
Austin, TX
Greg.yeric@cerfelabs.com

Cisco Systems, Inc.
170 West Tasman Drive
San Jose, CA 95134-1706
USA

December 13, 2021

Re: American Semiconductor Academy Initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security.

The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Cisco Systems, Inc. endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

If the ASA is established, Cisco will collaborate with ASA on workforce development activities in a manner designed to ensure its success.

Sincerely,

Jie Xue

Jie Xue
Vice President, Technology & Quality
Cisco Systems, Inc.

November 8, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that the semiconductor industry must re-think about the supply chain security. We must invest in both soft infrastructure and hard infrastructure for a resilient new semiconductor ecosystem, of which workforce development is the foundation. Modernization of educational curricula, and research and training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, IEEE Electron Devices Society endorses the establishment of a broad network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs

The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges around to meet the workforce development need for the whole supply chain of the semiconductor industry.

IEEE Electron Devices Society (EDS) is the largest professional society on microelectronics devices and technologies in the world. If the ASA is established, IEEE EDS intends to collaborate with ASA in various professional education and training activities to help ensure its success.

Sincerely,

Ravi Todi
IEEE EDS President

The IEEE Electron Devices Society
EDS Executive Office • 445 Hoes Lane • Piscataway, NJ 08854, USA
Phone +1 732 562 3927 • Fax +1 732 235 1626 • E-mail: eds@ieee.org • eds.ieee.org

GlobalFoundries™

400 Stonebreak Road Extension
Malta, NY 12020
USA
Tel: (518) 305-9013
www.gf.com

November 16, 2021

Re: American Semiconductor Academy Initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical not only for U.S. economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, GlobalFoundries ("GF") endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy ("ASA"), to:

1. Increase access to education and technical careers in semiconductor manufacturing, and
2. Accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The ASA should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

GF is engaged in, among other things, the research, design, development, bump, probe, packaging development, manufacture and sale of semiconductor devices and processes, for example, like those related to microprocessors and memory devices. If the ASA is established, GF shall strongly consider supporting the proposal by collaborating with ASA and/or committing resources to help ensure its success.

The aforementioned support, provided at GF's sole discretion, will enable a close working relatio nship between GF and ASA, one we hope we continue to expand in the coming years.

John Pellerin

VP and Chief Technologist, RF, SiPh and Advanced Si Packaging Technology Solutions
Technology, Engineering and Quality Org.
GlobalFoundries
Office Phone: 518.813.5045
Email john.pellerin@gf.com

December 15, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore <company> endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

The **Global Semiconductor Alliance (GSA)** represents the global semiconductor industry with 300 members advocating for business, technology, and pre-competitive collaboration to ensure value creation for the semiconductor industry allowing for more a healthy and profitable industry that can continue to make fundamental investments in R&D and Capex. We represent the entire ecosystem from IP to EDA to design to manufacturing as well as many of the end customers. We also represent companies like Tesla, Facebook, Amazon and Microsoft that have important internal hardware groups. Our membership encompasses those that have their own internal manufacturing like Intel and Microchip as well as those that utilize the fabless model like NVIDIA, Qualcomm and AMD. We also represent all the major foundries in the world.

If the ASA is established, the **Global Semiconductor Alliance (GSA)** intends to collaborate with ASA through its highly successful Women's Leadership Initiative ensuring that STEM focused university women and under-represented minorities are attracted to and prepared for participation in the semiconductor industry, as well as explore the opportunity to prepare High School educators with a semiconductor curriculum to ensure success at the university level.

Sincerely,

Jodi Shelton, CEO, Global Semiconductor Alliance
12400 Coit Road, Suite 650, Dallas, Texas 75251
(T) 972-866-7579 | U.S. Toll Free 888-322-5195
contact@gsaglobal.org

Friday, October 22, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Intel endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

If the ASA is established, Intel is interested in collaborating with ASA to help ensure our mutual success.

Sincerely,

Ann B Kelleher

Dr. Ann B. Kelleher
Senior Vice President, General Manager, Technology Development, Intel Corporation

Douglas Baney, Ph.D.
Corporate Director of Education

Keysight Technologies, Inc.
5301 Stevens Creek Boulevard
MS: 4U-SH
Santa Clara, CA 95051

408|425|1547 M
www.keysight.com

KEYSIGHT TECHNOLOGIES

November 23, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for economic competitiveness and national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced semiconductor development and manufacturing. Therefore, Keysight Technologies endorses the establishment of a nationwide network of universities and colleges, referred to here as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industries. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce required to support continuous innovation and deployment of semiconductors. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development needs for our country to become a dominant producer of semiconductor integrated circuits, ICs, once again.

Keysight Technologies, with corporate headquarters in Santa Rosa, California, is a leading provider of electronic and photonic IC test equipment and university experiential learning solutions used throughout the global semiconductor chip research, design, and manufacturing flow. We work with all the major semiconductor companies worldwide and are eager to support U.S. semiconductor manufacturing initiatives aimed at

Douglas Baney, Ph.D.
Corporate Director of Education

Keysight Technologies, Inc.
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MS: 4U-SH
Santa Clara, CA 95051

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www.keysight.com

KEYSIGHT TECHNOLOGIES

strengthening U.S. academic workforce training and development of semiconductor ICs.

If the ASA is established, Keysight intends to collaborate with ASA university partners with the provisioning of semiconductor test subject matter expertise and test equipment to help ensure its success in semiconductor workforce development and acceleration of U.S. semiconductor innovation and manufacturing.

Sincerely,

Dr. Douglas M. Baney, IEEE Fellow
Corporate Director of Education, Keysight Technologies
5301 Stevens Creek Blvd. Santa Clara, CA., 95051
Email: doug_baney@keysight.com

Corporate Office ▪ One Technology Drive ▪ Milpitas, CA 95035 ▪ www.kla.com

October 29, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, KLA Corporation ("KLA") endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

KLA develops industry-leading equipment and services that enable innovation throughout the electronics industry. We provide advanced process control and process-enabling solutions for manufacturing wafers and reticles, integrated circuits, packaging, printed circuit boards and flat panel displays. If the ASA is established and given our background, KLA intends to collaborate with ASA at multiple levels to help ensure its success, including:

- Provide guidance in defining a curriculum geared towards our industry
- Provide internships for undergraduate and graduate students
- Provide research grants in areas relevant to our industry
- Collaborate on maturing new technologies required for future design nodes

Sincerely,

R. Nyffenegger

Ralph Nyffenegger, Ph.D.
VP of Engineering
ralph.nyffenegger@kla.com

Lam Research Corporation
4650 Cushing Parkway
Fremont, CA 94538 U.S.A.
Main: 1-510-572-0200
lamresearch.com

December 2, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The current global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for national economic competitiveness. The U.S. must invest in both infrastructure and workforce development for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Lam Research endorses the establishment of a nationwide network of universities and colleges, referred to as the American Semiconductor Academy (ASA), to

1. increase access to education and technical careers in semiconductor manufacturing leading to a robust and diverse workforce, and
2. accelerate the commercialization of innovations that originate in university research labs through prototyping new technologies for manufacturing of future generations of chips.

As a global supplier of innovative wafer fabrication equipment and services to the semiconductor industry, Lam Research is positioned to play a role in the advancement of microelectronic technologies over the coming decades. One of the ways in which we do so is to partner with universities on basic research to enable transformative innovation. We also partner to inspire and educate students about career opportunities in the semiconductor industry.

The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to be a leader in developing innovative solutions for semiconductor fabrication. If the ASA is established, Lam Research intends to collaborate with ASA to help ensure its success.

Regards,

R.A. Gottscho

Executive Vice President and Chief Technology Officer
Lam Research Corporation

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008

November 29th, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical not only for economic competitiveness, but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure to create a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore MaxLinear, Inc., endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments have recently committed to invest heavily to expand university programs to support their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

As a fab-less analog, rf and mixed-signal communications IC company, MaxLinear relies on external semiconductor manufacturing supply-chains to produce its advanced ICs and SoC solutions. These suppliers include both advanced and specialist foundries, such as TSMC, UMC, Global Foundries, Key Foundry, Tower-Jazz, SMIC, along with overseas assembly and test (OSAT) companies such as ASE, SPIL, KCC, etc. We are especially vulnerable to supply-chain disruptions arising from the geopolitical concentration of these manufacturers in the greater China region. Further, many times, these manufacturers provide favorable supply capacity and pricing advantages to their co-domiciled companies, who are typically our competitors. Today, in the U.S., we have no credible semiconductor manufacturing ecosystem to support a fabless IC company, and consequently, 100% of MaxLinear's products are manufactured overseas. Over the last two decades, in the U.S., our ability to hire semiconductor technologists and experts in the areas of advanced IC fabrication process, device modeling, packaging technology and packaging design, has been greatly impacted due to a dearth of students who are pursuing semiconductor related curricula at our universities. As a result, we have been forced to move overseas many core functions and responsibilities in semiconductor process technology, device modeling, advanced packaging design, etc. to countries where a thriving semiconductor manufacturing ecosystem exists. Recent pandemic-driven supply-chain disruptions have only highlighted the need for developing a robust, world leading semiconductor manufacturing ecosystem within our country. This is a strategic imperative for us as a company and for the US, to not only secure supply of key semiconductor products, but also to maintain U.S. preeminence in semiconductor technology which is at the core of our new data network driven economy. If the ASA is established, MaxLinear intends to fully collaborate with ASA by providing internships for students in process technology, advanced packaging, device modeling and in IC design. We will also actively engage in joint research and development with the universities by involving our key engineers to help ensure its success.

Sincerely,

Kishore Seendripu, Ph.D.
CEO, MaxLinear Inc.

MicroLink Devices, Inc.
6457 Howard Street, Niles, IL 60714

October 29, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, MicroLink Devices endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.
3. promote the importance of semiconductors in numerous applications and ensure a stable supply chain of semiconductors

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

MicroLink Devices plays a key role in providing semiconductor parts to key industries such as RF test equipment, RF communication devices, high power devices, and solar cells for satellite applications. If the ASA is established, MicroLink Devices intends to collaborate with ASA to provide direction towards establishing a clear pathway towards research, education, training, and supply chain for compound semiconductor technology which is essential to help ensure its success.

Sincerely,

Noren Pan, CEO of MicroLink Devices
npan@mldevices.com
847 588 3001

November 18, 2021
Re: American Semiconductor Academy

To Whom It May Concern:

Semiconductors are essential in driving U.S. technology leadership and economic growth. To ensure the U.S. remains competitive in the semiconductor industry and develops a resilient domestic ecosystem there must be a commitment to invest in both soft infrastructure and hard infrastructure. Leadership in semiconductor manufacturing requires a well-trained workforce and continuous innovation. As the only U.S. based manufacturer of memory and storage and a world leader in semiconductor manufacturing, Micron strongly supports the creation of the American Semiconductor Academy (ASA), a network of diverse universities and community colleges that would prepare undergraduate and graduate students to enter the U.S. semiconductor manufacturing workforce.

The U.S. faces a sharp decline in college students starting in 2025 increasing the immediate need to prepare the next generation of semiconductor talent. The ASA directly aims to support the growing talent demands by increasing and broadening access to education, vocational training, and technical careers in semiconductor manufacturing. Additionally, the ASA would accelerate the commercialization of innovation by facilitating the transfer of talent and innovation from universities to make sure that leading-edge products will always be manufactured first in the U.S.

Governments from around the world have increased their investments in higher education programs and infrastructure to support their own growing talent need. Micron encourages the U.S. government to follow suit and appropriate funding to develop a well-trained workforce. Bringing together the best of industry, government and academia provides new opportunities and ways to explore leading-edge solutions that might not otherwise be possible.

Micron supports the concept of the ASA and, if established, would be interested in partnering to ensure a strong and enduring U.S. semiconductor industry.

Sincerely,

Scott DeBoer
Executive Vice President, Technology and Products
Micron Technology Inc.

Micron Technology, Inc. 8000 S. Federal Way Boise, ID 83707-0006 208.368.4000 **micron**.com

NORTHROP GRUMMAN

November 10, 2021

Subject: Support for University of Illinois's participation in the American Semiconductor Academy Initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Northrop Grumman Corporation endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy (ASA), to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor-manufacturing workforce and support continuous innovation. The ASA should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

As a leading global security company, Northrop Grumman, in particular, its Mission Systems sector (NGMS), provides our warfighters with the most advanced systems for situational awareness, aircraft survivability, navigation and communications, and long range precision targeting. To detect and defeat continuously evolving threats, these systems rely on state of the art multispectral semiconductor sources and sensors. Maintaining a domestic manufacturing base is critical for protecting thousands of Department of Defense platforms, and developing next generation systems. During the past year the defense industry has witnessed extraordinary delays in the delivery of semiconductor devices that has put warfighters at risk, and has exposed the vulnerability of our supply chain due to the lack of a strong domestic manufacturing base.

NGMS looks forward to collaborating with our UIUC ASA partner to help strengthen the supply chain, by develop and transferring revolutionary technologies, and recruiting, through our Future Technical Leaders program, new talent into its workforce, to stay at the forefront in the design and manufacturing of chips that are the key components of our next generation systems.

Sincerely,

Louise C. Sengupta

LOUISE SENGUPTA, Ph.D.
Director, Advanced Electronics,
Emerging Capabilities Development,
Northrop Grumman Mission Systems
1550 West Nursery Road, C425, Linthicum, MD
(E) louise.sengupta@ngc.com, (O) 410-993-9739

December 8, 2021

Subject: American Semiconductor Academy initiative

To Whom It May Concern:

The global semiconductor shortage has made clear an urgent need to reprise - and improve upon - earlier initiatives aimed at boosting domestic semiconductor manufacturing. This is a matter of both economic competitiveness, as well as national security. Key investments should focus on both soft and hard infrastructure to create a more resilient domestic semiconductor ecosystem. Given that one of the foundational elements of a strong domestic chip industry is a highly skilled workforce, NXP USA endorses the establishment of a nationwide network of universities and colleges, referred to as the American Semiconductor Academy, or ASA.

Per our discussions with one of the academic institutions involved (Arizona State University), the ASA will increase access to education and technical careers in semiconductor manufacturing. Moreover, the undertaking will help to significantly speed up commercialization of innovations that originate in university research labs. This in turn will help to reestablish significant leading-edge semiconductor manufacturing in the United States.

We urge the federal government to appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy aims to leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development needs of the United States in this important area. We are excited to lend support by endorsing the workforce development goals of this endeavor. NXP is well placed to offer guidance regarding curriculum and relevant projects. We also hope to be able to provide internships and employment opportunities for graduates of the ASA aligned to industry needs.

Sincerely,

Jennifer Wuamett, EVP and General Counsel
NXP USA

SEMI Global Headquarters
673 S. Milpitas Boulevard
Milpitas, CA 95035
Tel: +1.408.943.6900
www.semi.org

December 15, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, SEMI endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

SEMI is a global industry association of more than 2500 members supporting electronics manufacturing & design supply chain. SEMI is championing number of initiatives to support the Semiconductor Industry while talent shortage is one of the most challenging issue for our industry. SEMI has a comprehensive set of initiatives supporting STEM education in elementary to high schools, to University Connections, to Certifications & Apprenticeships Program, to Veterans reskilling, amongst others.

Given the context above about SEMI, formation of ASA will lead to a strong partnership between the two entities and that with pave the way to accelerate the talent pool development to support our industry, hence I strongly endorse formation of ASA.

Sincerely,

Ajit Manocha
President and Chief Executive Officer
SEMI

SILVACO

10/29/2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore <company> endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

As an EDA company, Silvaco TCAD-to-Signoff flow encompasses simulation tools to develop and optimize new semiconductor processes and devices prior to manufacturing. With this very strong background acquired in the last 35 years, Silvaco could certainly contribute and participate to make stronger the US semiconductor ecosystem.
If the ASA is established, Silvaco intends to collaborate with ASA in providing simulation solution, used to understand semiconductor physics to optimize and design existing and future semiconductor technologies and help ensuring its success.

Sincerely,

Eric Guichard
VP & GM TCAD BU
SILVACO, Inc.
2811 Mission College Blvd
Santa Clara, CA 95054
eric.guichard@silvaco.com

Doc ID: ff4aae1fe7e3cde688dbecc7ff1acccceb4c045

October 20, 2021

Re: American Semiconductor Academy Initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore SkyWater Technology endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to:

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

SkyWater Technology is the only U.S.-investor owned pure-play semiconductor foundry and works closely with the Department of Defense and the rest of the U.S. federal government to create a secure pipeline of microelectronics manufactured domestically.

If the ASA is established, SkyWater Technology intends to collaborate with ASA on workforce development initiatives to help ensure its success.

Sincerely,

Thomas J. Sonderman
President & CEO
(952) 851-5200

SYNOPSYS®
Synopsys, Inc.
690 East Middlefield Road
Mountain View, CA 94043-4033
T 650.584.5000
F 650.965.8637
www.synopsys.com

November 12, 2021

Re: American Semiconductor Academy initiative
To: Whom it may concern
From: Dr. Chi-Foon Chan, Co-Chief Executive Officer, Synopsys, Inc.

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for supply chain security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research and training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore *Synopsys endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy (ASA)*, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a leading producer of semiconductor chips once again.

Synopsys technology is at the heart of innovations that are changing the way people work and play. Self-driving cars. Machines that learn. Lightning-fast communication across billions of devices in the datasphere. These breakthroughs are ushering in the era of Smart Everything—where devices are getting smarter and connected, and security is an important consideration.Powering this new era of digital innovation are high-performance silicon chips and exponentially growing amounts of software content. Synopsys is at the forefront of Smart Everything with the world's most advanced technologies for chip design, verification, IP integration, and software security and quality testing.

Synopsys has a variety of Academic Partnerships and University Programs (APUP). The University Programs provide qualified university and research institutions access to the software tools and technology needed to prepare highly skilled graduates who can meet difficult challenges ranging from electronic and optical design to static analysis for software quality and security. The Academic Partnerships initiative foster research partnerships to innovate with leading academics to address the ever-evolving challenges of the semiconductor industry.

Synopsys spends significant efforts on APUP since the workforce and technology innovation requirements for Synopsys and its global customers are very demanding.

If the ASA is established, Synopsys proposes to collaborate with ASA to help ensure its success in a variety of ways, including:

- providing its leading edge products, labs and lecture material for education,
- hiring student interns from ASA member universities, and

- establishing Academic Partnerships with leading universities to research ground breaking integrated circuit architectures and revolutionary design automation technology.

We strongly support US government's funding and establishment of American Semiconductor Academy and look forward to exploring a fruitful partnership with ASA.

Sincerely,

Chi-Foon Chan, Co-CEO, Synopsys

Texas Instruments Incorporated
2900 Semiconductor Drive , MS 33140
Santa Clara, CA 95052

November 29, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Texas Instruments Incorporated endorses the establishment of a nationwide network of universities and colleges, such as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations based on university research, enabling leading-edge chip products to be manufactured first in the U.S.

Worldwide, governments have committed to invest heavily to expand university programs for their respective domestic semiconductor industry. We believe the U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy could leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a leading producer of semiconductor chips once again.

Texas Instruments Incorporated (TI) is a global semiconductor design and manufacturing company that develops analog integrated circuits and embedded processors. By employing the world's brightest minds, TI creates innovations that shape the future of technology. TI is helping more than 100,000 customers transform the future, today. TI focuses on industrial and automotive solutions that include microcontrollers, wireless communications, power management and sensor interfaces with associated signal conditioning and processing.

If the ASA is established, TI intends to collaborate with ASA to help ensure its success via the following:

- Provide guidance on workforce needs of the semiconductor industry – current and future
- Communicate opportunities for internships at all levels (BS, MS, PhD) to better

prepare students for industry

- Provide guidance on future fundamental precompetitive technology needs and associated research for future semiconductor leadership

Sincerely,

Dr. Ahmad Bahai
Senior Vice President, CTO and Director of Kilby Labs
Texas Instruments Incorporated
2900 Semiconductor Drive, MS 33140
Santa Clara, CA, 95052

Tower Semiconductor Where **Analog** and **Value** Meet

November 24, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The recent global integrated circuit shortage and dwindling onshore semiconductor manufacturing % has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem to support the commercial economy, the 16 Critical Infrastructure sectors and the DoD as well as the IC. Modernization of educational curricula and research & training facilities is needed to complement the investment in, and building of, production facilities in multiple process technologies including digital logic, memory & storage, compute, mixed signal, analog and legacy applications. In short, the US has lost its competitive edge in semiconductor research and development, technology development and manufacturing. However all good science and engineering starts in academia, and therefore Tower Semiconductor endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to:

1. Increase access to education and technical careers in semiconductor R&D, TD and Manufacturing
2. Accelerate the commercialization of R&D innovations that originate in university research labs, to ensure that digital, memory and analog leading-edge integrated circuit products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government is anticipated to appropriate funding that can be used to substantially grow the semiconductor development and manufacturing workforce and support continuous innovation. The American Semiconductor Academy must leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Tower Semiconductor (NASDAQ: TSEM) is the global leader in the manufacture of analog semiconductor components critical for consumer, infrastructure, and military electronic systems.
Tower Semiconductor operates at eight fabrication facilities on three continents with an annual capacity of more than 4.0B chips/year. These include multiple ITAR certified US facilities, one of which is certified to build DoD Trusted and Assured components, two fabs in Israel, one 12-inch fab in Italy and three fabs in Japan including a 12-inch facility certified to manufacture ITAR products.
Tower Semiconductor's focus areas of production include:

- World leading Radio Frequency (RF) chips for sub-6 GHz, 28GHz & 40GHz 5G & 6G telecommunications

Tower Semiconductor San Antonio
9651 Westover Hills Boulevard, San Antonio, Texas 78251, USA
+1 (210) 522-7000

Tower Semiconductor Where **Analog** and **Value** Meet

- Ultra-sensitive high-resolution image sensors (>200 megapixels) for low light surveillance and other imaging applications
- State of the art 65nm node High Voltage chips for data centers and industrial applications (i.e. smart power and energy efficiency)
- Leading Silicon Germanium and Silicon Photonics technologies for >400 gigabit/sec fiber optic data communications
- Aerospace & Defense (A&D) – Control circuits, image sensors, photonics and high frequency / high speed chips for DOD analog semiconductor needs for radar, communications, satellites, sensors & imaging, night vision, cyber and space

Tower Semiconductor supplies to Intel, Broadcom, Skyworks, Qorvo, FLIR, NASA, Semtech, Maxim Integrated, On Semiconductor and hundreds of non-publicly disclosed customers. Our "Jazz Semiconductor Trusted Foundry (JSTF)" cleared facility in Irvine, California handles Trusted and Assured projects for the DOD and other government entities, including tier one A&D customers.

If the ASA is established, Tower Semiconductor intends to collaborate with ASA in multiple areas of expertise listed above to help ensure its success.

Sincerely,

D Guy Eristoff

Chief Strategy Officer &
Head of Pathfinder Activities
Tower Semiconductor

guy.eristoff@towersemi.com
+1 (408) 202-3502

Veeco
MAKING A MATERIAL DIFFERENCE

11/5/2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Veeco Instruments Inc. endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Veeco endorses the establishment of the ASA in providing education and hands-on preparation for future semiconductor engineers. We expect to provide internship and employment opportunities for graduates of the ASA, and can provide guidance on curriculum and relevant projects, based on industry needs.

Sincerely,

Ajit Paranjpe

Dr. Ajit Paranjpe
Sr. Vice President
Chief Technology Officer
Veeco Instruments Inc.
145 Belmont Drive
Somerset, NJ 08873

December 9, 2021

The University of Illinois at Urbana-Champaign

Re: American Semiconductor Academy initiative

Dear Sir or Madam:

The 2020–21 chip shortage in Unites States manufacturing has been decades in the making due to risk averse United States'capital markets coupled with heavy foreign subsidy of technology companies. The chip shortage has made it clear that United States leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The United States must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Universities in the United States have consistently led the world in semiconductor device research and education since the inception of the industry. Modernization of educational curricula and research & training facilities is needed to stimulate complementary industry investments in advanced development and manufacturing. Therefore, Vega Wave Systems, Inc. endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industries. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation and maintain the United States' leadership in the semiconductor industry. The American Semiconductor Academy will leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Vega Wave Systems, Inc. is developing advanced vision systems that will dramatically increase the safety, security, and cost-effective operation of the world's nuclear power plants. Access to advanced integrated circuits and semiconductor devices is vital to our business. If the ASA is established, Vega Wave Systems, Inc. intends to collaborate with ASA through cooperative research and development and looks forward to employing highly skilled engineers trained at ASA members to help ensure our success.

Sincerely,

Alan Sugg, President
Vega Wave Systems, Inc.

1275 W ROOSEVELT RD, STE 104 • WEST CHICAGO, IL • 60185
PHONE: 630-562-9433 • FAX: 630-562-9431, INFO@VEGAWAVE.COM

XCOM Labs, Inc.
#keepinventing

December 2, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, XCOM Labs, Inc., endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

XCOM Labs is an American wireless technology innovator and developer which leverages the capabilities of advanced semiconductors to bring its products to market.

If the ASA is established, XCOM Labs intends to collaborate with ASA including the potential of offering internships to ASA participants to help ensure its success.

Sincerely,

Matt Grob
Chief Technology Officer
XCOM Labs, Inc.
mgrob@xcom-labs.com

XILINX.

November 23rd, 2021

Re: American Semiconductor Academy initiative

To Whom It May Concern:

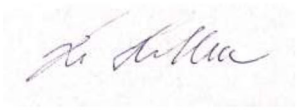
The 2020–21 global chip shortage has made it clear that leadership in semiconductor manufacturing is critical for not only for economic competitiveness but also for national security. The U.S. must invest in both soft infrastructure and hard infrastructure for a resilient domestic semiconductor ecosystem. Modernization of educational curricula and research & training facilities is needed to complement industry investments in advanced development and manufacturing. Therefore, Xilinx endorses the establishment of a nationwide network of universities and colleges, referred to herein as the American Semiconductor Academy, to

1. increase access to education and technical careers in semiconductor manufacturing, and
2. accelerate the commercialization of innovations that originate in university research labs, to ensure that leading-edge chip products will always be manufactured first in the U.S.

Worldwide, governments recently committed to invest heavily to expand university programs for their respective domestic semiconductor industry. The U.S. federal government should similarly appropriate funding that can be used to substantially grow the semiconductor manufacturing workforce and support continuous innovation. The American Semiconductor Academy should leverage the unparalleled diversity of universities and colleges across the U.S. to meet the workforce development need for our country to become a dominant producer of semiconductor chips once again.

Xilinx is inventor of FPGA and programmable, adaptive SoCs, and a world leading semiconductor IC design company. If the ASA is established, Xilinx intends to collaborate with ASA to help ensure its success in semiconductor workforce education and training.

Sincerely,



Xin Wu, Vice President, Silicon Technology, Xilinx INC
2100 Logic Drive, San Jose, California 95124, USA
xin.wu@xilinx.com

DOCUMENT SUBMITTED BY REPRESENTATIVE PAUL TONKO,

The Honorable Eddie Bernice Johnson, Chairwoman
Committee on Science, Space, and Technology
U.S. House of Representatives
2321 Rayburn House Office Building
Washington, DC 20515

December 1, 2021

Dear Chairwoman Johnson and Members of the Committee:

Thank you for conducting a public hearing on "Ensuring American Leadership in Microelectronics" – one of the most significant opportunities before our nation, which holds enormous consequence for national security, economic and workforce development, public health, and more.

The State University of New York (SUNY) is the most comprehensive higher education system in the nation, with 64 colleges, including several R&D centers. While NY CREATES, a state-affiliated non-for-profit, is New York's bridge to the global advance technology industry. Together, made possible by unparalleled support from New York State, we have constructed and developed the country's only 300mm nanotech complex; it is the most advanced publicly-owned semiconductor R&D facility in North America. In addition to the physical plant, we have ready-to-operationalize workforce development training programs interconnected with a vast network of public and private colleges and universities, as well as existing and emerging collaborative partnerships with private enterprise.

Indeed, the Albany Nanotech Complex holds untold potential in leading the U.S. microchip R&D agenda and is the only U.S. site prepared to begin work immediately once the House and Senate complete negotiations and pass the U.S. Innovation and Competition Act.

Attached for submission into the Committee's records, please find SUNY's official whitepaper, "Supporting the Future of US-Based Semiconductor Manufacturing: Innovation, Technology Development & Translation, And Workforce Enablement," in which we detail key elements for the future of semiconductor manufacturing, including:

- Bridging the gap between R&D and manufacturing/commercialization;
- Supporting the technology pipeline;
- Training and maintaining a strong workforce; and
- Creating technology transfer/industry partnerships.

Please do not hesitate to let us know if we can be helpful in any way. We would also be delighted to arrange a presentation about, or an on-site visit to, the Albany NanoTech Complex at your convenience. Thank you again for your efforts and consideration of our remarks.

Sincerely,

F. Shadi Shahedipour-Sandvik
Dr. F. Shadi Shahedipour-Sandvik
Provost-in-Charge
SUNY

Paul Kelly
Paul Kelly
Chief Operating Officer
NY CREATES

SUNY The State University of New York

SUPPORTING THE FUTURE OF US-BASED SEMICONDUCTOR MANUFACTURING:

Innovation, Technology Development & Translation, and Workforce Enablement

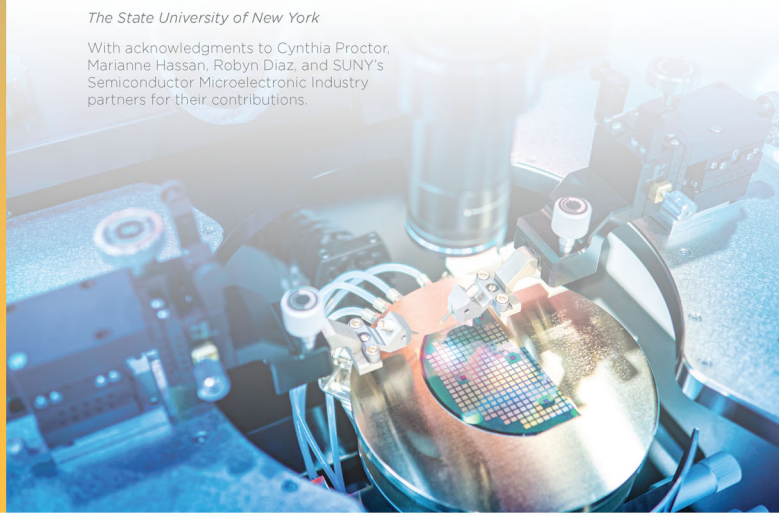
Draft finalized September 2021

AUTHORS:

F. Shadi Shahedipour-Sandvik, Robert Geer, Nathaniel Cady, Nicholas Querques

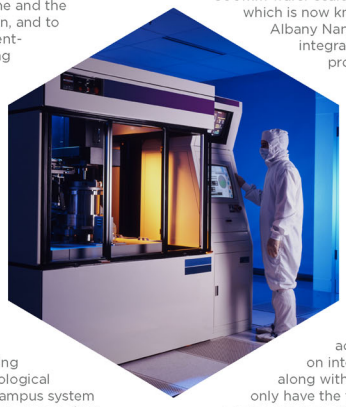
The State University of New York

With acknowledgments to Cynthia Proctor, Marianne Hassan, Robyn Diaz, and SUNY's Semiconductor Microelectronic Industry partners for their contributions.



EXECUTIVE SUMMARY

We live in a world that is increasingly dependent upon data, computing power, and communication. The far-reaching impact of computing technology touches all aspects of society, and is a key driver in both the US and global economies. Heavily based on semiconductor processing technology, computer chip manufacturing is complex, expensive, and labor intensive, requiring innovative technological practices and a highly-skilled workforce. While the United States is a leader in semiconductor technology research and development, on-shore manufacturing represents only a fraction of worldwide production. There is a clear and urgent need to bolster US-based semiconductor manufacturing, to bridge the gap between the R&D pipeline and the pathway to commercialization, and to enable workforce-development-at-scale. At the time of writing this position paper, others including China, EU countries, Japan, and Taiwan are making substantial investments in science, technology, workforce training and manufacturing to bolster their positions and competitiveness in microelectronics.



Universities and higher-education systems provide a fertile training ground for a skilled workforce and include an established network of research centers for developing the next generation of technological breakthroughs. With its 64-campus system of 1.3 million students, 3 million alumni, $1.6 billion annual R&D expenditures, and over 7,000 principal investigators, the State University of New York (SUNY) carries a massive responsibility to create transformational research opportunities in leading edge fields and advance commercialization of its inventions for the public benefit. A sustained, well-funded national strategy is essential for the U.S. to reassert its leadership and competitiveness in microelectronics and semiconductor manufacturing; however, *its success will rely on effective regional coordination with institutions of higher education to have the requisite impact on the workforce.* Large public university systems such as SUNY have well-established transfer paths between its two-year colleges, four-year comprehensive colleges, and large research universities, have established procedures for sharing research and education infrastructure, and have existing deep connections to local and regional industry, government, and economic development efforts. The latter is critically important as it is not feasible or sustainable to place capital intensive semiconductor laboratory equipment at every college campus for student education and workforce training. Hub-and-spoke models can be intrinsically more efficient and sustainable. *This system-based approach is essential for both disseminating new academic content and teaching modalities to re-engage students with microelectronics research and manufacturing, and for expanding the diversity and inclusivity of the pool of students engaged with microelectronics careers.*

SUNY is home to the only complete university-based chip fabrication facility operating at 300mm wafer scale, Albany Nanotech, which is now known as NYCREATES. The Albany Nanotech site offers a fully-integrated research, development, prototyping, and educational facility that provides strategic support through outreach, technology acceleration, business incubation, pilot prototyping, and test-based integration support for onsite corporate partners including IBM, GlobalFoundries, Samsung, Applied Materials, Tokyo Electron, ASML and Lam Research, as well as other "next generation" nanotechnology research activities, including hands-on internships for students along with career opportunities. Not only have the top four semiconductor equipment manufacturers (Applied Materials, Tokyo Electron, ASML, and LAM) located their most advanced tools and most talented R&D teams at Albany Nanotech, but these partnerships and infrastructure have enabled major breakthroughs, such as IBM's recent development of their 2nm chip technology[1].

Facilities like Albany Nanotech are prime examples of fabrication environments that replicate an industrial fabrication facility, but also enable innovation and workforce development. Such facilities are well poised for onboarding new technologies and educating the next generation of the semiconductor workforce. The role of the university is to provide the infrastructure, host the partners/tenants and to provide an instream of students/interns, post docs/contractors to support, feed, and accelerate this virtuous cycle of innovation. SUNY is a prime example of a higher-education institution with the size, scale, student diversity, and access to cutting-edge 300mm Si

fabrication facilities necessary to effectively 'move the U.S. workforce needle' to help reassert U.S. leadership and competitiveness in microelectronics and semiconductor manufacturing. Albany Nanotech represents a thriving microelectronics ecosystem that is the result of more than $15 billion in investment by New York State spanning more than two decades, with a current operating budget of approximately $300 million per year. While these types of sites and facilities take billions of dollars and decades to create, build, and operate, Albany Nanotech is already operational and positioned to scale to meet domestic demand for more computer chips. SUNY's highly unique experience pioneering this successful co-location model between industry and academia at Albany Nanotech positions it well to achieve the large-scale impact that is envisioned in the United States Innovation and Competition Act (USICA).

Strategic investments described herein will enable SUNY to realize such a large impact, in alignment with the impact that was envisioned in the 2020 National Defense Authorization Act (NDAA) and the United States Innovation and Competition Act (USICA) of 2021, which included provisions to fund research and development in the semiconductor industry from the bi-partisan CHIPS for American Act and the bi-partisan American Foundries Act.

USICA, landmark legislation championed by Majority Leader Schumer that would spark innovative collaboration between higher education, industry, and research enterprises, passed the Senate in June 2021 and included emergency appropriations to support the implementation of semiconductor R&D programs that were authorized in the 2020 NDAA. Specifically, USICA provides $12.5 billion over five years for a National Semiconductor Technology Center, a National Advanced Packaging Program, and other programs that support research, testing, and workforce development in coordination with the private sector, federal agencies, and higher education.

THE MULTI-FACETED NEED FOR SEMICONDUCTOR INNOVATION

While the United States is a leader in semiconductor technology research and development, onshore manufacturing represents only a fraction of worldwide production. The U.S. supply shortage pre-dated but continues to be exacerbated by the pandemic and weather-related disasters at international manufacturing facilities. The current computer chip shortage is already negatively impacting motor vehicle production and further shortages and increased costs are projected for everything from phones to tablets and computers. There is a clear and urgent need to bolster US-based semiconductor manufacturing, and to bridge the gap between the R&D pipeline and the pathway to commercialization.

The Semiconductor Research Corporation (SRC), which represent university researchers, government, and industry, released *The Decadal Plan for Semiconductors*[2] in November 2020. The plan was a call to action to "address a range of seismic shifts shaping the future of chip technology." These seismic shifts, identified by SRC members, involve "smart sensing, memory and storage, communication, security, and energy efficiency." The SRC called for the federal government/industry to "invest ambitiously in semiconductor research in these areas to sustain the future of chip innovation." The identified areas of focus include: 1) fundamental breakthroughs to address the "analog data deluge"; 2) growth of memory and storage demands; 3) communication capacity vs. data generation; 4) security challenges; and, 5) the need to improve efficiency and reduce the energy requirements for computation.

In its 2018 *Report of the Office of Science Workshop on Basic Research Needs for Microelectronics*,[3] the Department of Energy identified the following priority research priorities for microelectronics: 1) innovative material, device and architecture requirements driven by applications, algorithms, and software; 2) revolutionize memory and data storage; 3) reimagine information flow unconstrained by interconnects; 4) redefine computing by leveraging novel unexploited physical phenomena; and 5) reinvent the electricity grid through new materials, devices and architectures.

The common thread among these and other reports is that the US needs to: reduce power utilization

KEY ELEMENTS FOR THE FUTURE OF SEMICONDUCTOR FOR MANUFACTURING IN THE UNITED STATES

- Reduce power & improve efficiency
- Enable novel computing approaches
- Meet increasing data & communication needs
- Ensure computing & manufacturing security
- Train and maintain a strong workforce

Figure 1. *Key elements needed to address major semiconductor needs and challenges for establishing new technologies and a robust, US-based manufacturing base.*

and improve the efficiency of computation; enable novel computing approaches (devices, architectures, and beyond); meet the demands of increasing data and communication needs; ensure the security of computation and manufacturing; and, train and maintain a strong workforce (Figure 1). Although there is no question that substantial investments are needed to bolster innovation through basic science research, the monumental challenge is understanding how to bridge the gaps between what we currently see as "state-of-the-art," and what ultimately needs to be done to meet current, and anticipate future, needs from the market. Higher education has a significant role to play here but it requires both investment in research and development, as well as a paradigm shift in how R&D advancements are translated to commercialization and manufacturing.

THE ROLE OF UNIVERSITIES & HIGHER EDUCATION

The importance of this work and the consequences of inaction cannot be understated—strategic investments here are directly tied to the health (and comparative strength) of the US economy and well-being of its citizens. When research and development lag, there is a corresponding decline in jobs along with resources (i.e. tax receipts) to fund social programs including healthcare, education, and infrastructure, to name a few. Two Nobel prizes were given to studies that concluded that as much as 85 percent of the long-term growth in America's economy is ascribed to advancements in science and technology.[4] China is projected to become the world's largest economy when measured by GDP by 2030. By 2026 (the 250th anniversary of the United States), China's strategic plan calls for it to be well on its way to becoming the unchallenged world leader in science, technology, and innovation. These developments are perilous for America and a tipping point in its R&D position.[5]

The State University of New York (SUNY) is the largest comprehensive system of public higher education in the United States. Unique among U.S. university systems in its scope and range, SUNY comprises distinguished research universities, academic medical centers, liberal arts colleges, community colleges, technology colleges, and recognized centers of excellence. SUNY's 64 campus system of 1.3 million students, 3 million alumni, $1.6 billion annual R&D expenditures, and over 7,000 principal investigators carries a massive responsibility to create transformational research opportunities in leading edge fields and advance commercialization of its inventions for the public benefit. Through innovative academic/industry partnership led by the SUNY Polytechnic Institute (SUNY Poly) campus in Albany, New York known as Albany Nanotech,[6] SUNY has also become an internationally recognized hub for microelectronics and semiconductor manufacturing.

THE ALBANY NANOTECH COMPLEX IS HOME TO SUNY POLY'S COLLEGE OF NANOSCALE SCIENCE AND ENGINEERING.

It is imperative that a robust response to address innovation and competitiveness in science and technology, technology translation, and workforce enablement is implemented and well-resourced, now. This can be accomplished through investment in human capital, knowledge capital, an ecosystem conducive to innovation, and financial capital; all hallmarks of the University research and development infrastructure.

Universities and higher-education systems provide a fertile training ground for a skilled workforce and include an established network of research centers for developing the next generation of technological breakthroughs.

Key to reducing administrative barriers and supporting innovative partnerships, SUNY also has the largest comprehensive university-connected research foundation in the country. The Research Foundation of SUNY (SUNY RF) provides essential business services that enable faculty to focus on the education of students and the performance of life-changing research. SUNY RF proudly powers SUNY's technology transfer and commercialization activities, including managing a technology and innovation portfolio of 1,828 patents, 848 active licenses, 130 operational startups, 18 technology and business incubators, and a startup equity portfolio with a total fair value of over $500 million.

BRIDGING THE GAPS

A critical challenge to furthering innovations that impact manufacturing advances is to address known gaps that are preventing innovations in research laboratories, higher education institutions, and small businesses from translation into manufacturing and commercialization.

In industry, the so-called "valley of death" describes the difficulty in maturing technologies through the demonstration and validation stage, which ultimately leads to a failure to transfer many new technologies to industry.[7]

Thus, we need major investments to accelerate R&D in key areas (Figure 2) and to build the bridges needed to translate promising technologies and innovations from the discovery stage all the way through commercialization.

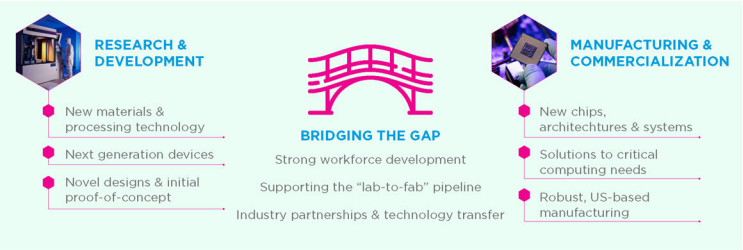


Figure 2. *Major gaps between R&D and ultimate manufacturing and commercialization of technologies yield a "valley of death" and lead to the failure of many innovations. By supporting the pipeline between the laboratory and fabrication/ manufacturing, investing in partnerships and technology transfer, and establishing a strong workforce, it is possible to bridge these gaps.*

SUPPORTING THE TECHNOLOGY PIPELINE

To address the key elements for semiconductor and microelectronics manufacturing in the US, there must be strong support for research and development that will lead to technological breakthroughs. This includes investment in basic research on: 1) new materials and processing technologies; 2) next generation devices; and 3) novel approaches to design, from the chip level to entire systems. With advances in each of these areas, intellectual property can be more efficiently and effectively transitioned from university laboratories and research centers to industry partners for manufacturing and commercialization. Simply increasing R&D output, however, is not enough. Bridging the aforementioned valley of death will require new investment in infrastructure as well as initiatives to transition technologies and practices.

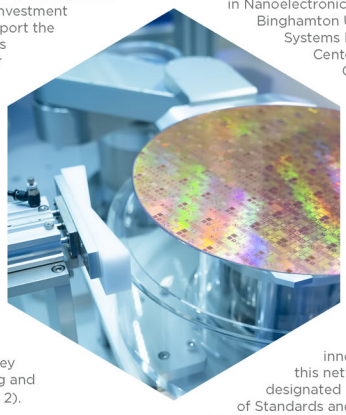
In the semiconductor industry, the principle of scale is important on many levels. As the individual transistors and device elements on chips continue to scale smaller and achieve higher density, the size of silicon wafers and the magnitude of manufacturing facilities (fabs, cleanrooms) has continued to grow. While university research laboratories and start-ups can demonstrate new materials and devices using relatively small-scale equipment (typically on 100mm - 200mm wafers or even wafer pieces), major equipment suppliers and chip manufacturers are focused on high volume manufacturing on a 300mm wafer substrate, in equipment optimized to deliver high throughput. *This dichotomy between research scale proof-of-concept and the reality of high-volume manufacturing is a significant contributor to the "valley of death."*

HOW DO WE ADDRESS THE MISMATCH BETWEEN RESEARCH-LEVEL ACTIVITIES AND MANUFACTURING-LEVEL PRODUCTION?

First, investments must be made to keep university and other key research laboratories up to date with state-of-the-art fabrication tools and equipment; however, this does not imply that university-based facilities should try to replicate and maintain a complete CMOS-capable process flow or toolset. The cost of maintaining such equipment and the lack of availability of state-of-the-art, small wafer (100-200mm) tools makes such an approach untenable. *Goals here are much better accomplished by using*

an industry-university co-location model, similar to what has been established in Albany, New York at the SUNY Poly campus (detailed below).

As such, universities need targeted investments in processing equipment (e.g., deposition, etch, lithography, metrology) that enable the next generation of discovery in materials, devices, packaging and testing. For example, atomic layer processing tools (e.g. deposition, etch, selective area growth) are needed to support extremely small-scale device development efforts and novel material stacks for emerging devices. As 2D and topological materials continue to demonstrate promise, there must also be investment in tools/toolsets that can support the processing, and in some cases transfer of these materials for wafer-scale fabrication. Likewise, cutting-edge metrology tools are needed to keep pace with aggressive device and materials scaling. Finally, investments are needed to support these research activities, not just the purchase of equipment and expansion of infrastructure. Basic funding to support the research programs (personnel, materials, tool time, etc.) is critical, and must be focused on research areas that support key semiconductor manufacturing and innovation needs (Figures 1 & 2).



WHAT IS NEEDED TO TRANSITION TECHNOLOGIES FROM LAB TO FAB?

Lab-scale demonstration of materials and devices on wafer pieces and small silicon wafers (100mm - 200mm) ultimately needs to be translated to fabrication in a high-volume manufacturing (HVM) environment. This typically means transition to a 300mm wafer platform. There is considerable mismatch, however, between the processing capability, materials compatibility, controls, and the overall process flow when moving from a research-level fabrication facility to HVM. Industry co-location facilities like Albany Nanotech are good examples of fabrication environments that replicate an industrial fabrication facility, but also enable innovation. Such facilities are well-poised for onboarding new technologies — but not without significant investment in "bridge" tools and infrastructure. To effectively demonstrate process and materials compatibility with 300mm "fabs" or "foundries," a dedicated set of tools and processing capability is needed. This is especially important in the areas of materials deposition, etch, and planarization, where novel materials and processing steps could negatively impact (and even shut down) a standard semiconductor production line. A bridge facility and set of equipment would enable unique processing capability in parallel to the strictly controlled 300mm process line, and would provide a unique "proving ground" for translating lab-based materials and process innovations into a manufacturing-ready, 300mm toolset. Such a facility would also constitute an efficient interface to established university-based research centers across the U.S. Current examples at SUNY institutions include New York State's university-based Centers of Excellence program; in particular, SUNY Poly's Center of Excellence in Nanoelectronics and Nanotechnology, Binghamton University's Small Scale Systems Integration and Packaging Center, Stony Brook University's Center of Excellence in Wireless and Information Technology, and the University at Buffalo's Center of Excellence in Materials Informatics. In addition, SUNY works closely with Empire State Development, New York's economic development arm, which deploys over $60 million annually to support a network of 70+ state-supported university research centers, incubators, and other advanced technology innovation assets. As part of this network, NYSTAR had been designated by the National Institute of Standards and Technology (NIST) Manufacturing Extension Partnership as the lead for all of New York, supporting a statewide center and ten regional centers.

WHAT WOULD A "BRIDGE" FACILITY AND TRANSLATIONAL PIPELINE LOOK LIKE?

Establishing a "bridge" facility requires a dedicated toolset in close proximity to a standard 300mm fabrication facility (co-location model), as well as a pipeline of processing innovation and metrology from distributed research-scale facilities/fabs. Placing flexible tools within, or in close proximity to a standard 300mm fab enables the seamless transfer of wafers back and forth to the "bridge" facility for unique process development. In effect, the "bridge" becomes a parallel loop for unique material and process development, and a sandbox for innovating and translating novel technologies onto the standard 300mm wafer platform. By including encapsulation tools (to protect/cover incompatible materials), as well as wafer cleaning and inspection tools (to remove and detect potential contaminants), wafers can ultimately proceed from the "bridge" space back into the standard fab (process line). This approach

requires dedicated space and dedicated tools, in order to allow for processing and materials flexibility, and to limit impact on the function and throughput of the standard fabrication facility. It also requires a pipeline of processing developments from research-level laboratories and fabrication facilities. A strong network of partners developing novel materials and processes must be able to perform initial proof-of-concept, which can then be translated to the "bridge" facility.

Examples of such technology development and translation that are enabled by the 300mm fabrication facility capabilities at Albany Nanotech include US Department of Defense-sponsored research programs in advanced radiation hardened and 2D material-based nanoelectronic devices[8] and integration of novel resistive switching devices with CMOS for neuromorphic computing and artificial intelligence applications[9]. In addition to individual projects, the Albany Nanotech 300mm fabrication capabilities are currently enabling multiple project wafer (MPW) programs that incorporate unique circuit designs from multiple research groups from across the country onto a single chip, saving cost and accelerating development time.

EDUCATING, TRAINING, AND MAINTAINING A STRONG WORKFORCE

U.S. colleges and universities are at the heart of the education and workforce engine that has supported the microelectronics and semiconductor ecosystems since the inception of the transistor. Reassertion of U.S. leadership in microelectronics and cutting-edge microelectronic manufacturing must begin with sustained reinvestment in the U.S. college and university-based workforce enterprise; not only to maintain and expand the continued knowledge creation and innovation that has advanced existing semiconductor R&D for the last 50+ years, but to enable onshoring of key manufacturing capabilities necessary for U.S. economic and national security.

Semiconductor manufacturing in the U.S. employed nearly 200,000 people in 2019 in 20 fabs across the nation. This employment has decreased by more than 100,000 from 2001 due, in large part, to automation and offshoring.[10] While regional partnerships between individual employers and educators have long existed to support the workforce needs of individual fab facilities (e.g. SUNY partnerships with IBM and GlobalFoundries) a broader strategic approach is needed for substantial and sustained expansion of the number of STEM students pursuing careers in semiconductor manufacturing necessary to support a revitalized U.S. microelectronics sector.

Ironically, the ubiquity of semiconductor technology has, to some degree, disconnected many STEM students from the science and technology necessary to maintain global leadership in microelectronics. The pervasive availability and performance of integrated circuits have driven an explosion in computational, communication, and bio-related disciplines which have played no small role in the substantial increase of STEM-based degrees in the U.S. over the last decade (Fig. 3). However, enrollment in STEM degree programs that have typically supplied the semiconductor R&D and manufacturing workforce (Electrical Engineering, Materials Science, Physics, etc.) has remained flat or declined. Fears that the subject matter is too difficult, perhaps because of lack of exposure in the nation's P-12 system, exacerbates the decline in interest in semiconductor-related STEM careers among America's youth.[11] The enrollment decline compounds the historic lack of diversity in these programs. The United States systematically fails to attract Americans of diverse backgrounds into STEM careers, whether this is measured by gender, socioeconomic status, religion, sexual orientation, geographic location within the U.S., or disability.[12]

A key contributor to this decline of interest is a growing disconnect between students' perception of socially impactful 'tech' careers versus career pathways in microelectronics R&D and manufacturing. In other words, students are not seeing how a future career in microelectronics and semiconductor technology and manufacturing can address many serious global social and environmental issues. Compounding this has been a lack of engagement with younger students. While middle school and high school 'coding camps' and robotics competitions have grown dramatically across the US, priming interest in the fields of computer science, robotics, and autonomous systems, there has not been a meaningful analogous engagement platform for microelectronics and integrated circuits to raise awareness of the world-changing impacts intrinsic to such careers for younger students.

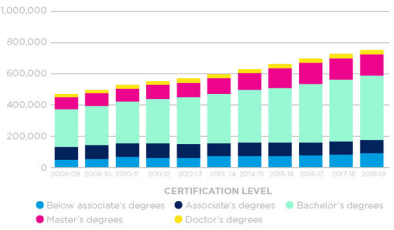


Figure 3. *Number of STEM degrees conferred by U.S. institutions, by degree level 2008-2019*

These systemic shortcomings must be addressed holistically, and at a meaningful scale of investment in U.S. higher education to promote a resurgence of student interest and career engagement in both microelectronics R&D and semiconductor manufacturing. Moreover, *the microelectronics workforce is hardly monolithic.* The R&D workforce is largely populated by those with bachelor's, master's, and doctoral degrees while the larger manufacturing workforce is dominated by two-year, associate degree recipients. Thus, a realistic approach to effective and impactful microelectronics education and workforce development must engage community colleges, comprehensive (four-year) colleges and research universities on a sufficiently large scale to 'move the needle.' No individual institution alone can have the required impact.

A sustained, well-funded national strategy is essential for the U.S. to reassert its global leadership and domestic competitiveness in microelectronics and semiconductor manufacturing; however, its success will rely on effective regional coordination with institutions of higher education to have the requisite impact on the workforce. This naturally favors large public university systems such as SUNY that have well-established transfer paths between its two-year colleges, four-year comprehensive colleges and large research universities; have existing and deep connections to local and regional industry and economic development efforts; and have established procedures for sharing research and education infrastructure. The latter is critically important as it is not feasible or sustainable to place capital-intensive semiconductor laboratory equipment at every college campus for student education and workforce training. Hub-and-spoke models can be intrinsically more efficient and sustainable. *This system-based approach is essential for both disseminating new academic content and teaching modalities to re-engage students with microelectronics research and manufacturing, and for expanding the diversity and inclusivity of the pool of students engaged with microelectronics careers.*

SUNY's diverse 64-campus system (including two-year colleges, four-year comprehensive colleges, technology colleges and research universities) serves nearly 400,000 students in for-credit degree and certificate programs, as well as its Educational Opportunity Centers (EOCs), and Pathways in Technology Early College High School (P-TECH) program, and a growing population of students in micro-credential and shorter-term certificate programs. SUNY campus leaders serve in senior roles on local regional economic development boards throughout New York State and many are very familiar with the workforce needs of the U.S. microelectronics industry.

In addition, SUNY's broad reach into the for-credit and not-for-credit education and training arenas for the trades, HVAC, environmental health and safety (EH&S), and industrial support career paths is equally important. In many regions of the U.S., the need for engineers and graduate level R&D positions at chip fabrication facilities is dwarfed by the need for process operators, maintenance technicians, facilities personnel, EH&S, and administrative operations staff. A successful workforce strategy must include these sectors as well.

SUNY is a prime example of a higher-education institution with the size, scale, degree diversity, student diversity, and access to cutting-edge 300mm Si fabrication facilities necessary to 'move the U.S. workforce needle' to help reassert U.S. leadership in microelectronics and semiconductor manufacturing.

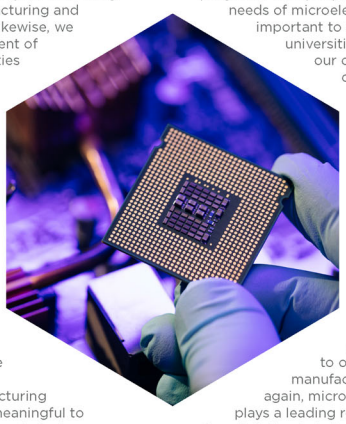
KEY ELEMENTS OF A SUCCESSFUL EDUCATION AND WORKFORCE STRATEGY FOR MICROELECTRONICS AND SEMICONDUCTOR MANUFACTURING

A successful strategy to support an effective workforce for the U.S. microelectronics and semiconductor manufacturing industry must be multi-pronged and financially well-supported for long-term success. Key elements include, but are certainly not limited, to the following seven-point approach:

1. **Pre-college student engagement:** Meaningful, career and skills-oriented summer academies, workshops and bootcamps for incoming two-year and four-year college students to introduce microelectronics career pathways and associated academic programs. These would include 'design and fab' academies, 'chip manufacturing' bootcamps, and 'emerging technology' career workshops or similar.
2. **Access to Design-Fab-Test experiences at the undergraduate level:** Student educational access to introductory electronic and photonic integrated circuit design tools (i.e., electronic design automation (EDA/EDPA) software tools) in courses and workshops that allow students to submit their own designs to multi-project wafer (MPW) tape-outs, fabrication, and packaging. This should be coupled with access to chip-testing facilities for students to complete the design/fab/test cycle. Long a staple of graduate research, this access needs to be pushed deep into undergraduate curricula to stimulate innovation and career interest. It is essential to leverage facilities with proven and scalable MPW capabilities, such as Albany Nanotech's 300mm Si prototyping facility, to engage students with multiple technologies, e.g. traditional CMOS, photonic integrated circuits (PICs), ReRAM, power electronics, biochip, and quantum-computing architectures. Designing and testing basic chip-based sensors or rudimentary neural network circuits is well within the grasp of a wide-range of undergraduate students. Providing

such 'innovation platforms' directly to students is essential. It is also worth noting that various manufacturing innovation institutes, including SUNY's AIM Photonics Institute, have already shown the efficacy of this approach for their educational outreach efforts.

3. **Expanded experiential learning:** Increased undergraduate participation in microelectronics R&D is clearly a key strategic component and requires expansion. However, a meaningful impact on the microelectronics manufacturing workforce requires a parallel expansion in experiential learning opportunities associated with advanced manufacturing, automation, machine learning, data literacy and Industry 4.0 principles. This is especially critical for the skilled technical workforce (e.g. those with A.S., A.A.S, and A.O.S. degrees) necessary for onshoring of microelectronics manufacturing and packaging technologies. Likewise, we must expand the engagement of students in advanced facilities management and the trades which support microelectronics fabrication facilities. Access to a university-based 300mm Si fab facility for experiential learning opportunities, which could be bundled with coursework in the form of micro-credentials—for two-year engineering tech students and four-year engineering students—is critical for all these sectors of the workforce. Such experience enables direct transition to the semiconductor manufacturing workforce in a timeframe meaningful to employers, while still putting students on a pathway to an initial or advanced degree.



4. **Expanded industry internships/co-ops:** Sustained support for a dramatic expansion in industry internships, co-ops and mentoring of students is likewise a key component. Although typically made available to upper-level undergraduates and graduate students, we must expand this engagement to include lower-level undergraduates (two-year/four-year) and, where appropriate, the trades to stimulate interest in microelectronics-related degrees, certificate programs and career pathways.

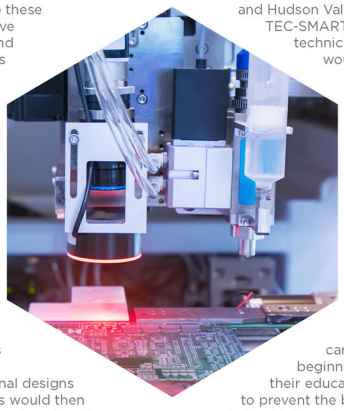
5. **Expanded initiatives in student diversity:** At each level of student engagement, the importance of sustained support for a diverse student pool cannot be overstated. A prime reason for the lack of growth in enrollment in microelectronics degree programs, whether at the technician, engineer, or R&D research professional level is the shrinking student pool. Entire sectors of our incoming student body have little connection to microelectronic career pathways. Tapping into these segments of our student body promises a rich and talented pool from which to rebuild our semiconductor workforce. A successful strategy will focus on embedding microelectronics and semiconductor manufacturing engagement activities (as outlined above) within specific institutions with diverse student populations.

6. **Incumbent worker training and Department of Defense transition assistance program support:** Colleges and universities are traditionally driven by enrollment of students in 'for-credit' courses and programs. To rapidly respond to the workforce needs of microelectronics it is equally important to support colleges and universities in reskilling and upskilling our current workforce. Flexible delivery and engagement mechanisms must be developed to leverage the same content and facilities available to registered students to support our incumbent workforce. Nowhere is this more important than supporting transitioning military personnel. The more than 200,000 highly diverse military personnel transitioning out of service every year bring ready-made skills and experience to our microelectronics manufacturing workforce. Here again, micro-credentials, in which SUNY plays a leading role nationally, could be a beneficial toolset. Supporting student access to custom education and training modules in microelectronics will hasten their transition to such career paths but give them credit toward a certificate or degree.

7. **Microelectronics career transitioning:** While colleges and universities have long supported the transitioning of their students from the classroom to the workforce, a national microelectronics education and workforce initiative must also include an innovative approach to connect the highly qualified students with employers. Graduating students (or incumbent workers/ transitioning DoD service members) should be able to construct a digital profile of their knowledge, skills, and abilities that can be made available to employers if they so choose. There

are novel approaches to do just this such as IBM's personal skills blockchain concept and SEMI's SEMI-Works® talent hub portal. These approaches should be scaled nationally to give graduating students and newly trained workers the ability to communicate verified details of their skills to potential employers — and for potential employers to highlight the knowledge, skills, and abilities they value the most for their future employees. SUNY's own Credential as You Go national effort can inform priorities in this area, as can SUNY's experience with open source digital badges.

8. **SUNY Microelectronics Workforce and Education Hubs:** To enable these key elements for an effective and impactful education and workforce strategy requires a system-level approach to avoid redundant and unsustainable infrastructure investment while providing the broadest possible access to a diverse student population.



For example, expansion of Albany Nanotech's 300mm Si prototyping facility to support large-scale educational MPW fabrication will create a design-fab hub where two-year/four-year/grad students from across the system and beyond can submit educational designs for fabrication. These designs would then be distributed back to fully equipped testing and application labs at SUNY research university centers, four-year comprehensive colleges, and community colleges to complete the student design-fab-test cycle and prepare students for direct entry into the microelectronics R&D and semiconductor manufacturing workforce. This MPW approach has been used successfully in SUNY Poly's AIM Photonics 300mm Si-wafer integrated photonics process flow for students from SUNY Poly, Rochester Institute of Technology, University of Rochester, University of California Santa Barbara, University of Arizona, Rensselaer Polytechnic Institute (RPI), and Massachusetts Institute of Technology (MIT).

The same 'hub and spoke' model would support critically important experiential learning models for the larger technician and engineer workforce. Leveraging workforce development facilities at SUNY community colleges (e.g. the Finger Lakes Workforce Development Center at Monroe Community College in Rochester, NY, the SUNY Erie Workforce Development Centers in Buffalo, NY, and Hudson Valley Community College's TEC-SMART facility, in Malta, NY), technician and engineering students would gain key hands-on technical experience before participating in 'capstone' internship experiences at SUNY Poly's 300mm Si Prototyping facility to enable transition directly into the U.S. 'fab' workforce.

A successful microelectronics and semiconductor manufacturing education and workforce development strategy must engage students with innovation and career pathways from the very beginning — and at each stage of their educational decision making — to prevent the broad pipeline of students entering higher education from becoming a modest trickle of entrants into microelectronics and semiconductor careers. *Such a coordinated resource model is highly scalable across the U.S. and represents a cost-effective approach to build a more diverse and better-trained semiconductor and microelectronics workforce.*

TECHNOLOGY TRANSFER AND INDUSTRY PARTNERSHIP

Translation from lab to fab, and eventually into the market, for most microelectronics technologies requires capital and time, as well as a combination of academic, government, and industry collaboration throughout various phases of the commercialization lifecycle. In order to maximize public dollars invested at the earliest stages of microelectronics research and technology development, and to increase the potential for the successful commercialization of these innovations, it is imperative that academic institutions engage and build strong relationships with the full spectrum of entities that operate across the various microelectronics industries and supply chains. Synergies across academic institutions can effectively accelerate the commercialization pathways for microelectronics innovations at scale by actively guiding and supporting the strategic and scientific vision for government-supported

technology development centers and related clusters dedicated to these activities.

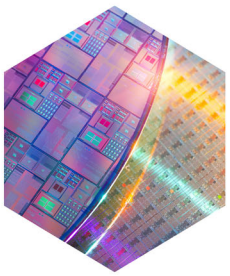
Universities are home to nascent and seasoned researchers, entrepreneurs, and startup companies that bring new microelectronics innovations to market. These innovators and entrepreneurial ventures, which are tackling some of the toughest problems facing the microelectronics industry, are critical to boosting innovation and increasing the nation's competitiveness. Academia is also critical in driving additional investment in technology and talent by larger, established corporations from the US and abroad, which in turn organically catalyzes more innovation and investment in the space. Further, to the betterment of all, there is clear recognition and existing commitment at the university level that program development in the microelectronics sector must be oriented to developing and attracting an inclusive, diverse, and high-performing workforce that draws from all segments of society and reflects the diversity of our increasingly global community.

New startup companies and growing small businesses developing and scaling breakthrough microelectronics innovations and processes from prototype to manufacturing require access to expensive and unique equipment, tools, and specialized facilities that are typically only available through a limited subset of academic, government, or industry partners. Providing affordable, straightforward, and streamlined access to these critical resources for qualified researchers, startups, and established small businesses that do not have the financial resources due to their stage of development or other factors will improve their likelihood for commercial success and spur more innovation domestically.

Established large companies that have a vested interest in the development and advancement of new microelectronics technologies and manufacturing techniques must be engaged by academic institutions with relevant research and commercial capabilities so they have a line of sight into the latest research and innovations being developed outside their walls. It also provides a natural opportunity to align interests between relevant startups or small businesses and willing large established companies, using the academic institutions as the common thread and vehicle for collaboration, at least initially. When executed correctly, this process opens up additional opportunities for more engagement between academia, government, and industry to advance the beneficiary researchers, startups, or small businesses, including joint development, non-recurring engineering, talent development and matchmaking, investment, licensing, access to customers or supply chain partners, etc.

The SUNY system, with grant and technology commercialization activity managed by the Research Foundation of SUNY, is uniquely positioned to be a leader and partner in serving this critical technology translation role between academia, government, and industry. SUNY's long track record (across its campuses) of providing accessible and affordable education and training opportunities for all New Yorkers on a massive scale (1.3 million students and nearly 3 million alumni), accessible via a single source, SUNYRF, has already demonstrated a proven ability to remove barriers in training and cross-fertilization and to facilitate connection to industry and academic partnership.

A truly impactful and thriving domestic microelectronics innovation ecosystem will require targeted investment by the public sector in the form of large, multi-institutional technology development and manufacturing centers or clusters focused on specific technology areas as well as record levels of non-dilutive government funding for technologies, companies, and projects. Based on previous periods of growth in government funding, like the investments made as part of the recovery from the great recession in 2008, it is highly likely similar investments in microelectronics research and education will lead to the mobilization of private investment across all categories, from equity investment to project capital and other debt financing. Those academic institutions operating centers focused on the advancement of microelectronics research, commercialization, manufacturing, and workforce development will need to offer wrap-around entrepreneurship and technology scaling support for their various stakeholders — students, faculty, startups, small companies, large established players, and the general public. This includes everything from basic training and advanced educational programs for innovators and entrepreneurs at all levels to business development mentoring and coaching support, subsidized access to shared facilities and bridge tools up to 300mm, and access to the pre-seed/seed-stage investment needed for technology de-risking, validating target markets, and building initial teams early on.

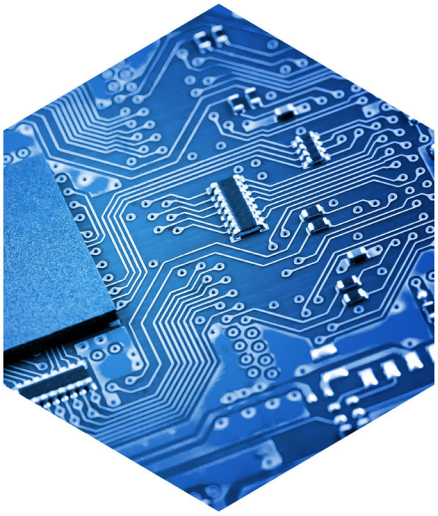


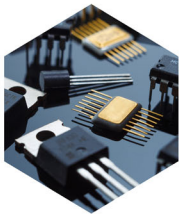
CONCLUSION

The nature of education and workforce training for microelectronics and semiconductor R&D and manufacturing is intrinsically challenging. Technology continually pushes the envelope of our fundamental understanding of materials and the very nature of information and communication itself. However, despite the complex and advanced nature of SUNY's enterprise we cannot demand students undertake an arduous career of study, only to be engaged with actual career pathways at the very end of their experience.

A successful microelectronics and semiconductor commercialization, manufacturing, education and workforce development strategy must engage students with innovation and career pathways early in their academic careers, and at each stage of their educational decision making, to prevent the broad pipeline of students entering higher education from becoming a modest trickle of entrants into microelectronics and semiconductor careers. *Industry-academia co-location facilities like Albany Nanotech are great examples of fabrication environments that replicate an industrial fabrication facility, but also enable innovation and workforce development.* Such facilities are well-poised for onboarding new technologies — but not without significant investment in "bridge" tools and infrastructure. SUNY's world-class microelectronics characterization, analysis, and fabrication facilities and capabilities make it a natural development partner and destination for global businesses of all sizes operating in the microelectronics industry. The public/private co-location model pioneered by SUNY Poly and partners at Albany Nanotech where a university campus, faculty, and students are co-located in the same facilities as industry partners, was focused exclusively on the microelectronics space. Investments here and in similar ventures to enhance opportunities for researchers, startups, and small businesses to connect and collaborate with industry players will result in more market-facing, commercially viable research and foster accelerated technology translation and commercialization from lab to fab for the domestic microelectronics industry.

Outlined in this document, we have put forward key elements of a successful innovation, technology translation, and education and workforce strategy for bolstering the U.S. microelectronics and semiconductor manufacturing of today, tomorrow and in the future. SUNY, with its integrated network of 64 campuses, premier 300mm facilities and bridge tools, and successful track record in workforce development and education, offers a proven model for the kind of scale-up strategy that the U.S. needs to retain leadership and competitiveness in the global microelectronic industry envisioned in USICA.





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